The Timepix3 readout chip for hybrid pixel detectors: design and first measurements

Massimiliano De Gaspari
CERN, European Organization for Nuclear Research
Geneva, Switzerland

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Outline

- Introduction to Timepix3
- Front-end architecture
- Tests on bare chips
- Measurements with sensor
- Summary

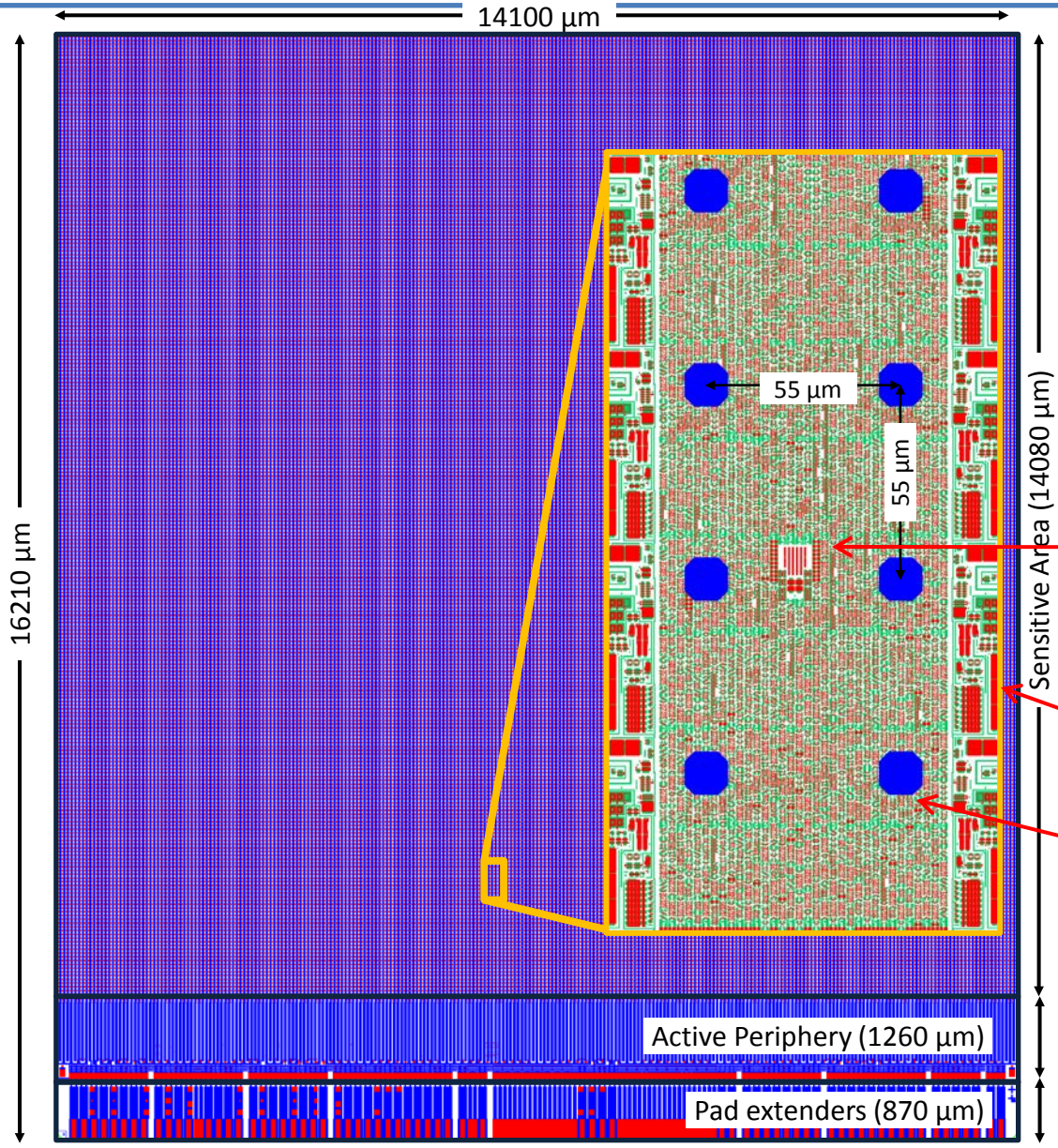
Timepix → Timepix3

	Timepix	Timepix3
Year	2006	2013
# pixels	256 x 256	
Pixel size	55 x 55 μm	
Technology	CMOS 250nm	CMOS 130nm
Measurement modes	- Time-Over-Threshold (TOT) - Time Of Arrival (TOA) - Event counting (PC)	- Simultaneous 10bit TOT and 18bitTOA - 18bit TOA only - 10bit PC and 14bit integral TOT (itot)
Readout type	Sequential (frame-based)	- Frame-based - Data Driven (zero suppressed)
Dead time	>300μs full frame readout	> 375ns packet transfer, maximum hit rate 40Mhits/s/cm^2
Time resolution	10ns	1.56ns
TOT monotonicity (h^+)	No	Yes
Power pulsing	No	Yes
Minimum threshold	~750e^-	>500e^-

Timepix3 is a joint design effort by **CERN**, **NIKHEF** and the **University of Bonn**

Main applications are:
- Fast readout of solid-state pixelated sensors
- Readout of gaseous detectors (TPC)
- Vertex Locator for LHCb (future VELOpix)
- Power pulsing tests for the Linear Collider
- Dosimetry

Timepix3



128 double columns:
2x256 pixels (64 SuperPixels) each

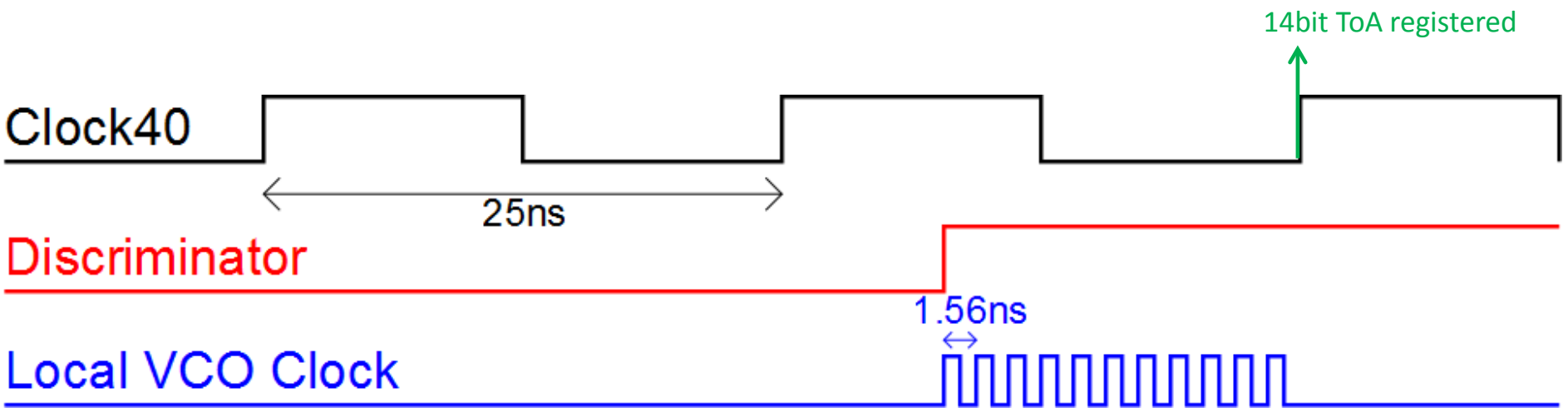
SuperPixel: 2 x 4 pixels

1 per SuperPixel:
VCO@640MHz
for the fast TOA

Analog Front-End 13 x 55 µm^2

Input pad on top of the digital area

Fast ToA measurement

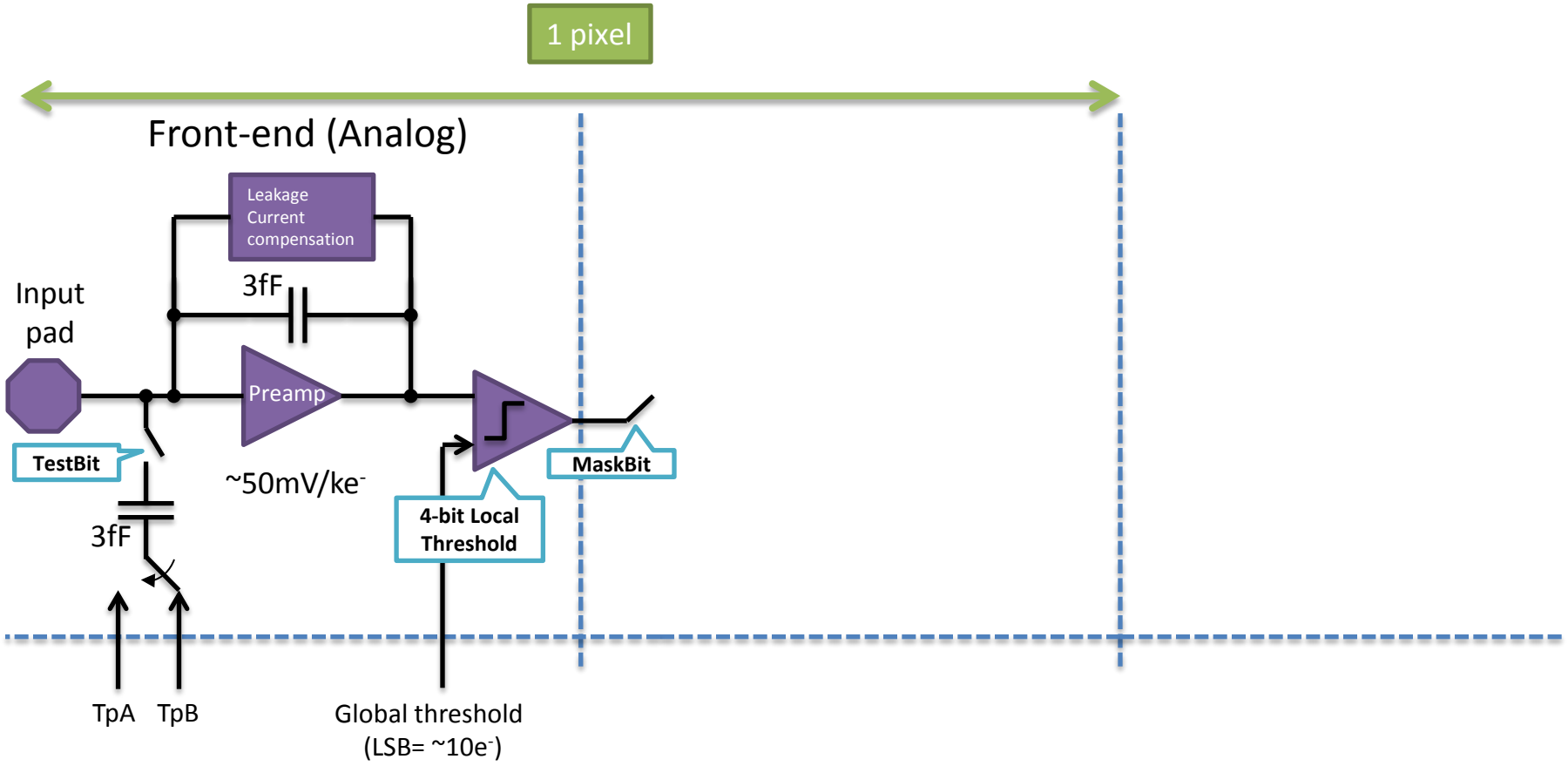


40MHz global clock always running (14bit ToA)

One 640MHz Voltage-Controlled Oscillator per SuperPixel (2x4 pixels) activated only when a discriminator fires (4bit fast ToA)

Pixel/SuperPixel diagram

T. Poikela



Pixel/SuperPixel diagram

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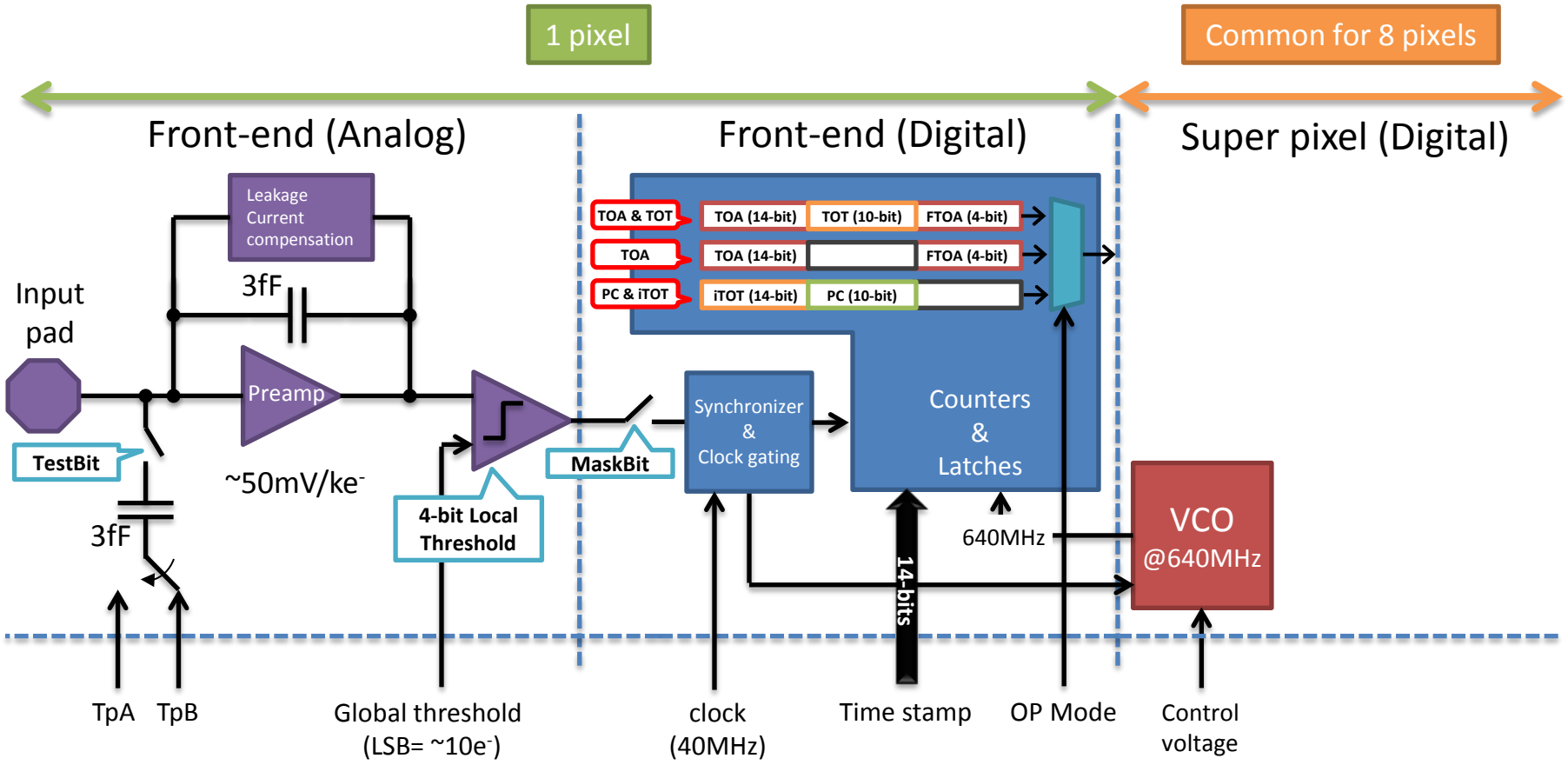

Pixel/SuperPixel diagram

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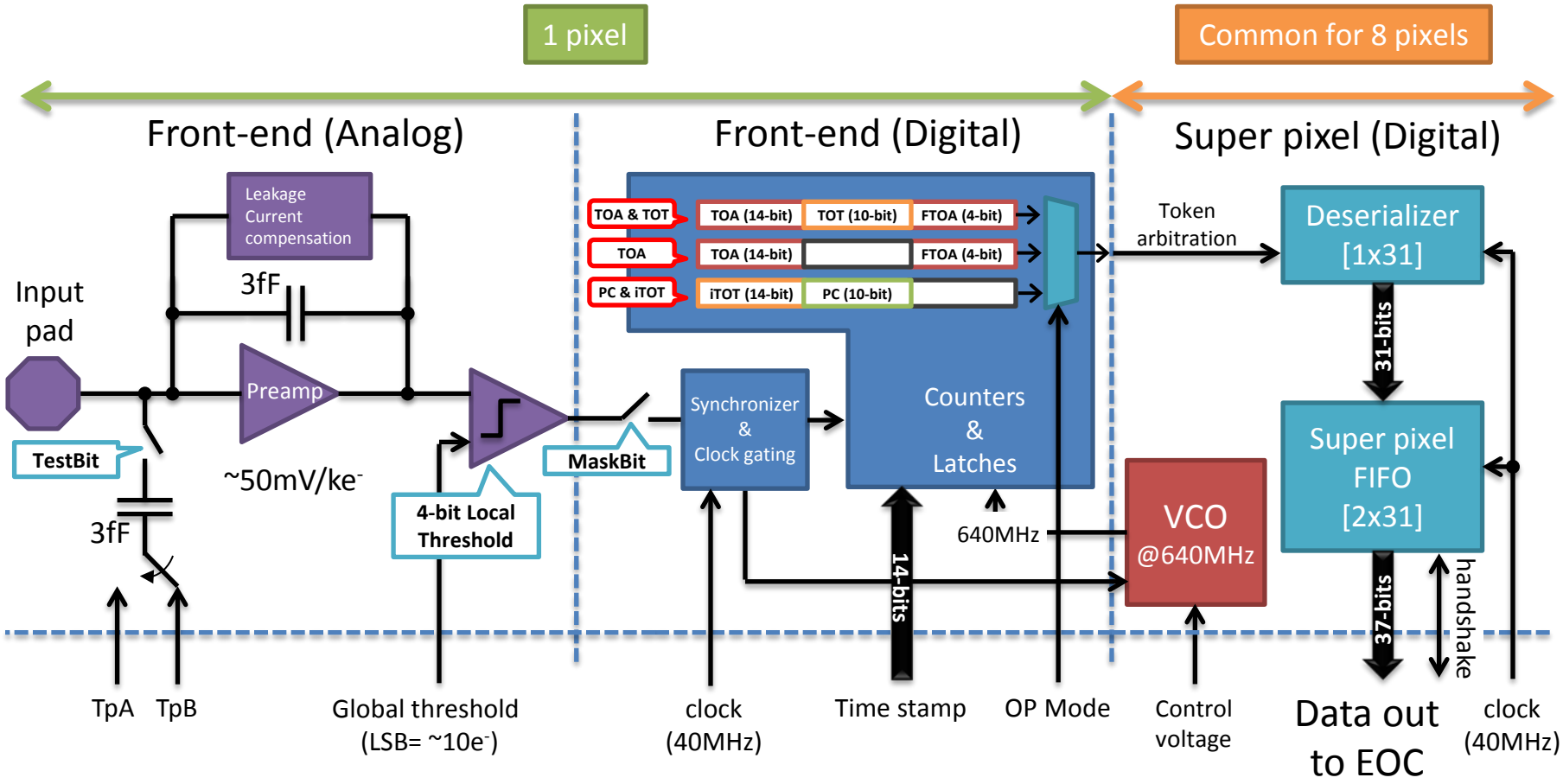

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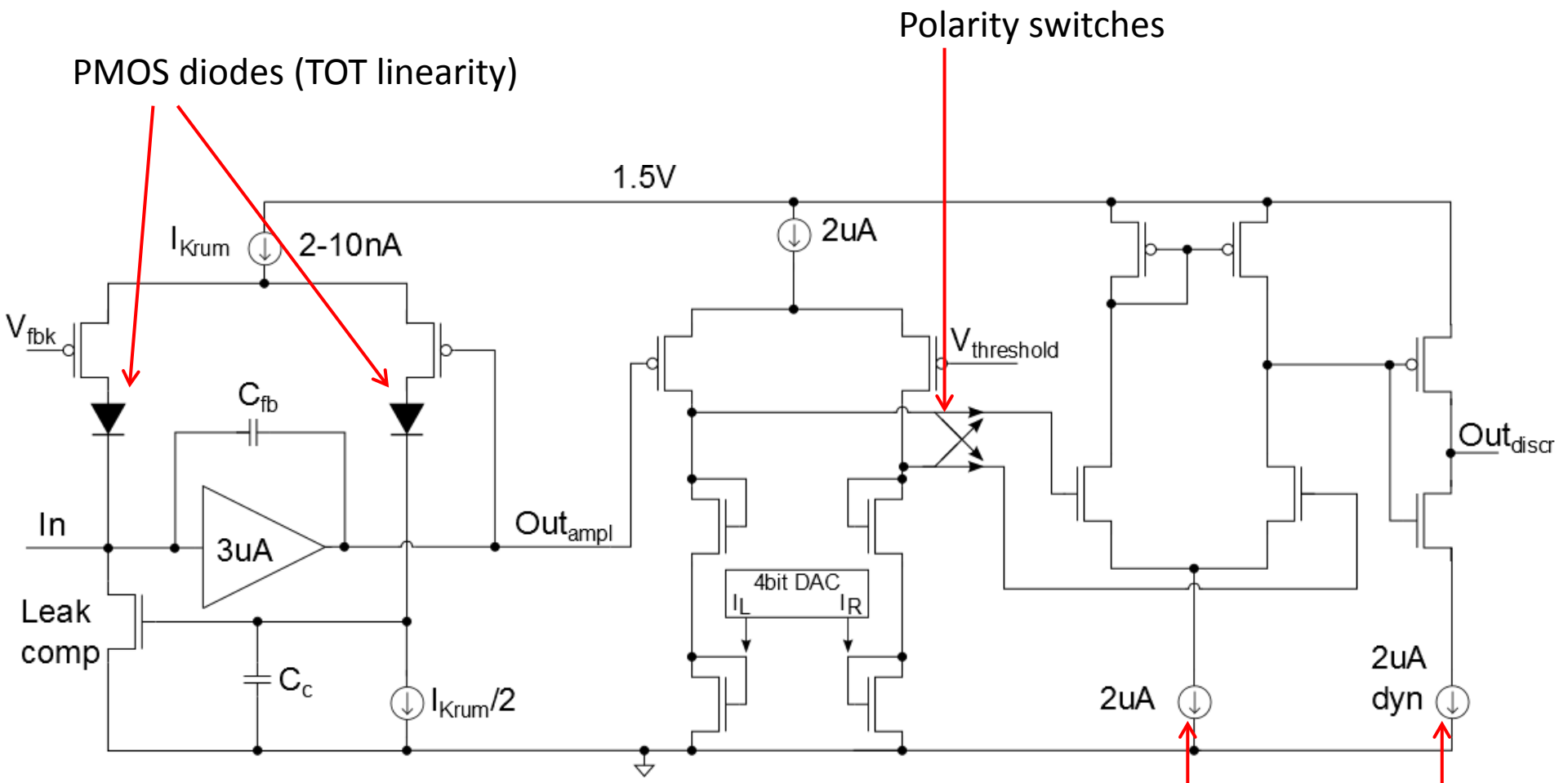
Front-end specifications

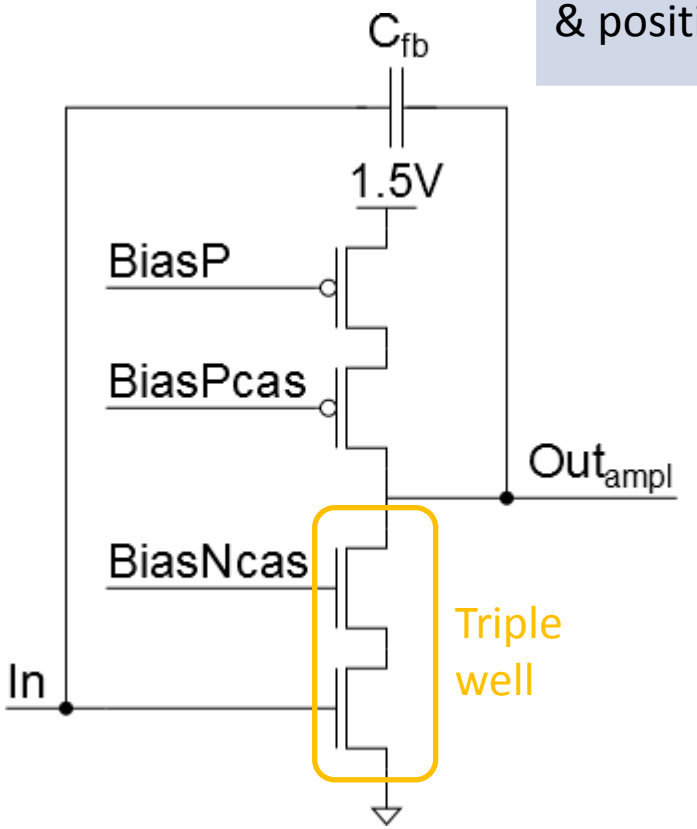
Parameter	Value	Notes
Area	55μmx13.5μm	
Signal polarity	Positive and negative	
Detector capacitance	~50fF	25fF to 100fF
Leakage current	-5nA to +20nA	
Amplitude linearity	Not required	Time measurement
TOT monotonicity	Yes, up to 300kh^{+}	
ToA jitter and mismatch	Compatible with 1.56ns resolution	Gas detector applications
Time-to-peak	Target 25ns	In view of VELOpix
Noise + threshold mismatch	~90e^{-}	for a minimum threshold ~500e^{-}
Equalization DACs	4bit	Compensate pixel-to-pixel threshold mismatch
Power consumption	12μW/pixel	

Front-end architecture



Timepix/Timepix3: preamplifier

	Timepix	Timepix3	Notes
Preamplifier	Differential	Single-ended	More efficient power usage
C_{fb}	8fF	3fF	Larger gain
Input pad size & positioning	20x20µm, over analog domain	12x12µm, over digital domain	Minimize parasitics, shielding to analog ground

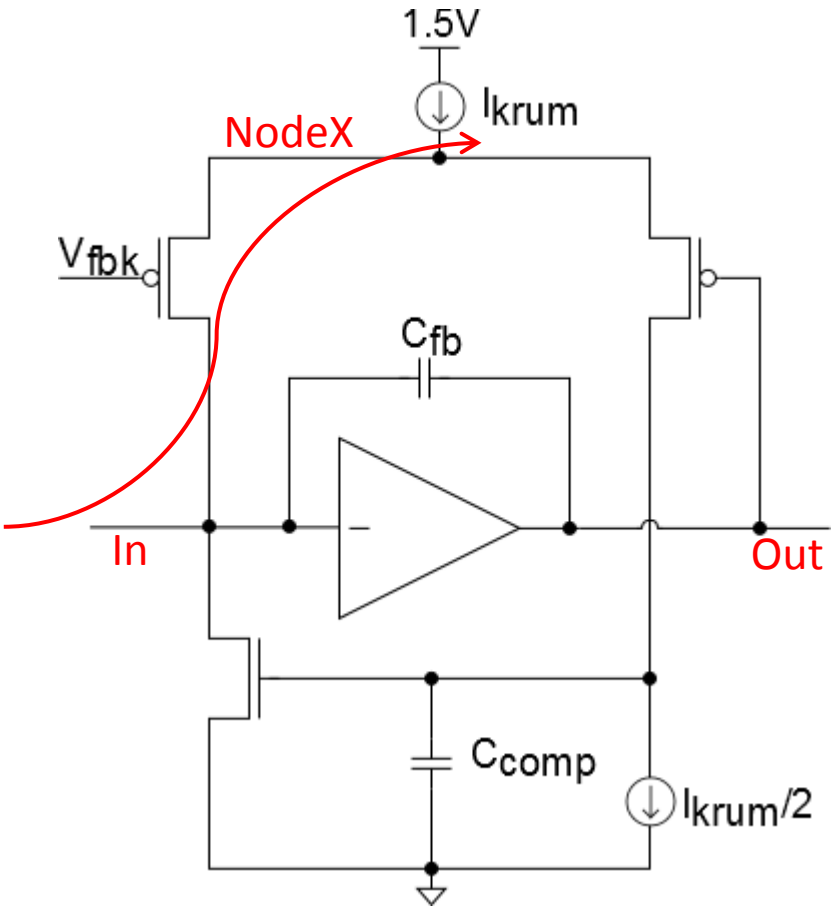


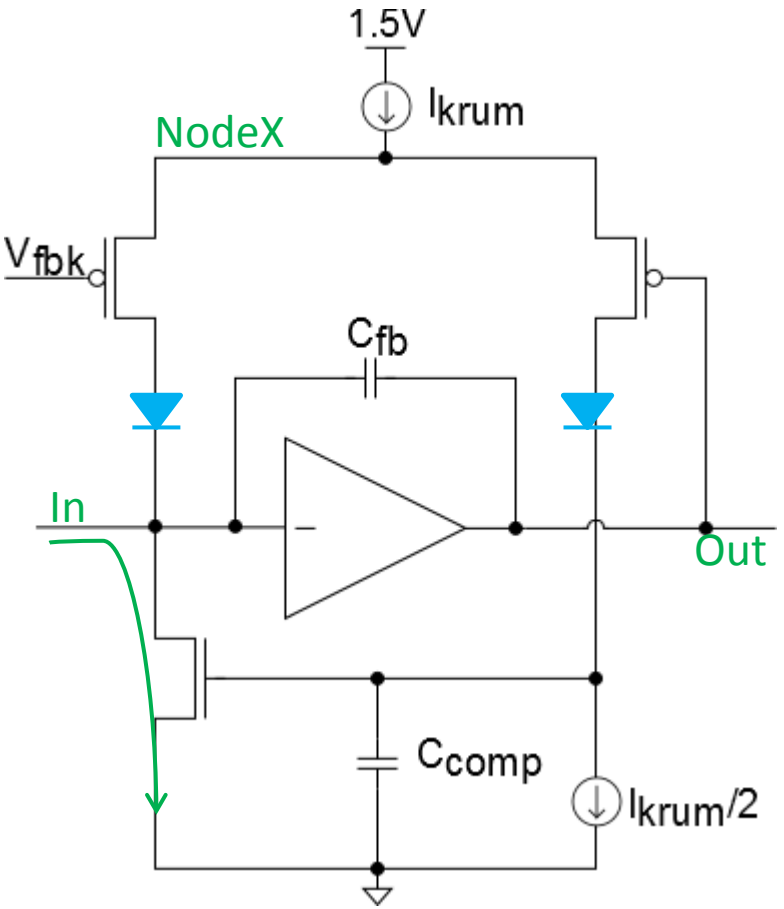
TOT monotonicity

TOT monotonicity issue for large positive input charges:

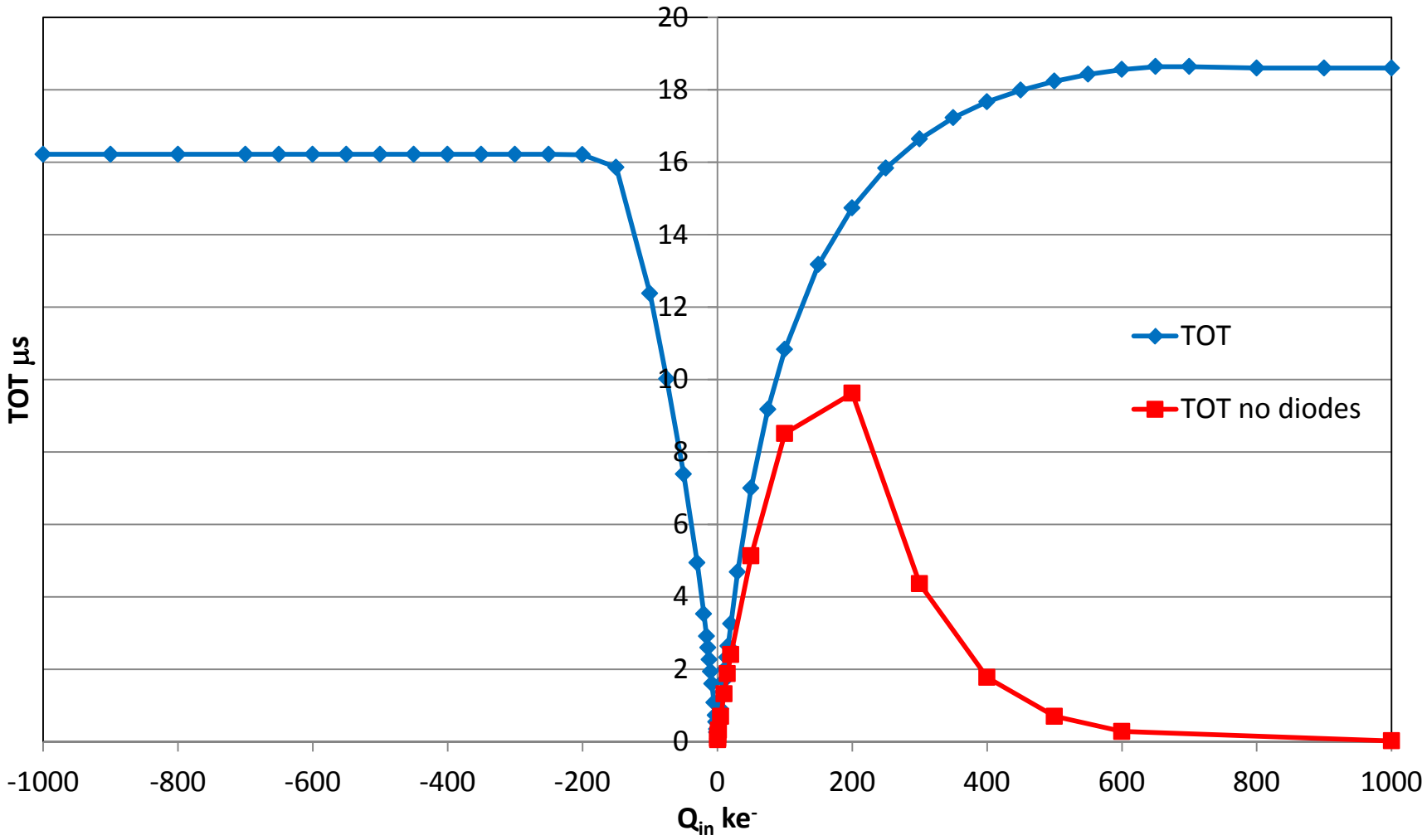
Q_{in}>100kh^{+} → V(In)>V(NodeX) → current through the wrong path

Added diode-connected PMOS transistors → good current path





TOT monotonicity



Comparison between TOT with and without monotonicity PMOS diodes.

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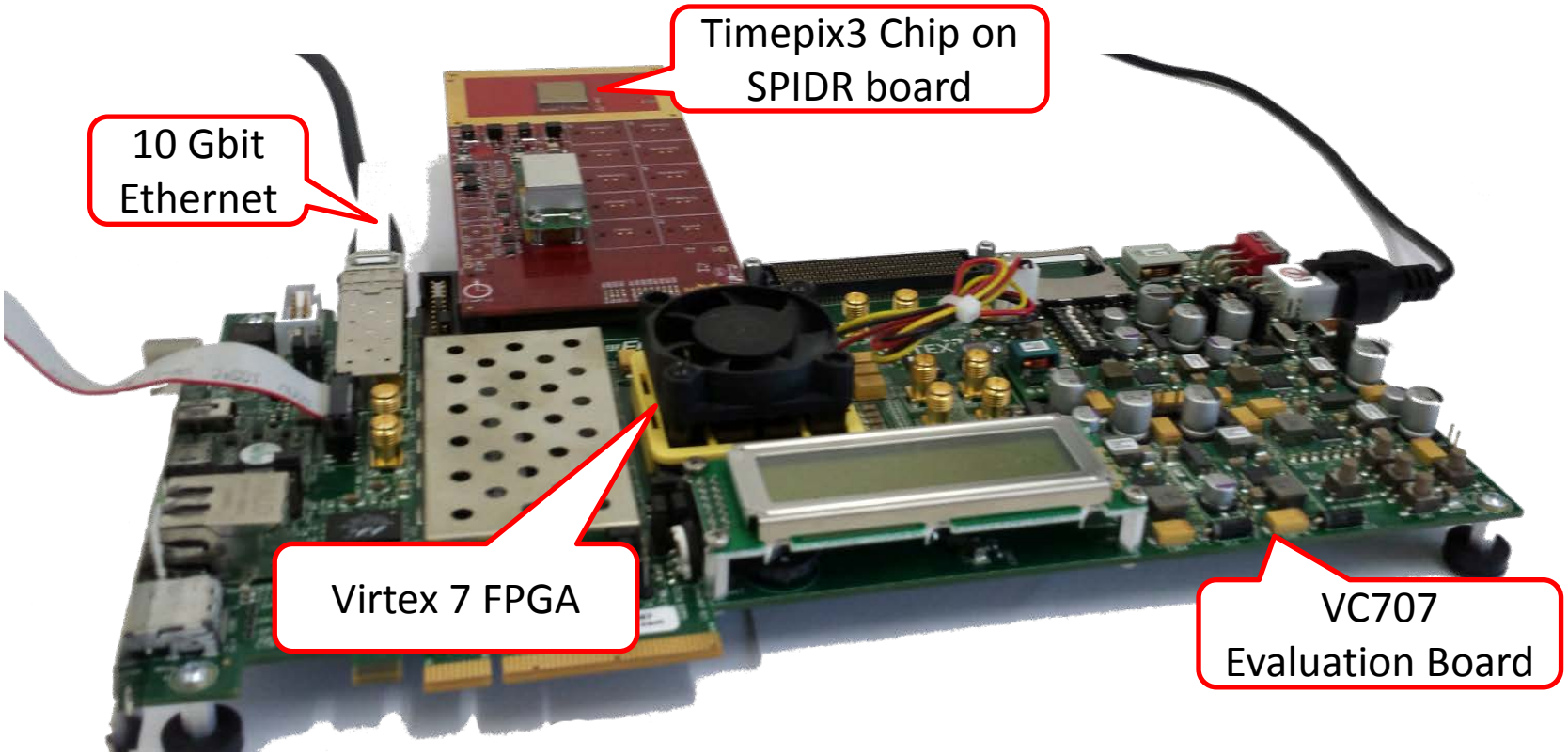
Test setup



SPIDR: Speedy PIxel Detector Readout

Developed for Timepix3 (from single chips up to quads)

1 x 10Gbps Ethernet link IO

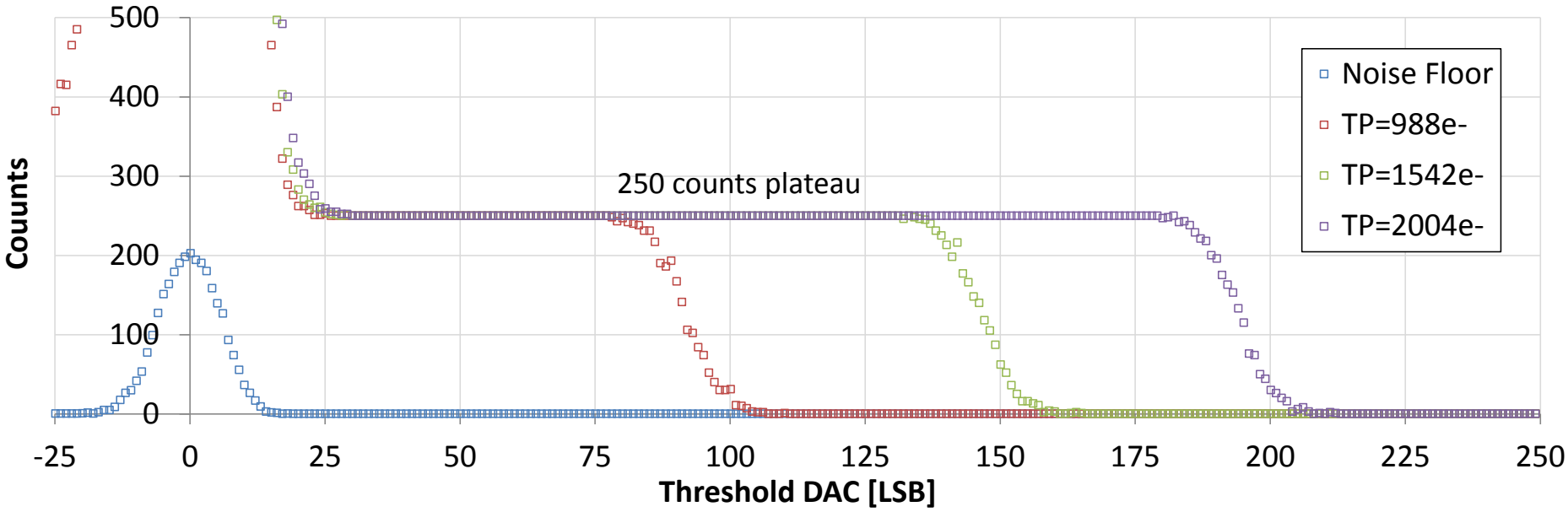
Credits:

Bas van der Heijden, Frans Schreuder, Henk Boterenbrood (NIKHEF)

Szymon Kulis (CERN)

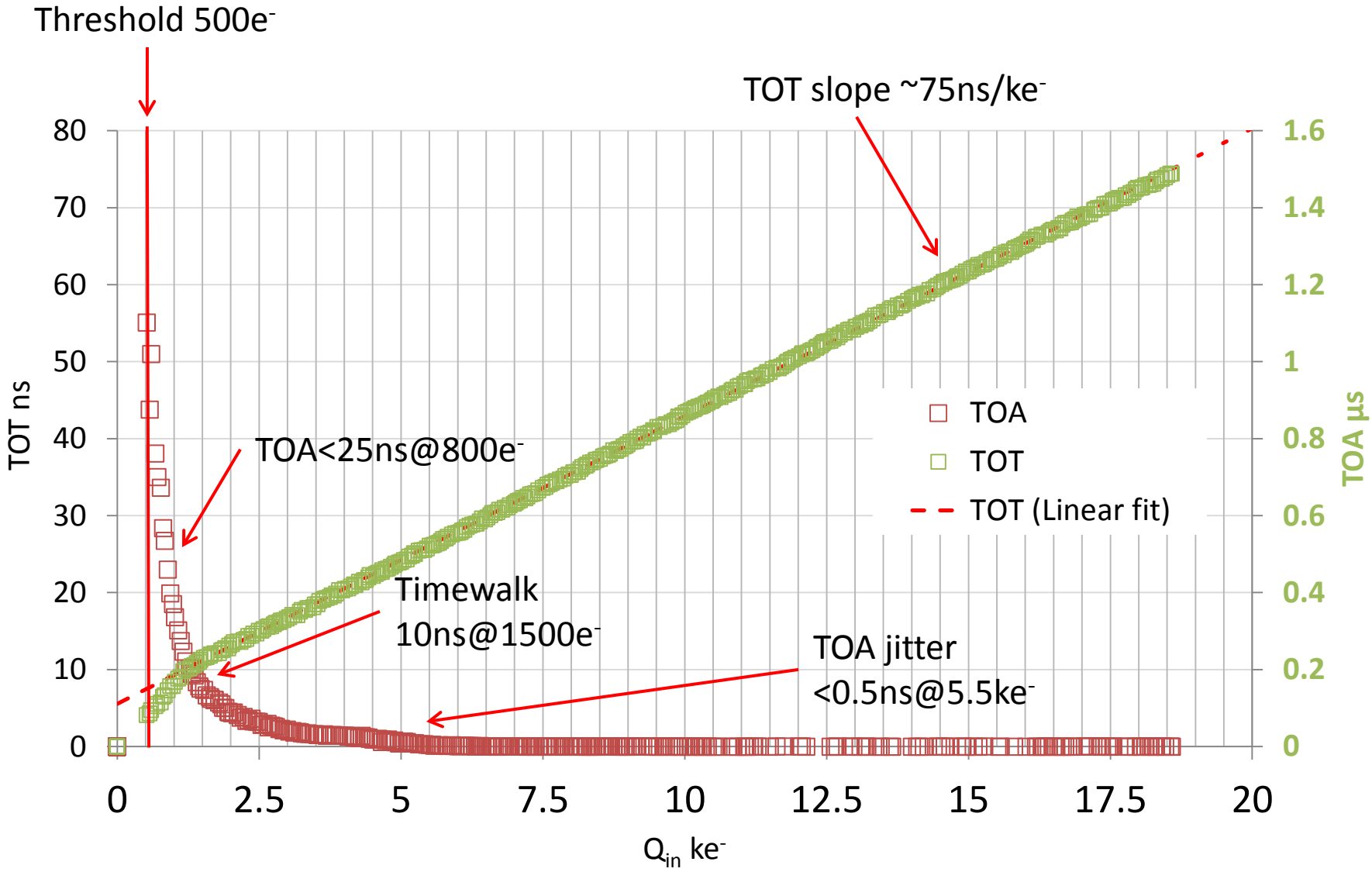
S-curves

X. Llopart



250 test pulses injected and counted in Photon Counting mode
ENC extracted from the S-width: 5.7LSB = 64e^- rms

Timewalk and TOT linearity



Measurements using test pulses, averaged over 64 acquisitions

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  300μm Silicon P-on-N
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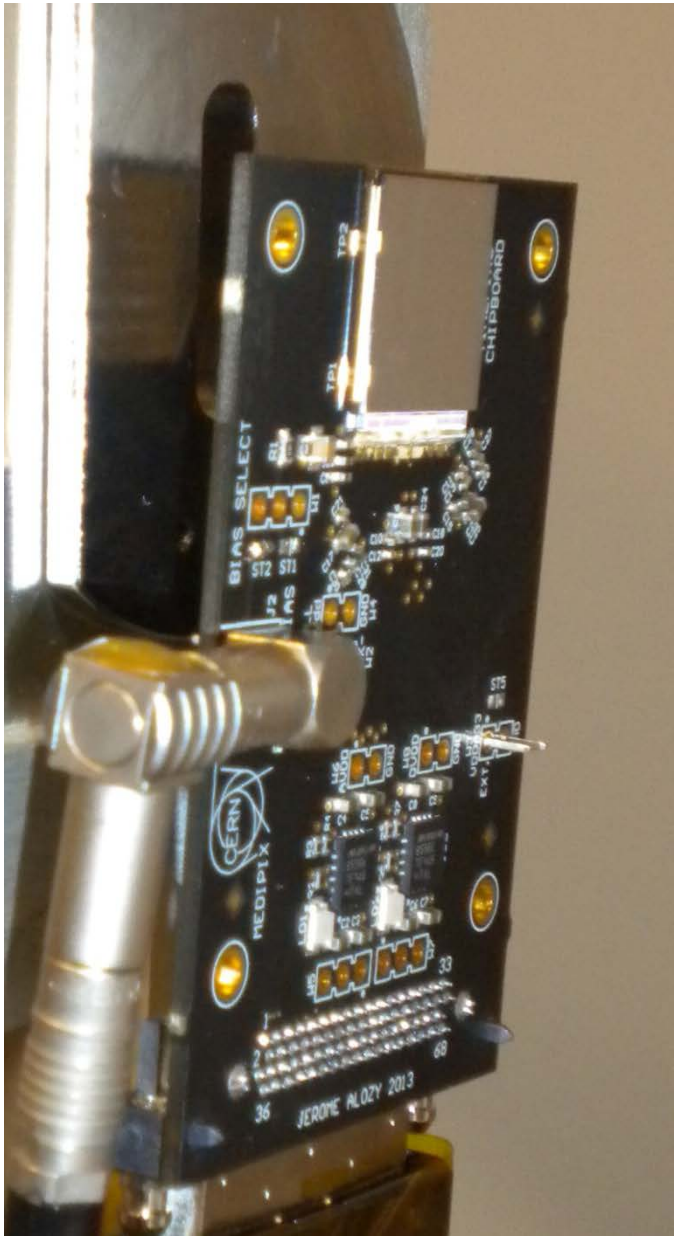
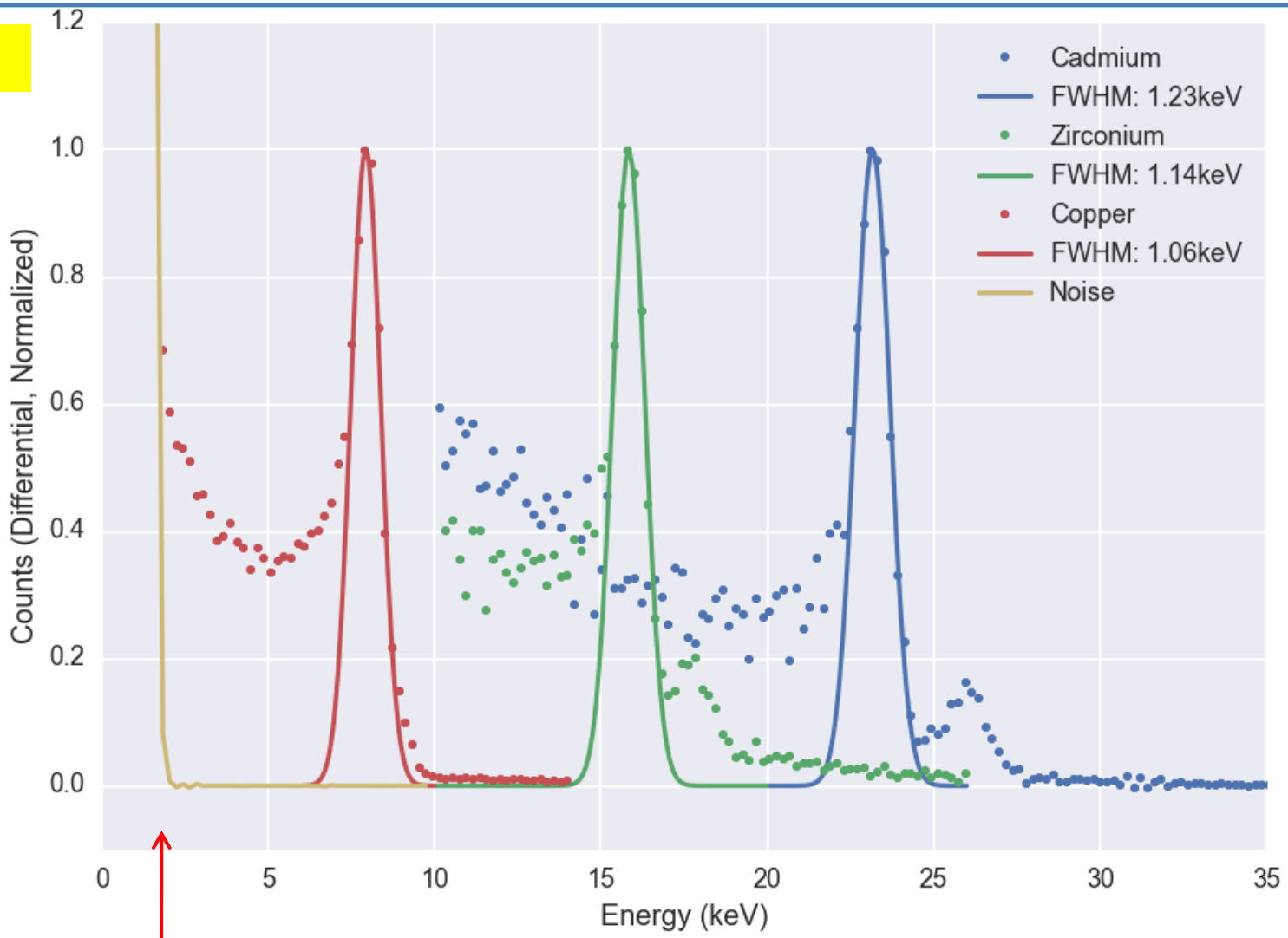


Fluorescence measurements (65k pixels)

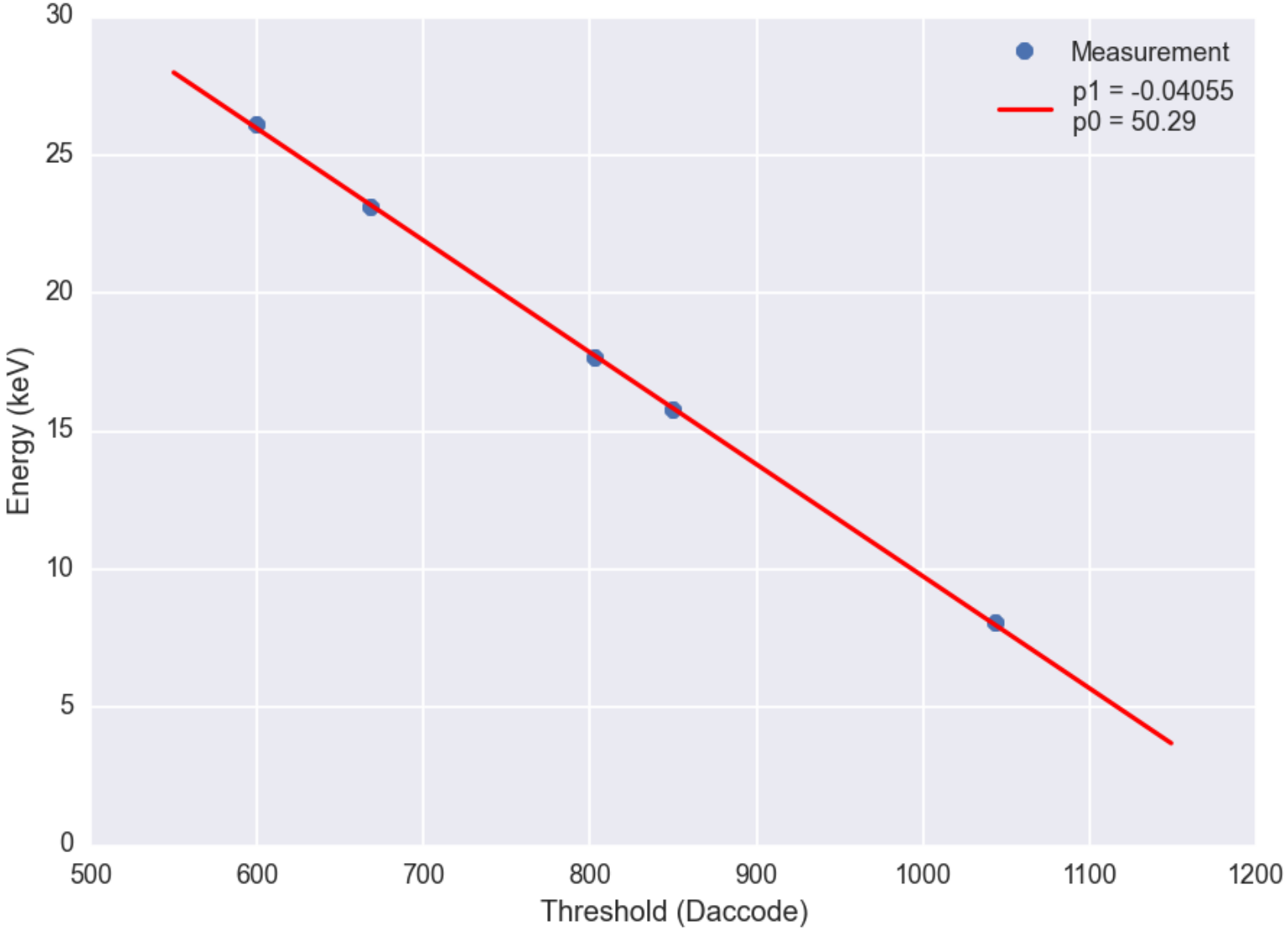
E. Fröjdh



Noise hits start at 2keV=550e$^-$

FWHM ➔ energy resolution σ=124e$^-$ (Cu)
Equalization using noise floor
Charge measured over full matrix

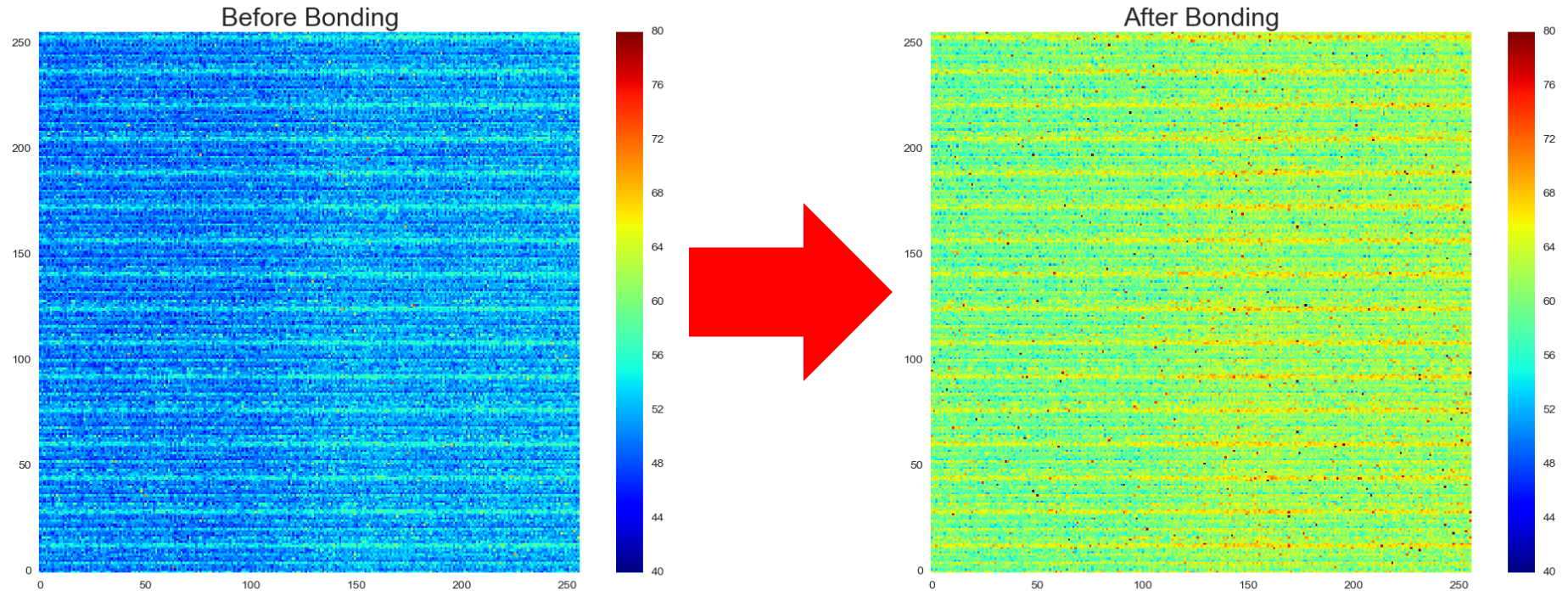
Gain calibration using fluorescence (65k pixels)



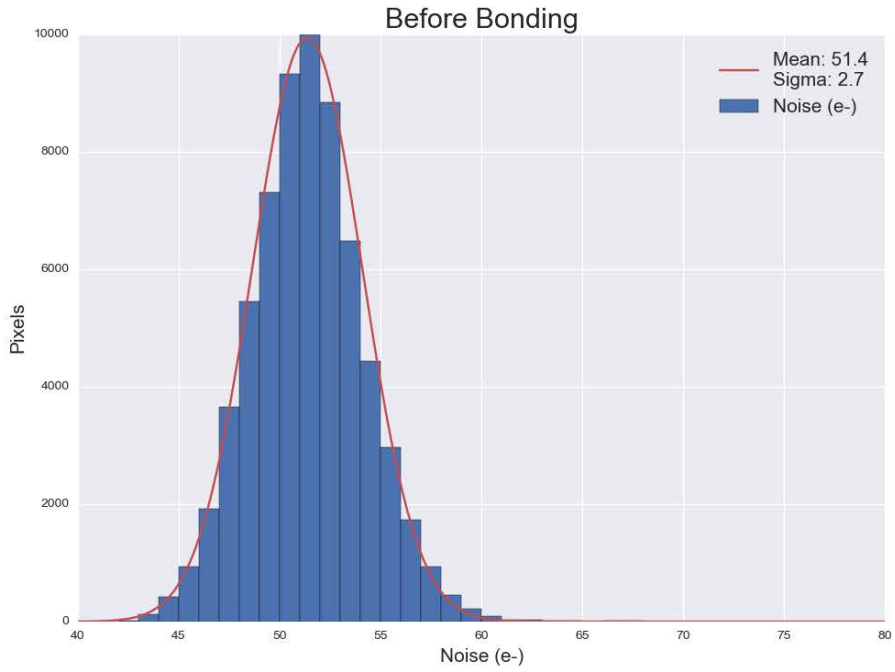
40.5eV/LSB = 11.2e^-/LSB = 44.6mV/ke^-

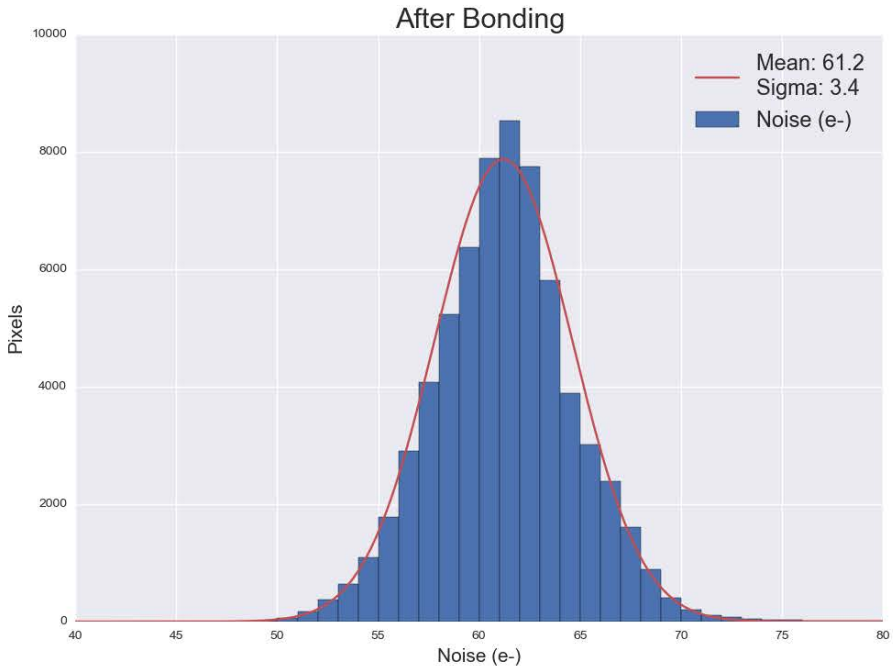
Noise map before/after bonding

Same chip measured at wafer level and after sensor bonding:



Noise distribution

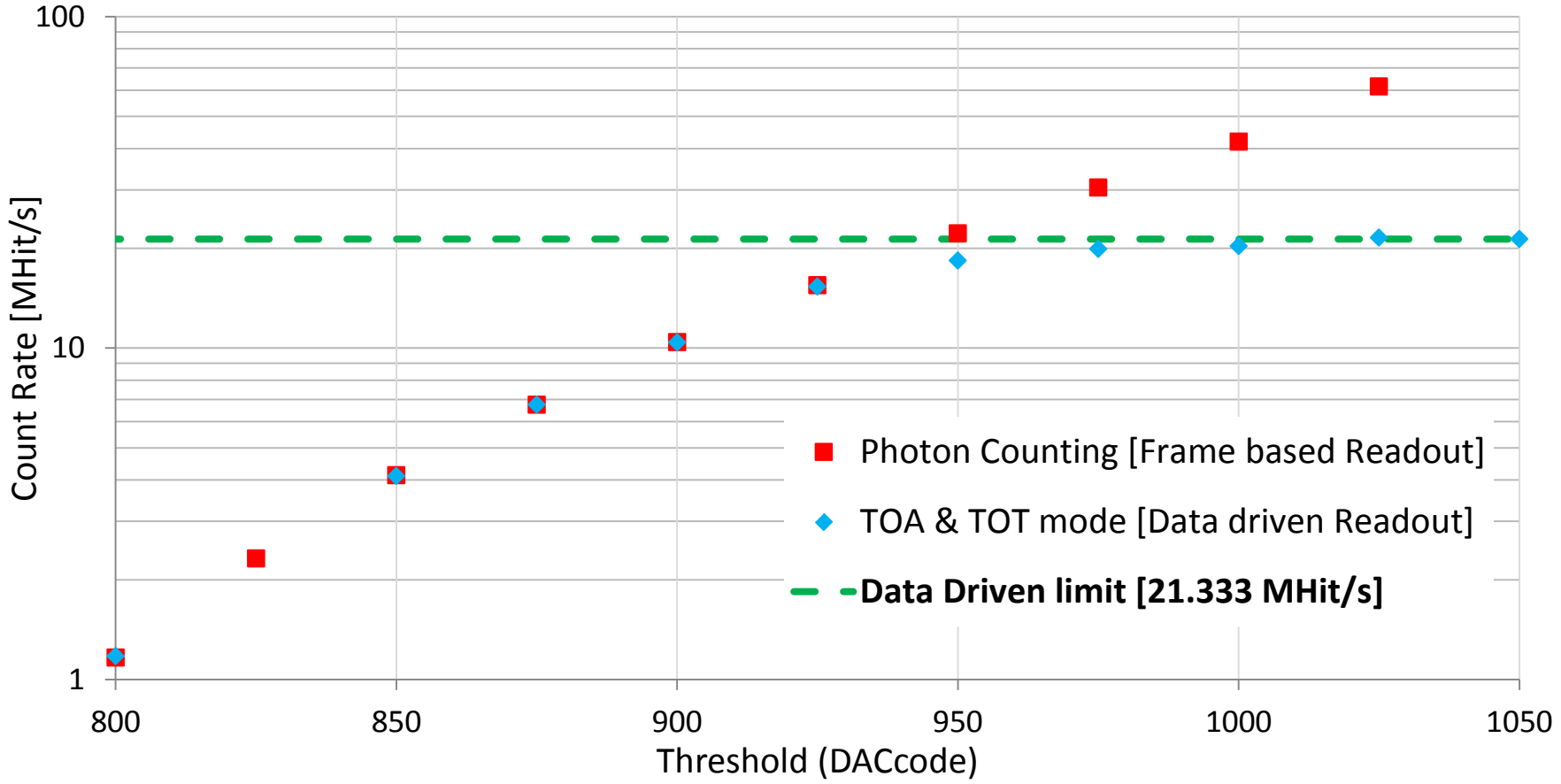




Average noise over the full matrix increases by 10e^- only. Its distribution widens a little bit.

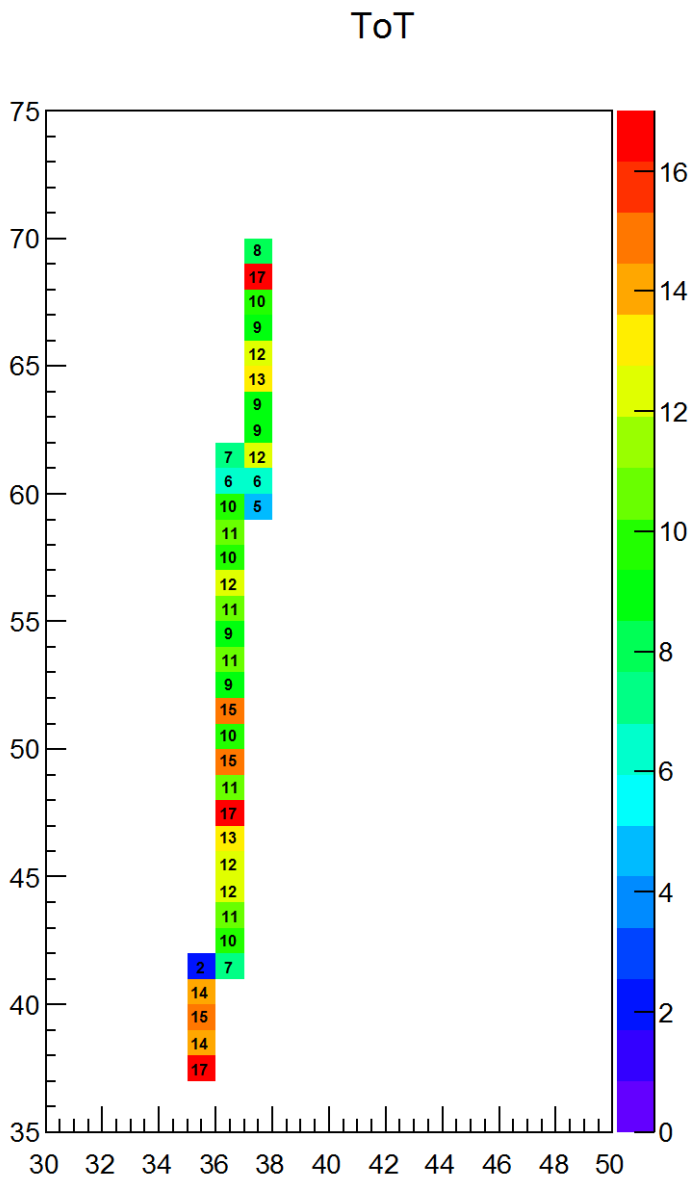
Count rate

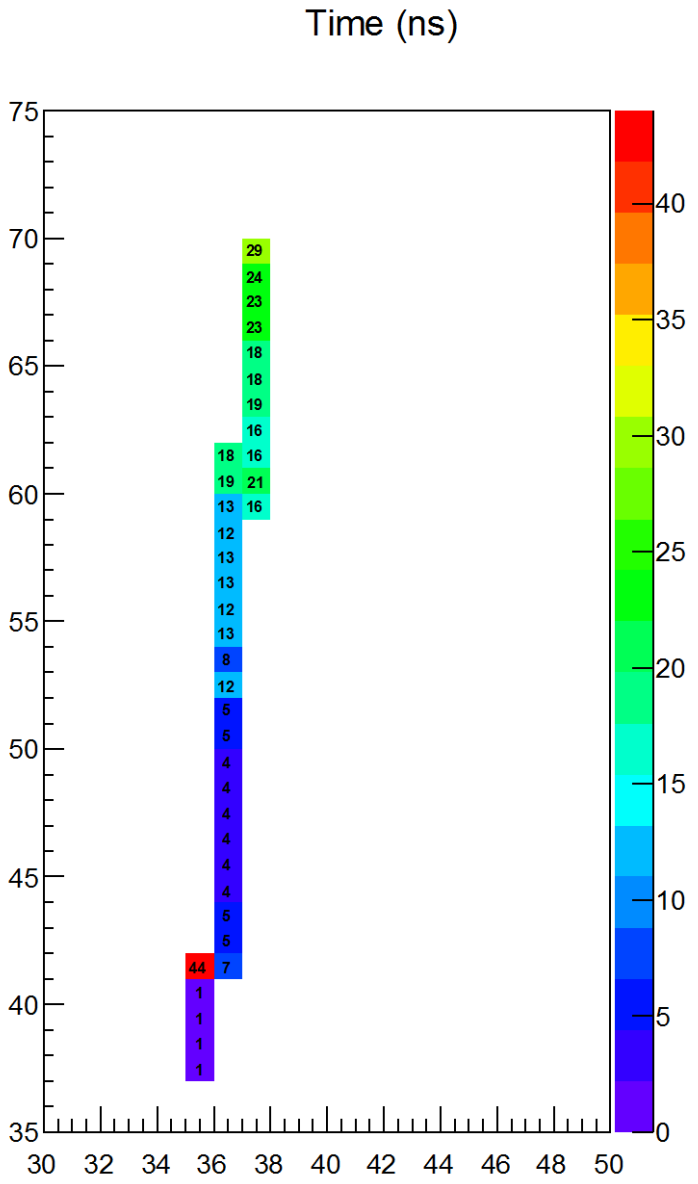
Measurement done with a Cu X-ray tube
Count rate modulated by adjusting the global threshold



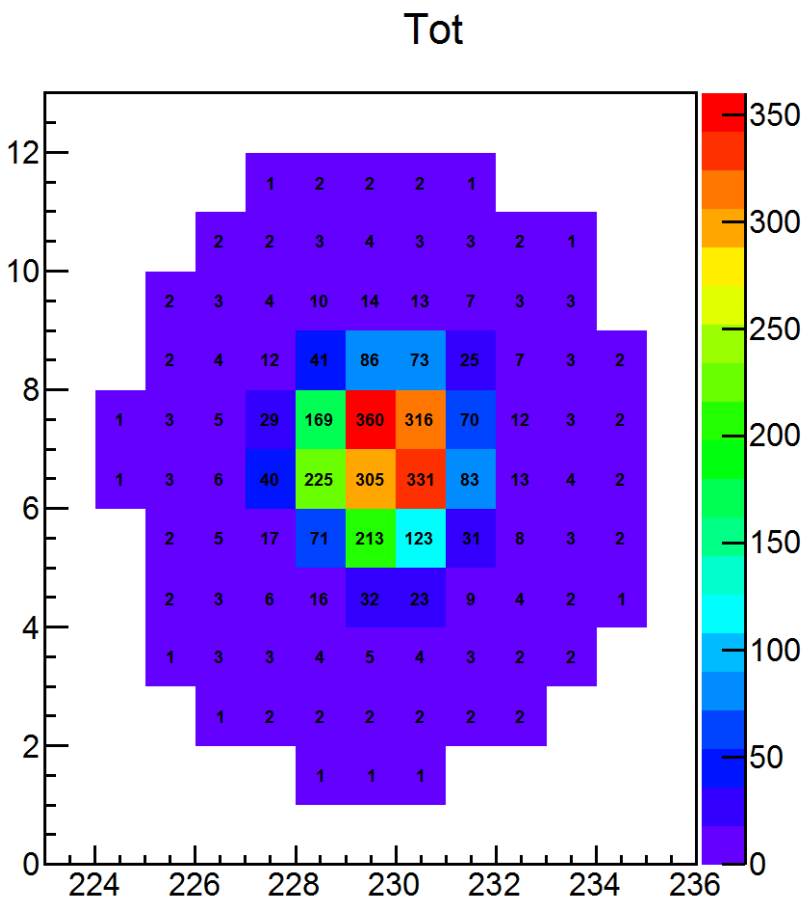
TOA & TOT mode limited by output block bandwidth (set at 8x160Mbps for this measurement)
Maximum count rate possible is **85.33 Mhit/s** @ 8x640Mbps links (43MHits/s/cm^2)

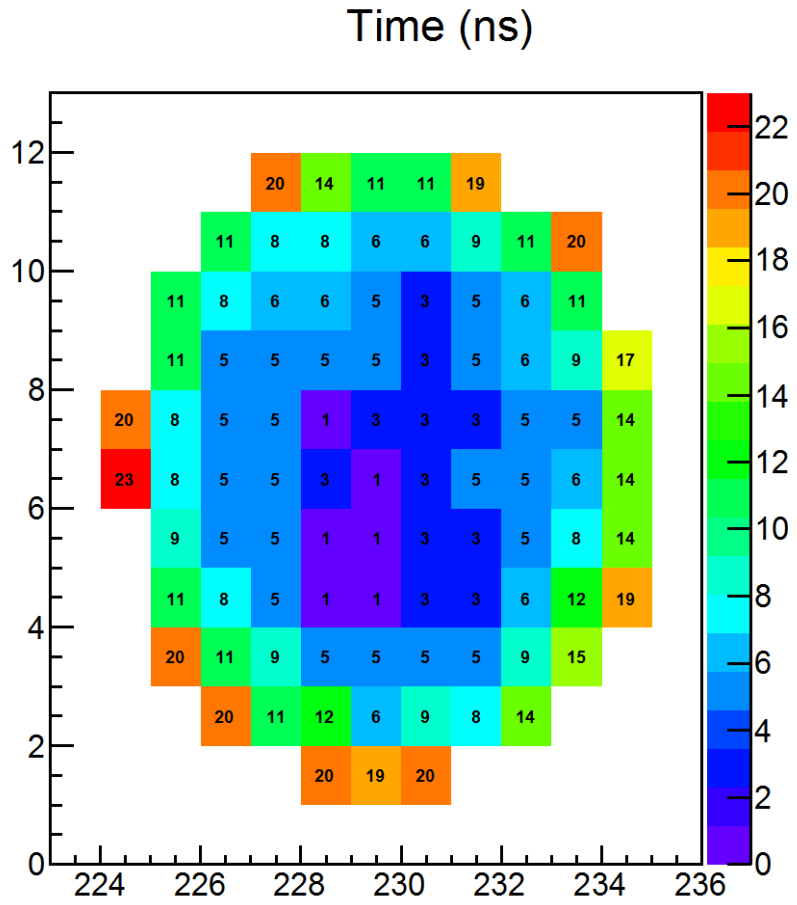
MIP (cosmic)


ToT
75
70
65
60
55
50
45
40
35
30 32 34 36 38 40 42 44 46 48 50
16
14
12
10
8
6
4
2
0


Time (ns)
75
70
65
60
55
50
45
40
35
30 32 34 36 38 40 42 44 46 48 50
40
35
30
25
20
15
10
5
0

Alpha particle





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Summary

- Timepix3 designed and fabricated in 2013
- Tests on bare chips and on wafers give good results
- First measurements with 300µm Silicon sensors look promising

	Bare chip	With 300µm Silicon sensor
Noise	51.4±2.7 e^- rms	61.2±3.4 e^- rms
Threshold mismatch (equalized)	35e^-	35e^-
Minimum threshold	500e^-	550e^-
TOT mismatch	6.5% rms	
Timewalk (1ke^- above threshold)	10ns	
TOA < 25ns	Charge > 0.8ke^-	
TOA jitter < 0.5ns	Charge > 5.5ke^-	
Energy resolution		124e^- (Cu) with equalization on noise floor
Maximum count rate		85 Mhit/s (43MHits/s/cm^2)

Thanks for your time and attention!

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Massimiliano De Gaspari for the CERN Medipix team (J Alozy, R Ballabriga, M Campbell, E Fröjdh, J Idarraga, S Kulis, X Llopart, T Poikela, P Valerio, W Wong) in collaboration with NIKHEF and the University of Bonn.

Thanks for your time and attention!

References:

- M. De Gaspari *et al.*

"Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130 nm CMOS technology," 2014 *JINST* 9 C01037

- T. Poikela *et al.*

"Digital column readout architectures for hybrid pixel detector readout chips," 2014 *JINST* 9 C01007

- Y. Fu *et al.*

"The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC," 2014 *JINST* 9 C01052

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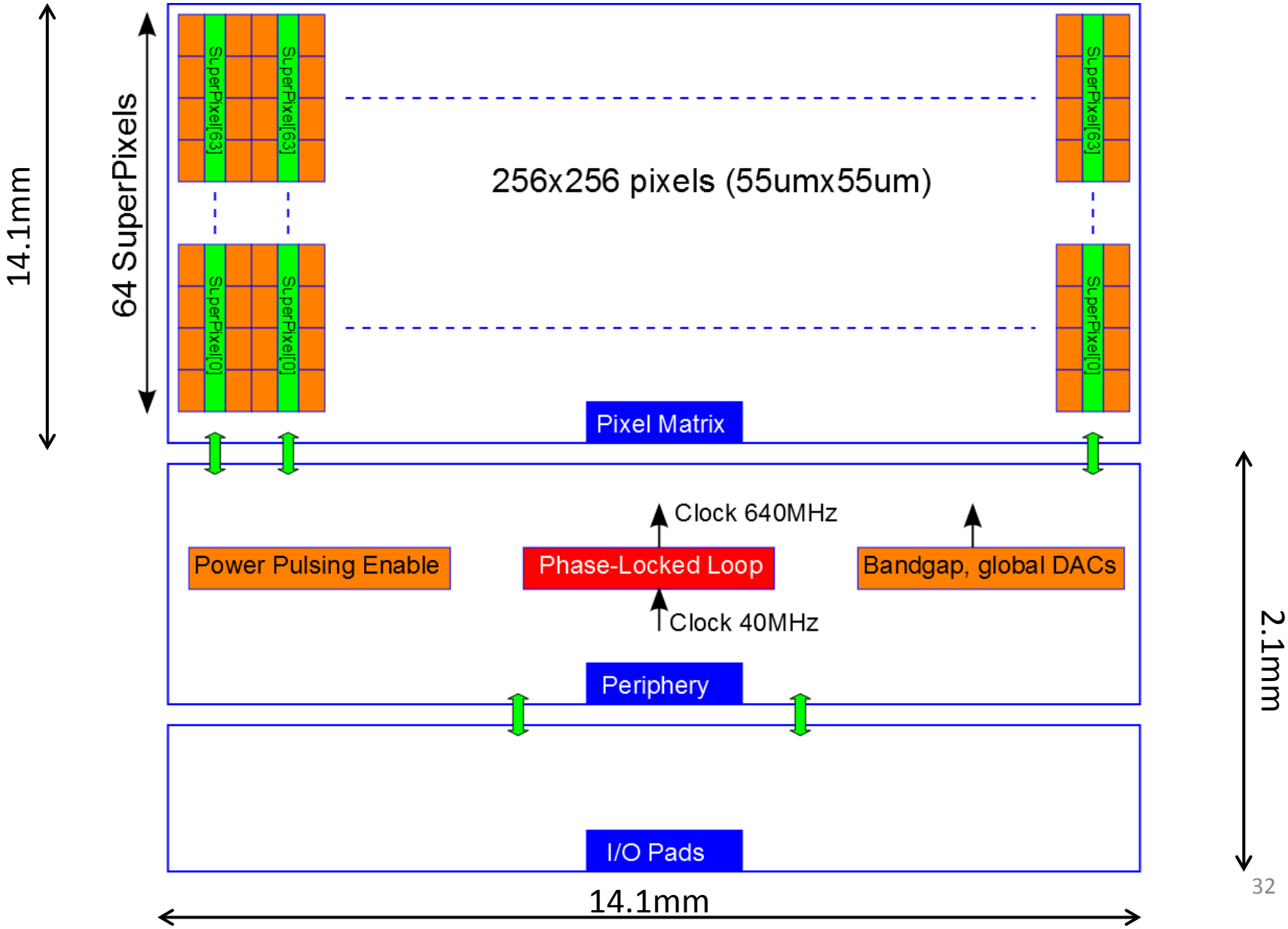
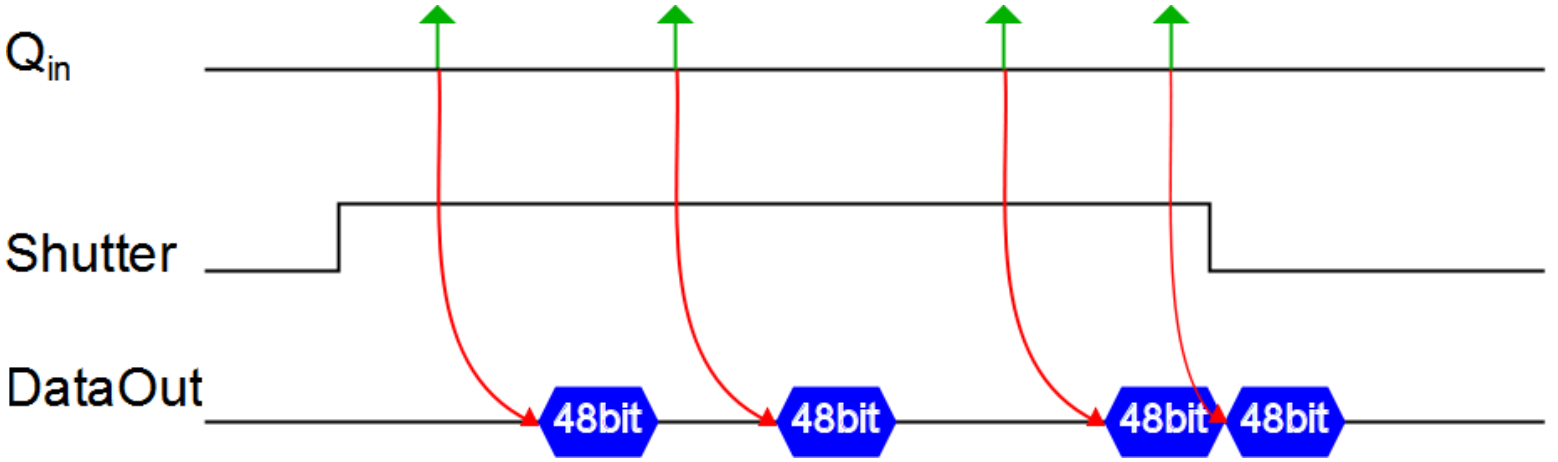
- Back up slides

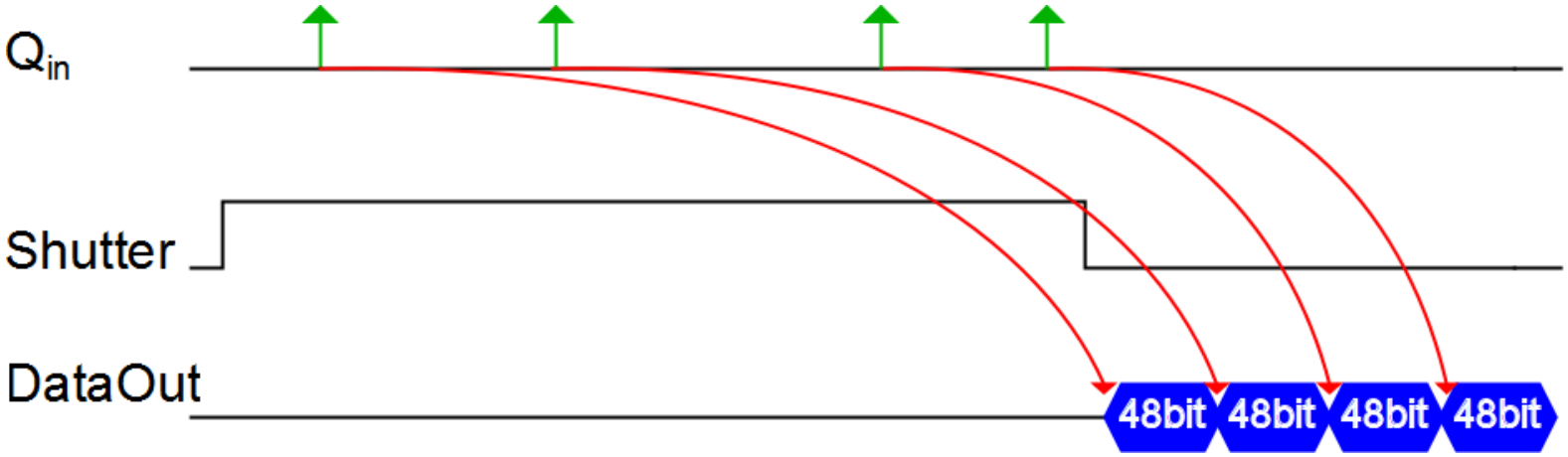
Timepix3 floorplan



Readout modes

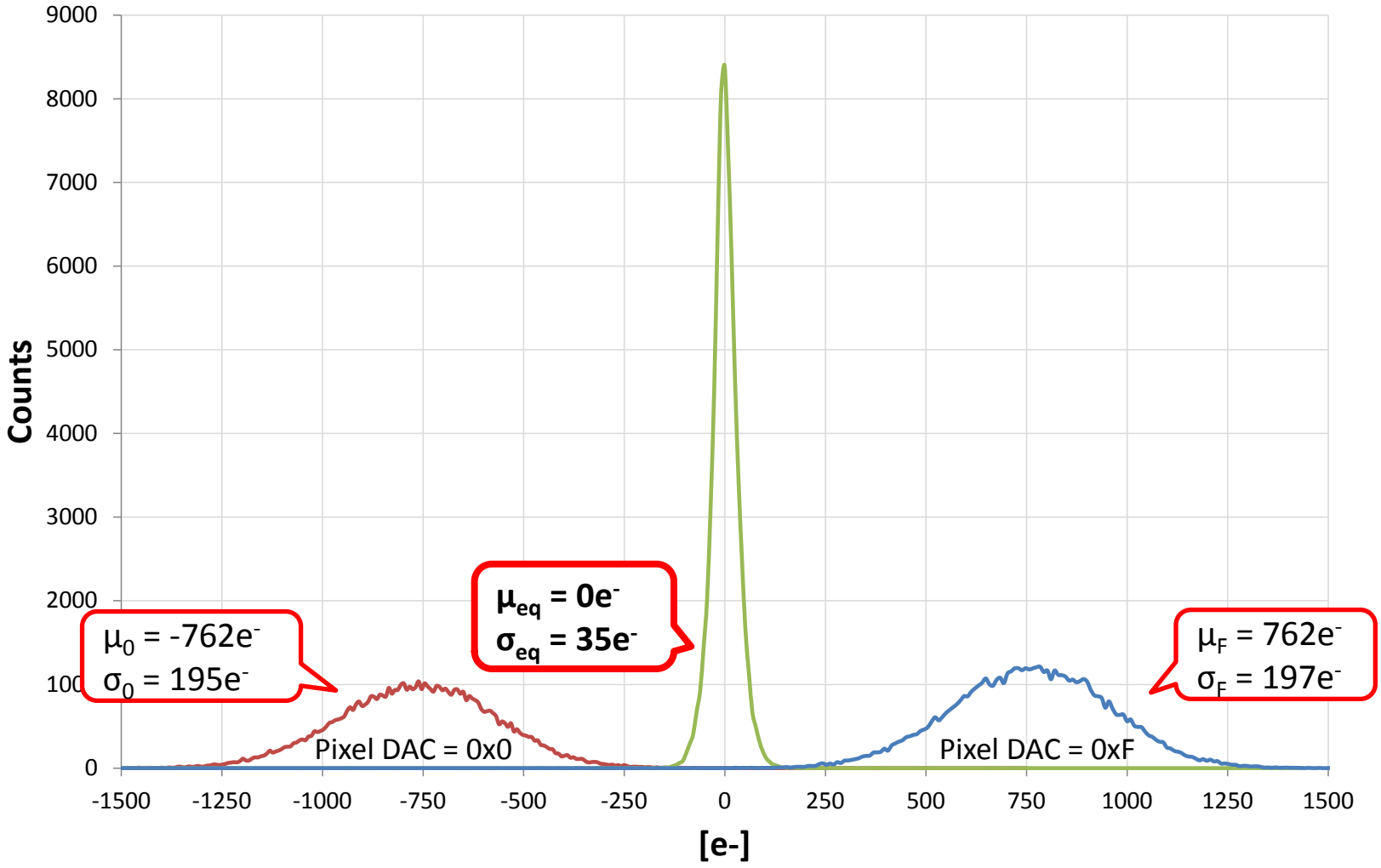


Data-driven readout mode.

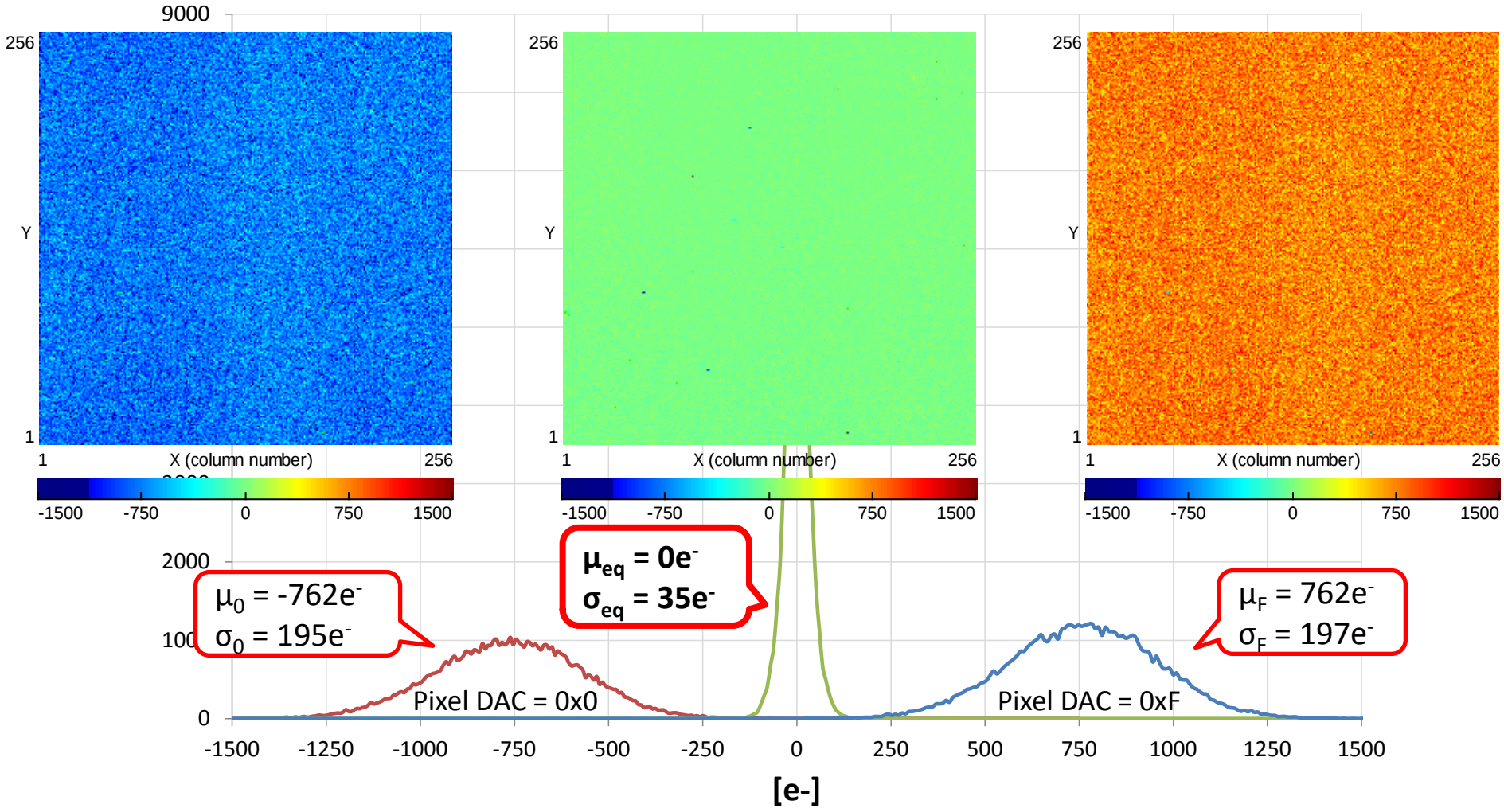


Sequential frame-based mode.

Threshold equalization



Threshold equalization



Fluorescence measurements