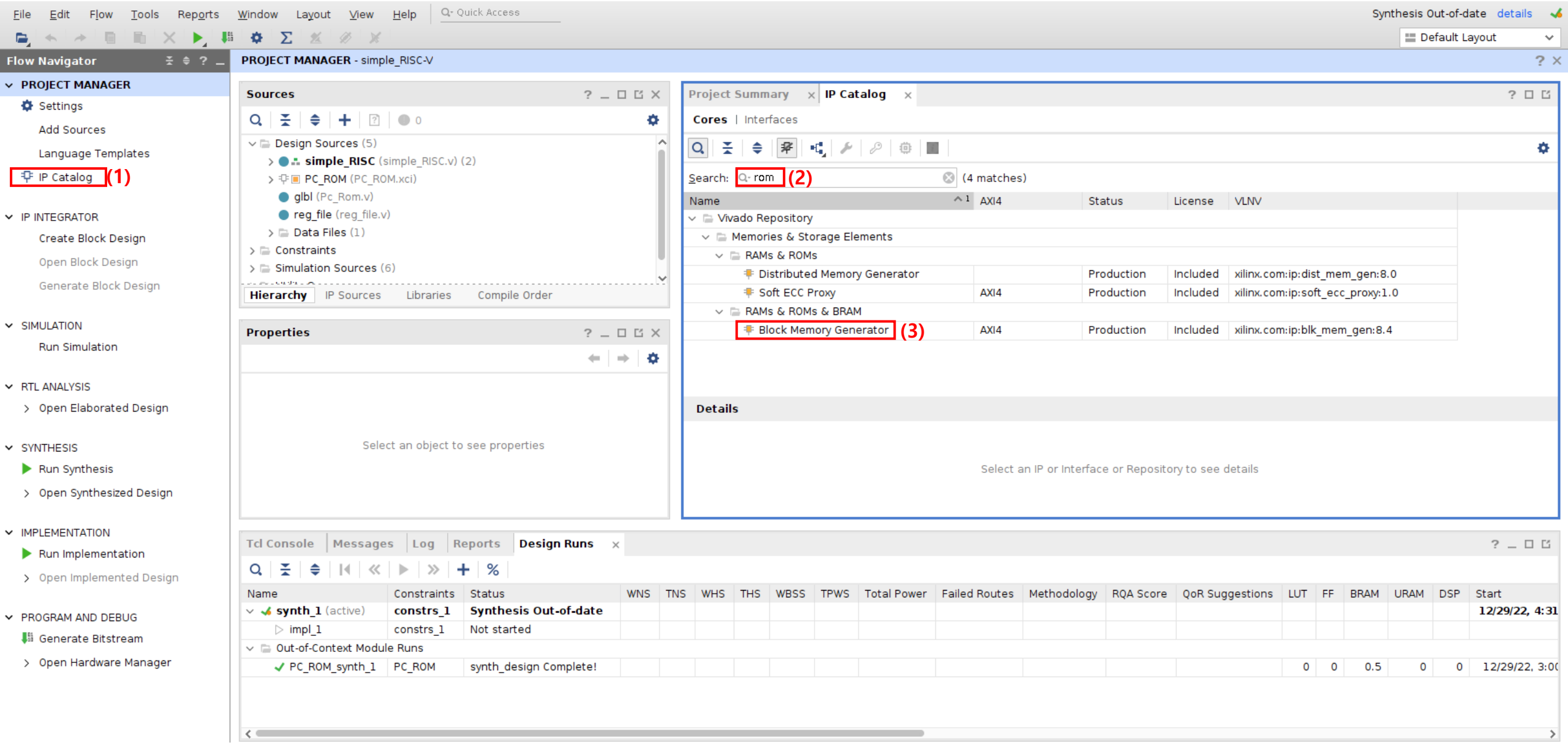
Generating Black rom/ram with Vivado


File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog (1)
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - simple_RISC-V
Sources
Design Sources (5)
simple_RISC (simple_RISC.v) (2)
PC_ROM (PC_ROM.xci)
glbl (Pc_Rom.v)
reg_file (reg_file.v)
Data Files (1)
Constraints
Simulation Sources (6)
Hierarchy IP Sources Libraries Compile Order
Properties
Select an object to see properties
Project Summary
IP Catalog
Cores | Interfaces
Search: rom (2)
(4 matches)
Name AXI4 Status License VLNV
Vivado Repository
Memories & Storage Elements
RAMs & ROMs
Distributed Memory Generator Production Included xilinx.com:ip:dist_mem_gen:8.0
Soft ECC Proxy AXI4 Production Included xilinx.com:ip:soft_ecc_proxy:1.0
RAMs & ROMs & BRAM
Block Memory Generator (3) AXI4 Production Included xilinx.com:ip:blk_mem_gen:8.4
Details
Select an IP or Interface or Repository to see details
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS WBSS TPWS Total Power Failed Routes Methodology RQA Score QoR Suggestions LUT FF BRAM URAM DSP Start
synth_1 (active) constrs_1 Synthesis Out-of-date 12/29/22, 4:31
impl_1 constrs_1 Not started
Out-of-Context Module Runs
PC_ROM_synth_1 PC_ROM synth_design Complete! 0 0 0.5 0 0 12/29/22, 3:0

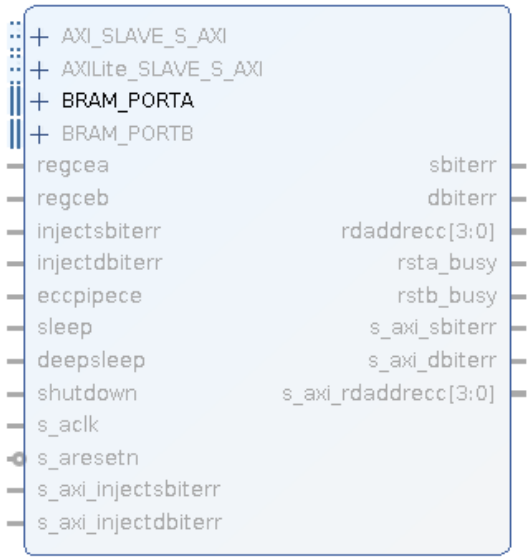
Customize IP (on saturn)

Block Memory Generator (8.4)

Documentation | IP Location | Switch to Defaults

IP Symbol | Power Estimation

Show disabled ports



Component Name: blk_mem_gen_0

Basic | Port A Options | Other Options | Summary

Interface Type: Native

Generate address interface with 32 bits

Memory Type: Single Port RAM

Common Clock

- Single Port RAM
- Simple Dual Port RAM
- True Dual Port RAM
- Single Port ROM
- Dual Port ROM

ECC Options

ECC Type

Error Inj... Injection

Write Enable

Byte Write Enable

Byte Size (bits): 9

Algorithm Options

Defines the algorithm used to concatenate the block RAM primitives.
Refer datasheet for more information.

Algorithm: Minimum Area

Primitive: 8kx2

OK | Cancel

Block Memory Generator (8.4)

Documentation | IP Location | Switch to Defaults

IP Symbol | **Power Estimation**

Show disabled ports

Component Name: PC_ROM

Basic | **Port A Options** | **Other Options** | **Summary**

Pipeline Stages within Mux: 0 — Mux Size: 1x1

Coe fle is needed

Memory Initialization

- [x] Load Init File

Coe File: ../../../simple_RISC-V.srcs/sources_1/new/ROM.coe — Browse — Edit

- [ ] Fill Remaining Memory Locations

Remaining Memory Locations (Hex): 0

Structural/UniSim Simulation Model Options

Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.

Collision Warnings: All

Behavioral Simulation Model Options

- [ ] Disable Collision Warnings
- [ ] Disable Out of Range Warnings

OK | Cancel