Huabin Wu

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Education

Stony Brook University - SUNY **Stony Brook, NY**

Bachelor of Engineering in Computer Engineering; GPA: 3.71 *Expected May 2026*

- **Relevant Coursework**: Computer Architecture, Advanced Digital System Design & Generation, Design of Secure IoT Embedded Systems, Real-Time Operating Systems, Digital Design Using VHDL & PLDs, PCB Design & Prototyping, Electrical Circuit Analysis

Technical Skills

Programming Languages: C/C++, Python, SystemVerilog, VHDL, Assembly (AVR, MIPS), Bash, TCL, MATLAB
Development Tools: VS Code, Git, Docker, Doxygen, Linux/Unix (User, Kernel), Xilinx Vivado, Siemens QuestaSim, Synplify Pro, Cadence Virtuoso, Altium Designer, LTspice, Autodesk Fusion 360, AWS IoT
Hardware Platforms & Lab: Microcontrollers (ARM Cortex, AVR, ESP) FPGAs/PLDs, PCB Prototyping, Oscilloscope, Logic Analyzer

Work Experience

Department of Electrical & Computer Engineering at Stony Brook University **Stony Brook, NY**

Teaching Assistant for Embedded Microcontroller Systems Design I *Aug. 2025 – Dec. 2025*

- Guided students on debugging bare-metal AVR Assembly firmware by inspecting memory-mapped I/O registers in Microchip Studio, and validating signal integrity/timing using oscilloscopes and logic analyzers.
- Held weekly office hours, assisting students with troubleshooting hardware interrupts, UART/I2C/SPI serial protocol failures, and analyzing datasheets to comply with schematic designs.
- Developed reference firmware alongside TAs for lab assignments (LoRaWAN inventory management system with SerLCD display on AVR128DB48) to standardize grading criteria.

Metropolitan Transportation Authority (MTA) **Brooklyn, NY**

Signal Operations Intern *July 2024 – Aug. 2024*

- Developed Excel VBA automation scripts to interface with external printers, reducing manual label processing time for 5,000+ records by 90%.
- Managed a large-scale inventory audit of 5,000+ MTA Signal Department files, using Excel spreadsheet to organize maintenance data for the general superintendents.
- Assisted dispatchers with MTA BusTrek analytics to optimize the operational structure of over 200 NYCT bus routes, streamlining maintenance logistics that drove a 4.3% MTA Bus ridership increase.

Projects

Dual-Issue Sony Cell Synergistic Processor Unit (SPU) | *SystemVerilog, C++, QuestaSim* Jan. 2026 – Present

- Architected a 2-way superscalar RISC core processor based on the IBM/Sony Cell SPU ISA, featuring a 128-bit SIMD data path, 128-entry unified register file, and 32KB local store.
- Implemented a 11-stage pipeline with heterogeneous (Even/Odd pipe) execution units, hazard detection logic to handle dual-instruction dependency-checking, and full operand forwarding networks.
- Developed a custom Assembler in C++ to map Assembly mnemonics to machine code, enabling the simulation of full Assembly programs in QuestaSim.

Low-Power IC for Neuromorphic Computing | *PyTorch, Virtuoso, Spectre* Sept. 2025 – Present

- Designing a mixed-signal ReRAM accelerator in SkyWater 130nm for ultra-low power keyword spotting, targeting sub-mW consumption on edge devices.
- Trained a Spiking Neural Network (SNN) in PyTorch with quantization-aware training and mapped weights directly to analog conductance values for compute-in-memory operations.
- Implementing analog peripherals including Leaky Integrate-and-Fire (LIF) neurons and current sense amplifiers in Virtuoso, and validated timing/power performance via Spectre transient simulations.

Parameterized 2D-Convolution Hardware Accelerator | *SystemVerilog, AXI4, Zynq SoC* Sept. 2025 – Present

- Architected a fully parameterized IP core in SystemVerilog, enabling build-time configuration of kernel size, bit-width, and matrix dimensions to optimize area/performance trade-offs for different AXI data workloads.
- Designed high-throughput microarchitecture with 3-stage pipelined MAC units, inputs memory buffers, FIFO buffers, and a top-level FSM controller, achieving 855 MHz post-synthesis frequency using the Nangate 45nm Open Cell.
- Validated functional correctness using constrained-random testbench with DPI-C co-simulation, and deploying the IP onto a Zynq-7000 SoC, using its Cortex-A9 to transfer weights/biases from DDR to the FPGA fabric via AXI DMA engine.