Contents

	SFLASH
	RT

Revisions

Rev	Description	Date	Approved
X10	Convert into FSL template	9/8/09	DESIGNER
X11	All parts FCL	9/14/09	Michael N
X12	Replaced U5 with the correct part	9/15/09	Michael N
X14	Replaced some components with similar per Micetek suggestion	9/22/09	Michael N
X15	Added a Jumper on SD WR per BU request	9/25/09	Michael N
X16	Replaced SC part with shorter one	9/28/09	Michael N
X17	Replaced SD/MMC connector	10/09/09	Michael N
A	Released to Fab	10/15/09	Michael N
B	Add J15, J16 and J17 per customer req Released to fab	10/15/09	Michael N
B1	Replace with alternate part LEDs	1/29/10	Michael N

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ICAP Classification: FCP: FIUO: X PUBI:

Designer: Rodolfo G	Drawing Title: TWR-MEM	
Drawn by: Rodolfo G	Page Title: Table of contents	
Approved: Michael N	Size C	Document Number SCH-26248 PDF: SPF-26248 Rev B1
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ecified:
ohms, 5%, 1/8 Watt
n uF, 20%, 50V
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: TWR-MEM

Page Title: NOTES

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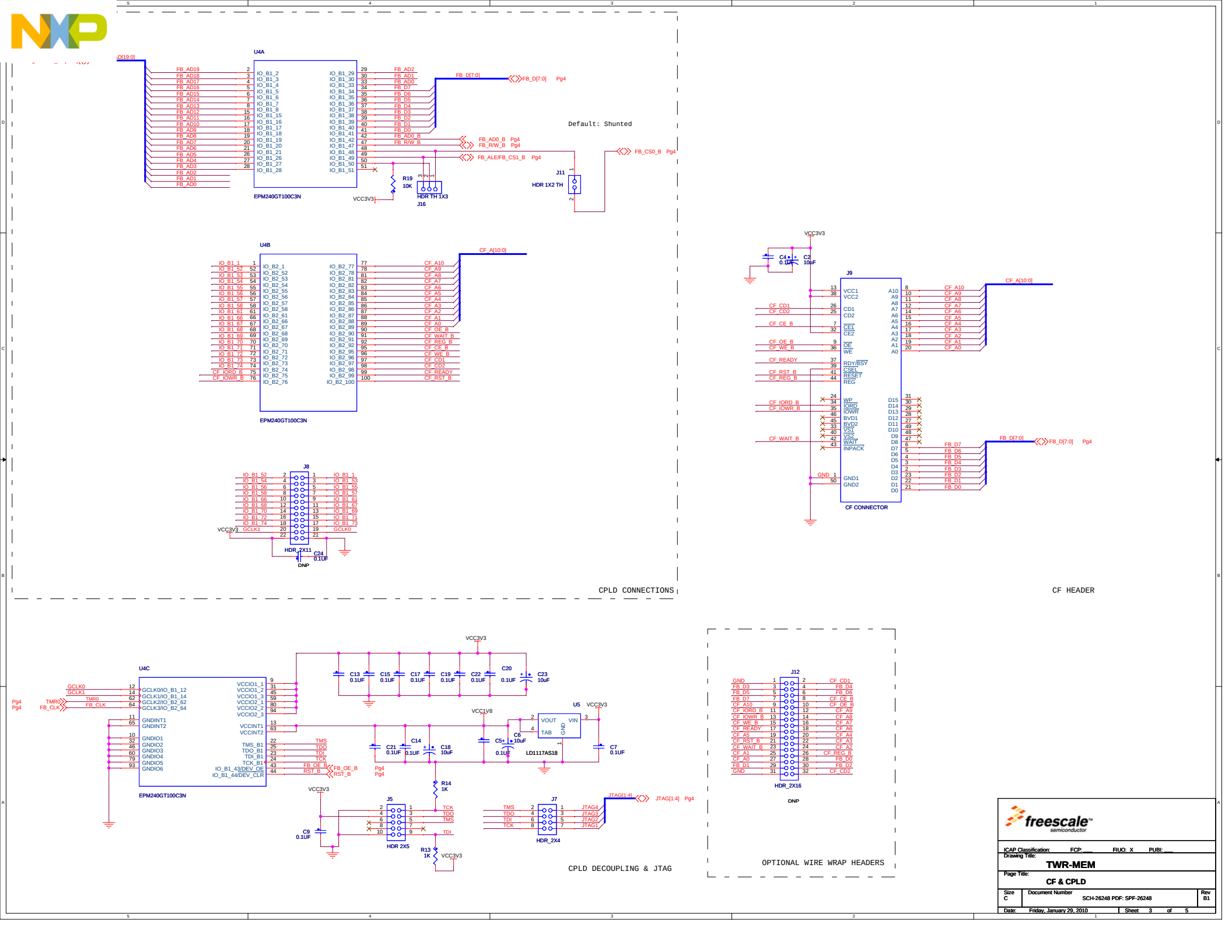
U4A
EPM240GT100C3N
Default: Shunted
R19
10K
HDR TH 1X3
J16
J11
HDR 1X2 TH
U4B
EPM240GT100C3N
J8
HDR_2X11
C24
0.1UF
DNP
CPLD CONNECTIONS
VCC3V3
C4
0.1UF
C2
10uF
J9
CF CONNECTOR
CF HEADER
U4C
EPM240GT100C3N
C13
0.1UF
C15
0.1UF
C17
0.1UF
C19
0.1UF
C22
0.1UF
C20
0.1UF
C23
10uF
U5
LD1117AS18
VCC1V8
C21
0.1UF
C14
0.1UF
C18
10uF
C5
0.1UF
C6
10uF
C7
0.1UF
R14
1K
J5
HDR 2X5
J7
HDR_2X4
C9
0.1UF
R13
1K
CPLD DECOUPLING & JTAG
J12
HDR_2X16
DNP
OPTIONAL WIRE WRAP HEADERS
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ICAP Classification:
FCP:
FIUO: X
PUBI:
Drawing Title:
TWR-MEM
Page Title:
CF & CPLD
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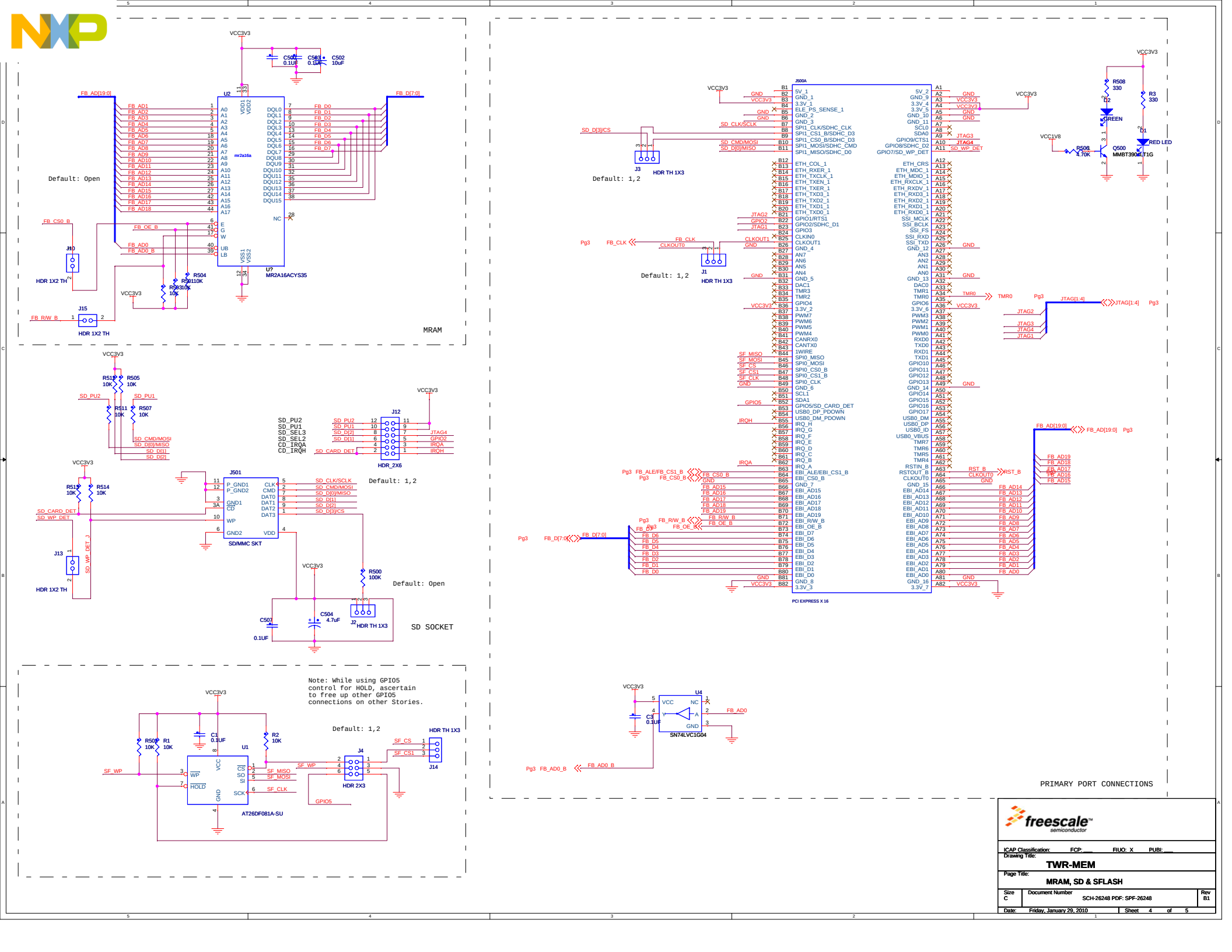
MRAM
Default: Open
HDR 1X2 TH
HDR 1X3 TH
Default: 1,2
SD SOCKET
SD/MMC SKT
HDR_2X6
HDR TH 1X3
HDR 2X3
AT26DF081A-SU
SN74LVC1G04
Note: While using GPIO5 control for HOLD, ascertain to free up other GPIO5 connections on other Stories.
PCI EXPRESS X 16
PRIMARY PORT CONNECTIONS
TWR-MEM
MRAM, SD & SFLASH
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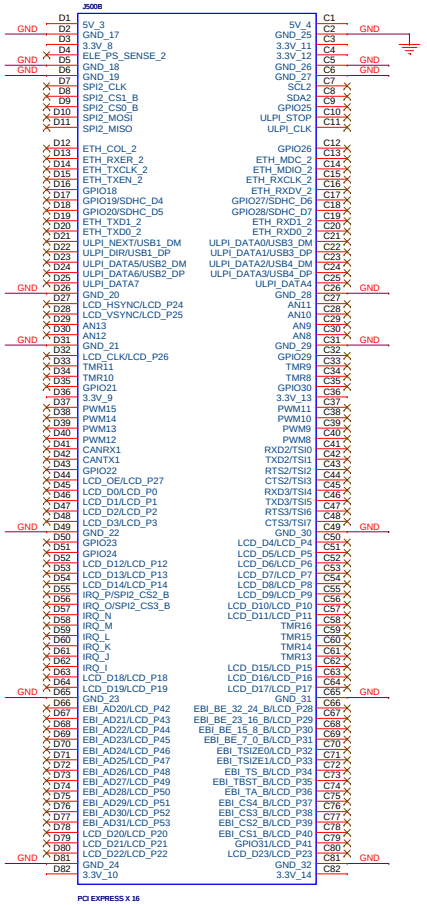

SECONDARY PORT

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **TWR-MEM**

Page Title: **OPTIONAL PORT**

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