

512K x 8 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM

AUGUST 2009

FEATURES

HIGH SPEED: (IS61/64WV5128ALL/BLL)

- High-speed access time: 8, 10, 20 ns
- Low Active Power: 85 mW (typical)
- Low stand-by power: 7 mW (typical) CMOS standby

LOW POWER: (IS61/64WV5128ALS/BLS)

- High-speed access time: 25, 35 ns
- Low Active Power: 35 mW (typical)
- Low stand-by power: 0.6 mW (typical) CMOS standby
- Single power supply
 - VDD 1.65V to 2.2V (IS61WV5128Axx)
 - VDD 2.4V to 3.6V (IS61/64WV5128Bxx)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

The *ISSI* IS61WV5128Axx and IS61/64WV5128Bxx are very high-speed, low power, 524,288-word by 8-bit CMOS static RAMs. The IS61WV5128Axx and IS61/64WV5128Bxx are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

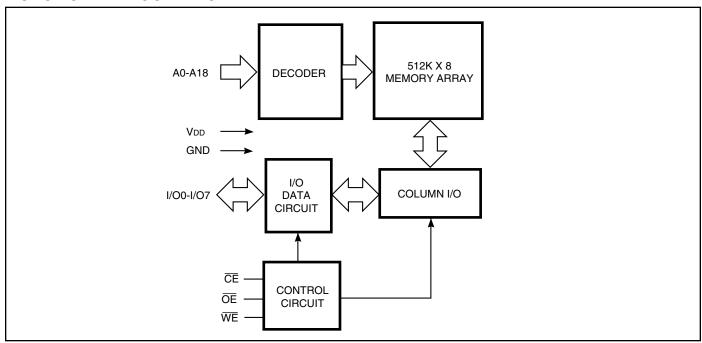
When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61WV5128Axx and IS61/64WV5128Bxx operate from a single power supply.

The IS61WV5128ALL and IS61/64WV5128BLL are available in 36-pin 400-mil SOJ, 36-pin mini BGA, and 44-pin TSOP (Type II) packages.

The IS61WV5128ALS and IS61/64WV5128BLS are available in 32-pinTSOP (Type I), 32-pin sTSOP (Type I), 32-pin SOP and 32-pin TSOP (Type II) packages.

FUNCTIONAL BLOCK DIAGRAM

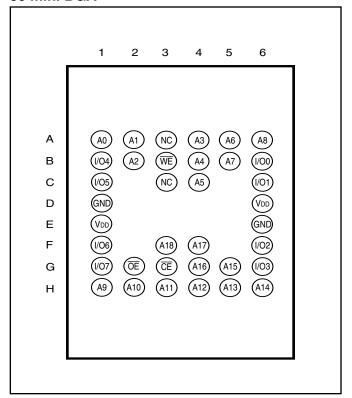


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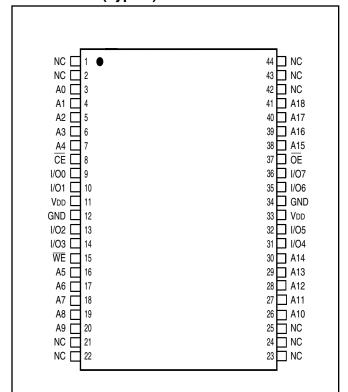


PIN CONFIGURATION (HIGH SPEED) (61/64WV5128ALL/BLL)

36 mini BGA



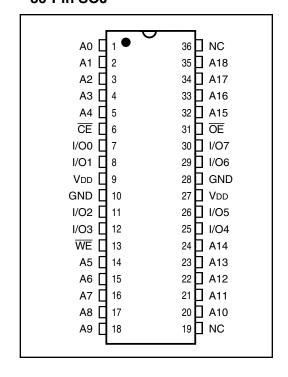
44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
WE	Write Enable Input
1/00-1/07	Bidirectional Ports
V _{DD}	Power
GND Ground	
NC	No Connection

36-Pin SOJ

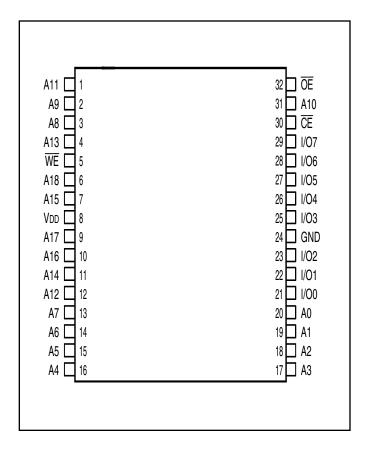


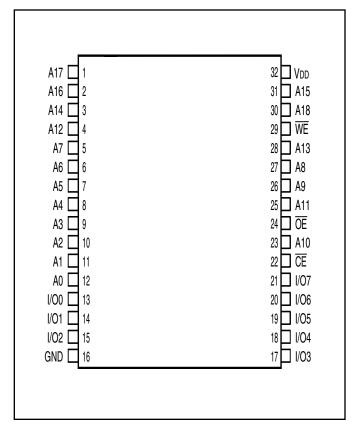


PIN CONFIGURATION (LOW POWER) (61/64WV5128ALS/BLS)

32-pin TSOP (TYPE I), (Package Code T) 32-pin sTSOP (TYPE I) (Package Code H)

32-pin SOP 32-pin TSOP (TYPE II) (Package Code T2)





PIN DESCRIPTIONS

A0-A18	Address Inputs
CE	Chip Enable 1 Input
ŌĒ	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
V _{DD}	Power
GND	Ground



DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 3.3V + 5\%$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	$V_{DD} = Min., I_{OH} = -4.0 \text{ mA}$	2.4	_	V
Vol	Output LOW Voltage	$V_{DD} = Min., IoL = 8.0 mA$	_	0.4	V
VIH	Input HIGH Voltage		2	V _{DD} + 0.3	V
VIL	Input LOW Voltage(1)		-0.3	0.8	V
ILI	Input Leakage	$GND \leq Vin \leq Vdd$	-1	1	μA
ILO	Output Leakage	$GND \le V_{OUT} \le V_{DD}$, Outputs Disabled	-1	1	μΑ

Note:

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 2.4V - 3.6V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	$V_{DD} = Min., I_{OH} = -1.0 \text{ mA}$	1.8	_	V
Vol	Output LOW Voltage	VDD = Min., IOL = 1.0 mA	_	0.4	V
VIH	Input HIGH Voltage		2.0	VDD + 0.3	V
VIL	Input LOW Voltage(1)		-0.3	0.8	V
lu	Input Leakage	$GND \leq Vin \leq Vdd$	-1	1	μA
ILO	Output Leakage	GND ≤ Vouт ≤ Vdd, Outputs Disabled	-1	1	μA

Note:

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 1.65V-2.2V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	V _{DD} = Min, Iон = -0.1 mA	1.4	_	V
Vol	Output LOW Voltage	VDD = Min, IOL = 0.1 mA	_	0.2	V
VIH	Input HIGH Voltage		1.4	V _{DD} + 0.2	V
VIL ⁽¹⁾	Input LOW Voltage		-0.2	0.4	V
ILI	Input Leakage	$GND \leq Vin \leq Vdd$	-1	1	μA
ILO	Output Leakage	$GND \le V_{OUT} \le V_{DD}$, Outputs Disabled	-1	1	μA

^{1.} V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested. VIH (max.) = VDD + 0.3V DC; VIH (max.) = VDD + 2.0V AC (pulse width <10 ns). Not 100% tested.

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TRUTH TABLE

Mode	WE	CE	ŌĒ	I/O Operation	VDD Current
Not Selected (Power-down)	Х	Н	Х	High-Z	ISB1, ISB2
Output Disable	ed H	L	Н	High-Z	Icc
Read	Н	L	L	D оит	Icc
Write	L	L	Х	Din	Icc

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit	
VTERM	Terminal Voltage with Respect to GND	-0.5 to $V_{DD} + 0.5$	V	
VDD	VDD Relates to GND	-0.3 to 4.0	V	
Тѕтс	Storage Temperature	-65 to +150	°C	
Рт	Power Dissipation	1.0	W	

Notes:

 Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

CIN Input Capacitance VIN = 0V 6 pF	Symbol	Parameter	Conditions	Max.	Unit	
	Cin	Input Capacitance	VIN = 0V	6	pF	
$C_{I/O}$ Input/Output Capacitance $V_{OUT} = 0V$ 8 pF	C _{I/O}	Input/Output Capacitance	Vout = 0 V	8	pF	

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions: $T_A = 25^{\circ}C$, f = 1 MHz, $V_{DD} = 3.3V$.



HIGH SPEED (IS61WV5128ALL/BLL) OPERATING RANGE (VDD) (IS61WV5128ALL)

Range	Ambient Temperature	V _{DD}	Speed	
Commercial	0°C to +70°C	1.65V-2.2V	20ns	
Industrial	–40°C to +85°C	1.65V-2.2V	20ns	
Automotive	-40°C to +125°C	1.65V-2.2V	20ns	

OPERATING RANGE (VDD) (IS61WV5128BLL)(1)

Range	Ambient Temperature	V _{DD} (8 ns) ¹	V _{DD} (10 ns) ¹	
Commercial	0°C to +70°C	3.3V <u>+</u> 5%	2.4V-3.6V	
Industrial	–40°C to +85°C	3.3V <u>+</u> 5%	2.4V-3.6V	

Note:

OPERATING RANGE (VDD) (IS64WV5128BLL)

Range	Ambient Temperature	V _{DD} (10 ns)	
Automotive	-40°C to +125°C	2.4V-3.6V	

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

				-	8	-10	-2	20	
Symbol	Parameter	Test Conditions		Min.	Max.	Min. M	ax. Min.	Max.	Unit
Icc	VDD Dynamic Operating	V _{DD} = Max.,	Com.		50		1 0 —	40	mA
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	55	_ 4	45 —	45	
11 7		Auto.	_	_	_ 6	65 —	65		
			typ.(2)			25			
lcc1	Operating	V _{DD} = Max.,	Com.	_	35	_ 3	35 —	30	mA
Supply	Supply Current	IOUT = 0 mA, f = 0	Ind.	_	40	_ 4	40 —	40	
			Auto.	_	_	_ 6	60 —	60	
ISB1	TTL Standby Current	V _{DD} = Max.,	Com.	_	10	_ 1	I0 —	10	mA
	(TTL Inputs)	VIN = VIH or VIL	Ind.	_	15	— 1	I5 —	15	
		$\overline{CE} \ge V_{IH}, f = 0$	Auto.	_	_	_ 3	B0 —	30	
IsB2	CMOS Standby	V _{DD} = Max.,	Com.	_	7	_	7 —	7	mA
	Current (CMOS Inputs)	$\overline{CE} \ge V_{DD} - 0.2V$,	Ind.	_	10	— 1	IO —	10	
	. ,	$V_{\text{IN}} \ge V_{\text{DD}} - 0.2V$, or	Auto.	_	_	_ 2	20 —	20	
		$Vin \leq 0.2V, f = 0$	typ.(2)			2			

^{1.} When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V \pm 5%, the device meets 8ns.

^{1.} At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

^{2.} Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25^{\circ}C$ and not 100% tested.



LOW POWER (IS61WV5128ALS/BLS)

OPERATING RANGE (VDD) (IS61WV5128ALS)

Range	Ambient Temperature	V DD	Speed	
Commercial	0°C to +70°C	1.65V-2.2V	35ns	
Industrial	–40°C to +85°C	1.65V-2.2V	35ns	
Automotive	-40°C to +125°C	1.65V-2.2V	35ns	

OPERATING RANGE (VDD) (IS61WV5128BLS)(1)

Range	Ambient Temperature	V _{DD}	Speed	
Commercial	0°C to +70°C	2.4V-3.6V	25 ns	
Industrial	–40°C to +85°C	2.4V-3.6V	25 ns	

OPERATING RANGE (VDD) (IS64WV5128BLS)

Range	Ambient Temperature	V DD	Speed	
Automotive	-40°C to +125°C	2.4V-3.6V	35 ns	

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

				-2	25	-3	5		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Unit	
Icc	VDD Dynamic Operating	V _{DD} = Max.,	Com.	_	20	_	20	mA	
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	25	_	25		
			Auto.	_	50	_	50		
			typ.(2)	1	1				
lcc1	Operating	V _{DD} = Max.,	Com.	_	10	_	10	mA	
	Supply Current	IOUT = 0 mA, f = 0	Ind.	_	12	_	12		
			Auto.	_	20	_	20		
ISB1	TTL Standby Current	V _{DD} = Max.,	Com.	_	5	_	5	mA	
	(TTL Inputs)	$V_{IN} = V_{IH} \text{ or } V_{IL}$	Ind.	_	7	_	7		
		$\overline{CE} \ge V_{IH}, f = 0$	Auto.	_	10	_	10		
ISB2	CMOS Standby	V _{DD} = Max.,	Com.	_	1	_	1	mA	
	Current (CMOS Inputs)	$\overline{CE} \ge V_{DD} - 0.2V$,	Ind.	_	2	_	2		
		$V_{\text{IN}} \ge V_{\text{DD}} - 0.2V$, or	Auto.	_	10	_	10		
		$V_{IN} \leq~0.2V,f=0$	typ.(2)	0.	2				

^{1.} At f = fmax, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

^{2.} Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25$ °C and not 100% tested.



ACTEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V <u>±</u> 10%)	Unit (1.65V-2.2V)	
Input Pulse Level	0V to 3V	0V to 3V	0V to 1.8V	
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns	
Input and Output Timing and Reference Level (V _{Ref})	1.5V	1.5V	0.9V	
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2	

ACTEST LOADS

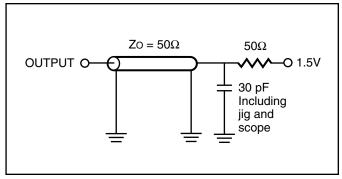


Figure 1.

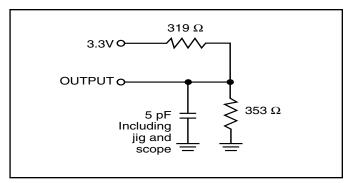


Figure 2.



READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

			8	-1	0		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	
t RC	Read Cycle Time	8	_	10	_	ns	
taa	Address Access Time	_	8	_	10	ns	
tона	Output Hold Time	2.0		2.0	_	ns	
t ACE	CE Access Time	_	8	_	10	ns	
t DOE	OE Access Time	_	4.5	_	4.5	ns	
thzoe(2)	OE to High-Z Output	_	3	_	4	ns	
tLZOE ⁽²⁾	OE to Low-Z Output	0		0	_	ns	
thzce(2	CE to High-Z Output	0	3	0	4	ns	
tLZCE ⁽²⁾	CE to Low-Z Output	3	_	3	_	ns	
tpu	Power Up Time	0	_	0	_	ns	
t PD	Power Down Time	_	8	_	10	ns	

^{1.} Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.

^{2.} Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.



READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

		-	20 ns	-25	i ns	-3!	5 ns	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
trc	Read Cycle Time	20	_	25		35		ns
taa	Address Access Time	_	20	_	25	_	35	ns
tона	Output Hold Time	2.5	_	4		4		ns
tace	CE Access Time	_	20	_	25	_	35	ns
t DOE	OE Access Time	_	8	_	12	_	15	ns
thzoe(2)	OE to High-Z Output	0	8	0	8	0	10	ns
tLZOE ⁽²⁾	OE to Low-Z Output	0		0	_	0		ns
thzce ⁽²	CE to High-Z Output	0	8	0	8	0	10	ns
tLZCE ⁽²⁾	CE to Low-Z Output	3	_	10	_	10	_	ns
t PU	Power Up Time	0	_	0	_	0	_	ns
t PD	Power Down Time	_	20	_	25	_	35	ns

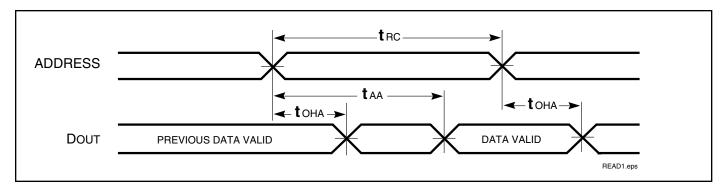
^{1.} Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to VDD-0.3V and output loading specified in Figure 1a.

^{2.} Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

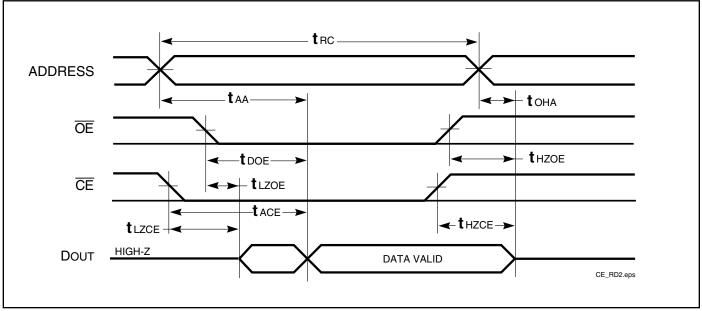
^{3.} Not 100% tested.



AC WAVEFORMS READ CYCLE NO. $1^{(1,2)}$ (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) ($\overline{\text{CE}}$ and $\overline{\text{OE}}$ Controlled)



- WE is HIGH for a Read Cycle.
 The device is continuously selected. OE, CE = VIL.
- 3. Address is valid prior to or coincident with $\overline{\text{CE}}$ LOW transitions.



WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

		-{	3	-10	0	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	8	_	10	_	ns
tsce	CE to Write End	6.5	_	8	_	ns
taw	Address Setup Time to Write End	6.5	_	8	_	ns
tна	Address Hold from Write End	0	_	0	_	ns
t sa	Address Setup Time	0	_	0	_	ns
tpwe1	WE Pulse Width (OE = HIGH)	6.5	_	8	_	ns
tPWE2	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}} = \text{LOW}$)	8.0	_	10	_	ns
tsd	Data Setup to Write End	5	_	6	_	ns
t HD	Data Hold from Write End	0	_	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	3.5	_	5	ns
tLZWE ⁽²⁾	WE HIGH to Low-Z Output	2	_	2	_	ns

^{1.} Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.

^{2.} Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

^{3.} The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development



WRITE CYCLE SWITCHING CHARACTERISTICS(1,2) (Over Operating Range)

•		-20	ns	-25	ns	-35	ns	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	20	_	25	_	35	_	ns
tsce	CE to Write End	12	_	18	_	25	_	ns
taw	Address Setup Time to Write End	12	_	15	_	25	_	ns
t HA	Address Hold from Write End	0	_	0	_	0	_	ns
t sa	Address Setup Time	0	_	0	_	0	_	ns
tPWE1	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ = HIGH)	12	_	18	_	30	_	ns
tPWE2	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ = LOW)	17	_	20	_	30	_	ns
tsp	Data Setup to Write End	9	_	12	_	15	_	ns
t HD	Data Hold from Write End	0	_	0	_	0	_	ns
thzwE ⁽³⁾	WE LOW to High-Z Output	_	9	_	12	_	20	ns
tLZWE ⁽³⁾	WE HIGH to Low-Z Output	3	_	5	_	5	_	ns

Notes:

2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

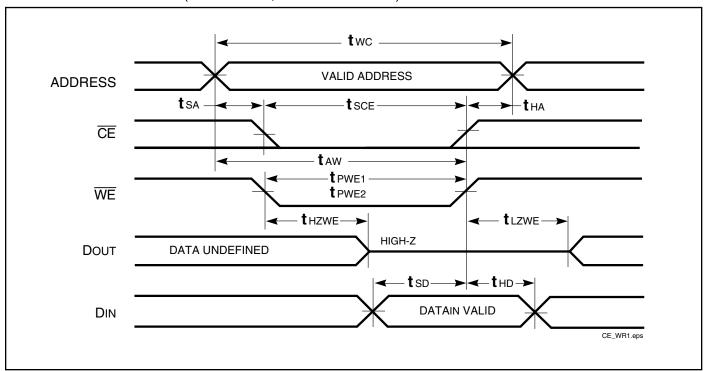
^{1.} Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to VDD-0.3V and output loading specified in Figure 1a.

^{3.} The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.



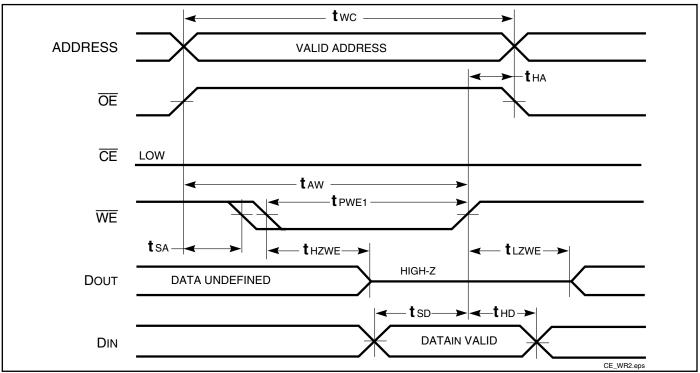
AC WAVEFORMS

WRITE CYCLE NO. $1^{(1,2)}$ (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)





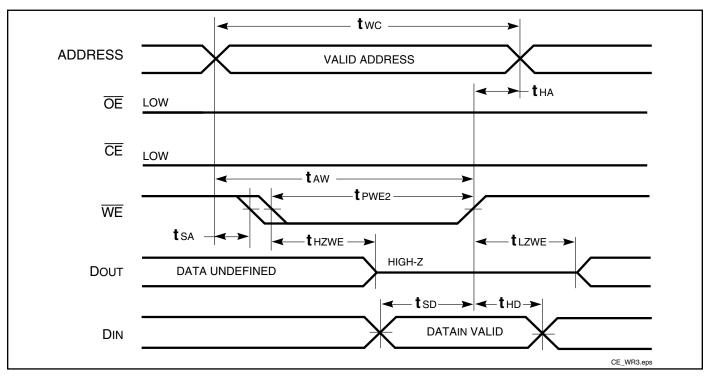
WRITE CYCLE NO. 2^(1,2) (WE Controlled: OE is HIGH During Write Cycle)



Notes:

- 1. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- 2. I/O will assume the High-Z state if $\overline{\text{OE}}$ > VIH.

WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)





HIGH SPEED (IS61WV5128ALL/BLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
VDR	VDD for Data Retention	See Data Retention Waveform		2.0	_	3.6	V
Idr	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \ge V_{DD} - 0.2V$	Com.	_	2	6	mA
			Ind. Auto.	_	_	8 15	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	_	ns
t rdr	Recovery Time	See Data Retention Waveform		t rc	_	_	ns

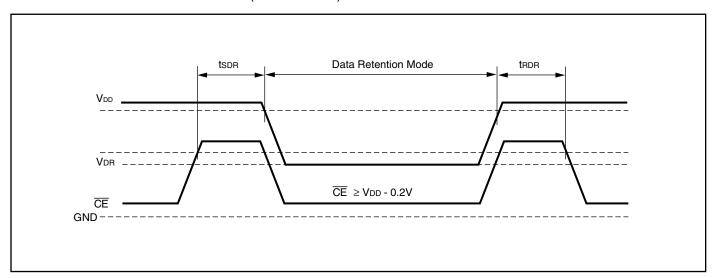
Note 1: Typical values are measured at VDD = 3.0V, TA = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	VDD for Data Retention	See Data Retention Waveform		1.2	_	3.6	V
Idr	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \ge V_{DD} - 0.2V$	Com.	_	2	6	mA
			Ind.	_	_	8	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	_	ns
trdr	Recovery Time	See Data Retention Waveform		t RC	_	_	ns

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CE Controlled)





LOW POWER (IS61WV5128ALS/BLS)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
VDR	VDD for Data Retention	See Data Retention Waveform		2.0	_	3.6	V
Idr	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \ge V_{DD} - 0.2V$	Com.	_	0.2	1	mA
			Ind.	_	_	2	
			Auto.			10	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	_	ns
trdr	Recovery Time	See Data Retention Waveform		t RC	_	_	ns

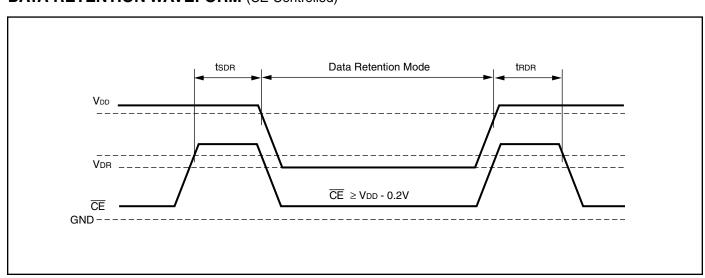
Note 1: Typical values are measured at VDD = 3.0V, TA = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	VDD for Data Retention	See Data Retention Waveform		1.2	_	3.6	V
IDR	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \ge V_{DD} - 0.2V$	Com.	_	0.2	1	mA
			Ind.	_	_	2	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	_	ns
trdr	Recovery Time	See Data Retention Waveform		t rc	_	_	ns

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CE Controlled)





ORDERING INFORMATION (HIGH SPEED)

Commercial Range: 0°C to +70°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8¹)	IS61WV5128BLL-10TL	TSOP (Type II), Lead-free
NI I		

Note:

Industrial Range: -40°C to +85°C Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8¹)	IS61WV5128BLL-10BI	36-ball mini BGA (6mm x 8mm)
	IS61WV5128BLL-10BLI	36-ball mini BGA (6mm x 8mm), Lead-free
	IS61WV5128BLL-10TI	TSOP (Type II)
	IS61WV5128BLL-10TLI	TSOP (Type II), Lead-free
	IS61WV5128BLL-10KLI	400-mil Plastic SOJ, Lead-free

Note:

Industrial Range: -40°C to +85°C Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV5128ALL-20BI	36-ball mini BGA (6mm x 8mm)
	IS61WV5128ALL-20TI	TSOP (Type II)

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV5128BLL-10BA3	36-ball mini BGA (6mm x 8mm)
	IS64WV5128BLL-10BLA3	36-ball mini BGA (6mm x 8mm), Lead-free
	IS64WV5128BLL-10CTA3	TSOP (Type II), Copper Leadframe
	IS64WV5128BLL-10CTLA3	TSOP (Type II), Copper Leadframe
		Lead-free

^{1.} Speed = 8ns for V_{DD} = 3.3V \pm 5%. Speed = 10ns for V_{DD} = 2.4V to 3.6V.

^{1.} Speed = 8ns for V_{DD} = 3.3V \pm 5%. Speed = 10ns for V_{DD} = 2.4V to 3.6V.



ORDERING INFORMATION (LOW POWER)

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
25	IS61WV5128BLS-25TLI	TSOP (Type II), Lead-free



