Document Title

1M x 16 bit Single Transistor RAM

Revision History

Revision No.	History		Draft Date	Remark
0.0	Initial Draft		Jul. 11 , 2005	Preliminary
0.1	1'st Revision	DNU pin location changed from E3 to H6. Added Pb-free&Green part.	Nov. 24 , 2005	Preliminary
0.2	2'nd Revision	Change tRC/tWC maximum from 40us to 10us.	Feb. 15 , 2006	Preliminary

Emerging Memory & Logic Solutions Inc.
4F Korea Construction Financial Cooperative B/D, 301-1 Yeon-Dong, Jeju-Si, Jeju-Do, Rep.of Korea Zip Code : 690-717
Tel : +82-64-740-1700 Fax : +82-64-740-1749~1750 / Homepage : www.emlsi.com

1M x16 bit Single Transistor RAM

GENERAL DESCRIPTION

The EM7164SU16 is 16,777,216 bits of Single Transistor RAM which uses DRAM type memory cells, but this device has refresh-free operation and extreme low power consumption technology. Furthermore the interface is compatible to a low power Asynchronous type SRAM. The EM7164SU16 is organized as 1,048,576 Words x 16 bit.

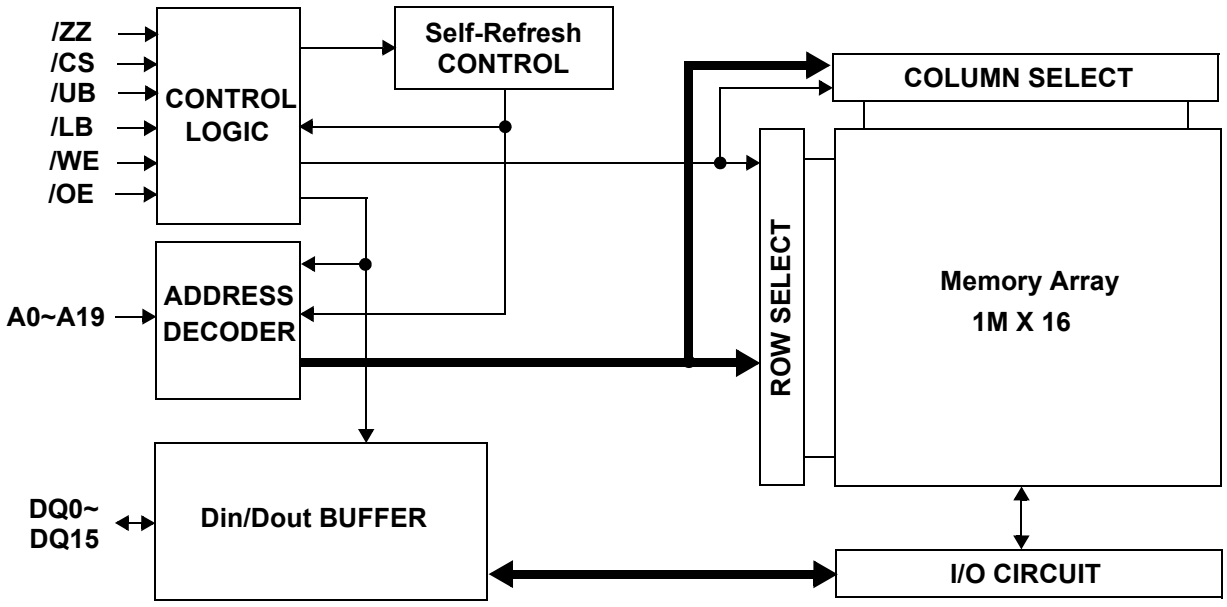
FEATURES

- Organization :1M x16
- Power Supply Voltage : 2.7 ~ 3.3V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state outputs
- Byte read/write control by $\overline{UB}$/$\overline{LB}$
- Support Direct Deep Power Down control by $\overline{ZZ}$ and Auto TCSR for power saving
- Package type : 48-FPBGA 6.0x7.0

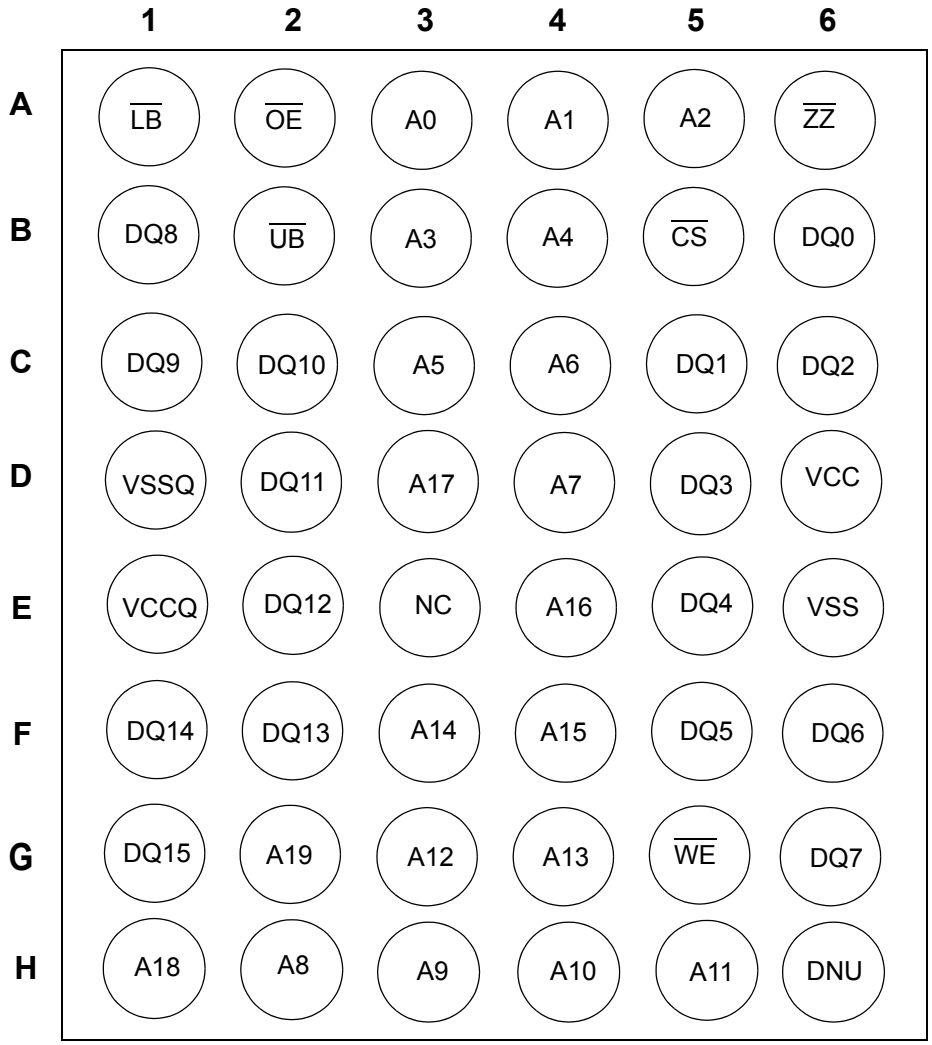
PRODUCT FAMILY

Part Number	Operating Temp.	Power Supply	Speed (t_{RC})	Power Dissipation	
				Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)
EM7164SU16	-25°C to 85°C	2.7V to 3.3V	70ns	80uA	25mA

FUNCTION BLOCK DIAGRAM



PIN DESCRIPTION (48-FBGA-6.00x7.00)



TOP VIEW (Ball Down)

Name	Function	Name	Function
/CS	Chip select inputs	/LB	Lower byte ($DQ_{0\sim7}$)
/OE	Output enable input	/UB	Upper byte ($DQ_{8\sim15}$)
/WE	Write enable input	VCC	Power supply
/ZZ	Low Power Control	VCCQ	I/O Power supply
DQ_{0-15}	Data In-out	VSS(Q)	Ground
A_{0-19}	Address inputs	NC	No connection
DNU	Do Not Use		

ABSOLUTE MAXIMUM RATINGS [1)]

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}, V_{CCQ}	-0.2[2)] to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Undershoot at power-off : -1.0V in case of pulse width ≤ 20ns

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	H	X	X	X	X	High-Z	High-Z	Deselected	Stand by
X	L	X	X	X	X	High-Z	High-Z	Deselected	Deep Power Down
X	H	X	X	H	H	High-Z	High-Z	Deselected	Stand by
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

Note: X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{CCQ}	2.7	3.0	3.3	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	0.8 * V_{CCQ}	-	V_{CCQ} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.2 * V_{CCQ}	V

1. T_A= -25 to 85°C, otherwise specified
2. Overshoot: Vcc +1.0 V in case of pulse width ≤ 20ns
3. Undershoot: -1.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CCQ} , V_{CC}=V_{CCmax}		-1	-	1	uA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} , /ZZ=V_{IH} , $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} , V_{IO}=V_{SS} to V_{CCQ} , V_{CC}=V_{CCmax}		-1	-	1	uA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$=V_{IH} , V_{IN}≤0.2V or V_{IN}≥V_{CCQ}-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{ZZ}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}		-	-	25	mA
Output low voltage	V_{OL}	I_{OL} = 0.5mA, V_{CC}=V_{CCmin}		-	-	0.2*V_{CCQ}	V
Output high voltage	V_{OH}	I_{OH} = -0.5mA, V_{CC}=V_{CCmin}		0.8*V_{CCQ}	-	-	V
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$,$\overline{ZZ}$≥V_{CCQ}-0.2V, Other inputs = 0 ~ V_{CCQ} (Typ. condition : V_{CC}=3.0V @ 25°C) (Max. condition : V_{CC}=3.3V @ 85°C)	LL	-	-	80	uA

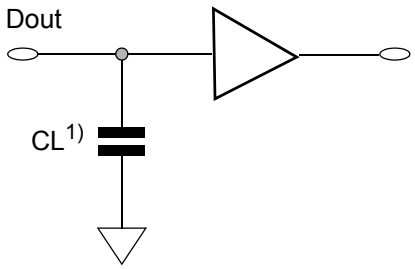
1. Maximum Icc specifications are tested with V_{CC} = V_{CCmax}.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.2V to V_{CCQ}-0.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : $V_{CCQ}/2$
Output Load (See right) : $CL^{1)}$ = 30pF

1. Including scope and Jig capacitance

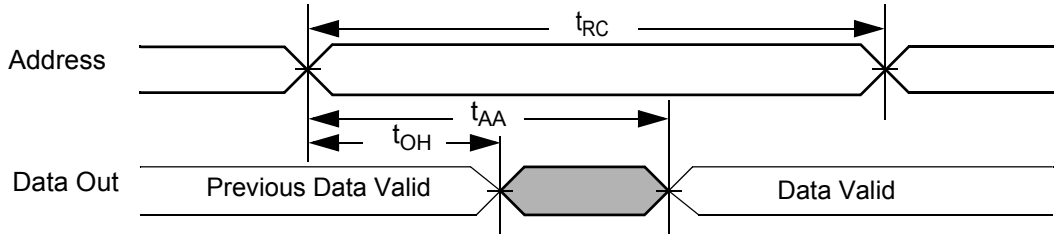


AC CHARACTERISTICS (V_{cc} = 2.7 to 3.3V, Gnd = 0V, T_A = -25C to +85°C)

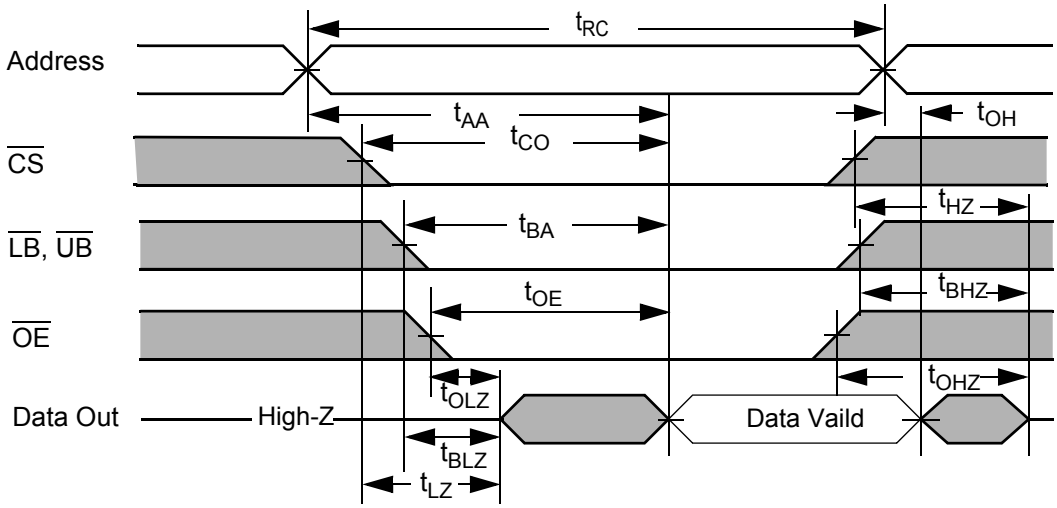
Parameter List		Symbol	Speed		Unit
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	10k	ns
	Address access time	t_{AA}	-	70	ns
	Chip enable to data output	t_{CO}	-	70	ns
	Output enable to valid output	t_{OE}	-	25	ns
	$\overline{UB}$, $\overline{LB}$ enable to data output	t_{BA}	-	70	ns
	Chip enable to low-Z output	t_{LZ}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	15	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	0	15	ns
	Output disable to high-Z output	t_{OHZ}	0	15	ns
	Output hold from Address change	t_{OH}	5	-	ns
Write	Write Cycle Time	t_{WC}	70	10k	ns
	Chip enable to end of write	t_{CW}	60	-	ns
	Address setup time	t_{AS}	0	-	ns
	Address valid to end of write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ valid to end of write	t_{BW}	60	-	ns
	Write pulse width	t_{WP}	50	-	ns
	Write recovery time	t_{WR}	0	-	ns
	Write to output high-Z	t_{WHZ}	0	15	ns
	Data to write time overlap	t_{DW}	20	-	ns
	Data hold from write time	t_{DH}	0	-	ns
	End write to output low-Z	t_{OW}	5	-	ns

TIMING DIAGRAMS

READ CYCLE (1) (Address controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{ZZ}$=$\overline{WE}$=VIH, $\overline{UB}$ or/and $\overline{LB}$=VIL)



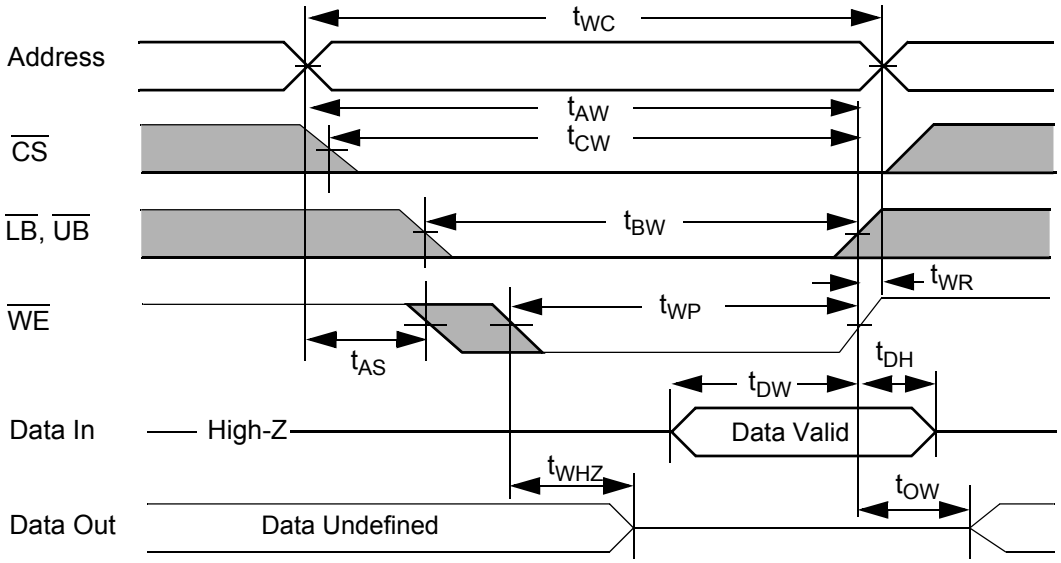
READ CYCLE (2) ($\overline{ZZ}$=$\overline{WE}$=VIH)



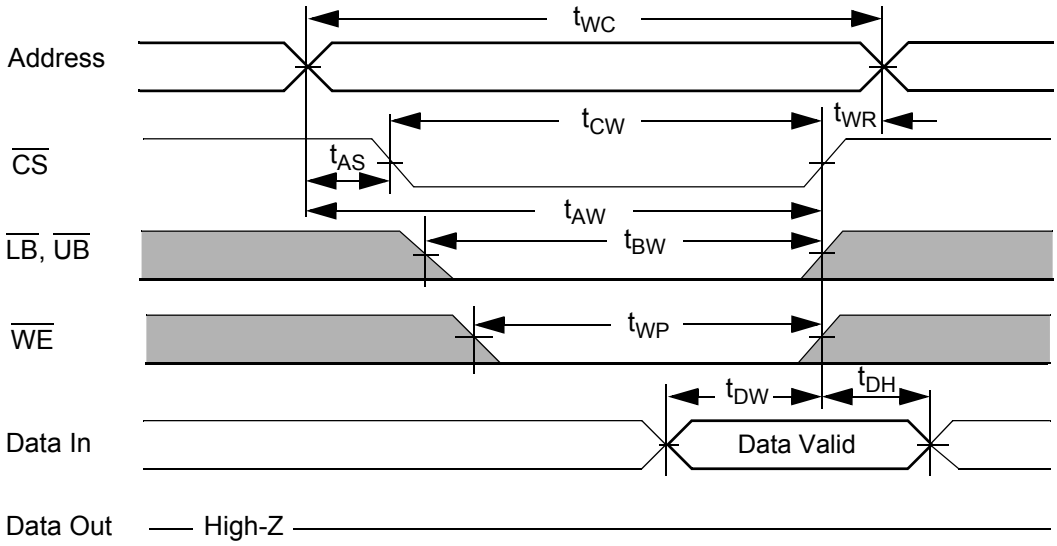
NOTES (READ CYCLE)

1. t_{HZ} , t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than t_{RC} for continuous periods > 40us.

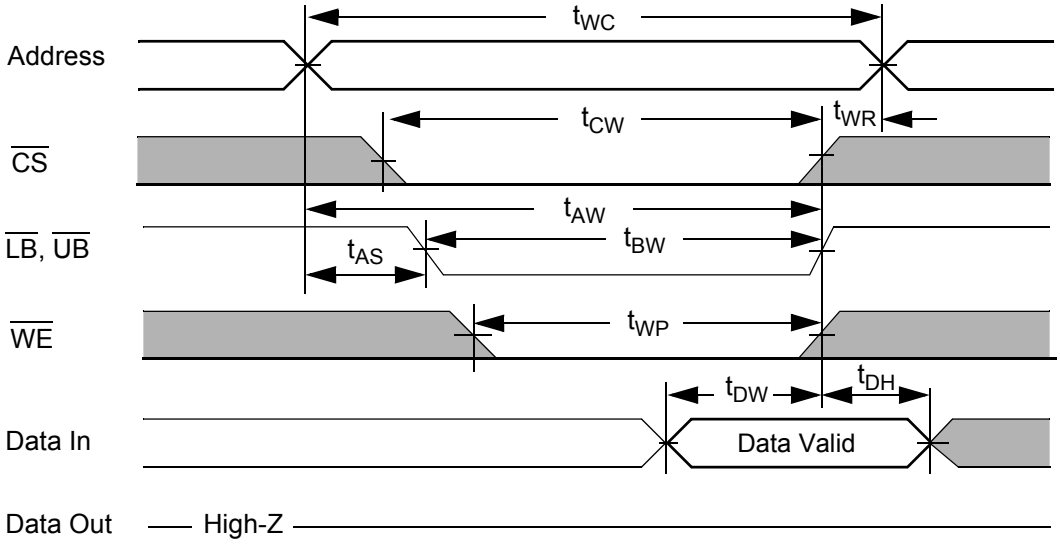
WRITE CYCLE (1) ($\overline{WE}$ controlled, $\overline{ZZ}$=$\overline{OE}$=VIH)



WRITE CYCLE (2) ($\overline{CS}$ controlled, $\overline{ZZ}$=$\overline{OE}$=VIH)



WRITE CYCLE (3) ($\overline{UB}$, $\overline{LB}$ controlled, $\overline{ZZ}$=$\overline{OE}$=VIH)

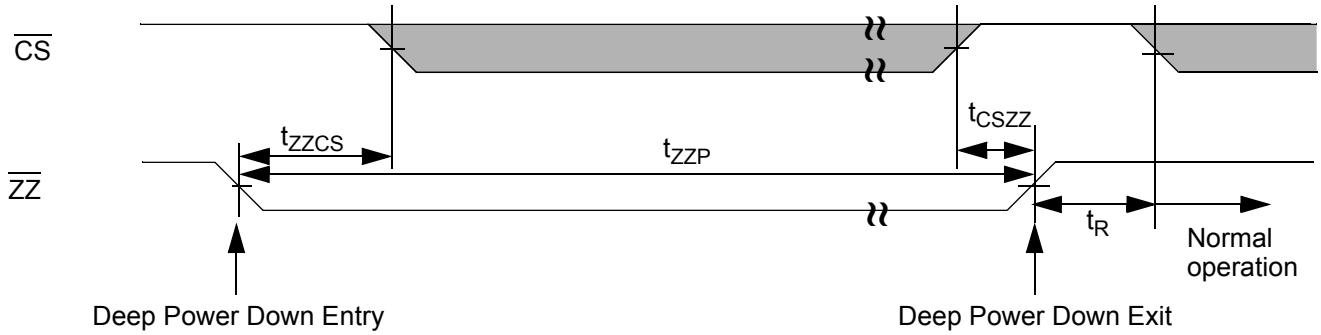


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$, low $\overline{WE}$ and low $\overline{UB}$ or $\overline{LB}$. A write begins at the last transition among low $\overline{CS}$ and low $\overline{WE}$ with asserting $\overline{UB}$ or $\overline{LB}$ low for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ low for word operation. A write ends at the earliest transition among high $\overline{CS}$ and high $\overline{WE}$. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from $\overline{CS}$ going low to end od write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
5. Do not Access device with cycle timing shorter than t_{WC} for continuous periods > 40us.

LOW POWER MODES

Deep Power Down Mode Entry/Exit



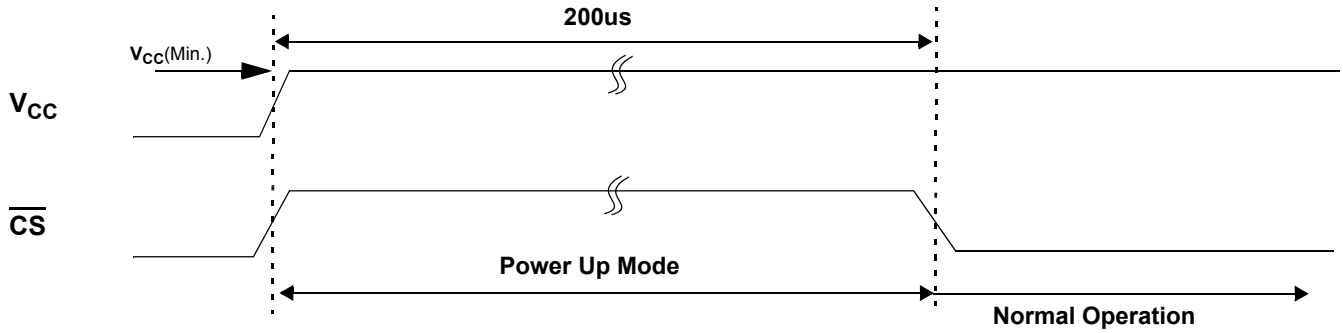
NOTES (DEEP POWER DOWN)
During Deep Power Down mode, all referesh related activity are disabled.

Parameter	Description	Min.	Max.	Units
t_{ZZCS}	$\overline{ZZ}$ low to $\overline{CS}$ low	0	-	ns
t_{CSZZ}	$\overline{CS}$ high to $\overline{ZZ}$ high	0	-	ns
t_R	Operation Recovery Time	200	-	us
t_{ZZP}	$\overline{ZZ}$ pulse width	20	-	ns

Low Power Mode Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Deep Power Down Current	I_{ZZ}	$\overline{ZZ} \leq 0.2V$, Other inputs = 0 ~ V_{CCQ} (Max. condition : V_{CC}=3.3V @ 85°C)	-	-	10	uA

TIMING WAVEFORM OF POWER UP



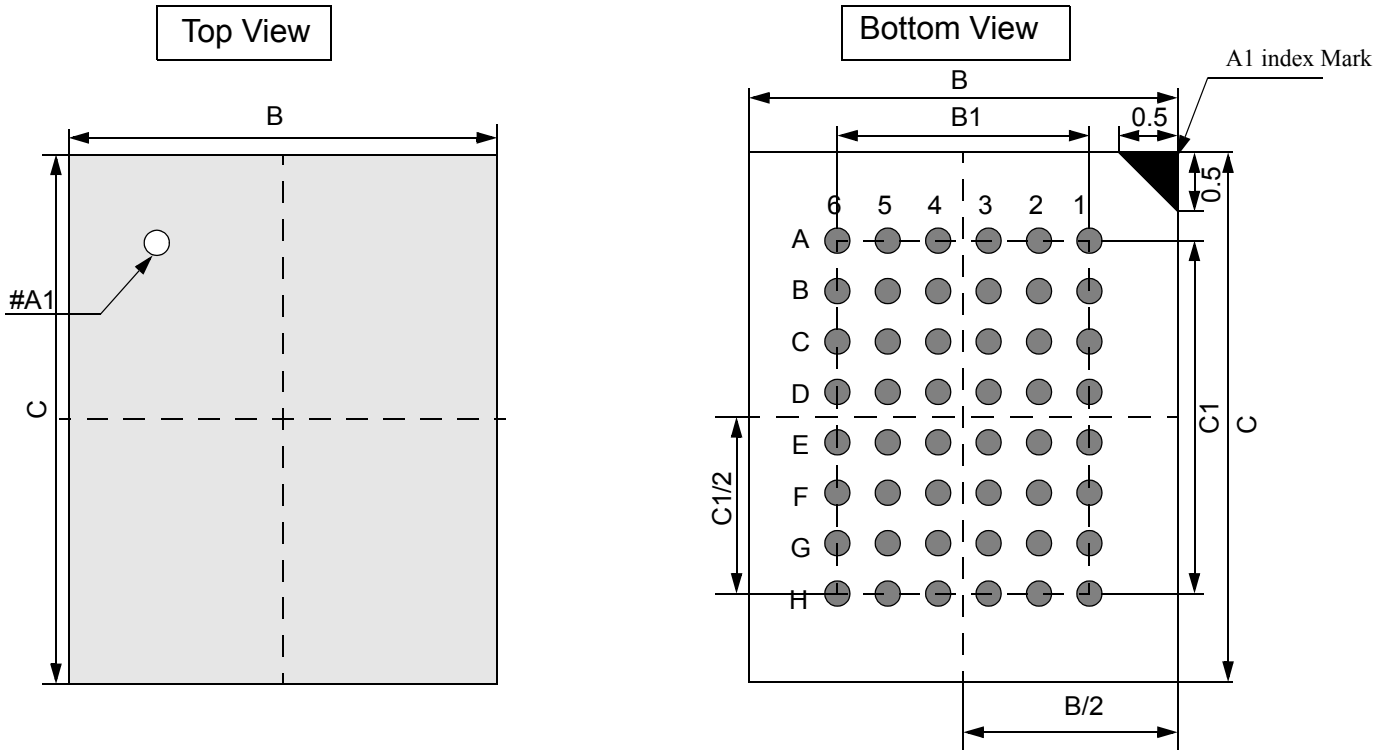
NOTE . (POWER UP)

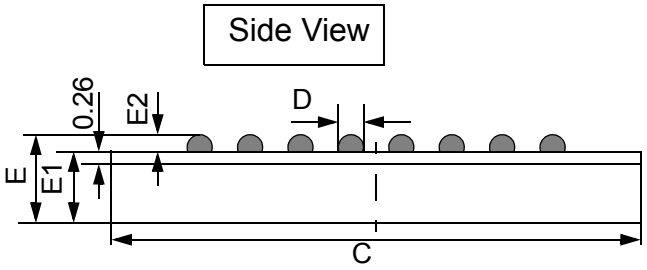
1. After Vcc reaches Vcc(Min.) , wait 200us with $\overline{CS}$ high. Then you get into the normal operation.

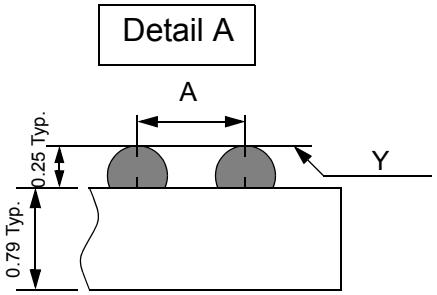
Unit: millimeters

PACKAGE DIMENSION

48 Ball Fine Pitch BGA (0.75mm ball pitch)







	Min	Typ	Max
A	-	0.75	-
B	5.93	6.00	6.03
B1	-	3.75	-
C	6.93	7.00	7.03
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

MEMORY FUNCTION GUIDE

EM X XX X X X XX X X - XX XX

1. EMLSI Memory
2. Device Type
3. Density
4. Option
5. Technology
6. Operating Voltage
7. Organization
8. Version
9. Packages
10. Speed
11. Power

1. Memory Component

2. Device Type
- 6 ---------- Low Power SRAM
- 7 ---------- STRAM

3. Density
- 1 ---------- 1M
- 2 ---------- 2M
- 4 ---------- 4M
- 8 ---------- 8M
- 16 ---------- 16M
- 32 ---------- 32M
- 64 ---------- 64M

4. Function
- 0 ---------- Dual CS
- 1 ---------- Single CS
- 2 ---------- Multiplexed
- 3---------- Single CS with /ZZ
- 4---------- Single CS with /ZZ & Direct DPD
- 5 ---------- Multiplexed with Sync. mode

5. Technology
- Blank ---------- CMOS
- F ---------- Full CMOS
- S ---------- Single Transistor

6. Operating Voltage
- Blank ---------- 5V
- V ---------- 3.3V
- U ---------- 3.0V
- S ---------- 2.5V
- R ---------- 2.0V
- P ---------- 1.8V
- O ---------- 1.5V

7. Organization
- 8 ---------- x8 bit
- 16 ---------- x16 bit
- 32 ---------- x32 bit

8. Version
- Blank ---------- Mother die
- A ---------- First version
- B ---------- Second version
- C ---------- Third version
- D ---------- Fourth version
- E ---------- Fifth version

9. Package
- Blank ---------- Package
- W ---------- Wafer

10. Speed
- 45 ---------- 45ns
- 55 ---------- 55ns
- 70 ---------- 70ns
- 85 ---------- 85ns
- 90 ---------- 90ns
- 10 ---------- 100ns
- 12 ---------- 120ns

11. Power
- LL ---------- Low Low Power
- LF ---------- Low Low Power(Pb-Free&Green)
- L ---------- Low Power
- S ---------- Standard Power