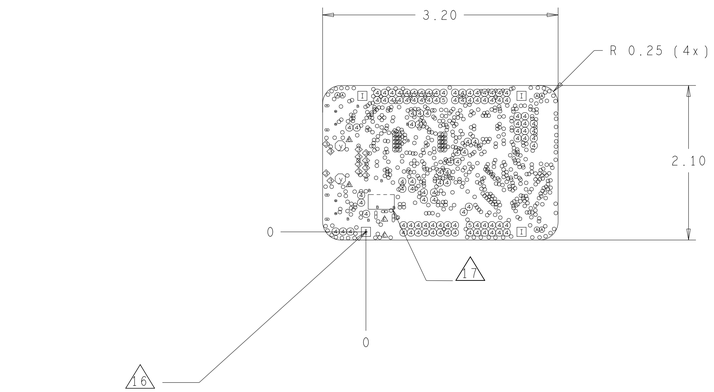
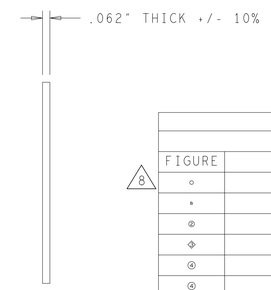
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	11-06-13	S. KP.
	B	RE-SPIN PER ECO48566	01-23-14	R.D.R.
	C	ADD SWO TRACE	02-06-14	R.D.R.
	D	RE-SPIN PER ECO49325	02-26-14	R.D.R.
	E	RE-SPIN PER ECO49784	07-31-14	R.D.R.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - REFER TO DETAIL B
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .0035"/.005"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - DARK BLUE GLOSS COLOR BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. 2 SOLDER SAMPLES TO BE PROVIDED.
16. BASIC GRID INCREMENT AT 1:1 IS .0001.
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (PB)
19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
22. .
    INTENTIONAL SHORT IN SH1 BETWEEN NETS P3V3 AND V_TGTMCU
    INTENTIONAL SHORT IN J5 BETWEEN NETS SDA_RST_TGTMCU_B AND SDA_RST_TGTMCU_J_B
    INTENTIONAL SHORT IN J7 BETWEEN NETS P3V3_SDA AND SDA_VOUT33
    INTENTIONAL SHORT IN J8 BETWEEN SWD_DIO_TGTMCU_BUF AND PTA3
    INTENTIONAL SHORT IN J11 BETWEEN NETS PTA0 AND SWD_CLK_TGTMCU
    INTENTIONAL SHORT IN J12 SWD_CLK_TGTMCU_BUF AND SWD_CLK_TGTMCU
    INTENTIONAL SHORT IN J16 BETWEEN VREGIN_K64 AND P5V_K64_USB
    INTENTIONAL SHORT IN J19 BETWEEN P3V3 AND P3V3_REG
    INTENTIONAL SHORT IN J20 BETWEEN P3V3 AND P3V3_K64F
    INTENTIONAL SHORT IN J23 BETWEEN P3V3_K64F AND VBAT
    5 INTENTIONAL DANGLING VIAS IN U8 AREA.
23. COPPER PADS FOR J4 AND J22 CAN BE SHAVED TO ALLOW .010" CLEARANCE FROM BOARD EDGE.





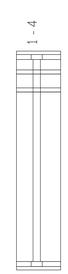
DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
○	10.0	+0.0/-10.0	PLATED	638
●	18.0	+2.0/-2.0	PLATED	9
⊗	28.0	+2.0/-2.0	PLATED	20
⊕	35.0	+2.0/-2.0	PLATED	12
⊕	40.0	+2.0/-2.0	PLATED	4
⊕	40.0	+3.0/-3.0	PLATED	103
⊕	50.0	+3.0/-3.0	PLATED	2
◬	63.0	+3.0/-3.0	PLATED	2
⊗	28.0	+2.0/-2.0	NON-PLATED	6
◬	63.0	+2.0/-2.0	NON-PLATED	2
1	125.0	+3.0/-3.0	NON-PLATED	4
2	128.0	+2.0/-2.0	NON-PLATED	2
▪	34.0x30.0	+2.0/-2.0	PLATED	4
▭	59.0x33.0	+2.0/-2.0	PLATED	4
▭	91.0x32.0	+3.0/-3.0	PLATED	1
▯	111.0x32.0	+3.0/-3.0	PLATED	2

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

Layers	Single Ended		Differential					
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)
L1_PS	4.50	50	4.50	6.30	90	3.50	6.50	100
L3_INT_1	5.10	50	4.70	7.00	90	3.50	6.80	100

		FINISHED Cu WEIGHT
LAYER 1	TOP SIDE	1 oz.
LAYER 2	GROUND PLANE	1 oz.
LAYER 3	INTERNAL 1	1 oz.
LAYER 4	BOTTOM SIDE	1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE



* SURFACE - AIR 0 MIL
* DIELECTRIC - DRY FILM MASK 1 MIL
L1: TOP CONDUCTOR - 1OZ COPPER 1.44 MIL
* DIELECTRIC - FR-4 3 MIL
L2: GND PLANE - COPPER 1.2 MIL
* DIELECTRIC - FR-4 4 MIL
L3: INT_1 CONDUCTOR - COPPER 1.2 MIL

* DIELECTRIC - FR-4 49 MIL

L4: BOTTOM CONDUCTOR - COPPER 1OZ 1.44 MIL
* DIELECTRIC - DRY FILM MASK 1 MIL
* SURFACE - AIR 0 MIL

DESIGN CROSS SECTION CHART
TOTAL THICKNESS 63.28 MIL

___ PUBI (PUBLIC INFORMATION)
_X_ FIUO (FREESCALE INTERNAL USE ONLY)
___ FCP (FREESCALE CONFIDENTIAL PROPRIETARY)

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF FREESCALE.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS .XX ±.01 .XXX ±.005
ANGLES ±0-30°
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-28163

APPROVALS	DATE
DRAWN A. CARRILLO	07-31-14
CHECKED R. VILLARREAL	07-31-14
DESIGN ENGINEER SUDHASHA KP.	07-31-14

FREESCALE
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD FRDM-K64F

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-28163	FAB-28163	E

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1