Sitronix

ST7539-G4

192 x 65 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7539 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 192-segment and 64-common with 1-icon-common driver circuits. This chip is connected directly to a microprocessor which accepts parallel interface (8-bit), serial peripheral interface (4-line SPI), I^2C interface. Display data stores in an on-chip display data RAM (DDRAM) of 192 x 65 bits. It performs Display Data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD Controller & Driver

Driver Output Circuits

- 192-segment / 64-common+1-icon-common

On-chip Display Data RAM (DDRAM)

- Capacity: 192x65= 12,480 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU
- 4-line SPI
- I^2C Interface

Built-in Oscillation Circuit

- Oscillator requires no external component
- Programmable frame frequency

External RST (hardware reset) Pin

Various Display Functions

- Partial display

Low Power Consumption Analog Circuit

- Voltage booster with internal capacitor (X6)
- Wide voltage regulator output range
- Built-in temperature compensation circuit
  Temperature Gradient: -0.06%/℃
- Built-in voltage follower for LCD bias voltages: 1/6 ~ 1/9 Bias

Wide Supply Voltage Range

- Digital Power (VDD1): 1.8V~3.3V (typical)
- Analog Power (VDD2,VDD3): 2.7V~3.3V (typical)

Temperature Range: -30℃ ~ +85℃

Package: COG

ST7539-G4	**6800 , 8080 , 4-Line Interface (without I^2C Interface)**	
ST7539i-G4	**I^2C Interface**	

3. PAD ARRANGEMENT

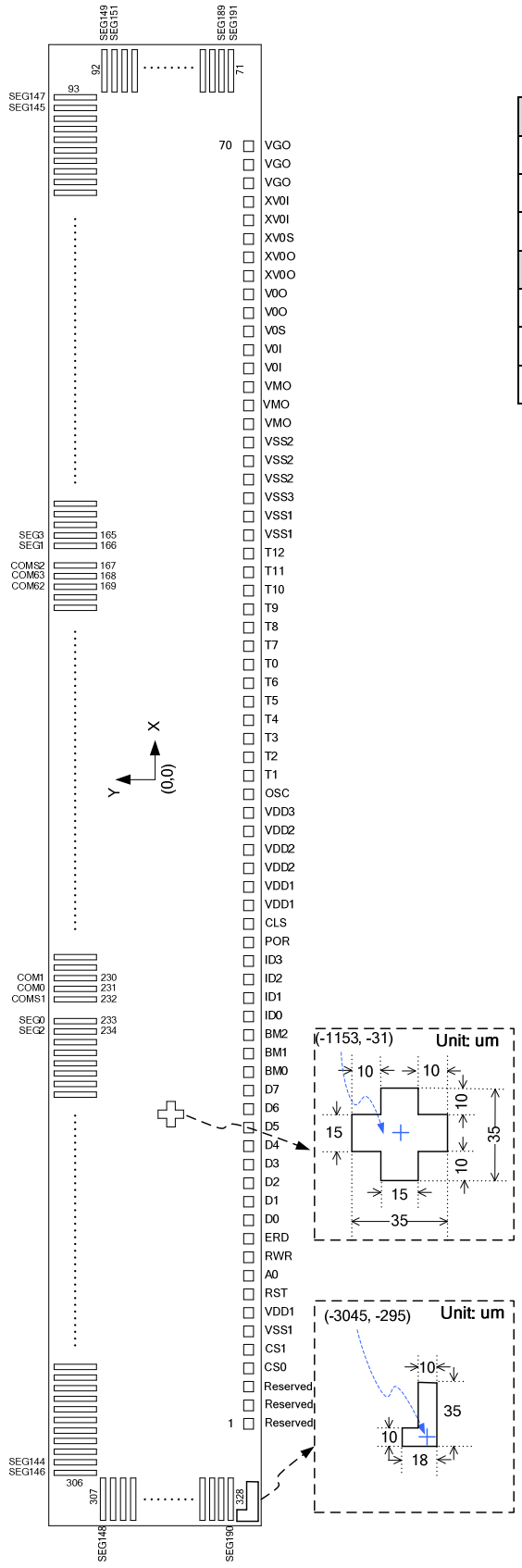


Fig 1.

ST7539-G4 **Bump Height: 10±3um**

Chip Size: (6160±50)um x (660±50)um **Chip Thickness: 300um**

PAD No.	Bump Size
1~35, 49~70	65 X 45
36~48	45 X 45
71~328	13 X120
PAD No.	**Bump Pitch (min)**
1~35, 49~70	80
36~48	60
71~328	25

Unit: um

*** Refer "PAD CENTER COORDINATES" section for ITO layout.**

4. PAD CENTER COORDINATES

PAD NO.	PAD NAME	X	Y
1	Reserved	-2505	-274.5
2	Reserved	-2425	-274.5
3	Reserved	-2345	-274.5
4	CS0	-2265	-274.5
5	CS1	-2185	-274.5
6	VSS1	-2105	-274.5
7	VDD1	-2025	-274.5
8	RST	-1945	-274.5
9	A0	-1865	-274.5
10	RWR	-1785	-274.5
11	ERD	-1705	-274.5
12	D0	-1625	-274.5
13	D1	-1545	-274.5
14	D2	-1465	-274.5
15	D3	-1385	-274.5
16	D4	-1305	-274.5
17	D5	-1225	-274.5
18	D6	-1145	-274.5
19	D7	-1065	-274.5
20	BM0	-985	-274.5
21	BM1	-905	-274.5
22	BM2	-825	-274.5
23	ID0	-745	-274.5
24	ID1	-665	-274.5
25	ID2	-585	-274.5
26	ID3	-505	-274.5
27	POR	-425	-274.5
28	CLS	-345	-274.5
29	VDD1	-265	-274.5
30	VDD1	-185	-274.5
31	VDD2	-105	-274.5
32	VDD2	-25	-274.5
33	VDD2	55	-274.5
34	VDD3	135	-274.5
35	OSC	215	-274.5
36	T1	285	-274.5
37	T2	345	-274.5
38	T3	405	-274.5
39	T4	465	-274.5
40	T5	525	-274.5
41	T6	585	-274.5

PAD NO.	PAD NAME	X	Y
42	T0	645	-274.5
43	T7	705	-274.5
44	T8	765	-274.5
45	T9	825	-274.5
46	T10	885	-274.5
47	T11	945	-274.5
48	T12	1005	-274.5
49	VSS1	1075	-274.5
50	VSS1	1155	-274.5
51	VSS3	1235	-274.5
52	VSS2	1315	-274.5
53	VSS2	1395	-274.5
54	VSS2	1475	-274.5
55	VMO	1555	-274.5
56	VMO	1635	-274.5
57	VMO	1715	-274.5
58	V0I	1795	-274.5
59	V0I	1875	-274.5
60	V0S	1955	-274.5
61	V0O	2035	-274.5
62	V0O	2115	-274.5
63	XV0O	2195	-274.5
64	XV0O	2275	-274.5
65	XV0S	2355	-274.5
66	XV0I	2435	-274.5
67	XV0I	2515	-274.5
68	VGO	2595	-274.5
69	VGO	2675	-274.5
70	VGO	2755	-274.5
71	SEG191	2987	-267.5
72	SEG189	2987	-242.5
73	SEG187	2987	-217.5
74	SEG185	2987	-192.5
75	SEG183	2987	-167.5
76	SEG181	2987	-142.5
77	SEG179	2987	-117.5
78	SEG177	2987	-92.5
79	SEG175	2987	-67.5
80	SEG173	2987	-42.5
81	SEG171	2987	-17.5
82	SEG169	2987	7.5

PAD NO.	PAD NAME	X	Y
83	SEG167	2987	32.5
84	SEG165	2987	57.5
85	SEG163	2987	82.5
86	SEG161	2987	107.5
87	SEG159	2987	132.5
88	SEG157	2987	157.5
89	SEG155	2987	182.5
90	SEG153	2987	207.5
91	SEG151	2987	232.5
92	SEG149	2987	257.5
93	SEG147	2897.5	237
94	SEG145	2872.5	237
95	SEG143	2847.5	237
96	SEG141	2822.5	237
97	SEG139	2797.5	237
98	SEG137	2772.5	237
99	SEG135	2747.5	237
100	SEG133	2722.5	237
101	SEG131	2697.5	237
102	SEG129	2672.5	237
103	SEG127	2647.5	237
104	SEG125	2622.5	237
105	SEG123	2597.5	237
106	SEG121	2572.5	237
107	SEG119	2547.5	237
108	SEG117	2522.5	237
109	SEG115	2497.5	237
110	SEG113	2472.5	237
111	SEG111	2447.5	237
112	SEG109	2422.5	237
113	SEG107	2397.5	237
114	SEG105	2372.5	237
115	SEG103	2347.5	237
116	SEG101	2322.5	237
117	SEG99	2297.5	237
118	SEG97	2272.5	237
119	SEG95	2247.5	237
120	SEG93	2222.5	237
121	SEG91	2197.5	237
122	SEG89	2172.5	237
123	SEG87	2147.5	237
124	SEG85	2122.5	237
125	SEG83	2097.5	237
126	SEG81	2072.5	237

PAD NO.	PAD NAME	X	Y
127	SEG79	2047.5	237
128	SEG77	2022.5	237
129	SEG75	1997.5	237
130	SEG73	1972.5	237
131	SEG71	1947.5	237
132	SEG69	1922.5	237
133	SEG67	1897.5	237
134	SEG65	1872.5	237
135	SEG63	1847.5	237
136	SEG61	1822.5	237
137	SEG59	1797.5	237
138	SEG57	1772.5	237
139	SEG55	1747.5	237
140	SEG53	1722.5	237
141	SEG51	1697.5	237
142	SEG49	1672.5	237
143	SEG47	1647.5	237
144	SEG45	1622.5	237
145	SEG43	1597.5	237
146	SEG41	1572.5	237
147	SEG39	1547.5	237
148	SEG37	1522.5	237
149	SEG35	1497.5	237
150	SEG33	1472.5	237
151	SEG31	1447.5	237
152	SEG29	1422.5	237
153	SEG27	1397.5	237
154	SEG25	1372.5	237
155	SEG23	1347.5	237
156	SEG21	1322.5	237
157	SEG19	1297.5	237
158	SEG17	1272.5	237
159	SEG15	1247.5	237
160	SEG13	1222.5	237
161	SEG11	1197.5	237
162	SEG9	1172.5	237
163	SEG7	1147.5	237
164	SEG5	1122.5	237
165	SEG3	1097.5	237
166	SEG1	1072.5	237
167	COMS2	937.5	237
168	COM63	912.5	237
169	COM62	887.5	237
170	COM61	862.5	237

PAD NO.	PAD NAME	X	Y
171	COM60	837.5	237
172	COM59	812.5	237
173	COM58	787.5	237
174	COM57	762.5	237
175	COM56	737.5	237
176	COM55	712.5	237
177	COM54	687.5	237
178	COM53	662.5	237
179	COM52	637.5	237
180	COM51	612.5	237
181	COM50	587.5	237
182	COM49	562.5	237
183	COM48	537.5	237
184	COM47	512.5	237
185	COM46	487.5	237
186	COM45	462.5	237
187	COM44	437.5	237
188	COM43	412.5	237
189	COM42	387.5	237
190	COM41	362.5	237
191	COM40	337.5	237
192	COM39	312.5	237
193	COM38	287.5	237
194	COM37	262.5	237
195	COM36	237.5	237
196	COM35	212.5	237
197	COM34	187.5	237
198	COM33	162.5	237
199	COM32	137.5	237
200	COM31	112.5	237
201	COM30	87.5	237
202	COM29	62.5	237
203	COM28	37.5	237
204	COM27	12.5	237
205	COM26	-12.5	237
206	COM25	-37.5	237
207	COM24	-62.5	237
208	COM23	-87.5	237
209	COM22	-112.5	237
210	COM21	-137.5	237
211	COM20	-162.5	237
212	COM19	-187.5	237
213	COM18	-212.5	237
214	COM17	-237.5	237

PAD NO.	PAD NAME	X	Y
215	COM16	-262.5	237
216	COM15	-287.5	237
217	COM14	-312.5	237
218	COM13	-337.5	237
219	COM12	-362.5	237
220	COM11	-387.5	237
221	COM10	-412.5	237
222	COM9	-437.5	237
223	COM8	-462.5	237
224	COM7	-487.5	237
225	COM6	-512.5	237
226	COM5	-537.5	237
227	COM4	-562.5	237
228	COM3	-587.5	237
229	COM2	-612.5	237
230	COM1	-637.5	237
231	COM0	-662.5	237
232	COMS1	-687.5	237
233	SEG0	-822.5	237
234	SEG2	-847.5	237
235	SEG4	-872.5	237
236	SEG6	-897.5	237
237	SEG8	-922.5	237
238	SEG10	-947.5	237
239	SEG12	-972.5	237
240	SEG14	-997.5	237
241	SEG16	-1022.5	237
242	SEG18	-1047.5	237
243	SEG20	-1072.5	237
244	SEG22	-1097.5	237
245	SEG24	-1122.5	237
246	SEG26	-1147.5	237
247	SEG28	-1172.5	237
248	SEG30	-1197.5	237
249	SEG32	-1222.5	237
250	SEG34	-1247.5	237
251	SEG36	-1272.5	237
252	SEG38	-1297.5	237
253	SEG40	-1322.5	237
254	SEG42	-1347.5	237
255	SEG44	-1372.5	237
256	SEG46	-1397.5	237
257	SEG48	-1422.5	237
258	SEG50	-1447.5	237

PAD NO.	PAD NAME	X	Y
259	SEG52	-1472.5	237
260	SEG54	-1497.5	237
261	SEG56	-1522.5	237
262	SEG58	-1547.5	237
263	SEG60	-1572.5	237
264	SEG62	-1597.5	237
265	SEG64	-1622.5	237
266	SEG66	-1647.5	237
267	SEG68	-1672.5	237
268	SEG70	-1697.5	237
269	SEG72	-1722.5	237
270	SEG74	-1747.5	237
271	SEG76	-1772.5	237
272	SEG78	-1797.5	237
273	SEG80	-1822.5	237
274	SEG82	-1847.5	237
275	SEG84	-1872.5	237
276	SEG86	-1897.5	237
277	SEG88	-1922.5	237
278	SEG90	-1947.5	237
279	SEG92	-1972.5	237
280	SEG94	-1997.5	237
281	SEG96	-2022.5	237
282	SEG98	-2047.5	237
283	SEG100	-2072.5	237
284	SEG102	-2097.5	237
285	SEG104	-2122.5	237
286	SEG106	-2147.5	237
287	SEG108	-2172.5	237
288	SEG110	-2197.5	237
289	SEG112	-2222.5	237
290	SEG114	-2247.5	237
291	SEG116	-2272.5	237
292	SEG118	-2297.5	237
293	SEG120	-2322.5	237
294	SEG122	-2347.5	237

PAD NO.	PAD NAME	X	Y
295	SEG124	-2372.5	237
296	SEG126	-2397.5	237
297	SEG128	-2422.5	237
298	SEG130	-2447.5	237
299	SEG132	-2472.5	237
300	SEG134	-2497.5	237
301	SEG136	-2522.5	237
302	SEG138	-2547.5	237
303	SEG140	-2572.5	237
304	SEG142	-2597.5	237
305	SEG144	-2622.5	237
306	SEG146	-2647.5	237
307	SEG148	-2987	257.5
308	SEG150	-2987	232.5
309	SEG152	-2987	207.5
310	SEG154	-2987	182.5
311	SEG156	-2987	157.5
312	SEG158	-2987	132.5
313	SEG160	-2987	107.5
314	SEG162	-2987	82.5
315	SEG164	-2987	57.5
316	SEG166	-2987	32.5
317	SEG168	-2987	7.5
318	SEG170	-2987	-17.5
319	SEG172	-2987	-42.5
320	SEG174	-2987	-67.5
321	SEG176	-2987	-92.5
322	SEG178	-2987	-117.5
323	SEG180	-2987	-142.5
324	SEG182	-2987	-167.5
325	SEG184	-2987	-192.5
326	SEG186	-2987	-217.5
327	SEG188	-2987	-242.5
328	SEG190	-2987	-267.5

Unit: um

5. BLOCK DIAGRAM

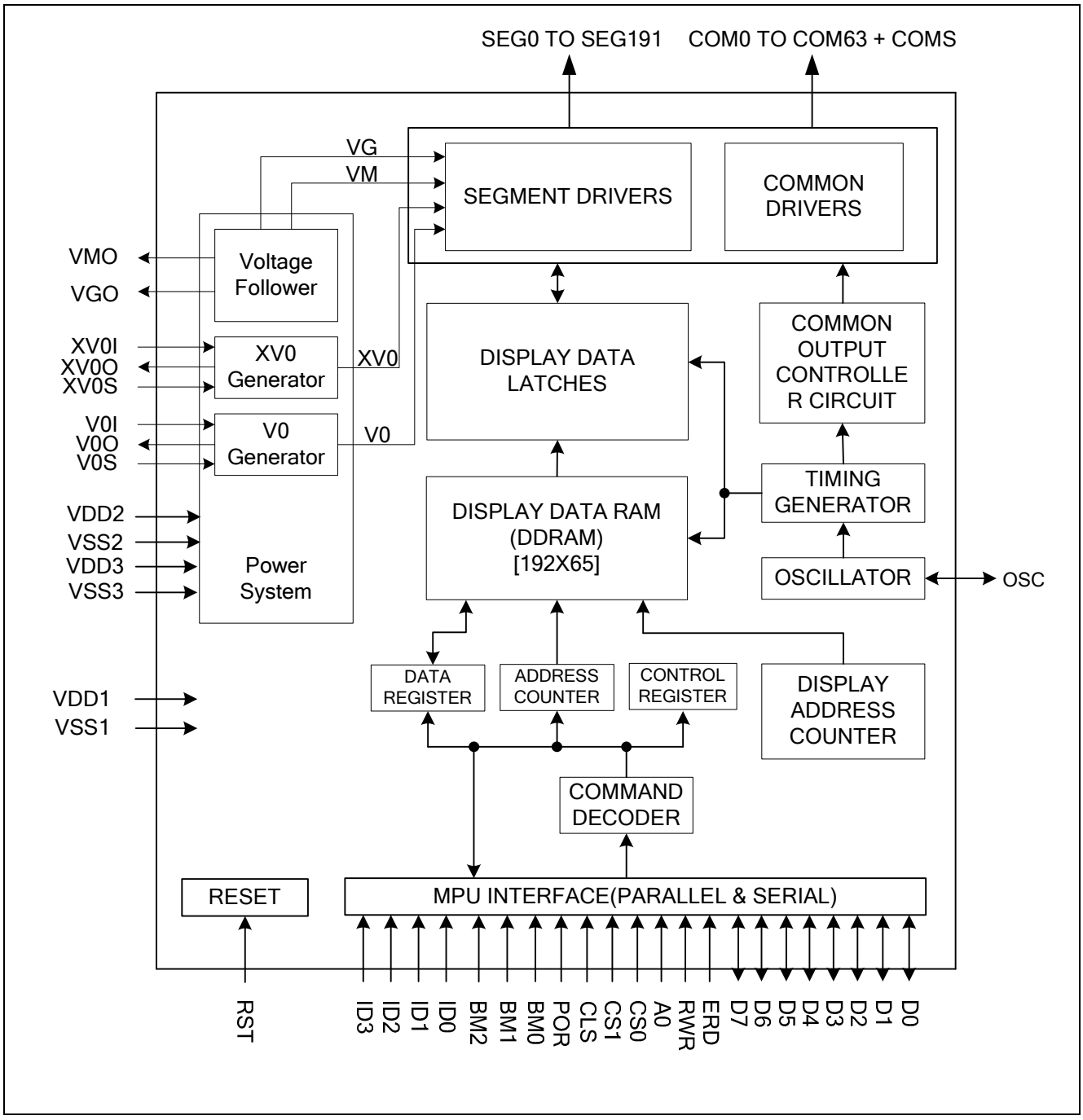


Fig 2. Block Diagram

6. PIN DESCRIPTIONS

LCD Driver Output Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>SEG[0:191]</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF (Power Save)</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM[0:63]</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Display OFF (Power Save)</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COMS1, COMS2
(COMS)</td><td>O</td><td>LCD common driver outputs for icons. These two pins are identical. Choose one of them if using icon. When icon is not used, left these pins open.</td></tr>
</table>

Clock System Input

Pin Name	Type	Description
CLS	**I**	Clock source selection pin. CLS=”H” : enable internal clock. CLS=”L” : disable internal clock and use external clock.
OSC	**I/O**	For external clock. If CLS=”H” : this pin should be left open. if CLS=”L” : this pin should apply the external clock (for testing only).

Power Supply Pins

Pin Name	Type	Description
VDD1	**Power**	Digital power. If VDD1=VDD2, connect to VDD2 by FPC. For select pins that are set to be “H”, connect them to this power (use VDD1 for “H”).
VDD2	**Power**	Analog power. If VDD1=VDD2, connect to VDD1 by FPC.
VDD3	**Power**	Analog power. Connect to VDD2 by ITO or FPC.
VSS1	**Power**	Digital ground. Connect to VSS2 by FPC. For select pins that are set to be “L”, connect them to this power (use VSS1 for “L”).
VSS2	**Power**	Analog ground. Connect to VSS1 by FPC.
VSS3	**Power**	Analog ground. Connect to VSS1 by FPC.

Built-in Power System Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>V0O
V0I
V0S</td><td>Power</td><td>LCD driving voltage for commons at negative frame.
V0I should be short with V0S in ITO then connect together with V0O in FPC layout.</td></tr>
<tr><td>XV0O
XV0I
XV0S</td><td>Power</td><td>LCD driving voltage for commons at positive frame.
XV0I should be short with XV0S in ITO then connect together with XV0O in FPC layout.</td></tr>
<tr><td>VGO</td><td>Power</td><td>LCD driving voltage for segments.
Be aware that: 1.8 ≤ VG < VDD2-0.4V.</td></tr>
<tr><td>VMO</td><td>Power</td><td>LCD driving voltage for commons.
Be aware that: 0.9 ≤ VM < VG.
When the internal power circuit is active, the VG and VM are generated according to the bias setting as shown below:
<table>
<tr><th>LCD bias</th><th>VG</th><th>VM</th></tr>
<tr><td>1/N bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
</td></tr>
</table>

Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BM[2:0]</td><td>I</td><td>Microprocessor interface select pins.
<table>
<tr><th>BM2</th><th>BM1</th><th>BM0</th><th>Interface Mode</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>4-line serial interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>I^2C serial interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>8-bit 6800 parallel interface</td></tr>
</table>
</td></tr>
<tr><td>POR</td><td>I</td><td>“Power-On Reset” control pin.
POR=”H” to disable “Power-ON Reset” mode.
POR=”L” to enable “Power-ON Reset” mode.</td></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin.
When RST is “L”, internal initialization is executed.</td></tr>
<tr><td>CS[1:0]</td><td>I</td><td>Chip select input pins and slave address pins (I^2C).
Interface access is enabled when CS0 is “L” and CS1 is “H” in parallel interface (8080/6800) and SPI interface (4-SPI).
CS[1:0] pins are used for slave address pins (SA[1:0]) in I^2C.</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H” : Indicates that D[7:0] are display data.
A0=“L” : Indicates that D[7:0] are control data.
There is no A0 pin in I^2C interface and should fix to “H” by VDD1.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When parallel interface is selected:
<table>
<tr><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
Note : RWR is not used in serial interfaces and should fix to “H” by VDD1.</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When parallel interface is selected:
<table>
<tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in an output status.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output status.</td></tr>
</table>
Note : ERD is not used in serial interfaces and should fix to “H” by VDD1.</td></tr>
<tr><td rowspan="3">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 6800 or 8080 mode
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
Note : When CS0 is non-active (CS0=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface: 4-line SPI mode
D[0] : serial input clock (SCL).
D[2:1] : fix to “H” by VDD1.
D[5:3] : serial input data (SDA).
D[7:6] : fix to “H” by VDD1.
<u>D3 to D5 must be connected together (SDA)</u>
Note : When CS0 is non-active (CS0=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I/O</td><td>When using I^{2}C interface
D[0] : SCL, serial clock input.
D[2:1] : fix to “H” by VDD1.
D[3] : SDA_IN, serial input data.
D[4:5] : SDA_ OUT, serial data acknowledge for the I^{2}C interface.
D[7:6] : fix to “H” by VDD1.
<u>D3 to D5 must be connected together (SDA)</u>
Note : SA[1:0] : CS[1:0], I^{2}C slave address bits of ST7539. Must connect to VDD1 or VSS1.</td></tr>
</table>

Note:

1. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^{2}C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider, which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledged-signal level and system cannot recognize this level as a valid logic “0” level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode that ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.
2. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

Test Pin

Pin Name	Type	Description
T[0]	**Test**	This pin is reserved for test only, recommend setting to VSS1.
T[12:1]	**Test**	These pins are reserved for test only, recommend setting to floating.
ID[3:0]	**Test**	These pins are reserved for test only, recommend setting to VDD1 or VSS1.
Reserved	**Test**	Reserve for testing only, recommend setting to floating.

Recommend ITO Resistance

Pin Name	ITO Resistance
Reserved	Floating
VDD1, VDD2, VSS1, VSS2	< 100Ω
VMO, VGO, V0(V0I, V0O, V0S), XV0(XV0I, XV0O, XV0S), VDD3, VSS3, SDA(I^2C), SCL(I^2C)	< 100Ω
A0, RWR, ERD, CS[1:0], D[7:0], T[12:0]	< 1KΩ
BM[2:0], ID[3:0], POR, OSC, CLS	< 5KΩ
RST *1	3KΩ ~ 10KΩ

Note:

1. The RST pin has the most priority over other control signals. It is important to prevent the ESD pulse or external noise flow into this pin. By adding a series resistor externally or increase the ITO resistance at this pin, the unexpected reset condition can be solved. The recommended resistance is around 3K~10K Ohm (the optimized value depends on the LCD module and application system).
2. If using I^2C interface mode, the resistance of SDA signal is recommended to be lower than 100Ω (if the system pull up resistor is 4.7KΩ).
3. If using 4-Line SPI interface with VDD1 less than 2.4V, the SDA signal resistance should be less than 100Ω.
4. This table defines the actual ITO resistance. The actual ITO resistance should in these ranges, not the calculated ITO resistance value. The ITO tolerance should be considered.
5. The option setting to be “H” should connect to VDD1.
6. The option setting to be “L” should connect to VSS1.

ITO Layout Notes

1. The limitations include the bottleneck of ITO layout.
2. Make sure that the ITO resistance of all COM outputs are equal, and so are SEG outputs.
3. To avoid the noise in different power systems affect other power system, please separate them on ITO layout.
4. The V0 and XV0 circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC. The FPC layout and the equivalent circuit are shown below:

The FPC layout is shown below:

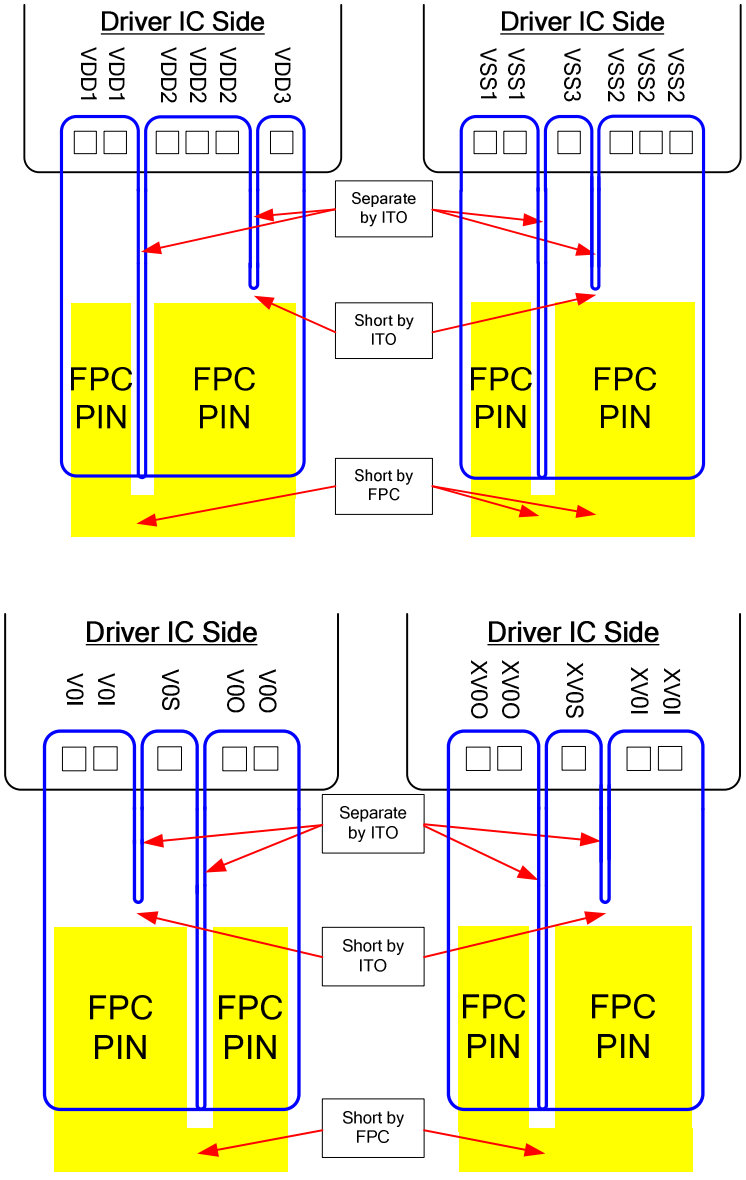
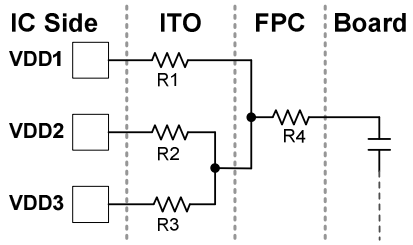
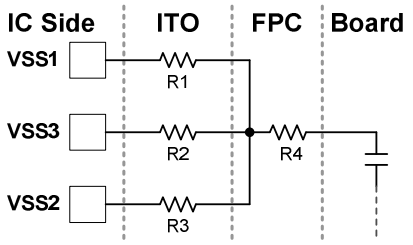
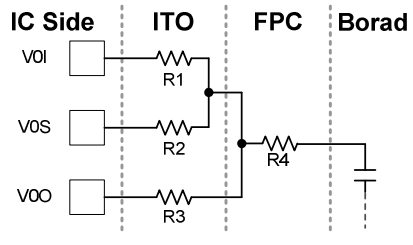
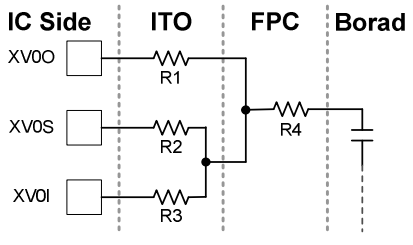


Fig 3.

The equivalent circuit is shown below:

VDD	VSS
	
Ideal Layout: => R4=0 Ohm. R3>>R1>R2. **Acceptable Layout:** => R4≠0. R3>>R1>R2>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).	**Ideal Layout:** => R4=0 Ohm. R2>>R1>R3. **Acceptable Layout:** => R4≠0. R2>>R1>R3>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).

V0	XV0
	
Ideal Layout: => R4=0 Ohm. R2>>R3>R1. **Acceptable Layout:** => R4≠0. R2>>R3>R1>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).	**Ideal Layout:** => R4=0 Ohm. R2>>R1>R3. **Acceptable Layout:** => R4≠0. R2>>R1>R3>R4. **Not Acceptable:** => R4 ≥ (R1 or R2 or R3).

7. FUNCTIONS DESCRIPTION

Microprocessor Interface

Chip Select Input

CS0 pin is used for chip selection. ST7539 can interface with an MPU when CS0 is "L" and CS1 is “H”. When CS0 is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial interface, the internal shift register and serial counter are reset when CS0 is “H”.

Parallel / Serial Interface

ST7539 has types of interface for kinds of MPU. The MPU interface is selected by BM[2:0] pins as shown in table 1.

Table 1. Parallel/Serial Interface Mode

Type	BM2	BM1	BM0	Interface mode
Parallel	H	H	L	8bit 8080-series MPU mode
	H	H	H	8 bit 6800-series MPU mode
Serial	L	L	L	4-line serial interface
	H	L	H	I^2C serial interface

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by BM[2:0] as shown in table 2. The data transfer type is determined by signals of A0, ERD and RWR as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

BM2	BM1	BM0	CS0	CS1	A0	ERD	RWR	D[7:0]	MPU Interface
H	H	L	CS0	CS1	A0	/RD	/WR	D[7:0]	8080-series
H	H	H				E	R/W		6800-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

Setting Serial Interface

Interface	CS0	CS1	A0	ERD	RWR	D[7:0]
4-Line SPI	CS0	CS1	A0	--	--	D[7:6]= --, D[5:3]=SDA, D[2:1]=--, D[0]=SCL
I^2C	SA0	SA1	--	--	--	D[7:6]=--, D[5:4]=SDA_ OUT, D[3]=SDA_ IN, D[2:1]=-- , D[0]=SCL, CS[1:0]=SA[1:0]. Refer to I^2C interface.

* The un-used pins are marked as “--” and should be fixed to “H” by VDD1.

Note:

1. The option setting to be “H” should connect to VDD1.
2. The option setting to be “L” should connect to VSS1.

4-Line Serial interface

ST7539 is active when CS0 is “L” and CS1 is “H”, serial data (SDA) and serial clock (SCL) inputs are enabled. When CS0 and CS1 are “H”, ST7539 is not active, and the internal 8-bit shift register and 3-bit counter are reset. Some specified information (status byte) can be read out in this mode. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

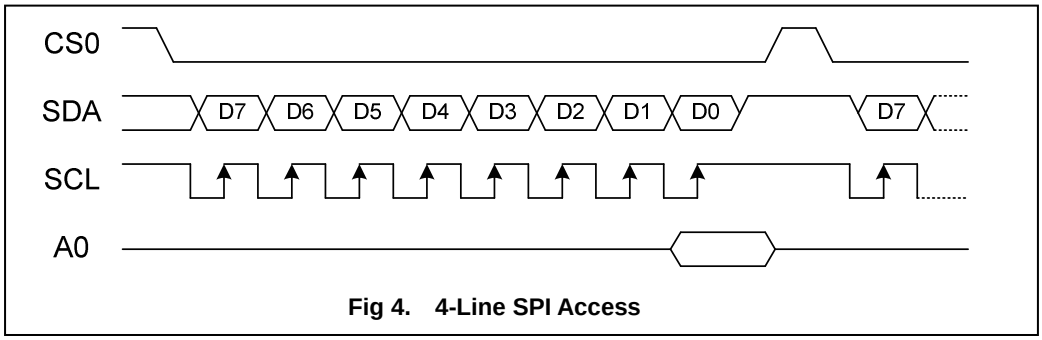


Fig 4. 4-Line SPI Access

I^{2}C Interface

The I^{2}C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.

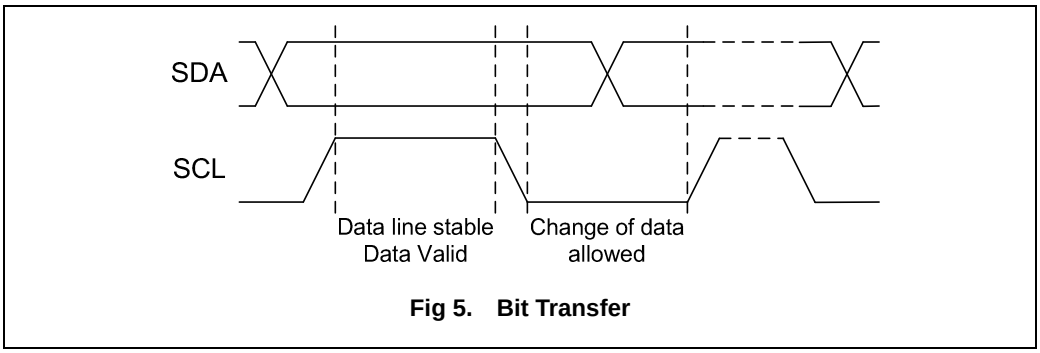


Fig 5. Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

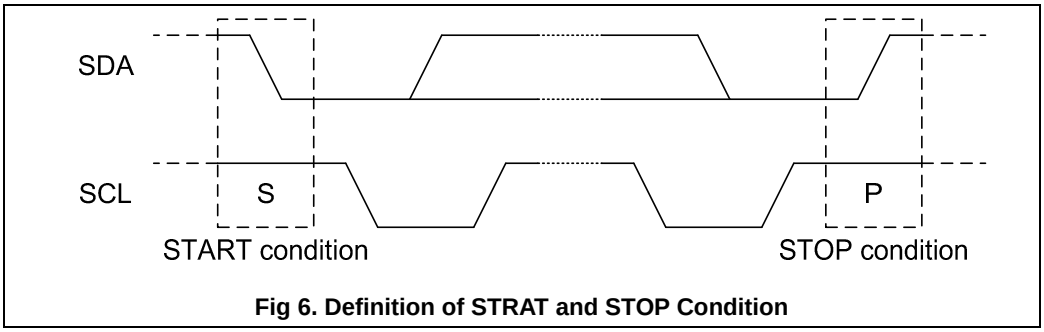


Fig 6. Definition of STRAT and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7. and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

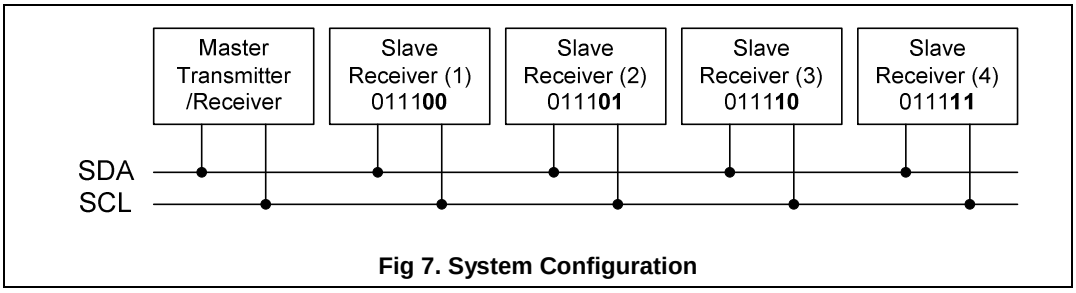


Fig 7. System Configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in Fig 8.

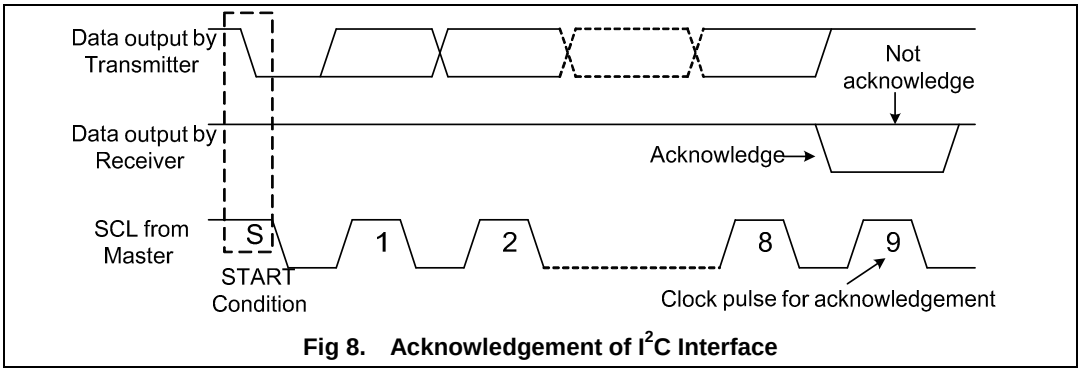


Fig 8. Acknowledgement of I^2C Interface

I²C INTERFACE PROTOCOL

ST7539 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 6-bit slave addresses (0111**00**, 0111**01**, 0111**10** and 0111**11**) and A0 (011100**0** or 011100**1**) are reserved for ST7539. The bit 2 and bit 1 are slave address that set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1). The I²C Interface protocol is illustrated in Fig 9.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address and A0. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

The slave address and control byte is tagged with a cleared most significant bit. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7539 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7539 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

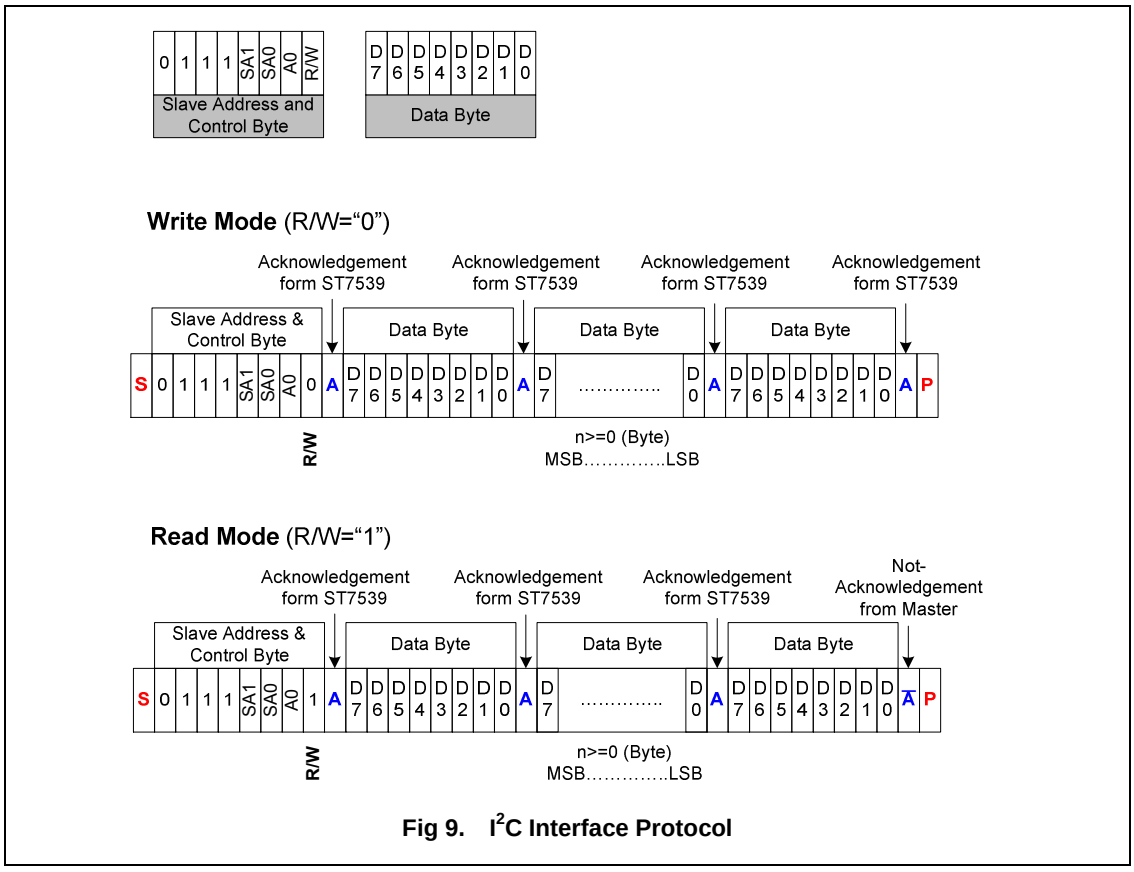


Fig 9. I²C Interface Protocol

Data Transfer

ST7539 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig 10. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig 11. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

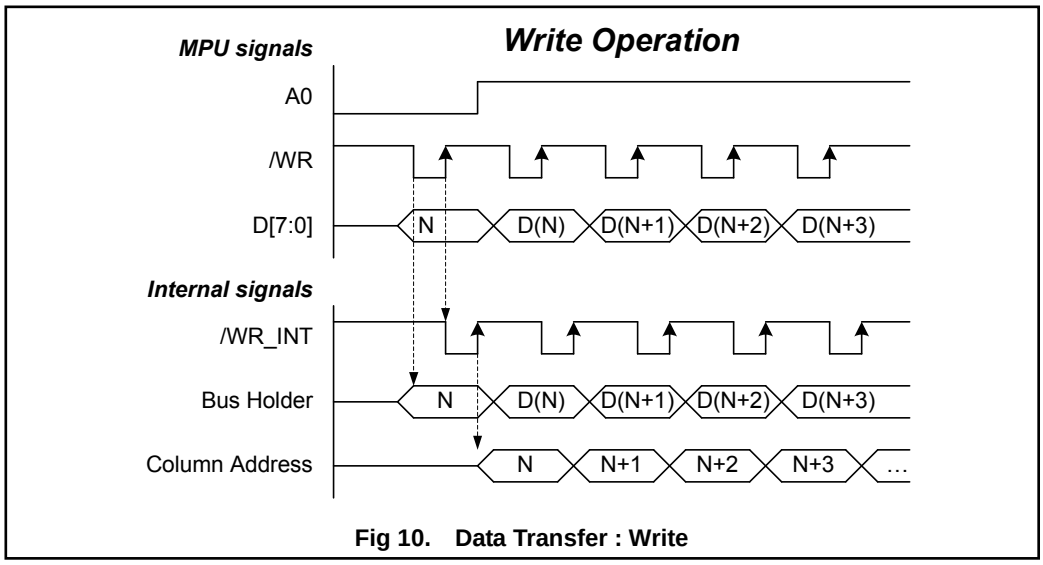


Fig 10. Data Transfer : Write

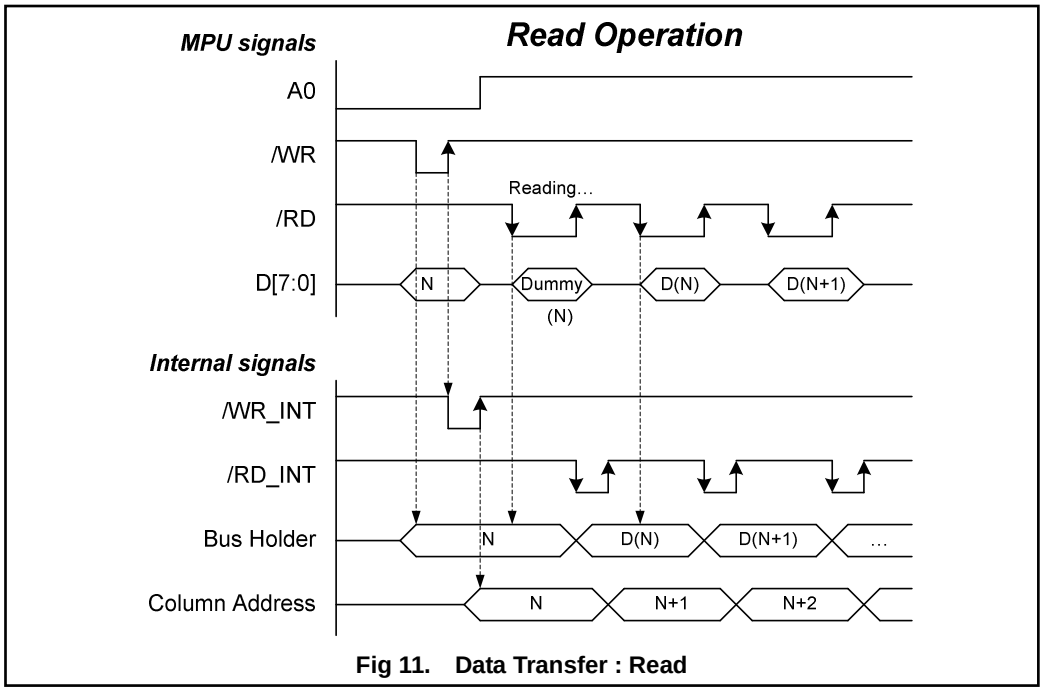


Fig 11. Data Transfer : Read

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 192-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages (Page 0~Page 7) of 8 lines and the 9th page (Page 8) with a single line (D0 only). Data is written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The LCD controller and MPU interface operate independently, data can be written into RAM at the same time when data is being displayed without flicker on LCD.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page Address” instruction. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 192-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). The DDRAM column address is specified by the “Set Column Address” command. The specified column address is incremented (+1) with each display data read/write access. This allows the MPU display data to be accessed continuously.

Control flag MY can invert the output order of the COM pads. And the MX flag makes it possible to invert the relationship between the Column Address and the SEG outputs. It is necessary to rewrite the display data into DDRAM after changing MX flag setting.

SEG Output

MX	Segment Pads	
	SEG0	SEG191
0	Col-0 → Column Address → Col-191	
1	Col-191 ← Column Address ← Col-0	

COM Output

MY	Common Pads		
	COM0	COM63	COMS
0	Com0 → Common Address → Com63 →		COMS
1	Com63 ← Common Address ←	Com0 →	COMS

DDRAM Organization

When accessing to RAM, sixteen addressing mode are provided:

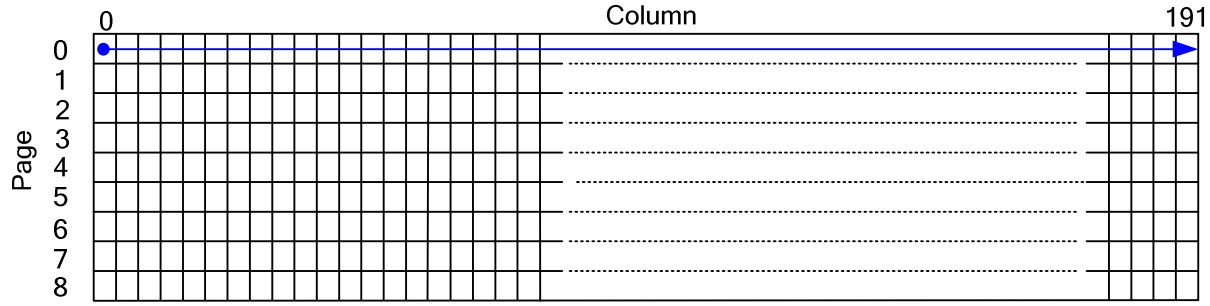


Fig 12. DDRAM Access Mapping (MX=0, AC[2:0]=0, PA[3:0]=0, CA[3:0]=0)

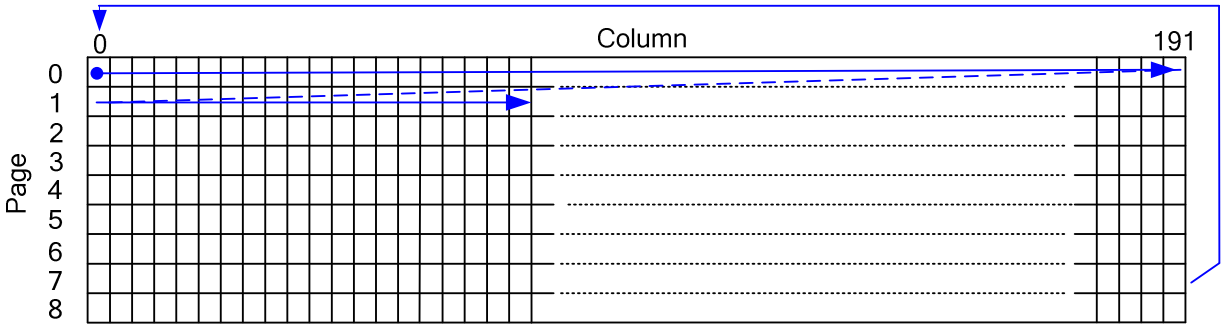


Fig 13. DDRAM Access Mapping (MX=0, AC[2:0]=1, PA[3:0]=0, CA[3:0]=0)

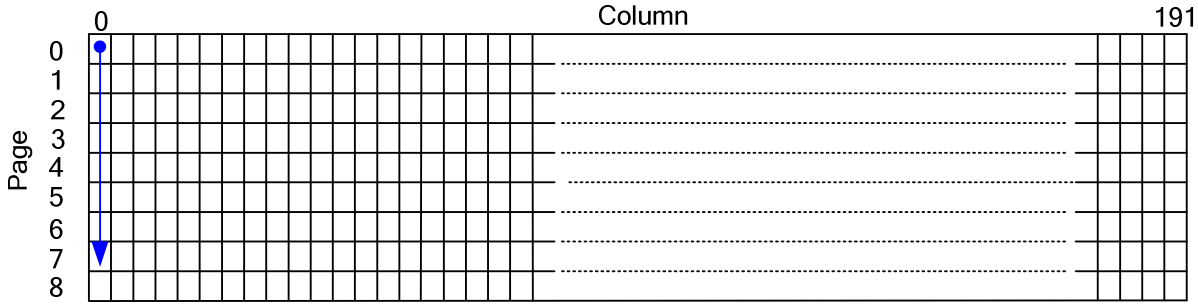


Fig 14. DDRAM Access Mapping (MX=0, AC[2:0]=2, PA[3:0]=0, CA[3:0]=0)

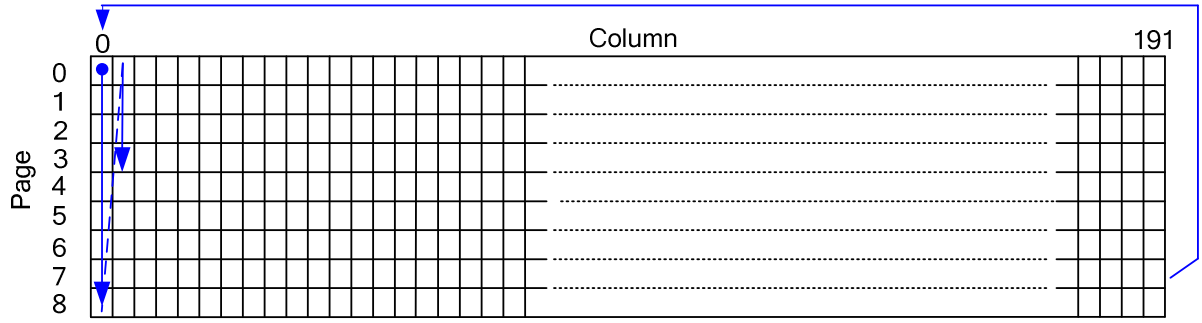


Fig 15. DDRAM Access Mapping (MX=0, AC[2:0]=3, PA[3:0]=0, CA[3:0]=0)

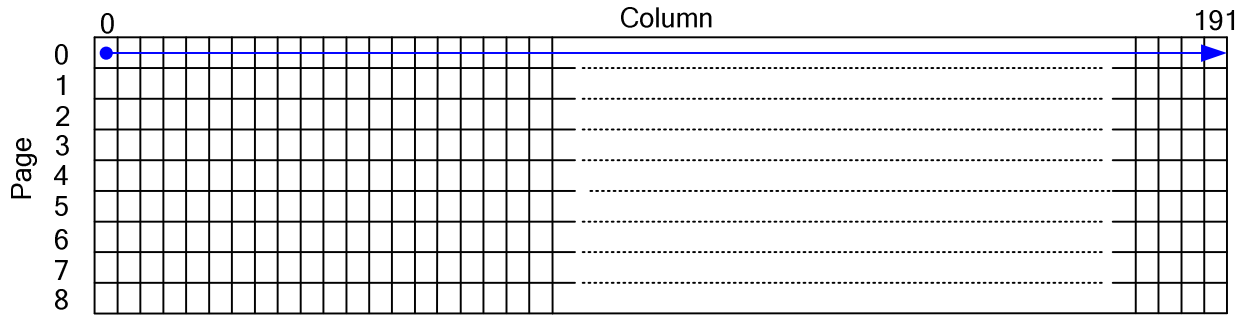


Fig 16. DDRAM Access Mapping (MX=0, AC[2:0]=4, PA[3:0]=0, CA[3:0]=0)

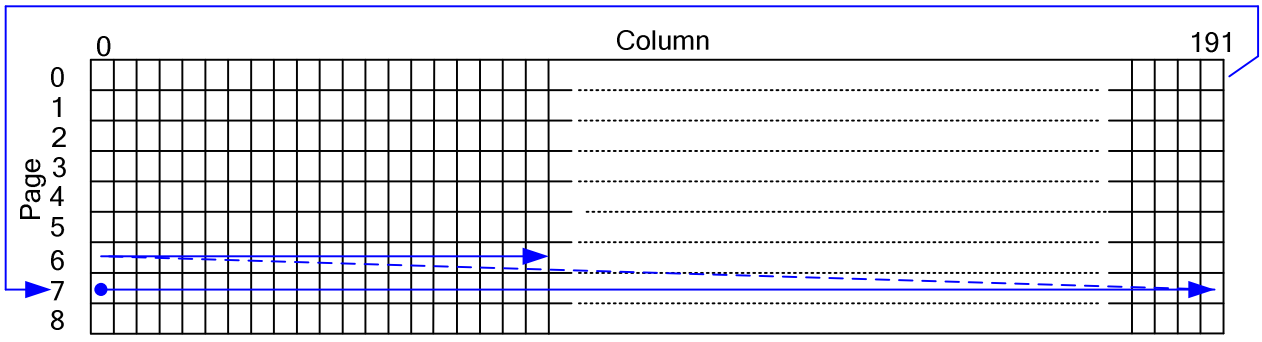


Fig 17. DDRAM Access Mapping (MX=0, AC[2:0]=5, PA[3:0]=7, CA[3:0]=0)

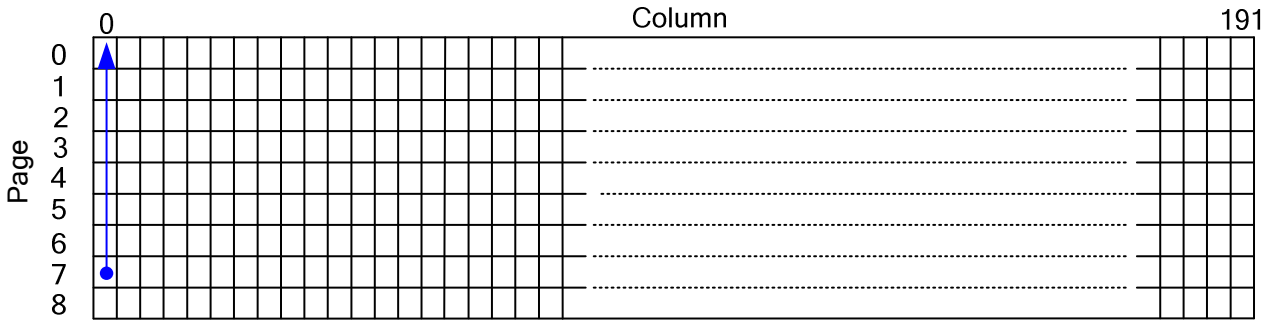


Fig 18. DDRAM Access Mapping (MX=0, AC[2:0]=6, PA[3:0]=7, CA[3:0]=0)

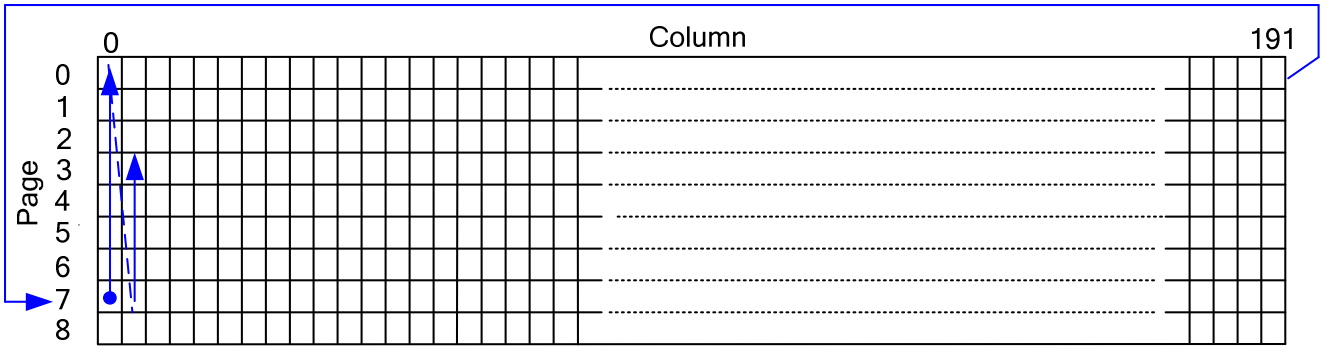


Fig 19. DDRAM Access Mapping (MX=0, AC[2:0]=7, PA[3:0]=7, CA[3:0]=0)

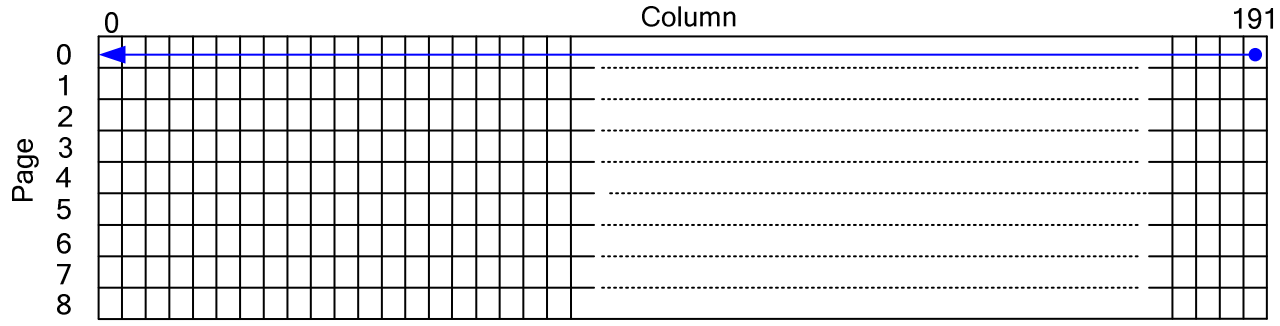


Fig 20. DDRAM Access Mapping (MX=1, AC[2:0]=0, PA[3:0]=0, CA[3:0]=0)

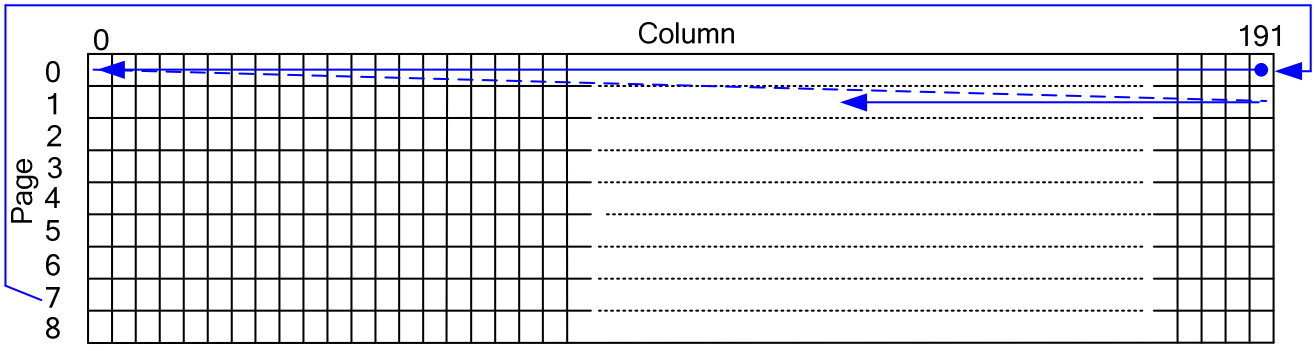


Fig 21. DDRAM Access Mapping (MX=1, AC[2:0]=1, PA[3:0]=0, CA[3:0]=0)

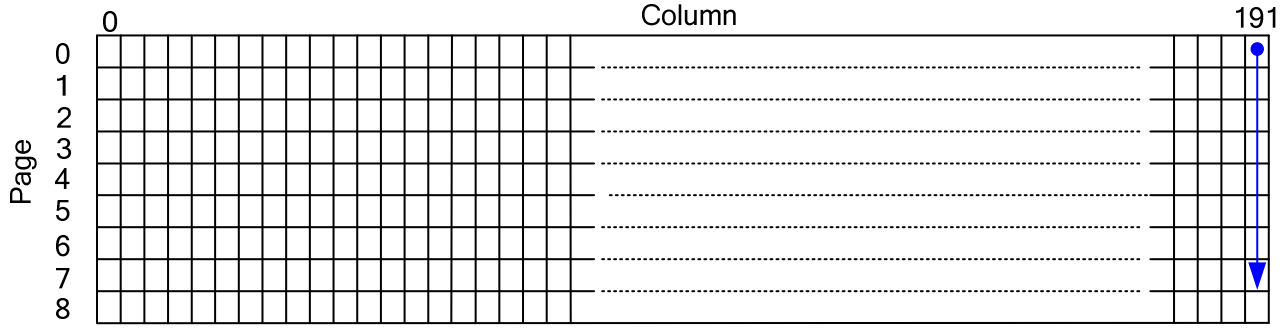


Fig 22. DDRAM Access Mapping (MX=1, AC[2:0]=2, PA[3:0]=0, CA[3:0]=0)

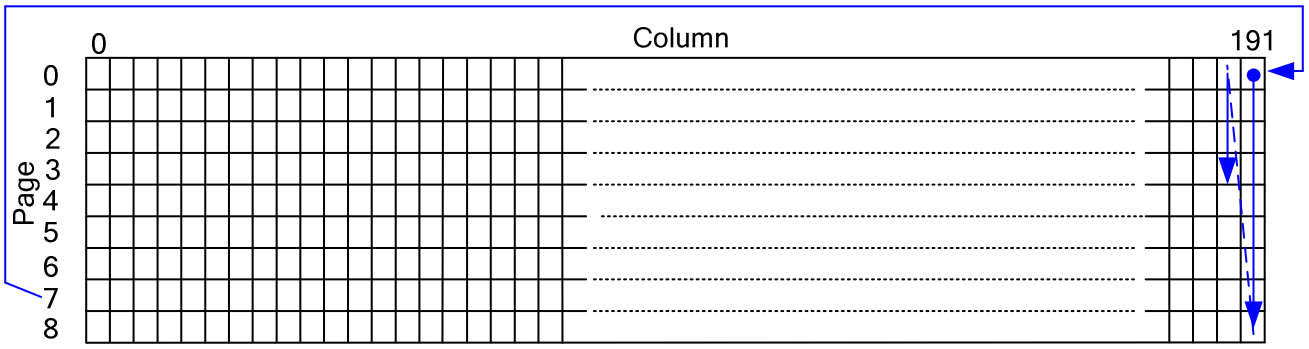


Fig 23. DDRAM Access Mapping (MX=1, AC[2:0]=3, PA[3:0]=0, CA[3:0]=0)

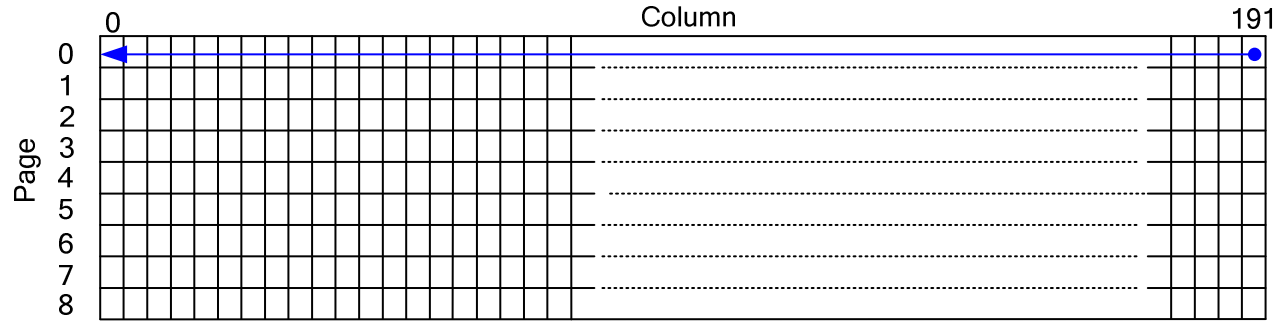


Fig 24. DDRAM Access Mapping (MX=1, AC[2:0]=4, PA[3:0]=0, CA[3:0]=0)

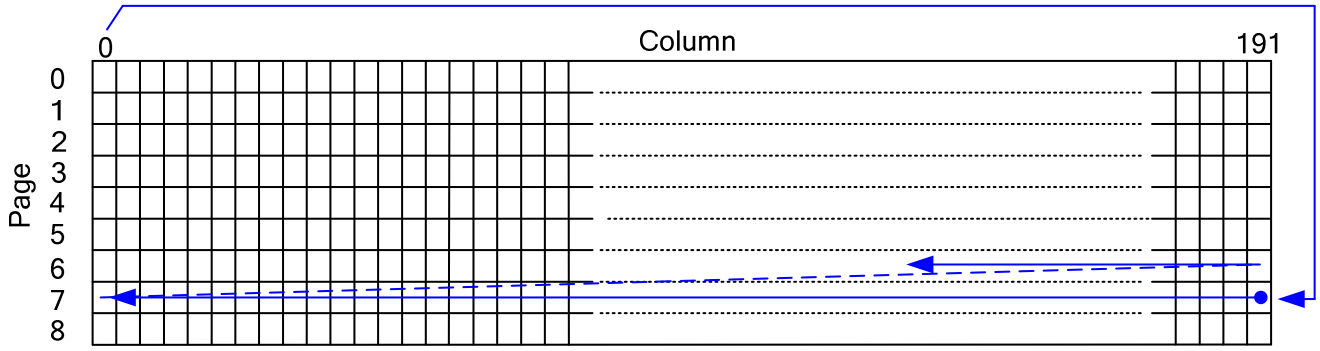


Fig 25. DDRAM Access Mapping (MX=1, AC[2:0]=5, PA[3:0]=7, CA[3:0]=0)

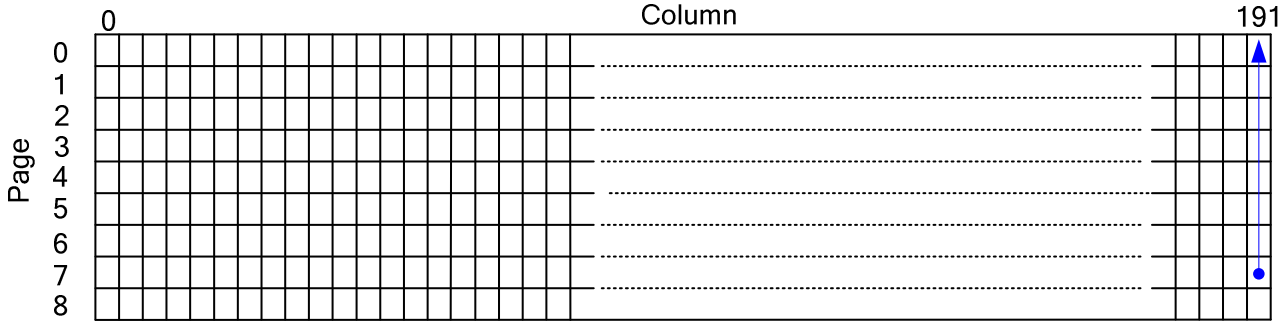


Fig 26. DDRAM Access Mapping (MX=1, AC[2:0]=6, PA[3:0]=7, CA[3:0]=0)

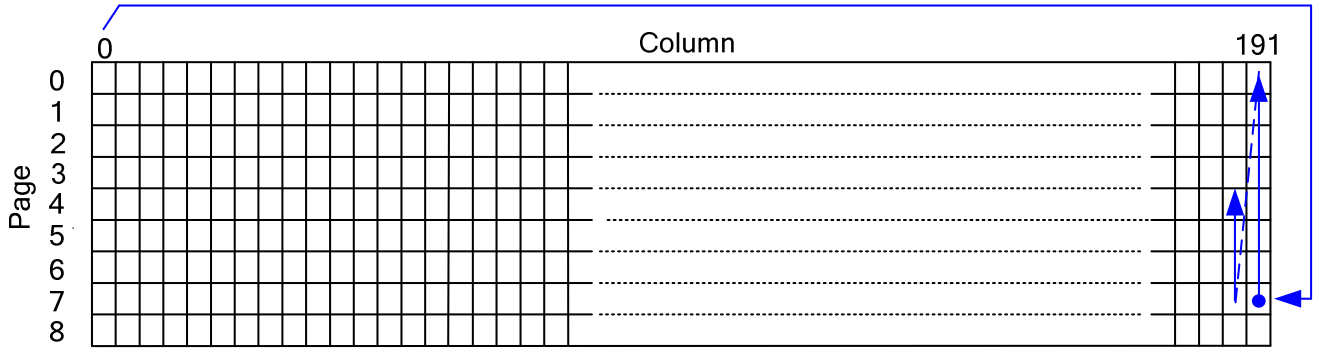


Fig 27. DDRAM Access Mapping (MX=1, AC[2:0]=7, PA[3:0]=7, CA[3:0]=0)

Partial Display on LCD

ST7539 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias ratio are programmable via the instruction. Moreover, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages. If the partial display region is out of the maximum display range, it would be abnormal. When the partial mode is active, the setting rule of “Partial Start Address” and “Partial End Address” are according to below relationship:

CEN[5:0] ≥ DEN[5:0] ≥ DST[5:0] + 9.

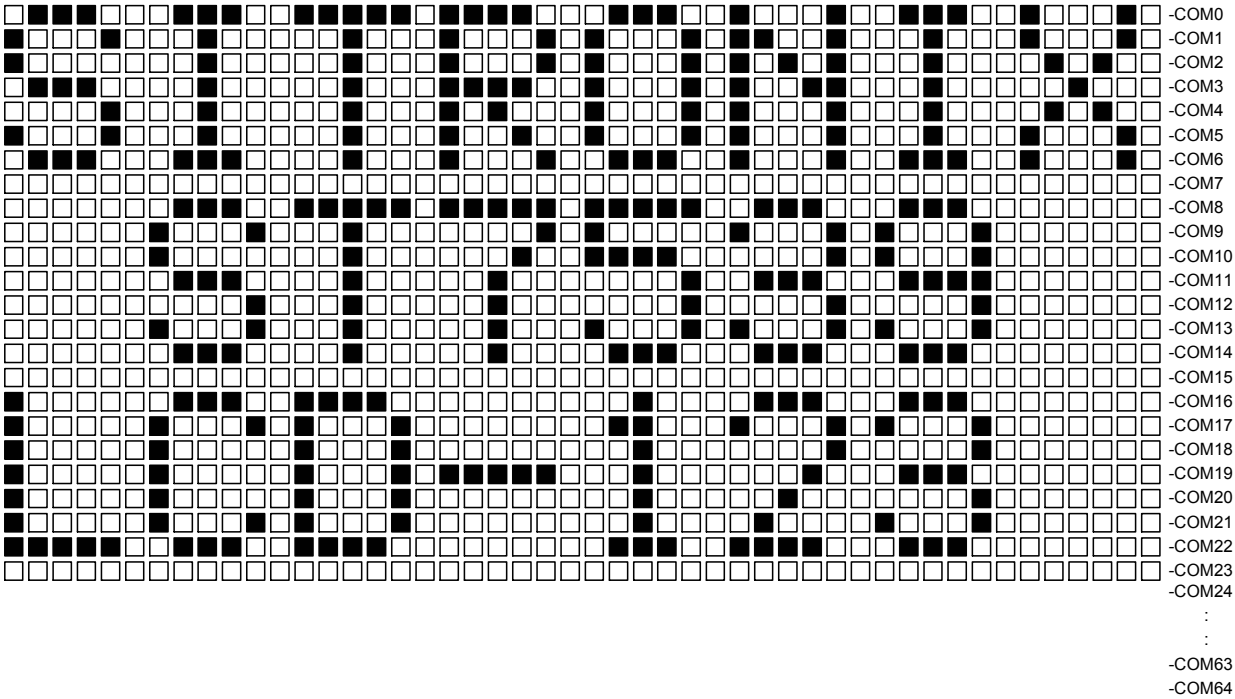


Fig 28. Partial Display (CEN[5:0]=23, SL[5:0]=0, PS=0)

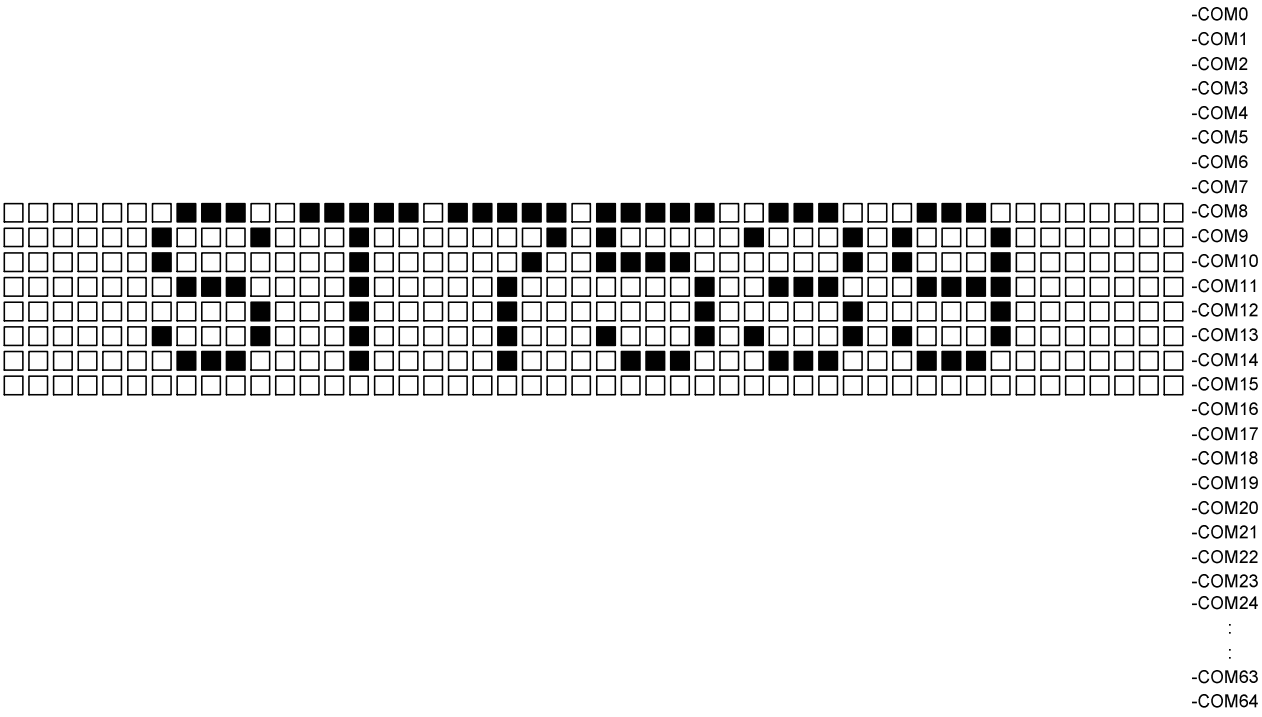


Fig 29. Partial Display (CEN[5:0]=23, SL[5:0]=0, DST[5:0]=8, DEN[5:0]=15, PS=1)

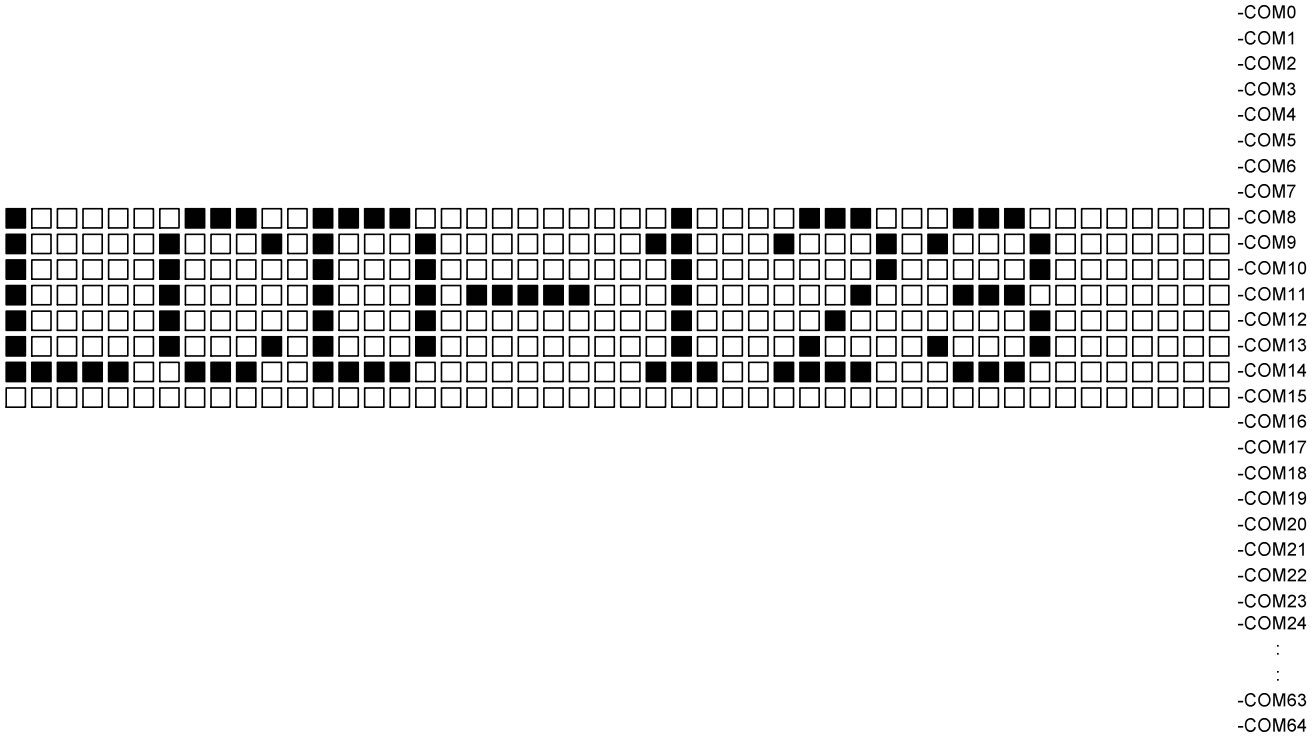


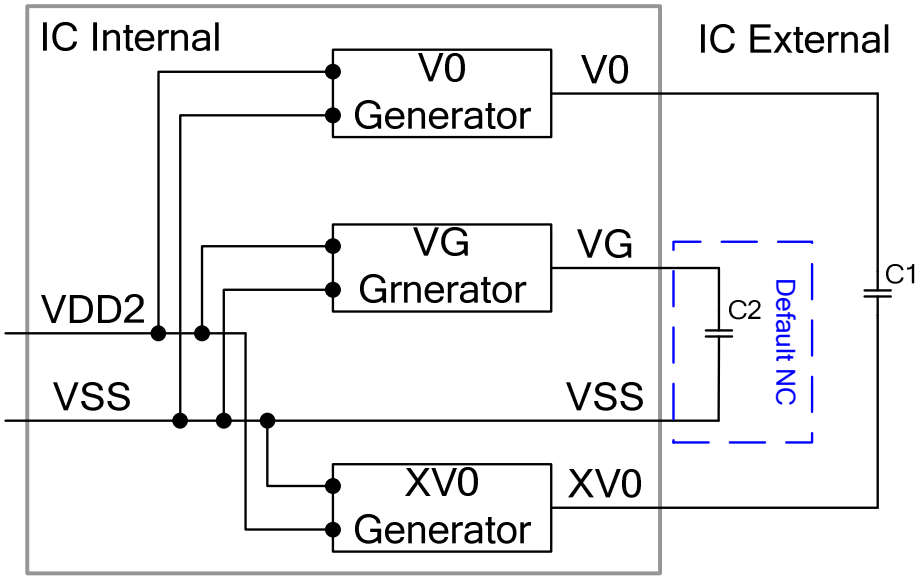
Fig 30. Partial Display (CEN[5:0]=23, SL[5:0]=8, DST[5:0]=8, DEN[5:0]=15, PS=1)

Power Supply Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by Set Display Enable instruction.

External Power Components

The default external power component is only 1 capacitor. It is connection method and capacitance value is shown below. The detailed values are determined by the panel size and loading.



The referential external component values are listed below.

1. C1=0.1uF~2.2uF (Non-Polar/25V, default 1uF)
2. C2=0.1uF~2.2uF (Non-Polar/6.3V, default N.C.)

Components selection notes:

- Higher capacitor values are recommended for ripple reduction.
- In order to avoid the characteristic differences of the LCD panel. The capacitor values should be verified according to the display performance on LCD panel.
- If the panel size is greater than 2” or loading heavy, must be added the capacitor C2.
- If the V0 voltage exceeds 11V, must be added the capacitor C2.
- Those values of capacitor can be determined by customer’s LCD module (panel loading and ITO resistance) and application (VDD, V0, bias...etc).

Voltage Regulator Circuits

The internal Voltage Regulator circuit provides the liquid crystal operating voltage (V0) by adjusting registers (BR[1:0] and EV[7:0]). The Vop calculation formula is shown below:

$$V0 = (C_{V0} + C_{EV} \times EV) \times (1 + (T - 25) \times C_T\%)$$

Where

1. C_{V0} and C_{EV} are two constants, whose value depends on the setting of bias register (BR[1:0]).
2. **EV** is the register setting by EV[7:0].
3. **T** is ambient temperature in ℃
4. C_T is the temperature compensation coefficient as -0.06%/℃.

BR	C_{V0}	C_{EV} (mV)	EV	V0 Range (V)
6	4.80	12.24	0	4.80
			255	7.92
7	5.60	14.28	0	5.60
			255	9.24
8	6.40	16.32	0	6.40
			255	10.56
9	7.20	18.36	0	7.20
			234	11.50

Fig 31 shows V0 voltage measured by adjusting bias register and electronic volume registers for each temperature coefficient at Ta = 25℃.

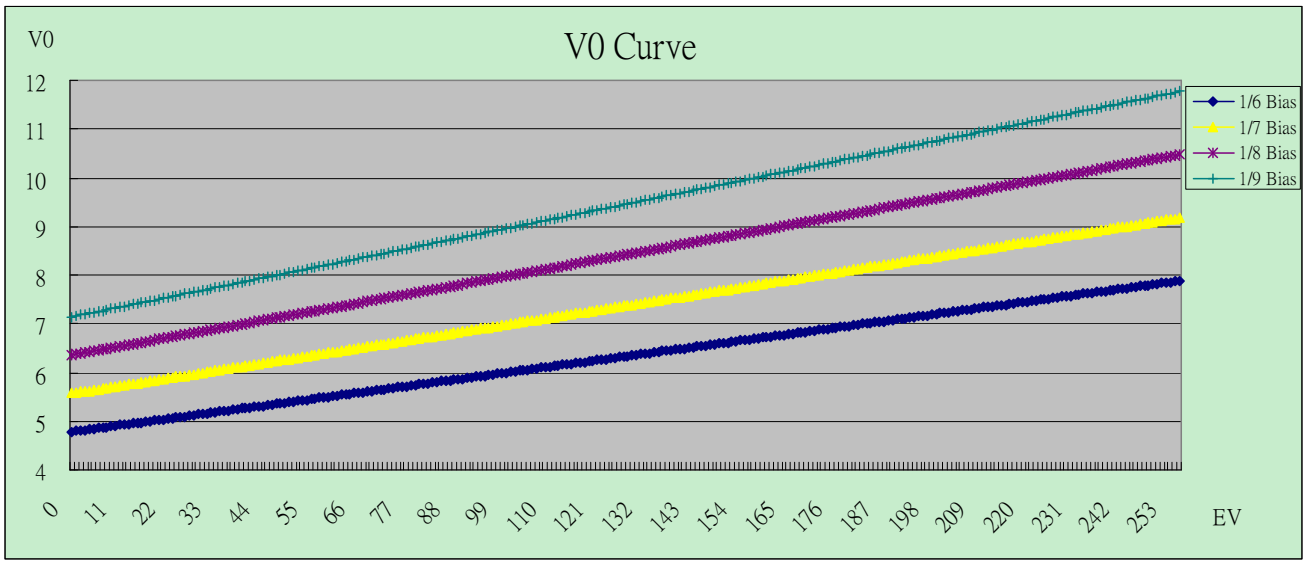


Fig 31. Electronic Volume Level (25℃)

8. RESET CIRCUIT

Setting RST to “L” can initialize internal function. While RST is “L”, no instruction can be accepted. RST pin must connect to the reset pin of MPU and initialization by RST pin is essential before operating. Please note the RST (hardware reset) function is not the same as the SRESET (software reset) function.

Procedure	Hardware Reset	Software Reset
DDRAM Content	No Change	No Change
Column Address Counter	CA[7:0]=0	CA[7:0]=0
Scroll Line	SL[5:0]=0	No Change
Page Address Counter	PA[3:0]=0	PA[3:0]=0
Contrast Control	EV[7:0]=49h	No Change
Partial Screen Enable	PS=0	No Change
Ram Address Control	AC[2:0]=1h	AC [2:0]=1h
Frame Rate	FR[1:0]=1h	No Change
All Pixel ON	AP=0	No Change
Inverse Display	INV=0	No Change
Display Enable	PD=0	No Change
Scan Direction	MX=0, MY=0	No Change
LCD Bias	BR[1:0]=3h	No Change
COM End	CEN[5:0]=3Fh	No Change
Partial Start Address	DST[5:0]=0	No Change
Partial End Address	DEN[5:0]= 3Fh	No Change

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern, such as logo) before turning the Display ON.

9-1. INSTRUCTION TABLE

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to DDRAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM Only for parallel interface and I^2C
Read Status Byte (parallel interface)	0	1	ID0	MX	MY	WA	DE	0	0	0	Read status byte Only for parallel interface
			0	POR	0	0	0	ID3	ID2	ID1	
Read Status Byte (4-SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte Only for 4 line SPI
	0	1	ID0	MX	MY	WA	DE	0	0	0	
			0	POR	0	0	0	ID3	ID2	ID1	
Set Column Address LSB	0	0	0	0	0	0	CA3	CA2	CA1	CA0	Set column address of RAM
Set Column Address MSB	0	0	0	0	0	1	CA7	CA6	CA5	CA4	
Set Scroll Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of DDRAM (vertical scrolling)
Set Page Address	0	0	1	0	1	1	PA3	PA2	PA1	PA0	Set page address of RAM
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Set Vop voltage
			EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
Set Partial Screen Mode	0	0	1	0	0	0	0	1	0	PS	PS=1: Enable partial mode
Set RAM Address Control	0	0	1	0	0	0	1	AC2	AC1	AC0	Set column and page address behavior
Set Frame Rate	0	0	1	0	1	0	0	0	FR1	FR0	Set frame frequency
Set All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all display segments on
Set Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display
Set Display Enable	0	0	1	0	1	0	1	1	1	PD	PD=0: Chip is in power down mode
Scan Direction	0	0	1	1	0	0	0	MY	MX	0	Set COM and SEG scan direction
Software Reset	0	0	1	1	1	0	0	0	1	0	Set software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Bias	0	0	1	1	1	0	1	0	BR1	BR0	Set internal bias circuit
Set COM End	0	0	1	1	1	1	0	0	0	1	2-byte instruction. Set display duty
			--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	
Partial Start Address	0	0	1	1	1	1	0	0	1	0	Set partial start for partial display screen
			--	--	DST5	DST 4	DST 3	DST 2	DST 1	DST 0	
Partial End Address	0	0	1	1	1	1	0	0	1	1	Set partial end for partial display screen
			--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0	
Test Control	0	0	1	1	1	1	1	1	1	1	Set test command table
			--	--	--	--	--	--	H1	H0	

Note: 1. Do not use instructions not listed in these tables (Command Table).

2. "--" = Disabled bit. It can be either logic 0 or 1.

9-2. INSTRUCTION DESCRIPTION

Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read Status Byte

Indicate the status of ST7539.

1. Parallel interface (8080/ 6800)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	ID0	MX	MY	WA	DE	0	0	0
0	1	0	POR	0	0	0	ID3	ID2	ID1

2. Serial interface (4-Line SPI)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	1	0
0	1	ID0	MX	MY	WA	DE	0	0	0
0	1	0	POR	0	0	0	ID3	ID2	ID1

Flag	Description
MX	SEG bi-direction selection MY=0:normal direction (SEG0→SEG191); MY=1:reverse direction (SEG191→SEG0)
MY	COM bi-direction selection MY=0:normal direction (COM0→COM63); MY=1:reverse direction (COM63→COM0)
WA	Indicate the AC0 setting.
DE	Display Enable status. DE=0:Display OFF; DE=1:Display ON
POR	Power-ON reset selection
ID0	Indicate the ID0 setting.
ID1	Indicate the ID1 setting.
ID2	Indicate the ID2 setting.
ID3	Indicate the ID3 setting.

Set Column Address

These instructions set the specified Column Address of DDRAM into the internal CA address (Column Address). The CA address register points to the address of DDRAM for accessing display data. The CA address register is automatically increased by 1 when the microprocessor accesses the display data in DDRAM.

1. Set Column Address (LSB)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CA3	CA2	CA1	CA0

2. Set Column Address (MSB)

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	CA7	CA6	CA5	CA4

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	1	1	1	1	0	0	188
1	0	1	1	1	1	0	1	189
1	0	1	1	1	1	1	0	190
1	0	1	1	1	1	1	1	191

Set Scroll Line

The 2-byte instruction sets the line address of DDRAM to determine the first display line. The display data of the selected line will be displayed at the top of row (COM0) on the LCD panel.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0

SL5	SL4	SL3	SL2	SL1	SL0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
:	:	:	:	:	:	:
1	1	1	1	0	0	60
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

This instruction sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the CA address, the PA address defines the address of the display RAM to write display data. Changing the page address doesn't affect the display status.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	PA3	PA2	PA1	PA0

PA3	PA2	PA1	PA0	Page Address	Allowed CA-Range
0	0	0	0	Page0 (display RAM)	0 to 191
0	0	0	1	Page1 (display RAM)	0 to 191
0	0	1	0	Page2 (display RAM)	0 to 191
0	0	1	1	Page3 (display RAM)	0 to 191
0	1	0	0	Page4 (display RAM)	0 to 191
0	1	0	1	Page5 (display RAM)	0 to 191
0	1	1	0	Page6 (display RAM)	0 to 191
0	1	1	1	Page7 (display RAM)	0 to 191
1	0	0	0	Page8 (icon RAM)	0 to 191

Set Contrast

This instruction sets operating voltage V0 (Vop).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0

EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV Value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Set Partial Screen Mode

This instruction controls partial display enable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	1	0	PS

Flag	Description
PS	Full display mode or partial screen mode selection. PS=0 : Full display mode. PS=1 : Partial screen mode.

Set RAM Address Control

This instruction controls DDRAM display scan behaviors.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	AC2	AC1	AC0

Flag	Description		
AC0	Automatic column or page wrap around.		
	AC1 = 0	AC0 = 0	Column address will stop increasing by 1 while reaching each boundary.
		AC0 = 1	Column address will go on next page after reaching each boundary.
	AC1 = 1	AC0 = 0	Page address will stop increasing by 1 while reaching each boundary.
		AC0= 1	Page address will go on next column after reaching each boundary.
AC1	Address auto increment order. AC1=0 : Column address increase by 1 first until column address reach each boundary, then page address will increase or decrease by 1(depend on AC2). AC1=1 : Page address increase by 1 first until page address reach each boundary, then column address will increase by 1.		
AC2	Page address auto increment direction. AC2=0 : Page address increase by 1 (PA +1, downward). AC2=1 : Page address decrease by 1 (PA -1, upward).		

Set Frame Rate

This command is used to set the frame frequency.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	FR1	FR0

FR1	FR0	Frame Frequency
0	0	76 fps
0	1	95 fps
1	0	132 fps
1	1	168 fps

Note : The frame frequency is shown at temperature 25°C.

Set All Pixel ON

This instruction sets all segments output ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	Force all display segments on. AP=0 : Normal display mode. AP=1 : All segments output ON.

Set Inverse Display

This instruction sets the display inverse mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	Inverse video mode. INV=0 : Normal display mode. INV=1 : Inverse display mode.

Set Display Enable

This instruction sets display off and enters power down mode. All LCD outputs at VSS (display off) bias generator and power generator off, oscillator off (external clock possible), RAM contents not cleared and RAM data can be written.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	PD

Flag	Description
PD	Display off and power down mode. PD=0 : Display off and power down mode. PD=1 : Display on and power on mode.

Scan Direction

This instruction sets COM and SEG bi-direction selection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	MY	MX	0

Flag	Description
MY	COM bi-direction selection. MY=0 : Normal direction (COM0 → COM63) MY=1 : Reverse direction (COM63 → COM0)
MX	SEG bi-direction selection. MX=0 : Normal direction (SEG0 → SEG191) MX=1 : Reverse direction (SEG191 → SEG0)

Software Reset

This is software reset. It resets internal registers. This instruction cannot initialize the LCD power supply, which is initialized by a hardware reset.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

NOP

No operation.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

Set Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	0	BR1	BR0

BR1	BR0	Bias
0	0	1/6
0	1	1/7
1	0	1/8
1	1	1/9

Set COM End

This 2-byte instruction sets the display duty within the range of 1/(9+1) to 1/(64+1) to realize partial display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	0	1
0	0	--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0

CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	Selected Partial Duty Ratio
0	0	0	0	0	0	Reserved
:	:	:	:	:	:	
:	:	:	:	:	:	
0	0	1	0	0	0	1/(9+1)
0	0	1	0	0	1	1/(10+1)
:	:	:	:	:	:	:
1	1	1	1	1	0	1/(63+1)
1	1	1	1	1	1	1/(64+1)

Set Partial Start Address

This instruction can select partial screen display start line address.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	1	0
0	0	--	--	DST5	DST4	DST3	DST2	DST1	DST0

DST5	DST4	DST3	DST2	DST1	DST0	Selected Partial Start Line Address
0	0	0	0	0	0	1
0	0	0	0	0	1	2
:	:	:	:	:	:	:
1	1	1	1	1	0	63
1	1	1	1	1	1	64

Set Partial End Address

This instruction can select partial screen display end line address.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	0	0	1	1
0	0	--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0

DEN5	DEN 4	DEN 3	DEN 2	DEN 1	DEN 0	Selected Partial End Line Address
0	0	0	0	0	0	1
0	0	0	0	0	1	2
:	:	:	:	:	:	:
1	1	1	1	1	0	63
1	1	1	1	1	1	64

Set Test Control

This instruction can select test command table.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	1	1
0	0	--	--	--	--	--	--	H1	H0

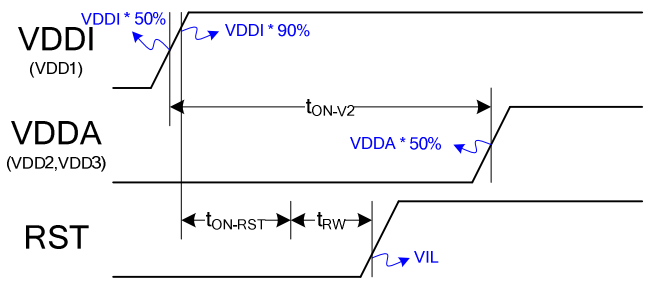
10. COMMAND SEQUENCE

This section introduces some reference operation flows.

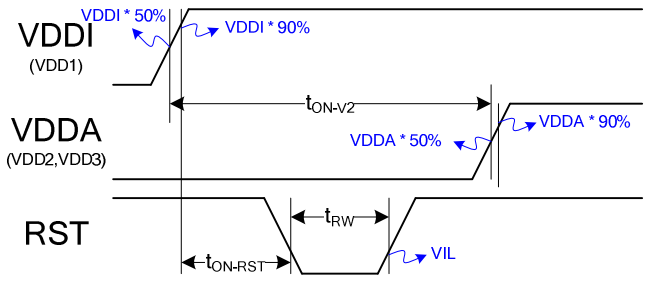
Power ON Flow and Sequence:

Power Sequence

Case 1: RSTB=L while Power ON



Case 2: RSTB=H while Power ON



Note:

The detailed description can be found in the respective sections listed below.

1. Be sure the power is stable and the internal reset is finished (refer to RST timing specification).
2. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● Applying VDDI and VDDA in any order will not damage IC.
RST input time	t_{ON-RST}	No Limitation	● If RST is Low, High or unstable during power ON, a successful hardware reset by RST is required after VDDI is stable. ● RST=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RST. ● To prevent abnormal display, the recommended timing is: $0 \le t_{ON-RST} \le 30$ ms.

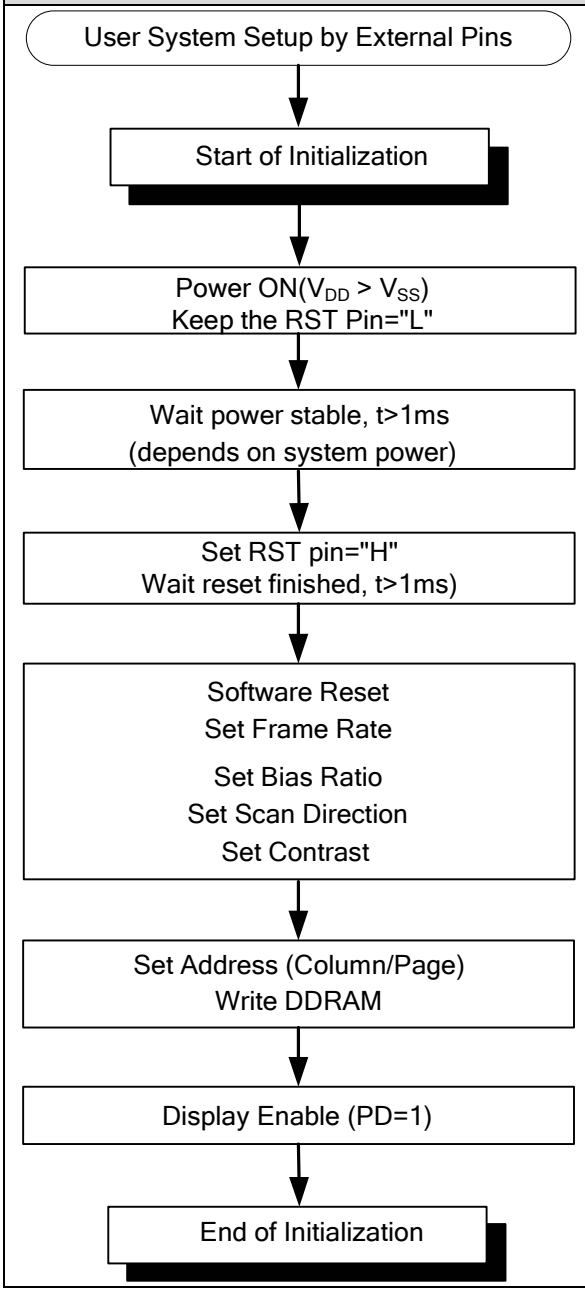
Note :

IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.

Referential Operation Flow : Initializing with internal power system

The detailed instruction functionality is described in Section “INSTRUCTION DESCRIPTION”.

Referential Initial Flow



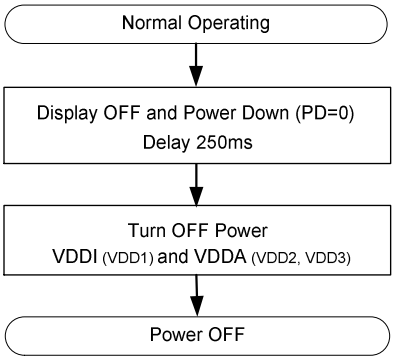

```
Void ST7539_Initial (void)
{
    Reset();
    Delay(100);                 //Delay 100ms

    Write(COMMANF, 0xE2);       //Software Reset
    Write(COMMANF, 0xA0);       //Set Frame Rate 76 fps
    Write(COMMANF, 0xEB);       //Set Bias 1/9
    Write(COMMANF, 0xC0);       //MX = 0, MY = 0
    Write(COMMANF, 0x81);       //Set EV
    Write(COMMANF, 0x99);       //EV = 153

    Write(COMMANF, 0xB0);       //Set Page Address = 0
    Write(COMMANF, 0x10);       //Set Column Address = 0
    Write(COMMANF, 0x00);       //Set Column Address = 0
    Write data into DDRAM;      //Boot Logo

    Write(COMMANF, 0xAF);       //Display On
    Delay(100);                 //Delay 100ms
}
```

Power OFF Flow and Sequence

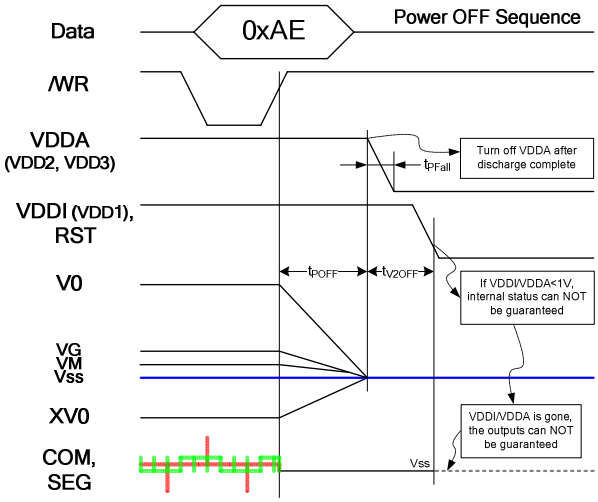
By setting PD="0", the power down procedure starts. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts. The power save mode can be triggered by the following two methods.

Referential Power OFF Flow	Operation Sequence

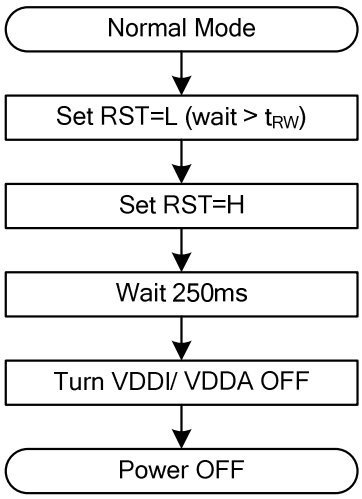
CASE 1: Use Display Enable Instruction



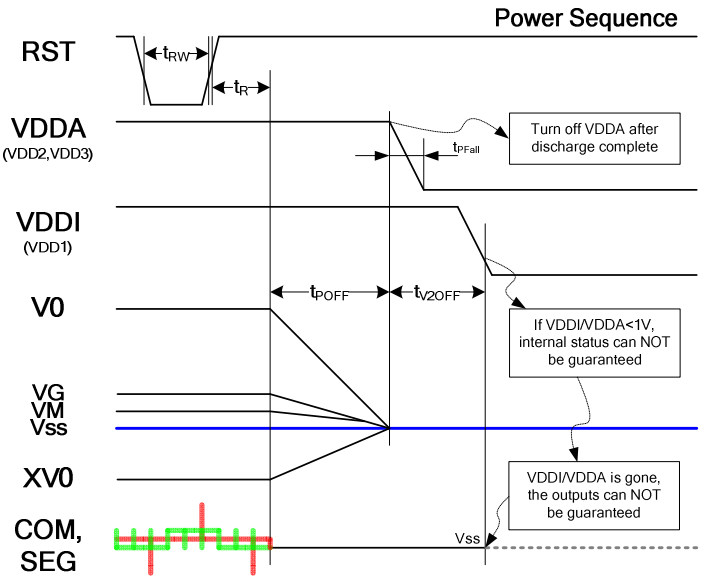
After the built-in power circuits are turned OFF and completely discharged, the power (VDDI and VDDA) can be removed.



CASE 2: Use Hardware Reset Function



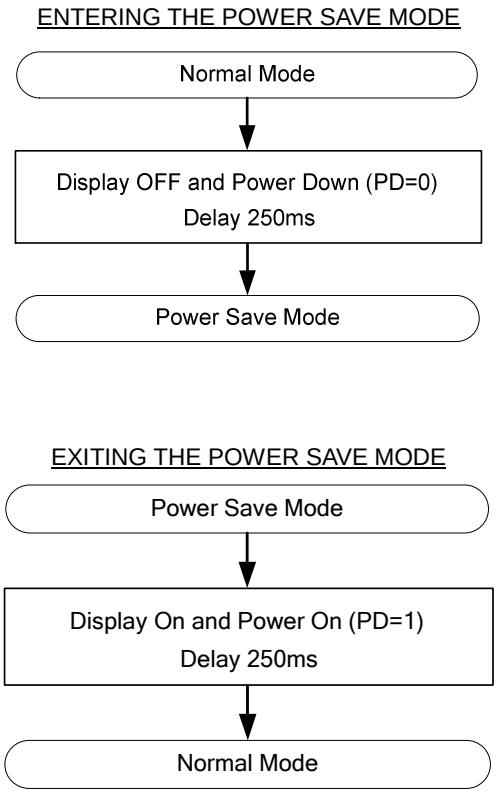
After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.



Note:

1. t_{POFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDDI and VDDA OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.8" with C1=1uF.
7. When turning VDDA OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec

Power-Save Flow



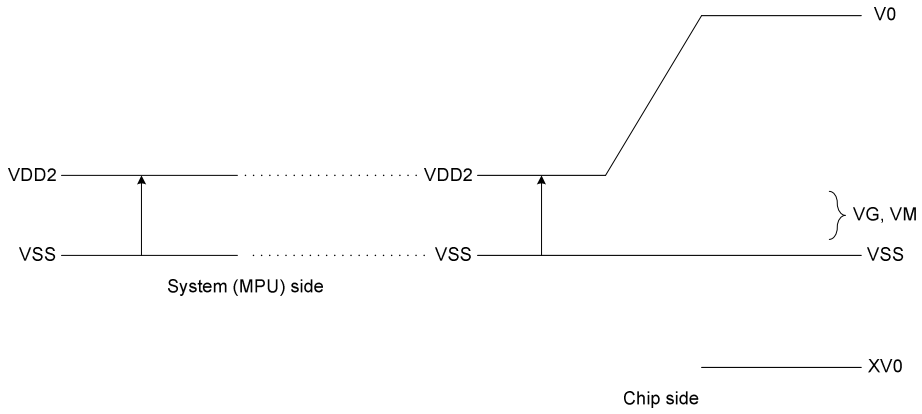
11. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

12. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1~ 4.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1)	-0.3 ~ 4.0	V
Analog Power Supply Voltage	VDDA (VDD2 & VDD3)	-0.3 ~ 4.0	V
LCD Power Supply Voltage	Vop	-0.3 ~ 13.0	V
LCD Power Supply Voltage	VG	-0.3 ~ 4.0	V
LCD Power Supply Voltage	VM	-0.3 ~ 4.0	V
Input Voltage	VIN	-0.3 ~ VDD1+0.3 *4	V
Operating Temperature	TOPR	-30 to +85	°C
Storage Temperature	TSTR	-55 to +125	°C



Notes

1. Insure the voltage levels of V0, VDDA, VG, VM, VSS and XV0 always match the correct relation while operating:
   V0 ≥ VDDA > VG > VM > VSS ≥ XV0
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Stresses exceed the Limiting Values listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/Timing Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
4. Interface input voltage range can not exceed the maximum limitation of digital power supply voltage.
   VIN ≤ 3.6V

13. DC CHARACTERISTICS

VSS=VSS1=VSS2=VSS3=0V; Bare chip, Temp. = -30°C to +85°C; unless otherwise specified.

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		1.65	—	3.6	V	VDD1
Operating Voltage (2)	VDD2 VDD3		2.4	—	3.6	V	VDD2 VDD3
LCD Power Supply Voltage	Vop		4.8	—	11.5	V	V0-XV0
Input High-Level Voltage	V_{IHC}		0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-Level Voltage	V_{ILC}		VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-Level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V	0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-Level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V	VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		-1.0	—	1.0	μA	MPU Interface
LCD Driver ON Resistance	R_{ON}	Ta=25°C, Vop=10V, ΔV=1.0V	—	0.7	—	KΩ	COMx
		Bias=1/9, VG=2.2V, ΔV=0.22V	—	0.7	—	KΩ	SEGx
Frame Frequency	fFR	1/65 Duty, FR[1:0]=(0,0), Ta = 25℃	68	76	82	Hz	

Note:

- The LCD Output Voltage (Vop) range of the measurement environment is as follows:
  V0 to XV0 : 1uF
- The heavy loading pattern may cause variation of Vop output voltage. It means the Vop voltage maybe exceed the range of LCD operation voltage with heavy loading.

Bare chip current consumption with internal power system:

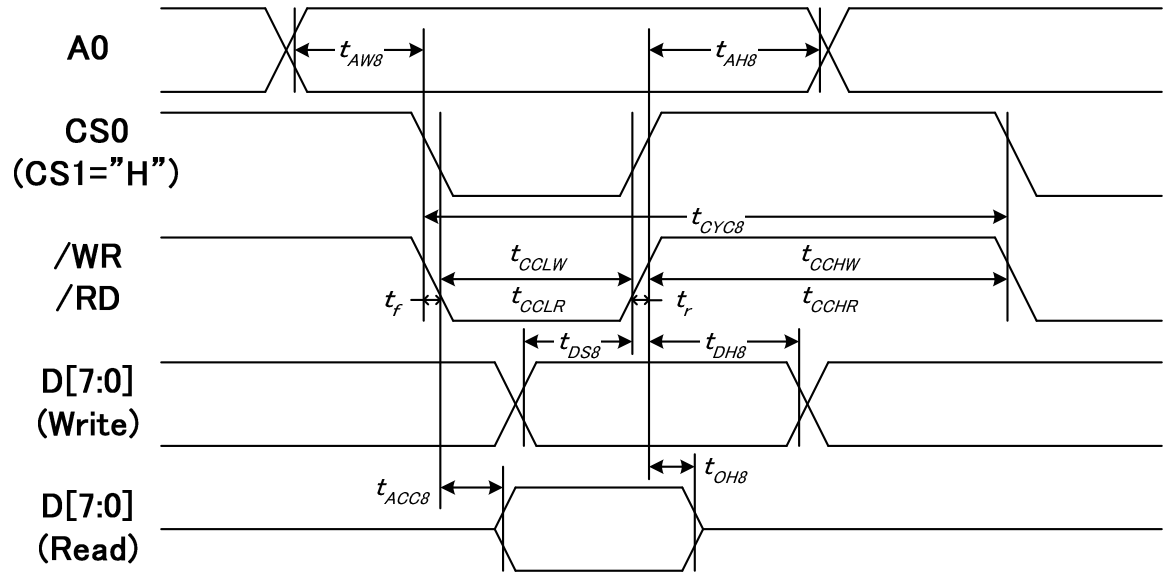
Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=VDD3=3V, Vop=10V, Bias=1/9, Frame Rate=76Hz, Ta=25°C	—	150	—	μA	
Power Down	ISS	VDD1=VDD2=VDD3=3V, Ta=25°C	—	2	5	μA	

Note:

The Current Consumption is DC characteristics.

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		5	-	ns
Address hold time		tAH8		10	-	
System write cycle time	/WR	tCYC8		100	-	
Write L pulse width		tCCLW		35	-	
Write H pulse width		tCCHW		35	-	
Read L pulse width	/RD	tCCLR		50	-	
Read H pulse width		tCCHR		50	-	
Data setup time (Write)	D[7:0]	tDS8		30	-	
Write Data hold time (Write)		tDH8		5	-	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		5	-	ns
Address hold time		tAH8		10	-	
System write cycle time	/WR	tCYC8		110	-	
Write L pulse width		tCCLW		40	-	
Write H pulse width		tCCHW		40	-	
Read L pulse width	/RD	tCCLR		60	-	
Read H pulse width		tCCHR		60	-	
Data setup time (Write)	D[7:0]	tDS8		35	-	
Write Data hold time (Write)		tDH8		5	-	

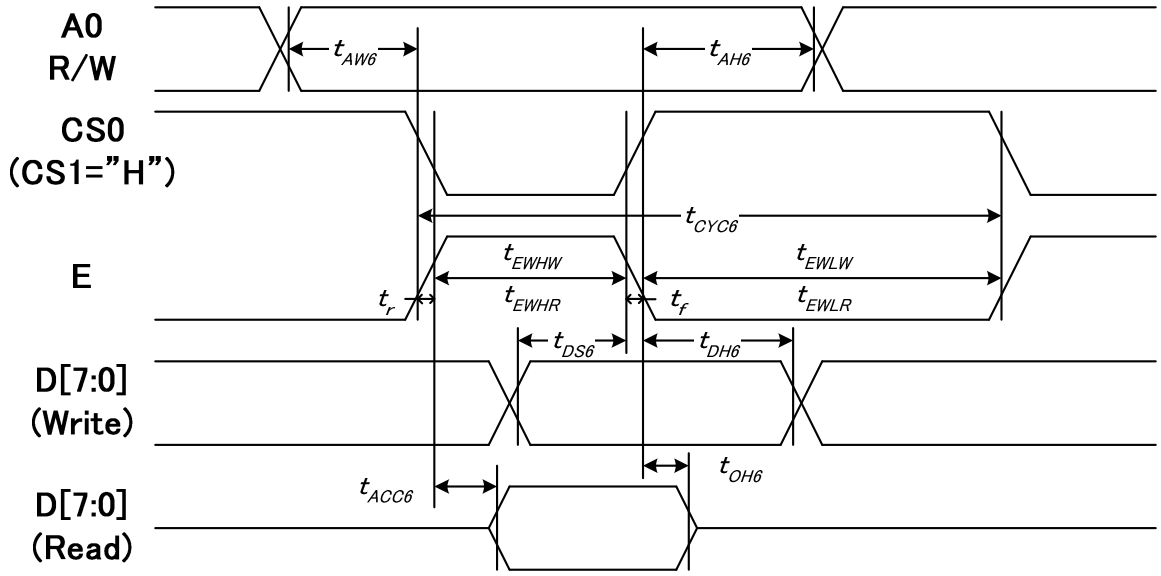
(VDD1 = 1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		5	-	ns
Address hold time		tAH8		10	-	
System write cycle time	/WR	tCYC8		190	-	
Write L pulse width		tCCLW		80	-	
Write H pulse width		tCCHW		80	-	
Read L pulse width	/RD	tCCLR		100	-	
Read H pulse width		tCCHR		100	-	
Data setup time (Write)	D[7:0]	tDS8		60	-	
Write Data hold time (Write)		tDH8		5	-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 - tCCLW - tCCHW) for (tr + tf) ≤ (tCYC8 - tCCLR - tCCHR) are specified.
3. tCCLW (tCCLR) is specified as the overlap between CS0 being “L” and /WR (/RD) being “L”.

System Bus Read/Write Characteristics (For the 6800 Series MPU)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Control setup time	A0	tAW6		5	-	ns
Control hold time	R/W	tAH6		10	-	
System cycle time	E	tCYC6		100	-	
Enable H pulse width (WRITE)		tEWHW		30	-	
Enable L pulse width (WRITE)		tEWLW		50	-	
Enable H pulse width (READ)		tEWHR		50	-	
Enable L pulse width (READ)		tEWLR		50	-	
Write data setup time	D[7:0]	tDS6		30	-	
Write data hold time		tDH6		5	-	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Control setup time	A0 R/W	tAW6		5	-	ns
Control hold time		tAH6		10	-	
System cycle time	E	tCYC6		110	-	
Enable H pulse width (WRITE)		tEWHW		40	-	
Enable L pulse width (WRITE)		tEWLW		50	-	
Enable H pulse width (READ)		tEWHR		60	-	
Enable L pulse width (READ)		tEWLR		60	-	
Write data setup time	D[7:0]	tDS6		35	-	
Write data hold time		tDH6		5	-	

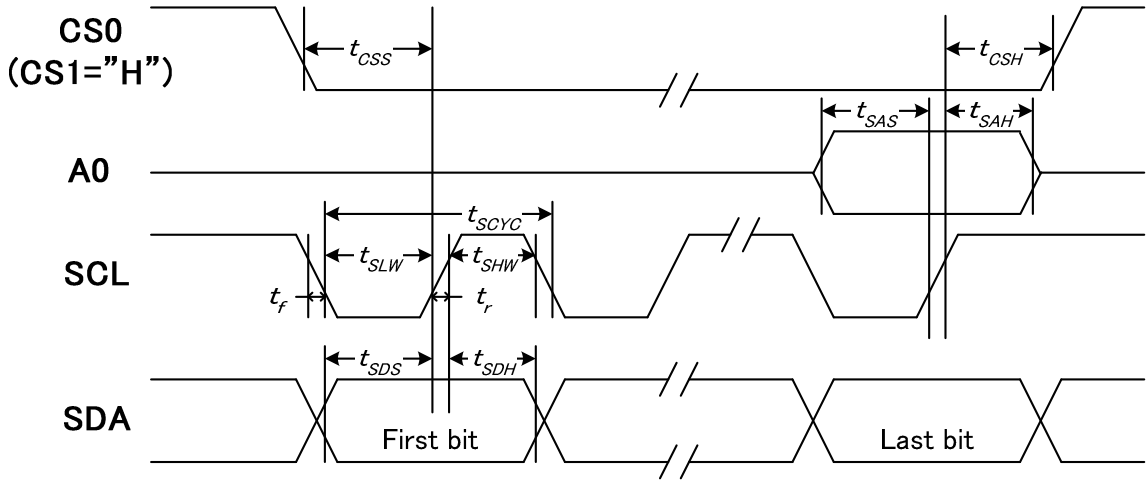
(VDD1 = 1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Control setup time	A0 R/W	tAW6		5	-	ns
Control hold time		tAH6		10	-	
System cycle time	E	tCYC6		190	-	
Enable H pulse width (WRITE)		tEWHW		80	-	
Enable L pulse width (WRITE)		tEWLW		100	-	
Enable H pulse width (READ)		tEWHR		100	-	
Enable L pulse width (READ)		tEWLR		100	-	
Write data setup time	D[7:0]	tDS6		60	-	
Write data hold time		tDH6		5	-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤ (tCYC6 - tEWLR - tEWHR) are specified.
3. tEWLW and tEWLR are specified as the overlap between CS0 being “L” and E being “H”.

SERIAL INTERFACE (4-Line Interface)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		60	-	ns
SCL "H" pulse width		tSHW		15	-	
SCL "L" pulse width		tSLW		15	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		10	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		15	-	
CS0 hold time		tCSH		10	-	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		70	-	ns
SCL “H” pulse width		tSHW		20	-	
SCL “L” pulse width		tSLW		20	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		15	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		15	-	
CS0 hold time		tCSH		10	-	

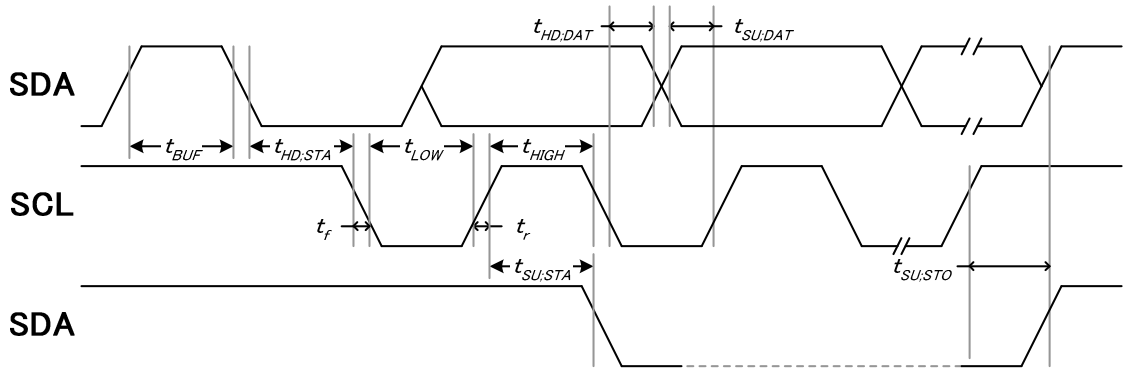
(VDD1 = 1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		110	-	ns
SCL “H” pulse width		tSHW		40	-	
SCL “L” pulse width		tSLW		40	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		20	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		20	-	
CS0 hold time		tCSH		10	-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the standard.
2. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

SERIAL INTERFACE (I^2C Interface)

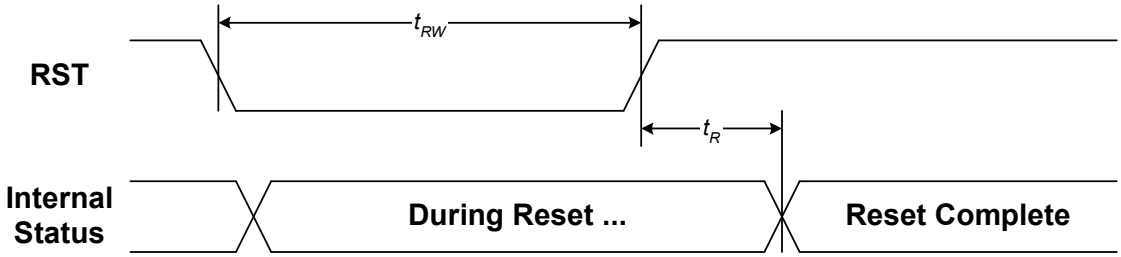


(VDD1 = 1.8V ~ 3.3V, Ta=25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock frequency	SCL	fSCL		-	400	KHz
SCL clock LOW period		tLOW		1.3	-	us
SCL clock HIGH period		tHIGH		0.6	-	
BUS free time between a STOP and START		tBUF		1.3	-	
Data setup time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Signal rise time	SDA SCL	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns

Note : All timing is specified using 20% and 80% of VDD1 as the standard.

RESET TIMING



(VDD1 = 1.8V ~ 3.3V , Ta =25°C)

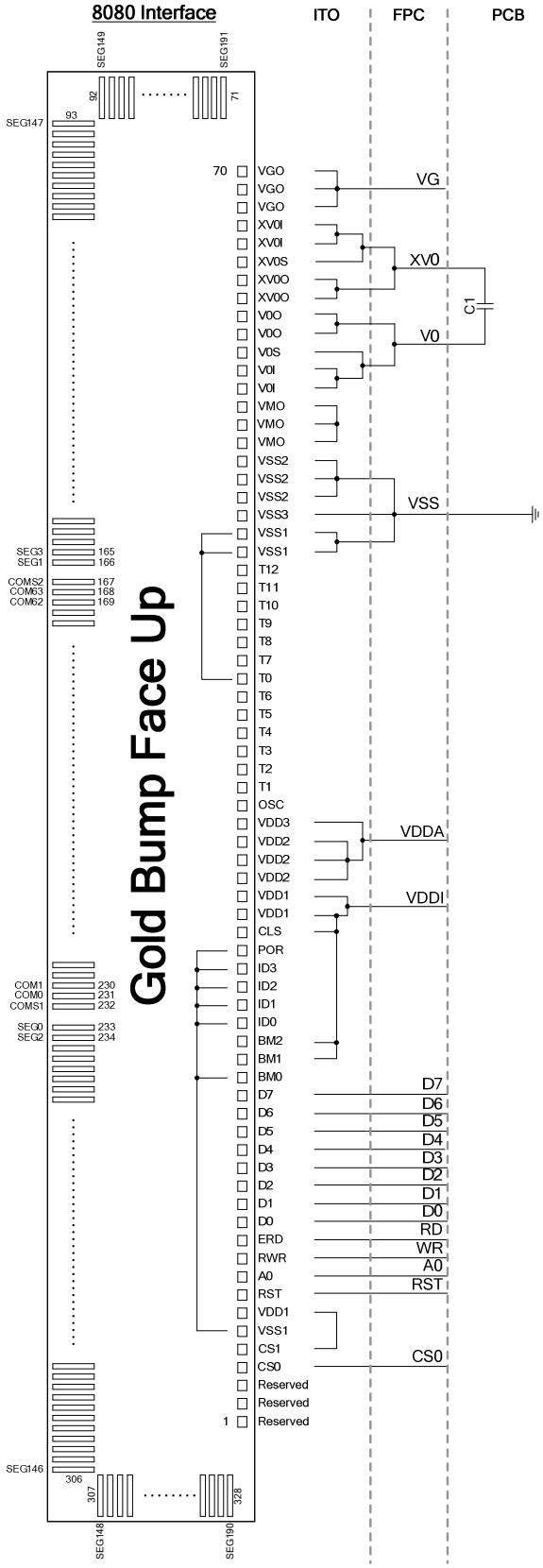
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	1	ms
Reset “L” pulse width	tRW		1	-	

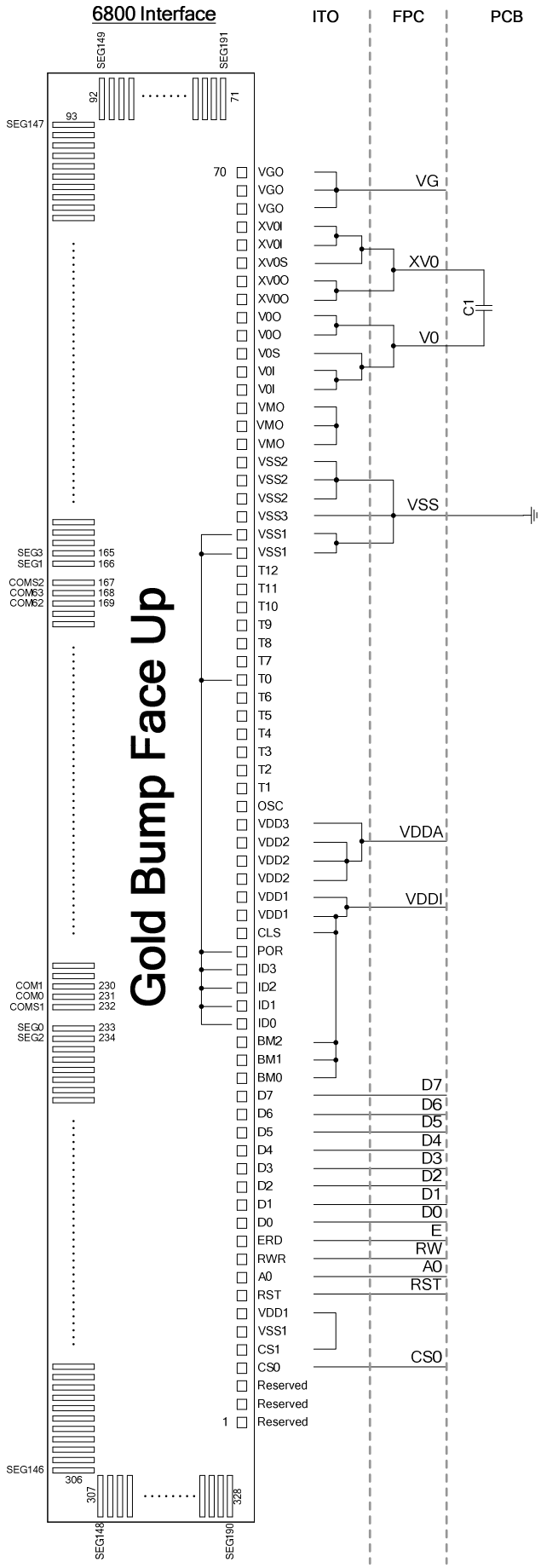
APPLICATION NOTE

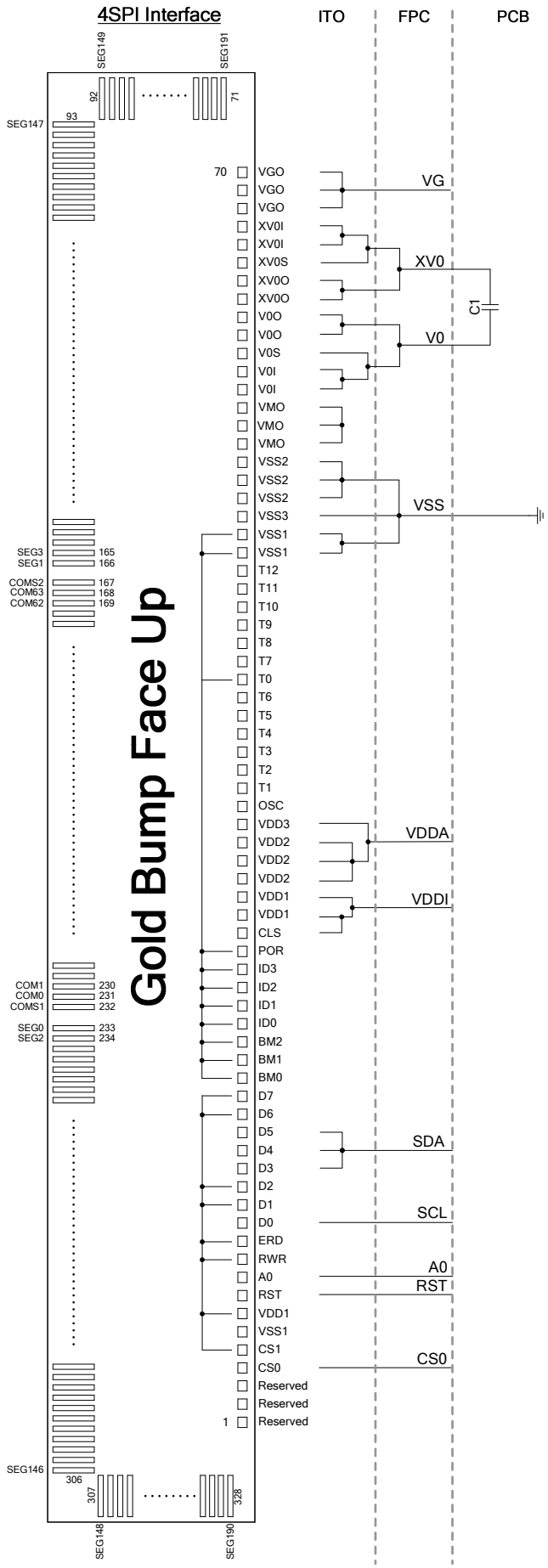
Application Circuits

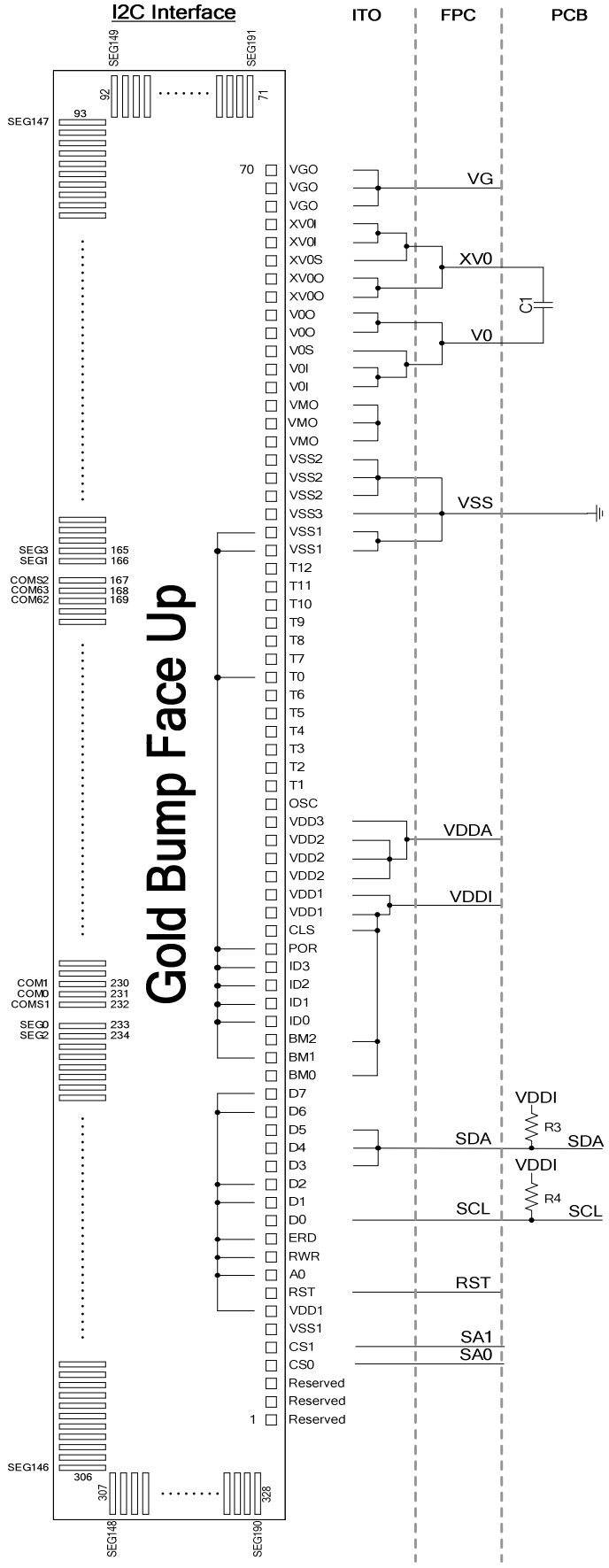
1. The application circuits are for reference only and actual settings are dependent on LCD module characteristics.

2. The detailed external power instructions please refer to Chapter 7 of Power Supply Circuit.




6800 Interface
ITO
FPC
PCB
Gold Bump Face Up
SEG149
SEG191
SEG147
SEG146
SEG148
SEG190
SEG3
SEG1
COMS2
COM63
COM62
COM1
COM0
COMS1
SEG0
SEG2
VGO
XV0I
XV0S
XV0O
V0O
V0S
V0I
VMO
VSS2
VSS3
VSS1
T12
T11
T10
T9
T8
T7
T0
T6
T5
T4
T3
T2
T1
OSC
VDD3
VDD2
VDD1
CLS
POR
ID3
ID2
ID1
ID0
BM2
BM1
BM0
D7
D6
D5
D4
D3
D2
D1
D0
ERD
RWR
A0
RST
CS1
CS0
Reserved
VG
XV0
C1
V0
VSS
VDDA
VDDI
E
RW
A0
RST
CS0


4SPI Interface
ITO
FPC
PCB
Gold Bump Face Up
SEG149
SEG191
SEG147
SEG146
SEG148
SEG190
VG
XV0
V0
C1
VSS
VDDA
VDDI
SDA
SCL
A0
RST
CS0


I2C Interface
ITO
FPC
PCB
Gold Bump Face Up
SEG149
SEG191
SEG147
SEG146
SEG148
SEG190
VG
XV0
V0
C1
VSS
VDDA
VDDI
SDA
SCL
RST
SA1
SA0
R3
R4
VDDI
SDA
VDDI
SCL
VGO
XV0I
XV0S
XV0O
V0O
V0S
V0I
VMO
VSS2
VSS3
VSS1
T12
T11
T10
T9
T8
T7
T0
T6
T5
T4
T3
T2
T1
OSC
VDD3
VDD2
VDD1
CLS
POR
ID3
ID2
ID1
ID0
BM2
BM1
BM0
D7
D6
D5
D4
D3
D2
D1
D0
ERD
RWR
A0
RST
CS1
CS0
Reserved

REVERSION HISTORY

Version	Date	Description
1.0	2012/10/30	Official Release.
1.1	2013/04/25	1. Modify Chip Size and Tolerance. 2. Modify Typing Error (Bump Pitch). 3. Modify Operating Voltage (2) form 2.5V to 2.4V.
1.1a	2013/04/29	Modify Bare Chip Current Consumption.