

CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Basic Concepts and Architectures

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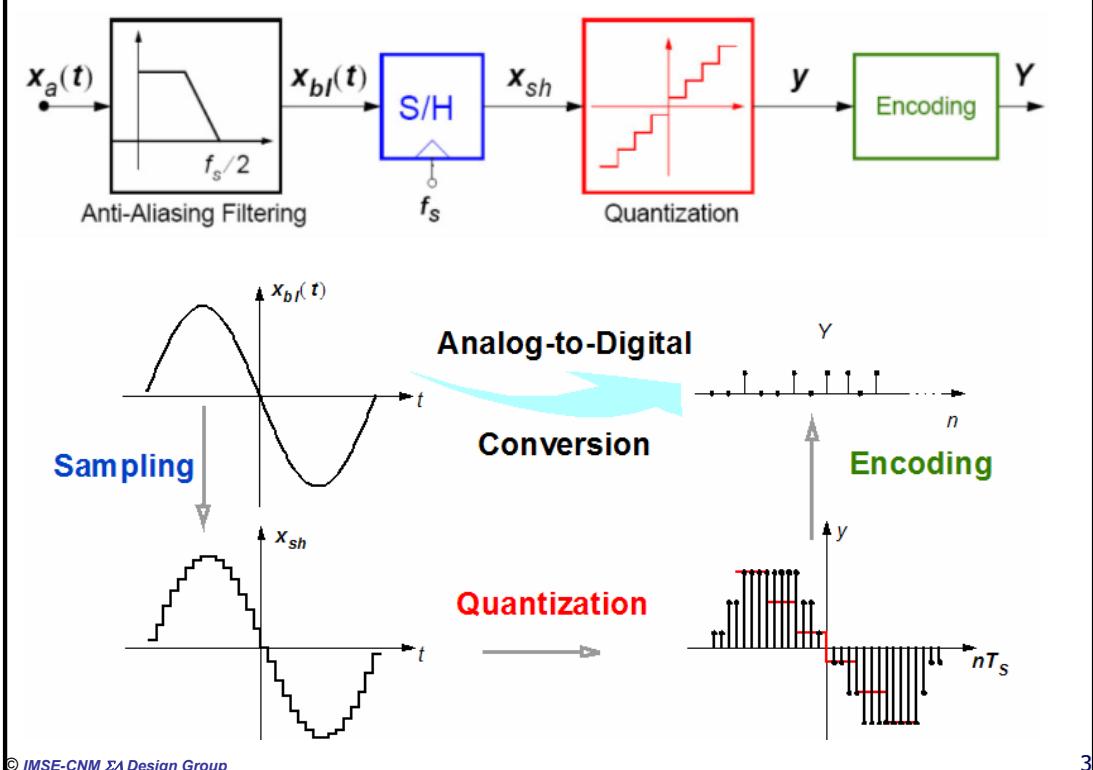
KTH, Stockholm, April 23-27

OUTLINE



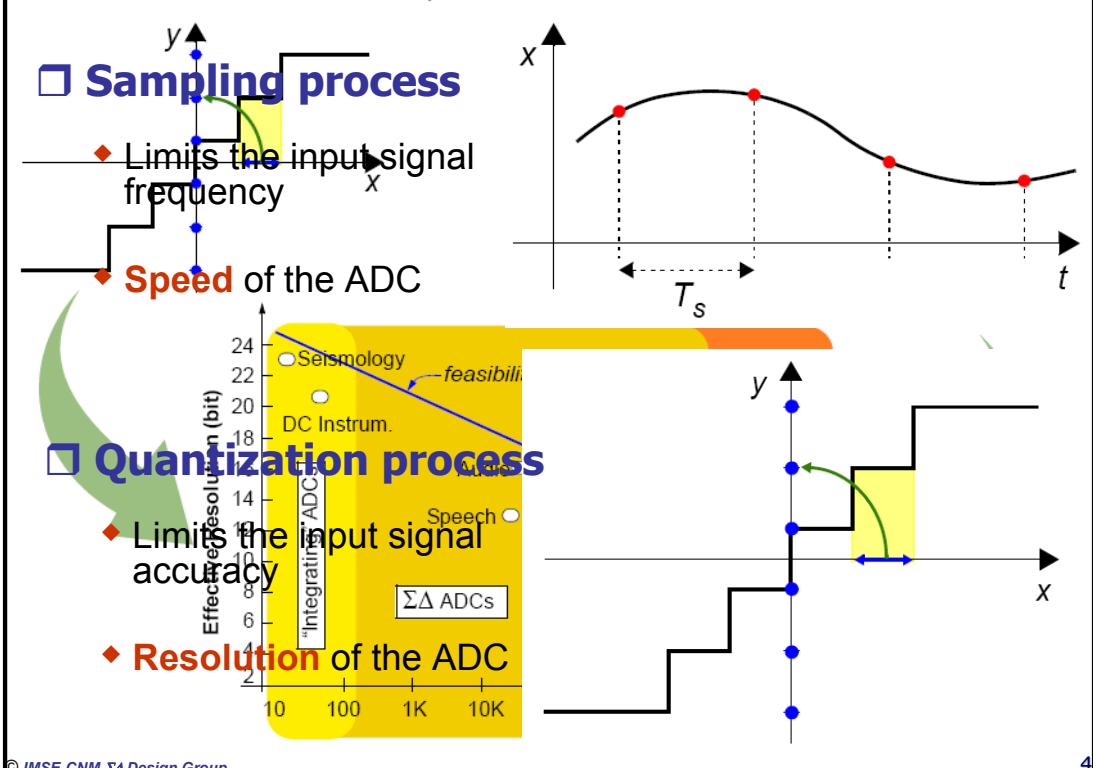
- 1. Introduction**
- 2. Fundamentals of $\Sigma\Delta$ ADCs**
 - Oversampling
 - Quantization noise shaping
 - Basic architecture
 - Classification of $\Sigma\Delta$ ADCs
- 3. Discrete-Time $\Sigma\Delta$ Modulators**
 - Single-bit single-quantizer architectures
 - Dual quantization
 - Multi-bit quantization
 - Bandpass $\Sigma\Delta$ modulators
- 4. Continuous-Time $\Sigma\Delta$ Modulators**
 - Basic concepts and topologies
 - Synthesis methods

Introduction: Basic ADC process



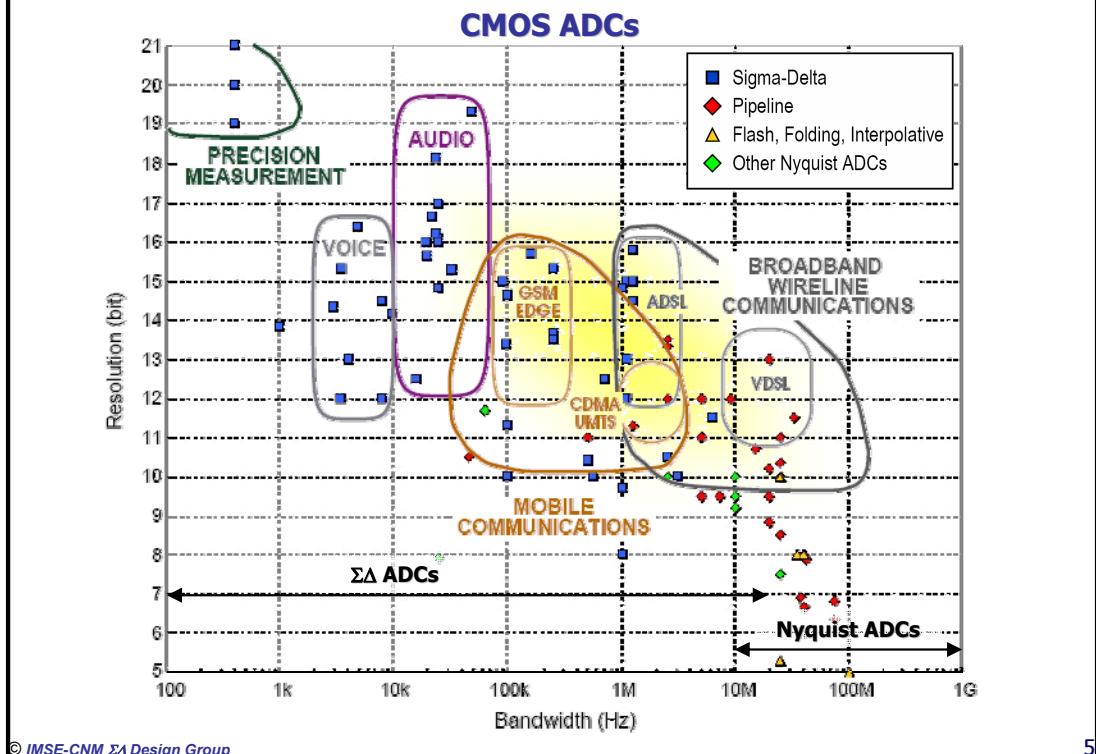
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Introduction: Basic ADC process



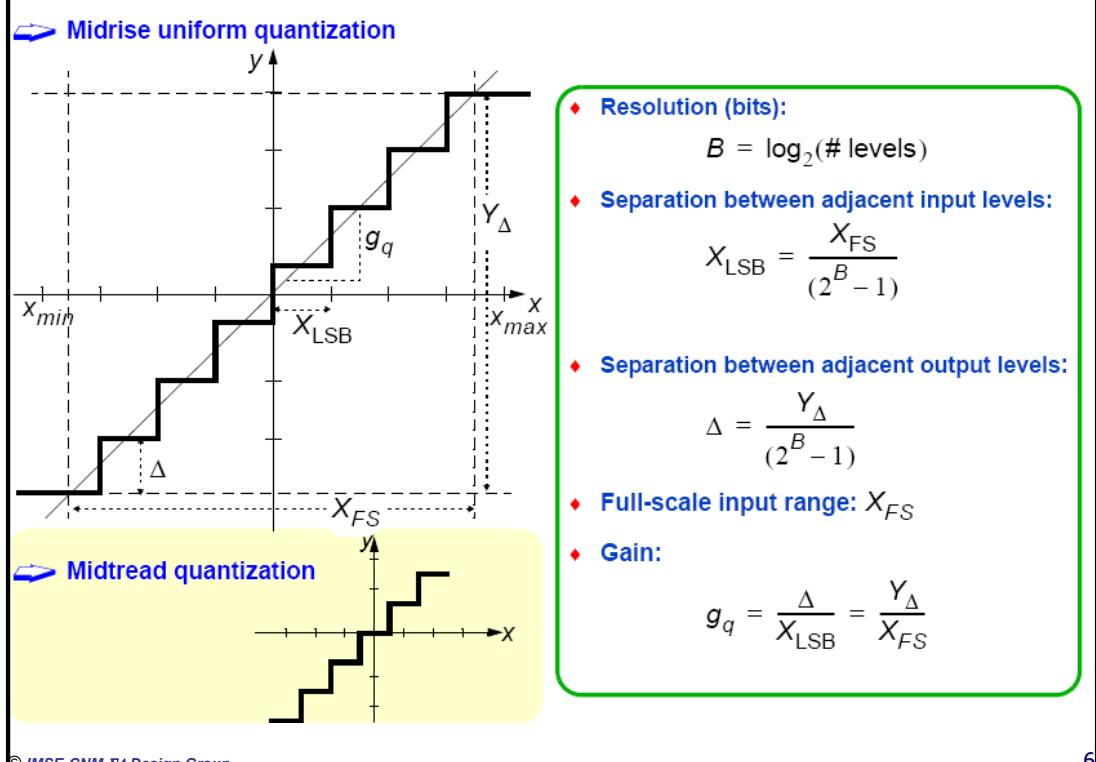
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Introduction: Resolution vs. conversion rate



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Introduction: Quantization

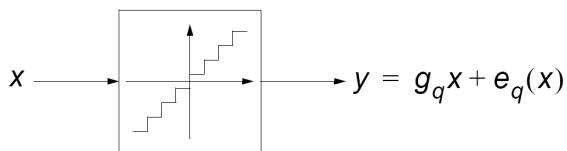


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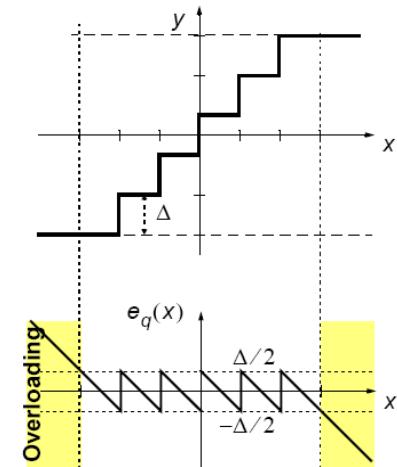
Introduction: Quantization



Quantization input-output characteristic

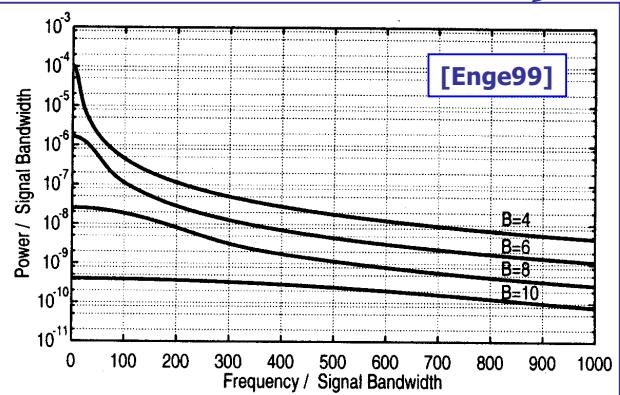


Quantization error



White noise model

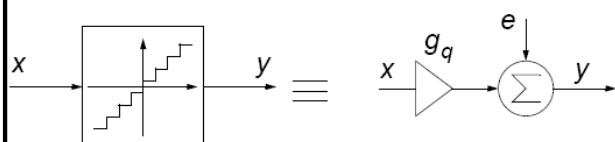
- If x varies randomly from sample to sample
- If the # of quantizer levels is high



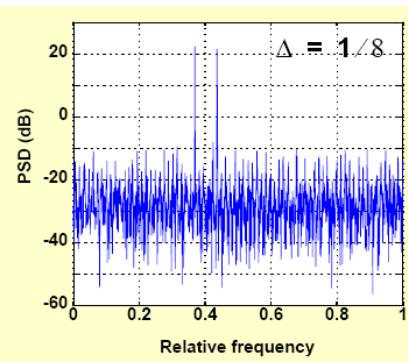
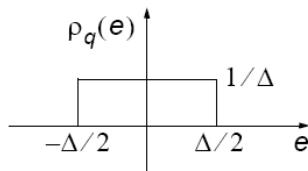
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Introduction: Quantization - white noise model



Probability Density Function

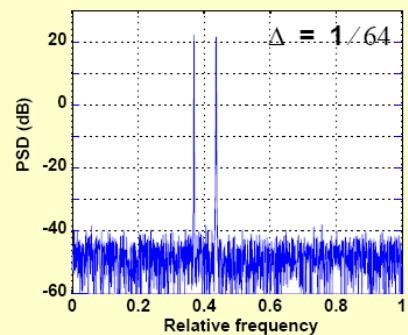


Quantization error power

$$\sigma^2(e) = \left[\frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de \right] = \frac{\Delta^2}{12}$$

Quantization error Power Spectral Density

$$S_E(f) = \frac{\sigma^2(e)}{f_s} = \frac{\Delta^2}{12f_s}$$



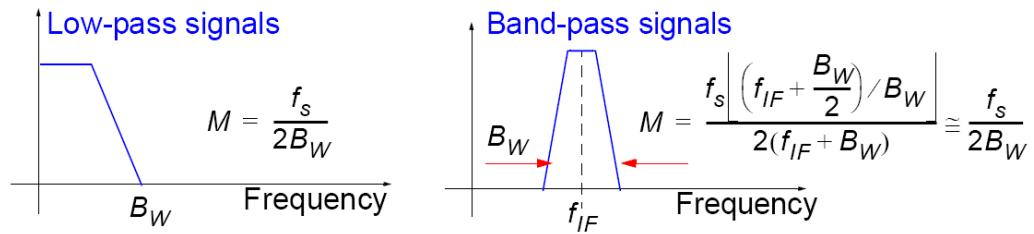
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Introduction: Sampling



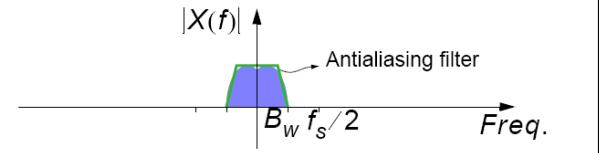
□ Oversampling



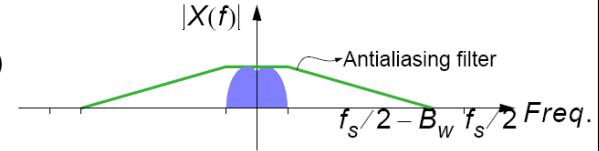
OSR $\equiv M \equiv$ Oversampling Ratio

□ Classification of ADCs

- ◆ Nyquist-rate ADCs ($M \sim 1$)



- ◆ Oversampling ADCs ($M > 1$)



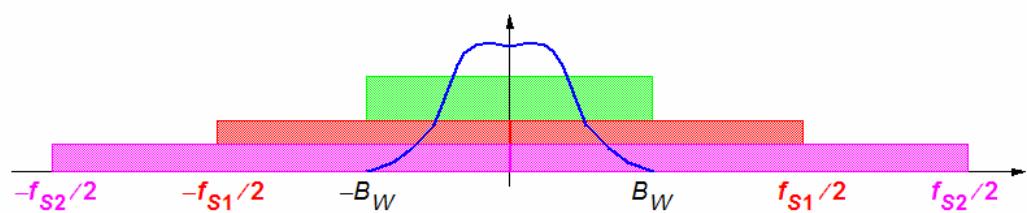
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Fundamentals of $\Sigma\Delta$ ADCs: Oversampling

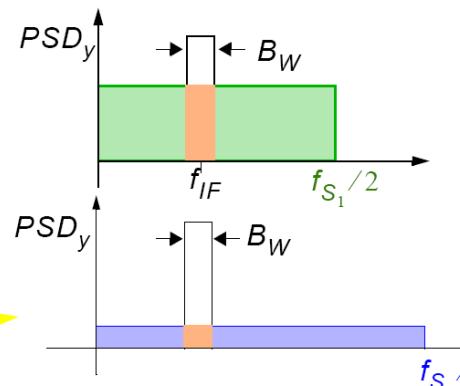


■ PSD of oversampled quantization noise



■ In-Band Noise power (IBN or P_Q)

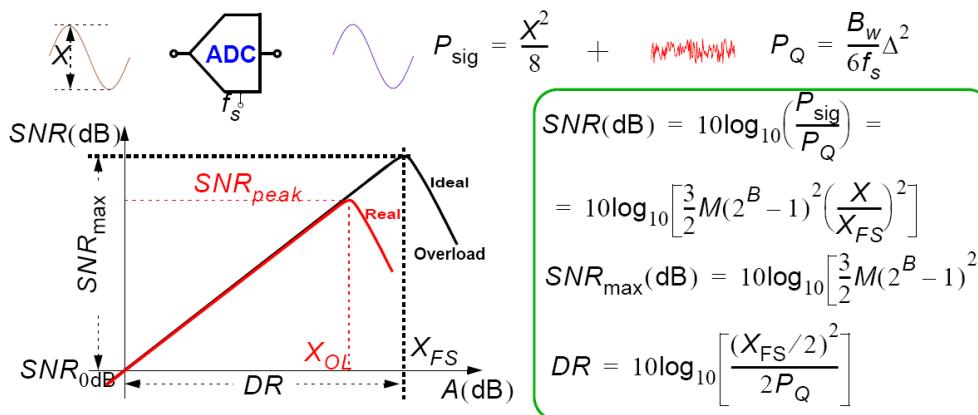
$$P_Q = \int_{f_{IF}-B_W/2}^{f_{IF}+B_W/2} 2S_E(f)df = \frac{B_W \Delta^2}{6f_s} = \frac{\Delta^2}{12M}$$



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Fundamentals of $\Sigma\Delta$ ADCs: Performance Metrics



♦ N-bit Nyquist-Rate ADC

- $f_{s1} = f_N \equiv 2B_w$
- $\text{SNR}_{\max} = 10\log_{10}\left[\frac{3}{2}(2^N - 1)^2\right]$

♦ B-bit Oversampled ADC

- $f_{s2} = Mf_N (M > 1)$
- $\text{SNR}_{\max} = 10\log_{10}\left[\frac{3}{2}M(2^B - 1)^2\right]$



$$ENOB \approx \frac{\text{SNR}_{\max} - 1.76}{6.02} \approx \log_2(2^B - 1) + \frac{1}{2}\log_2(M) \quad (N > 1)$$

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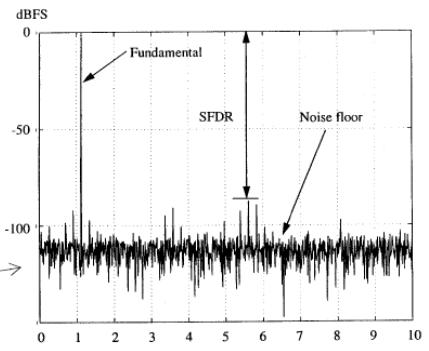
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Fundamentals of $\Sigma\Delta$ ADCs: Performance Metrics



• SNDR / SINAD:

$$SNDR(\text{dB}) = 10\log_{10}\left(\frac{P_{\text{sig}}}{P_Q + P_H}\right)$$



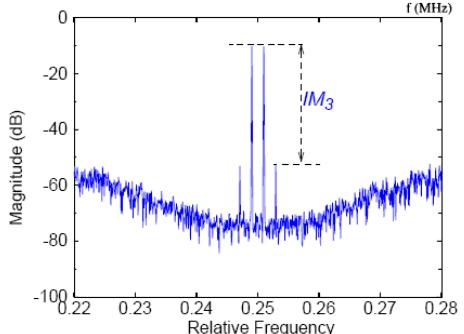
• Effective Number Of Bits ENOB:

$$ENOB \approx \frac{SNDR - 1.76}{6.02}$$

• SFDR: Spurious-Free Dynamic Range

• Harmonic Distortion:

- ♦ HD_k , THD ,
- ♦ IM_3 , IP_3
- ♦ ...

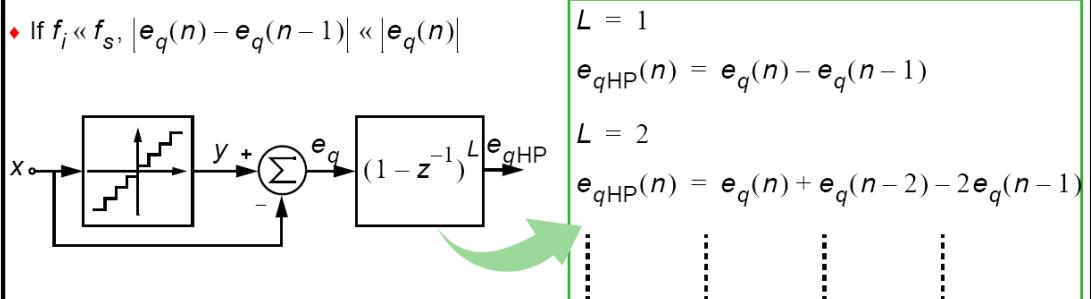


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Fundamentals of $\Sigma\Delta$ ADCs: Quantization Noise Shaping

Processing of the quantization error

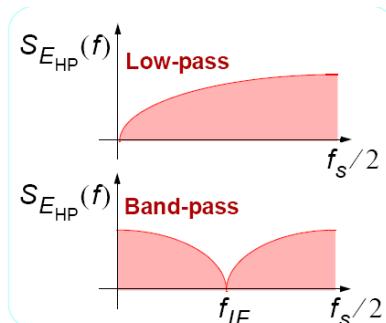


In-band noise power and effective resolution

$$N_{TF}(z) = (1 - z^{-1})^L \Rightarrow S_{E_{HP}} = |N_{TF}(f)|^2 S_E$$

$$P_{E_{HP}} = \int_0^{B_w} S_{E_{HP}}(f) df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)M^{2L+1}}$$

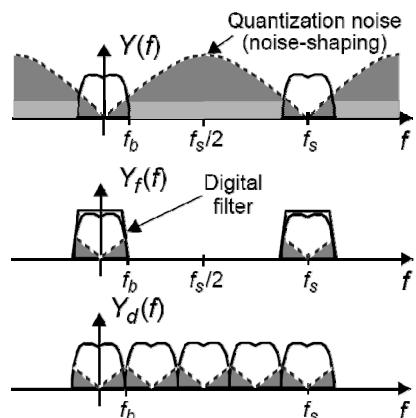
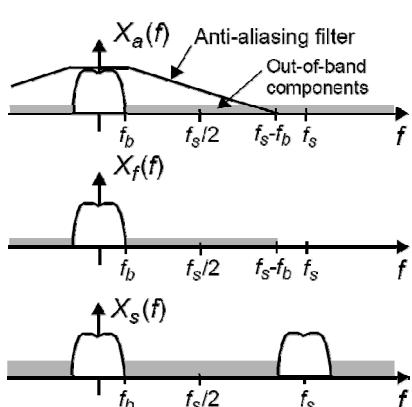
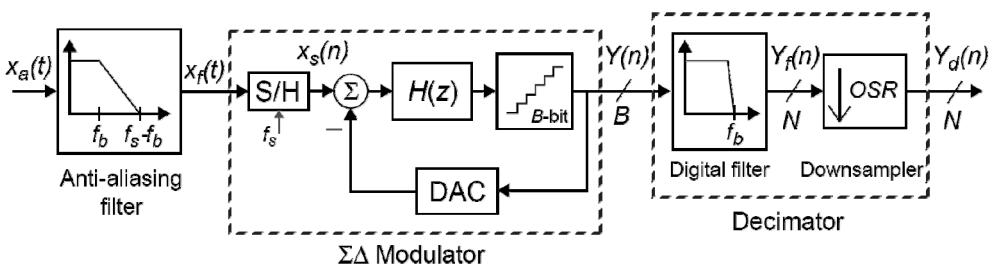
$$N \approx \log_2 \left[\frac{(2^B - 1)(2L+1)}{\pi^{2L}} \right] + \left(L + \frac{1}{2} \right) \log_2(M)$$



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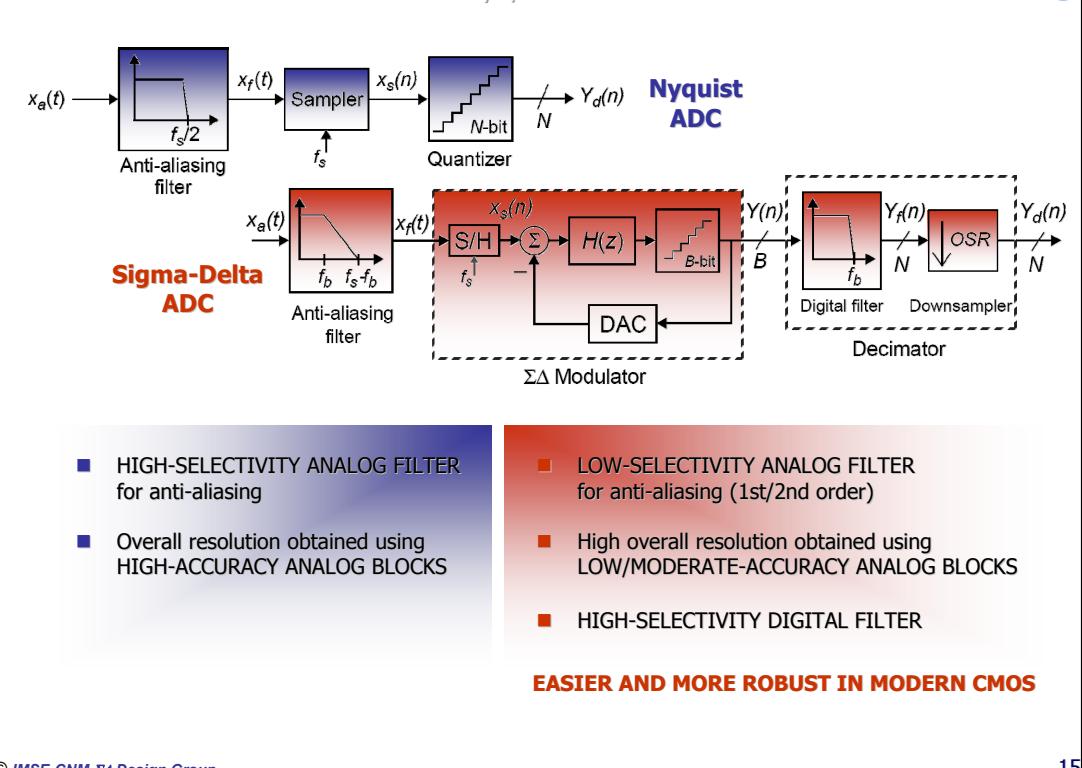
Fundamentals of $\Sigma\Delta$ ADCs: Basic $\Sigma\Delta$ ADC architecture



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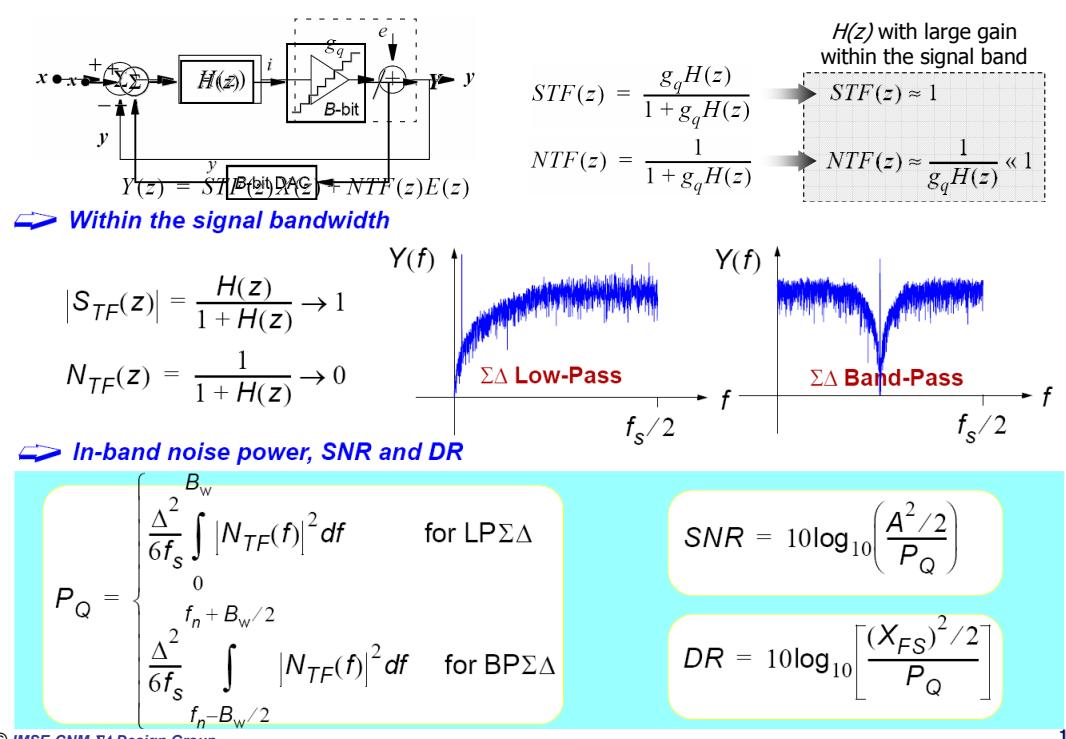
Fundamentals of $\Sigma\Delta$ ADCs: Nyquist-rate vs. $\Sigma\Delta$ ADCs



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Fundamentals of $\Sigma\Delta$ ADCs: Basic $\Sigma\Delta M$ architecture



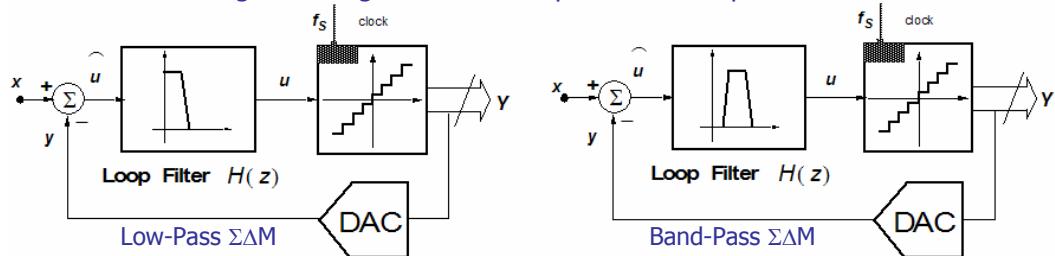
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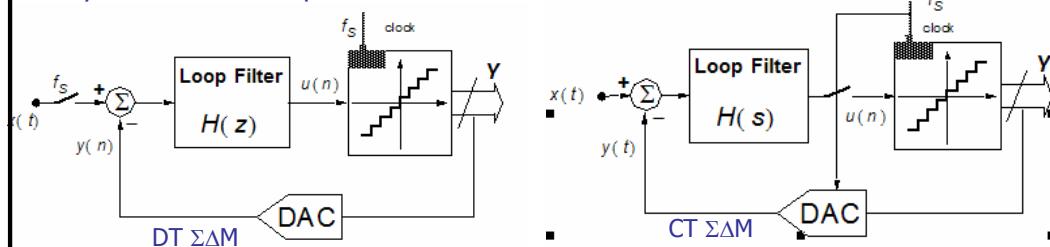
Fundamentals of $\Sigma\Delta$ ADCs: Classification of $\Sigma\Delta$ s



- Nature of the signals being handled: Low-pass vs. Band-pass



- Dynamics of the loop filter: Discrete-Time vs. Continuous-Time

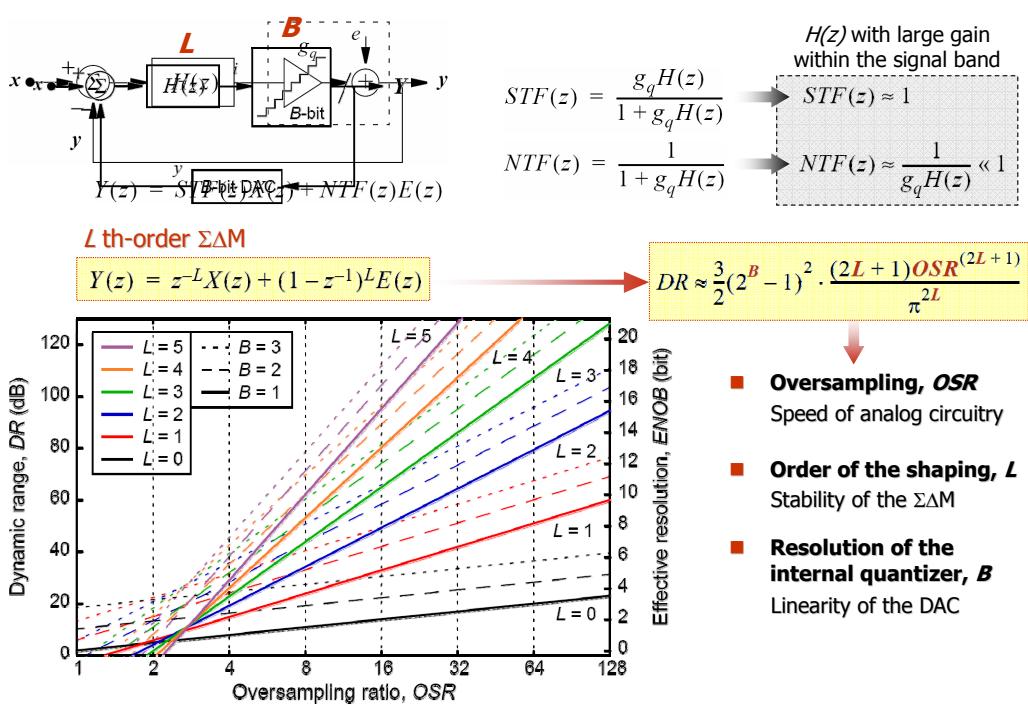


- Number of bits of the embedded quantizer: single-bit vs. multi-bit
- Number of quantizers employed: single-loop, cascade, etc..
- Type of primitives available in the fabrication technology...

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Fundamentals of $\Sigma\Delta$ ADCs: Basic control parameters



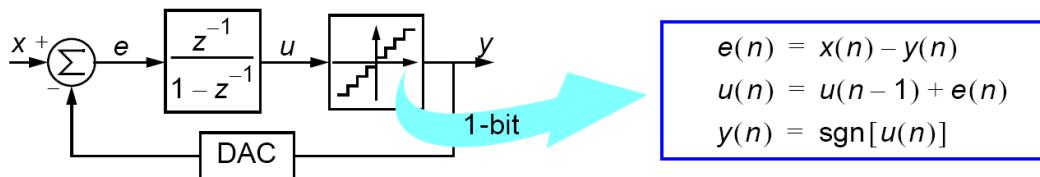
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DT- $\Sigma\Delta$ Ms: 1st-order LP $\Sigma\Delta$ Modulator



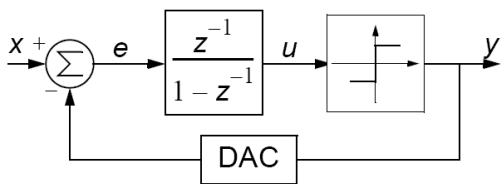
$$N_{TF}(z)|_{z=1} \rightarrow 0 \quad \Rightarrow \quad \frac{1}{1+H(z)}|_{z=1} \rightarrow 0 \quad \Rightarrow \quad H(z) = \frac{1}{z-1}$$



- Using a linear model for the quantizer

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z)$$

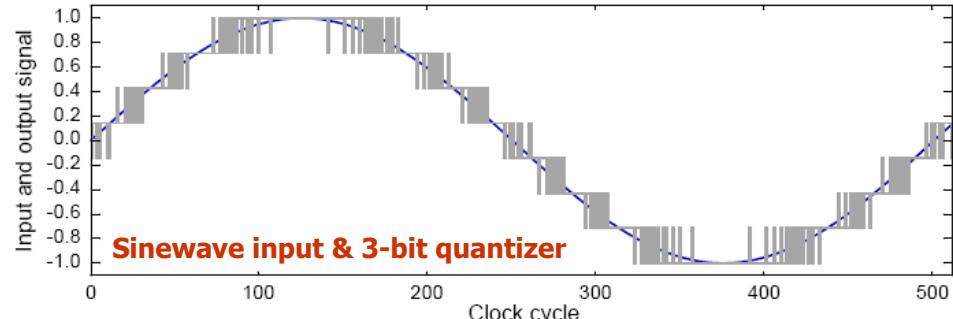
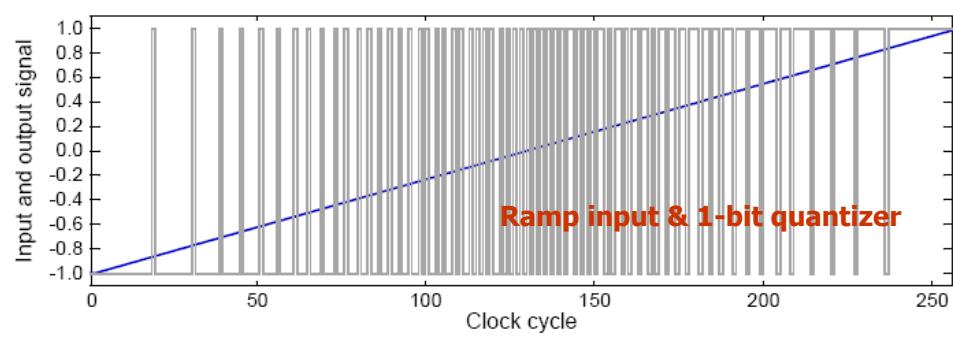
$$DR(\text{dB}) \cong 10 \log_{10} \left(\frac{9M^3}{2\pi^2} \right)$$



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DT- $\Sigma\Delta$ Ms: 1st-order LP $\Sigma\Delta$ Modulator



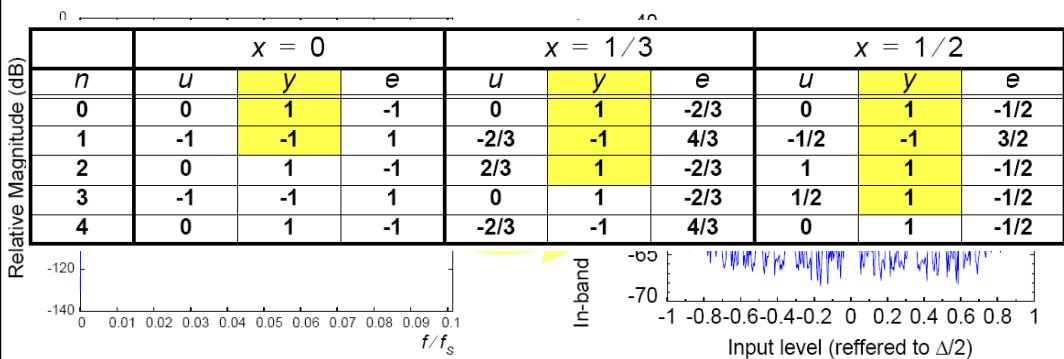
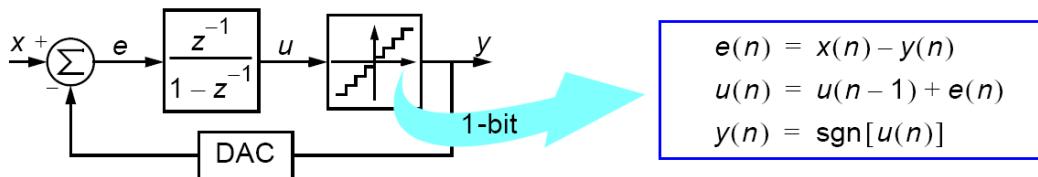
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DT- $\Sigma\Delta$ Ms: 1st-order LP $\Sigma\Delta$ Modulator



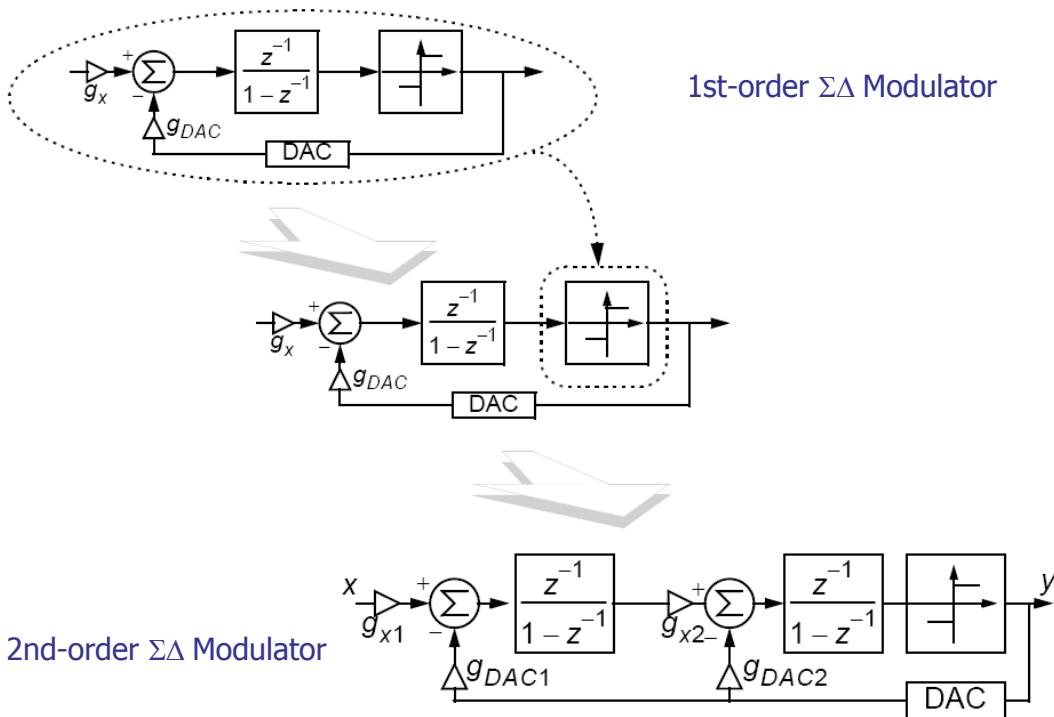
Noise pattern



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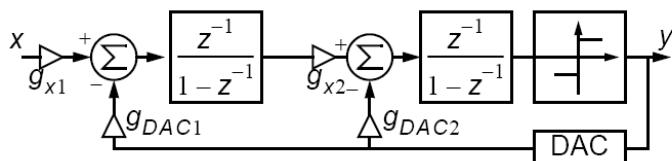
DT- $\Sigma\Delta$ Ms: 2nd-order LP $\Sigma\Delta$ Modulator



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DT- $\Sigma\Delta$ Ms: 2nd-order LP $\Sigma\Delta$ Modulator



➡ Stability conditions:

$$g_{DAC1}g_{x2}g_q = 1$$

$$g_{DAC2} = 2g_{DAC1}g_{x2}$$

Linear analysis

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z)$$

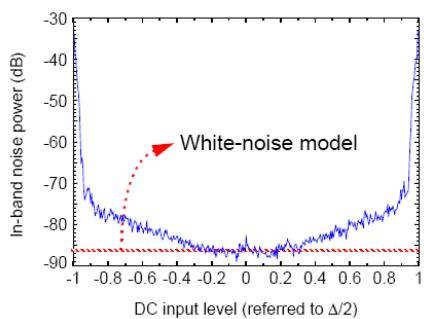
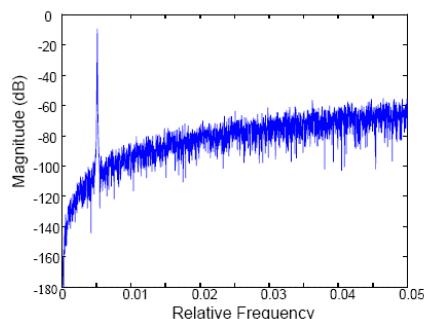
$$P_Q \cong \frac{\Delta^2 \pi^4}{60 M^5} \Rightarrow DR \cong \frac{15 M^5}{2\pi^4}$$

♦ Dependence on M : 15 dB/oct.

♦ Example: digitize a 10kHz signal with 16 bits

- $M = 150$ ($f_s = 3$ MHz) for a 2nd-order $\Sigma\Delta$ M
- $M = 1500$ ($f_s = 30$ MHz) for a 1st-order $\Sigma\Delta$ M

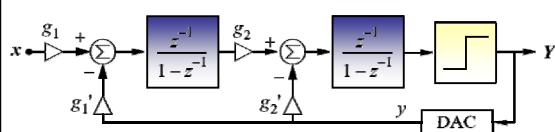
Output spectrum and noise pattern



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DT- $\Sigma\Delta$ Ms: High-order Single-loop $\Sigma\Delta$ Modulators



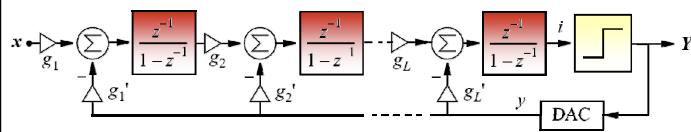
2nd-order $\Sigma\Delta$ M

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z)$$

$$g_1'g_2g_q = 1$$

$$g_2' = 2g_1'g_2$$

Stable for inputs in $[-0.9\Delta/2, +0.9\Delta/2]$
if $g_2' > 1.25g_1'g_2$ [Candy85]

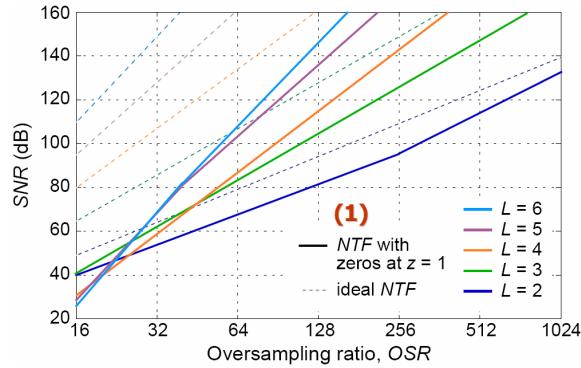


Lth-order $\Sigma\Delta$ M

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^L E(z)$$

pure-differentiator FIR NTF

$$\|NTF\|_\infty = 2^L \text{ Prone to instability}$$



High-order $\Sigma\Delta$ loops are only conditionally stable [OptE90]

IIR NTFs

[Lee87]

$$NTF(z) = \frac{(z-1)^L}{D(z)} \quad (1)$$

- Zeros at $z = 1$
- Butterworth/Chebyshev poles

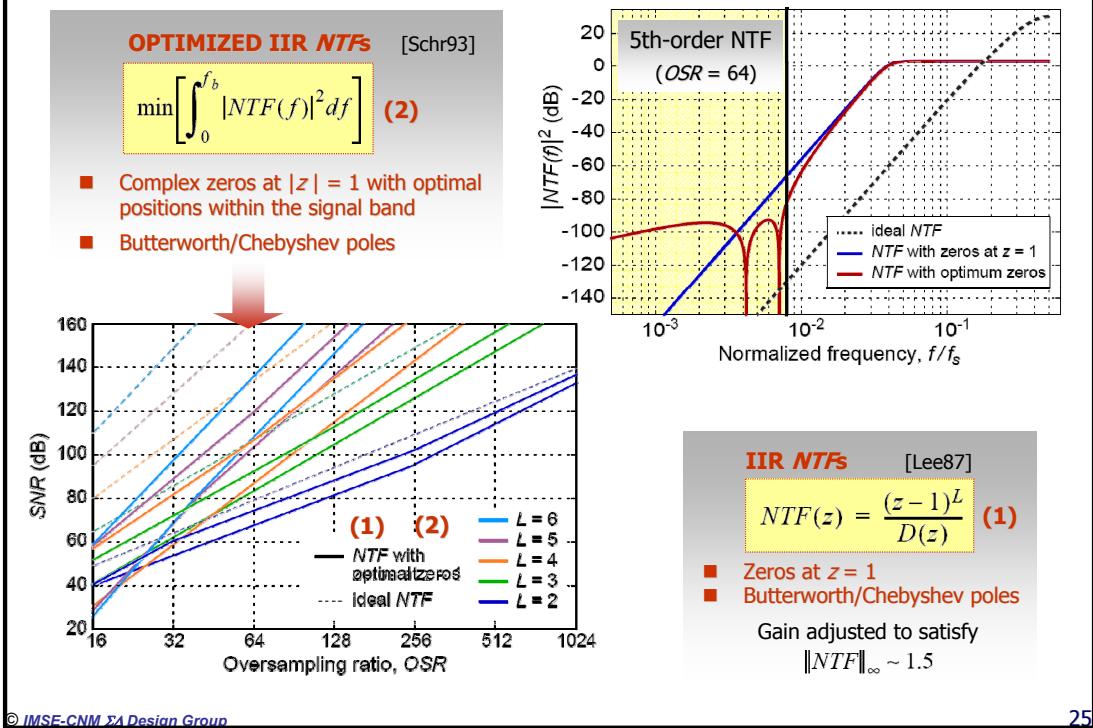
Gain adjusted to satisfy

$$\|NTF\|_\infty \sim 1.5$$

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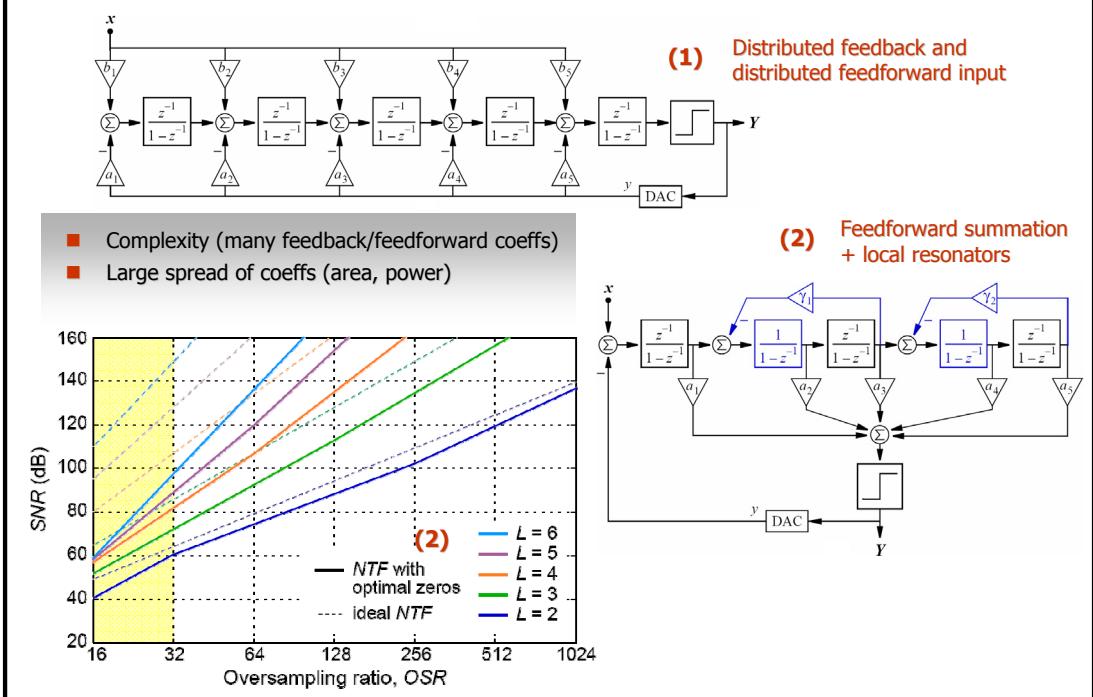
DT- $\Sigma\Delta$ Ms: High-order Single-loop $\Sigma\Delta$ Modulators



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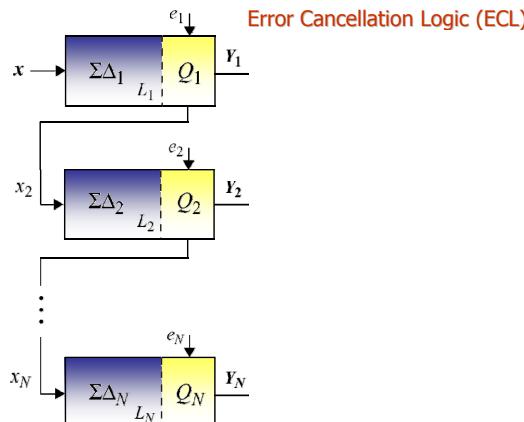
DT- $\Sigma\Delta$ Ms: High-order Single-loop $\Sigma\Delta$ Modulators



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DT- $\Sigma\Delta$ Ms: High-order Cascade $\Sigma\Delta$ Modulators



$$Y(z) = z^{-L} X(z) + d_{2N-3} (1-z^{-1})^L E_N(z)$$

$$L = L_1 + L_2 + \dots + L_N$$

- HIGH-ORDER STABLE OPERATION is ensured by cascading low-order stages ($L_i = 1, 2$).
- Relationships among ECL and $\Sigma\Delta$ M to be fulfilled for perfect cancellation (NOISE LEAKAGE).

$d > 1$, interstage coupling

$$P_Q \cong d_{2N-3}^2 \cdot \frac{\Delta_N^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}}$$

Systematic loss of resolution, but:

- Smaller than for single loops
- Independent of OSR

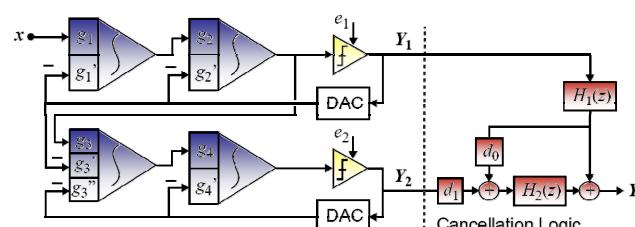
MASH $\Sigma\Delta$ Ms

- Each stage re-modulates a signal containing the quantization error in the previous one.
- Digital processing is used to cancel out all quantization errors, but that in the last stage.

$$NTF_i(z) = 0 \quad , i = 1, \dots, N-1$$

- Small spread of analog coeffs
- ECL can be easily implemented
- Performance close to ideal
- Suited at low oversampling

DT- $\Sigma\Delta$ Ms: High-order Cascade $\Sigma\Delta$ Modulators



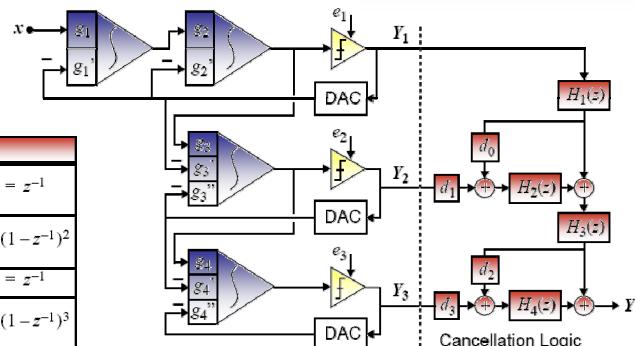
Analog	Digital	
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$	$H_1(z) = z^{-2}$
$g_4' = 2g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1-z^{-1})^2$

2-2 $\Sigma\Delta$ M [Kare90]
4th-order 2-stage cascade

Noise leakage precludes the cascading of a large number of stages to be practical

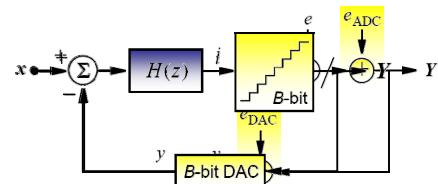
- 1-1-1 $\Sigma\Delta$ M** [Mats87]
- 2-1 $\Sigma\Delta$ M** [Longo88]
- 2-2-1 $\Sigma\Delta$ M** [Vleu01]
- 2-1-1-1 $\Sigma\Delta$ M** [Rio00]
- 2-2-2 $\Sigma\Delta$ M** [Dedic94]

2-1-1 $\Sigma\Delta$ M [Yin94]
4th-order 3-stage cascade

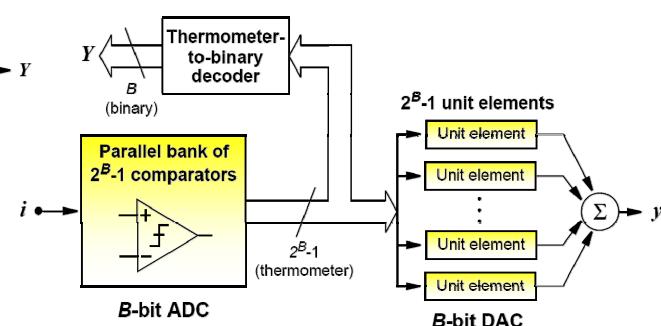


Analog	Digital	
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$	$H_1(z) = z^{-1}$
$g_4' = g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$	$H_2(z) = (1-z^{-1})^2$
$d_2 = 0$		$H_3(z) = z^{-1}$
$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$		$H_4(z) = (1-z^{-1})^3$

DT- $\Sigma\Delta$ Ms: Multi-bit $\Sigma\Delta$ Modulators



- ▼ Increased dynamic range
 B can trade for OSR (wideband)
- ▼ Better stability properties
More aggressive high-order NTFs
- ▼ DAC non-linearities are directly added to the input
The linearity of the $\Sigma\Delta$ M will be no better than that

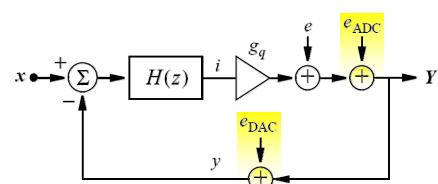


DAC linearity limited by component mismatch

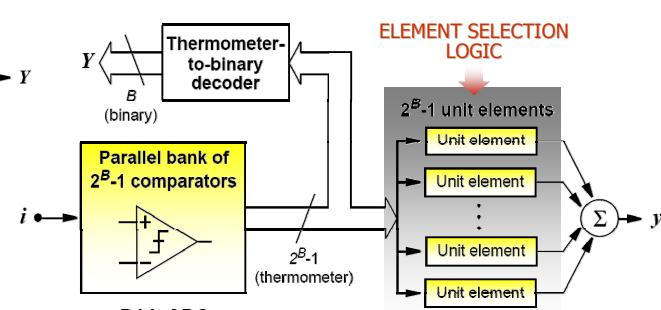
POSSIBLE APPROACHES

- Correcting DAC errors
 - Element Trimming
 - Analog Calibration
 - Digital Correction
- Decorrelating DAC errors from the input
 - DEM techniques
- Introducing DAC errors at a non-critical position
 - Dual quantization

DT- $\Sigma\Delta$ Ms: Multi-bit $\Sigma\Delta$ Modulators



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The linearity of the $\Sigma\Delta$ M will be no better than that



DAC linearity limited by component mismatch

Dynamic Element Matching (DEM)

- Elements selected to make DAC errors independent of the input signal
- Algorithms that try to average the error in each DAC level to zero (to push DAC errors to high freq.)
 - ▼ Randomization: Distortion transforms into white noise
 - ▼ Rotation: Distortion moves out of band (CLA)
 - ▼ Mismatch-shaping: 1st/2nd order (ILA, DWA, DDS)

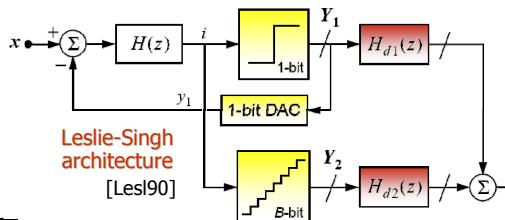
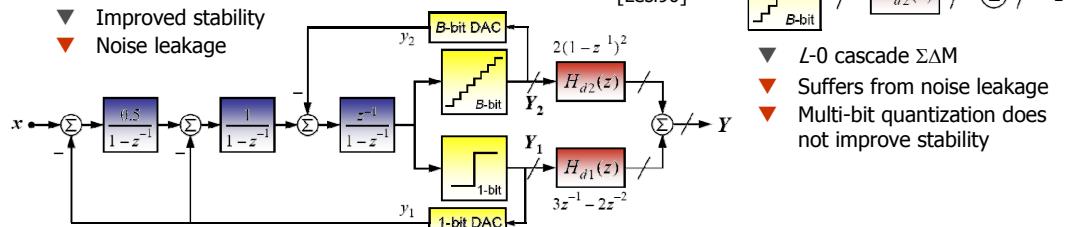
DT- Σ Ms: Dual-quantization $\Sigma\Delta$ Modulators



Dual Quantization

- Combines 1-bit and multi-bit quantizers (linearity/reduced error)

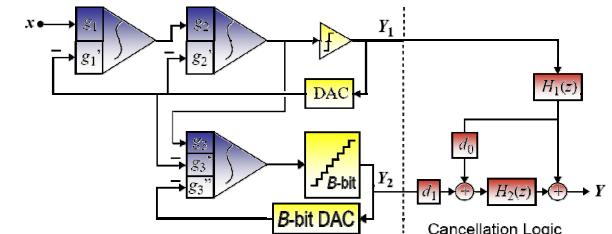
Concept applied to single-loop $\Sigma\Delta$ Ms [Harr91]



- L-0 cascade $\Sigma\Delta$ M
- Suffers from noise leakage
- Multi-bit quantization does not improve stability

Concept applied to cascade $\Sigma\Delta$ Ms [Bran91]

- Multi-bit quantization usually applied only in the last stage
- DAC errors shaped by $L-L_N$
Relaxes DAC requirements
- Noise leakage (inherent to cascades)



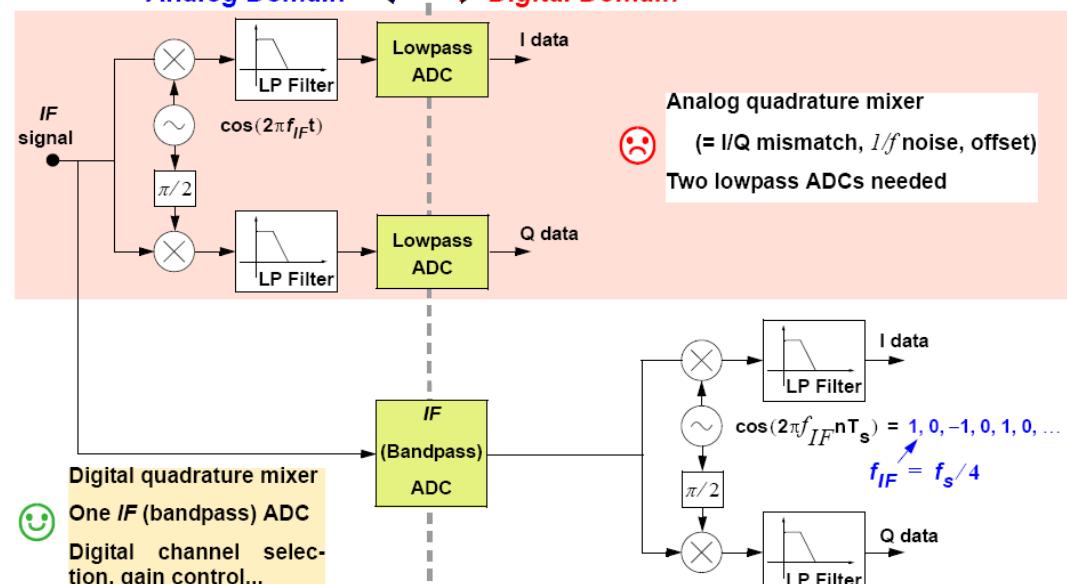
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DT- $\Sigma\Delta$ Ms: Bandpass $\Sigma\Delta$ Modulators - IF Digitization



Analog Domain ← → Digital Domain



Analog quadrature mixer

(= I/Q mismatch, 1/f noise, offset)
Two lowpass ADCs needed

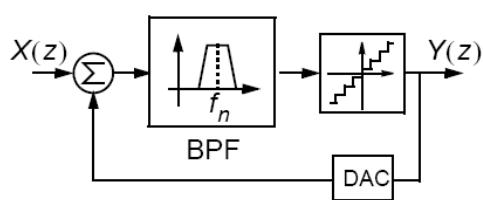
☺ One IF (bandpass) ADC
Digital channel selection, gain control...

Digital mixing simplified for $f_{IF} = f_s/4$

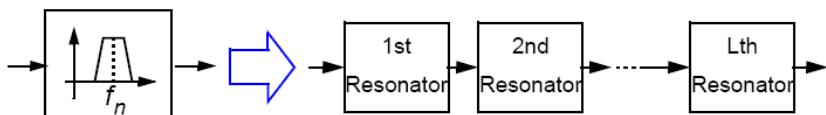
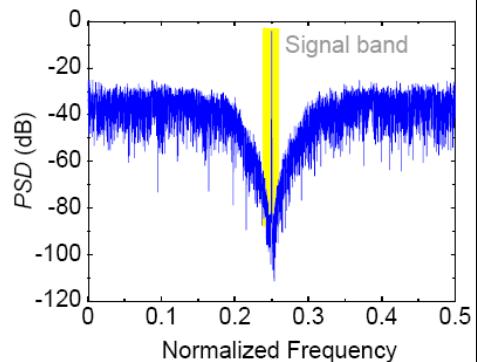
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DT- $\Sigma\Delta$ Ms: Bandpass $\Sigma\Delta$ Modulators



$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z)$$



$$H_{bp}(z) = \left[\frac{N_{RES}(z)}{(1-z^{-1}z_n)(1-z^{-1}z_n^*)} \right]^L \quad (z_n = e^{2\pi f_n T_s})$$

$$(N_{RES}(z) + (1-z^{-1}z_n)(1-z^{-1}z_n^*) = 1) \Rightarrow N_{TF}(z) = [1 - 2 \cos(2\pi f_n T_s) z^{-1} + z^{-2}]^L$$

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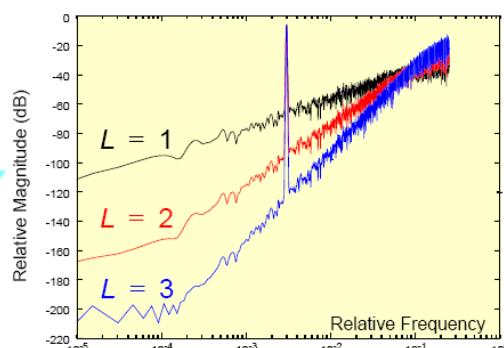
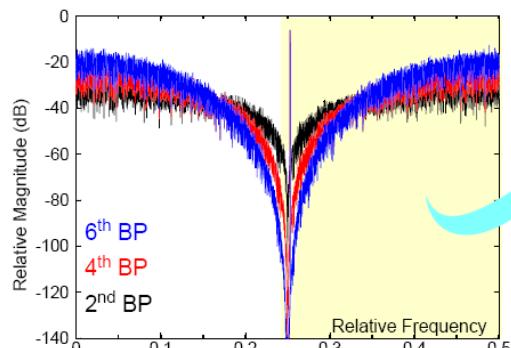
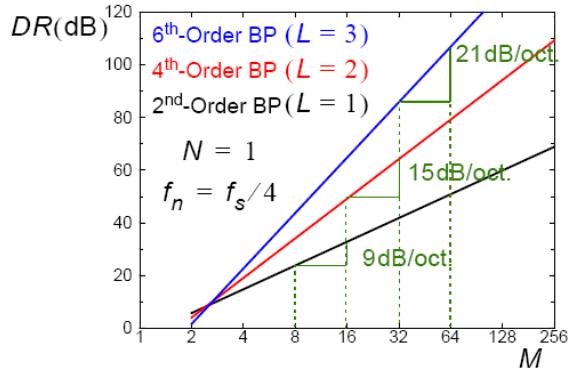
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DT- $\Sigma\Delta$ Ms: Bandpass $\Sigma\Delta$ Modulators



$$P_Q \equiv \frac{(\sin[2\pi f_n T_s])^{2L} \pi^{2L} X_{FS}^2}{12(2^N - 1)^2 (2L + 1) M^{(2L + 1)}}$$

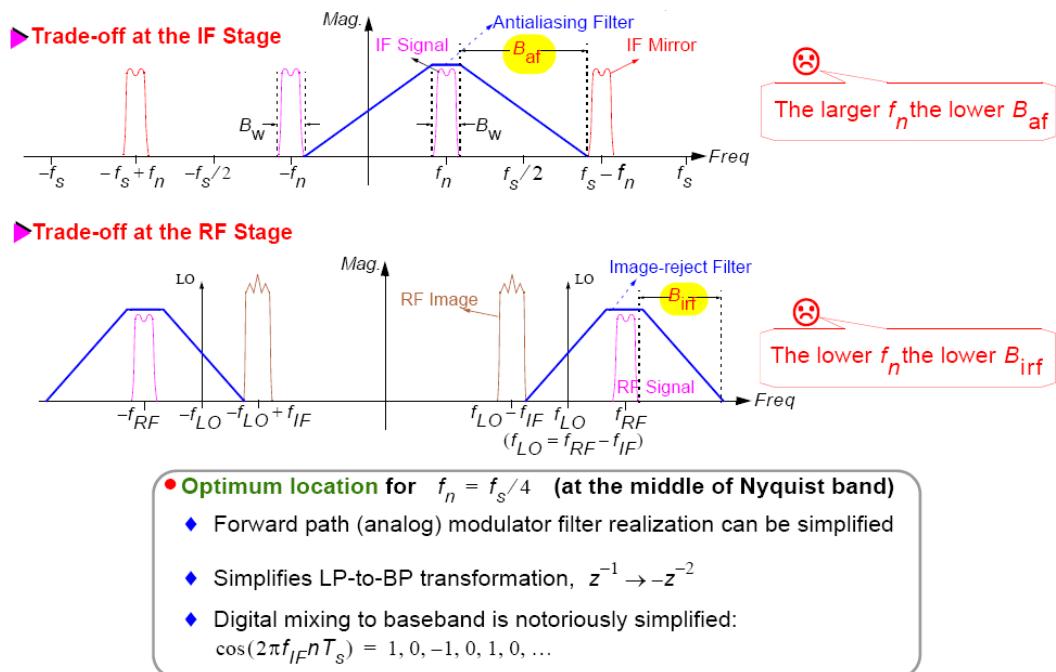
$$DR \equiv \frac{3(2^N - 1)^2 (2L + 1) M^{2L + 1}}{2\pi^{2L} (\sin[2\pi f_n T_s])^{2L}}$$



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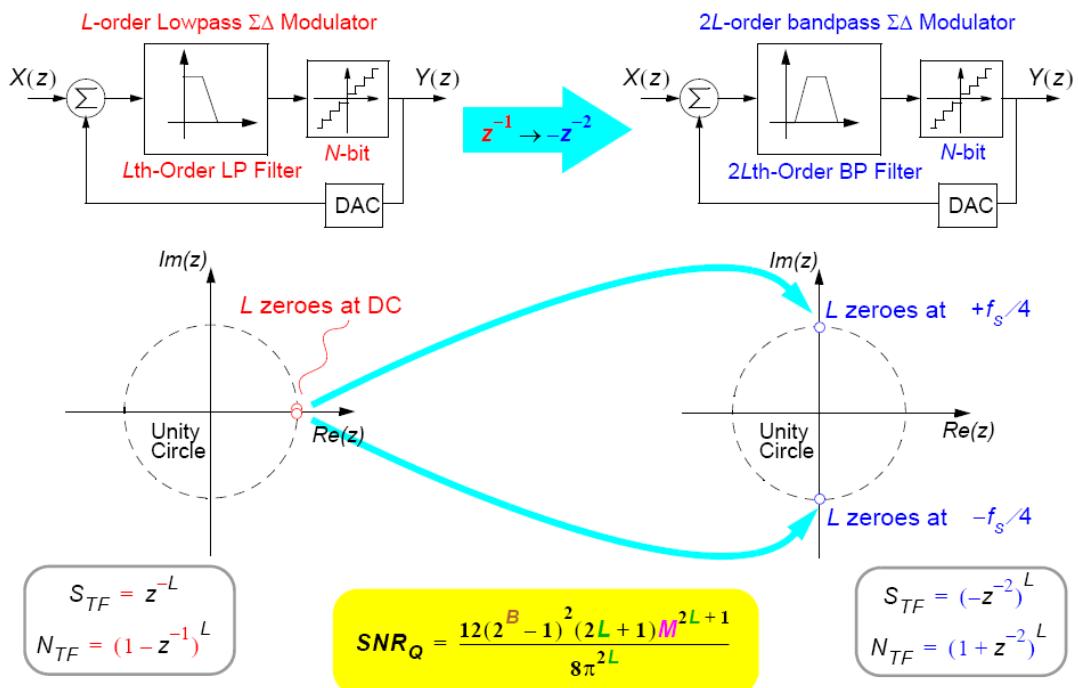
DT- $\Sigma\Delta$ Ms: Bandpass $\Sigma\Delta$ Ms - Signal band location



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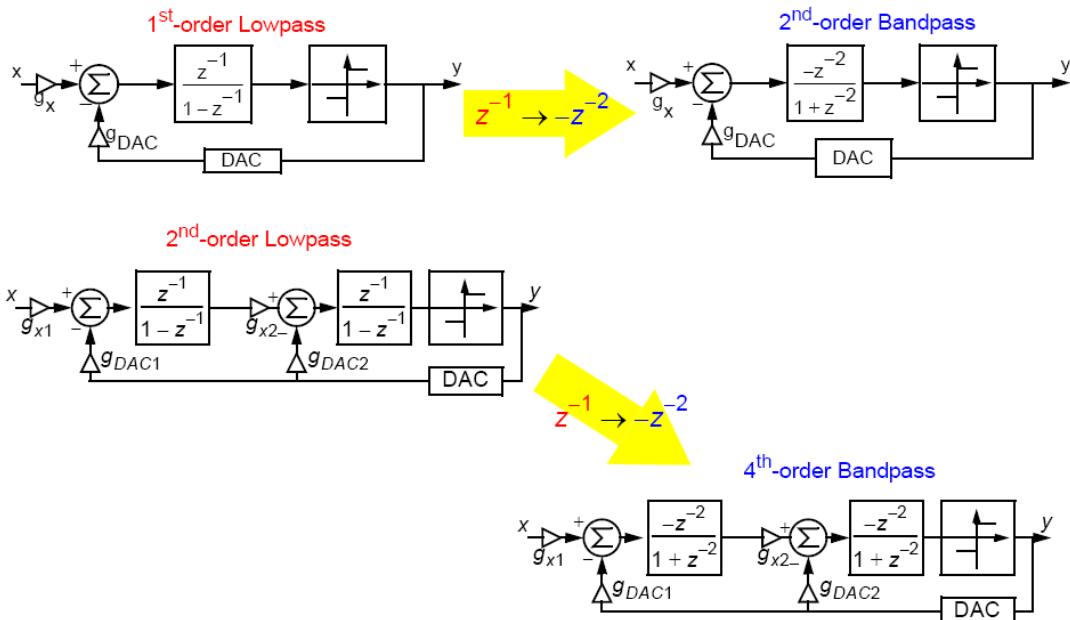
DT- $\Sigma\Delta$ Ms: LP-to-BP Transformation Method



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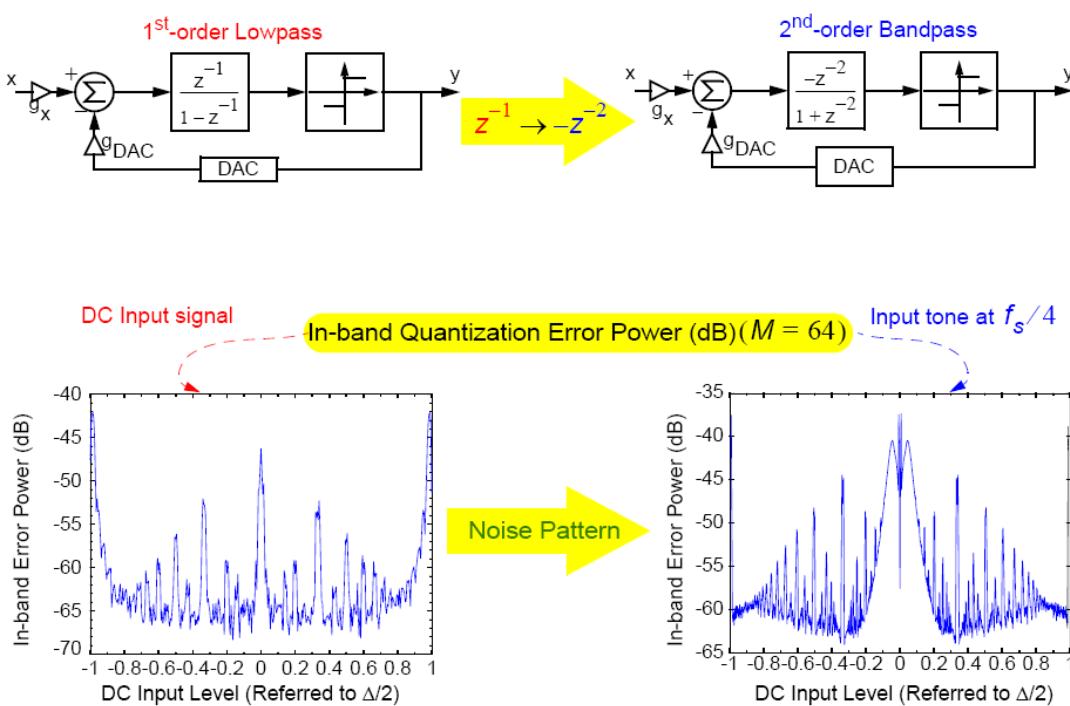
DT- $\Sigma\Delta$ Ms: LP-to-BP Transformation Method



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DT- $\Sigma\Delta$ Ms: LP-to-BP Transformation Method



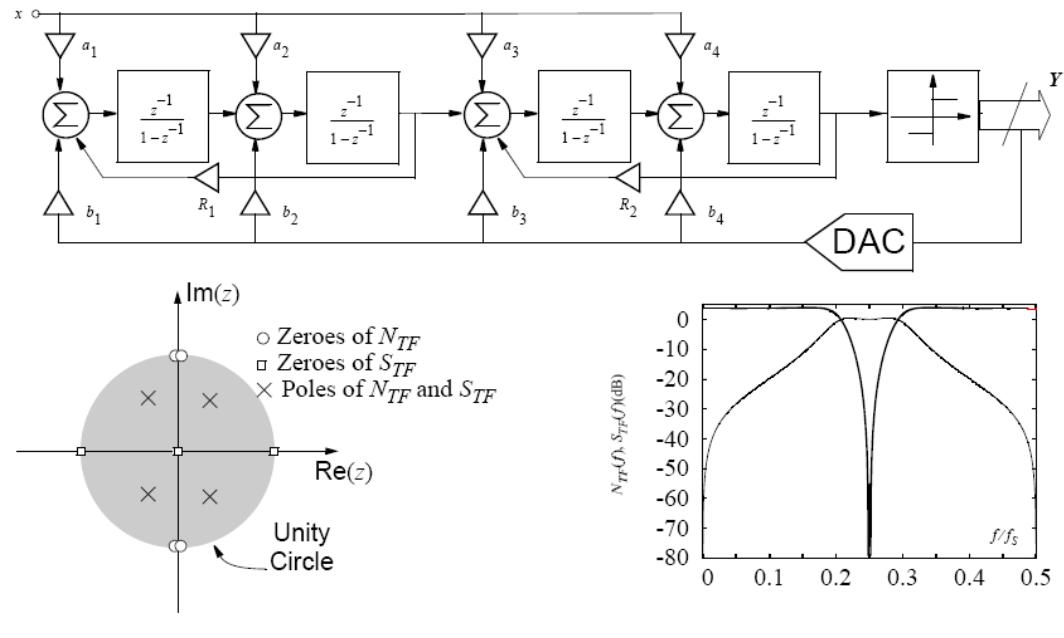
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DT- $\Sigma\Delta$ Ms: Bandpass $\Sigma\Delta$ Modulators



■ Other BP- $\Sigma\Delta$ M architectures



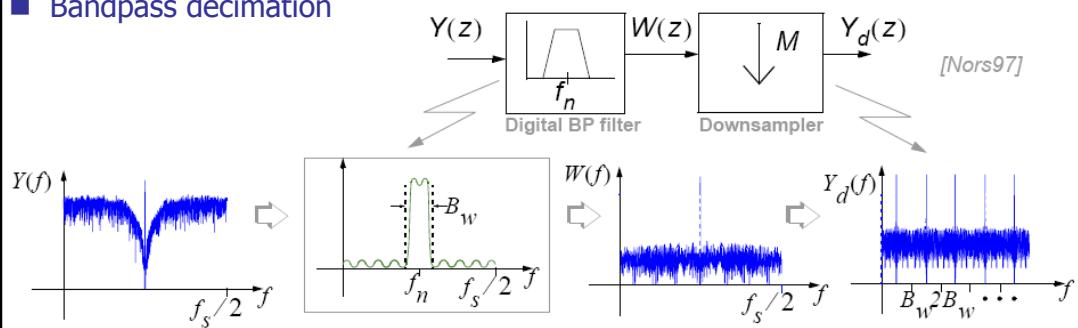
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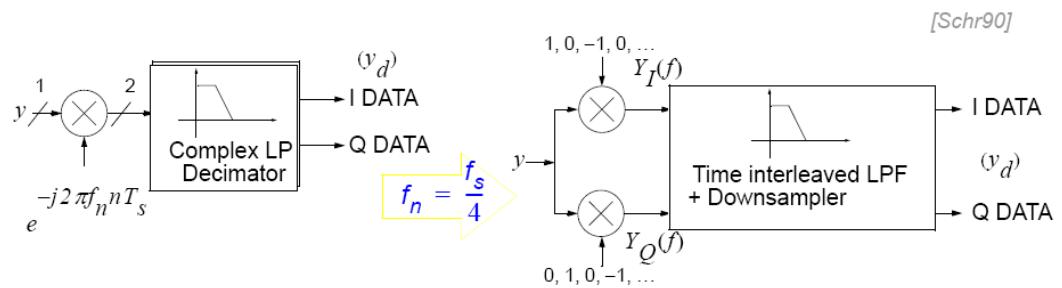
DT- $\Sigma\Delta$ Ms: Bandpass $\Sigma\Delta$ ADCs - Decimation



■ Bandpass decimation



■ Efficient decimation



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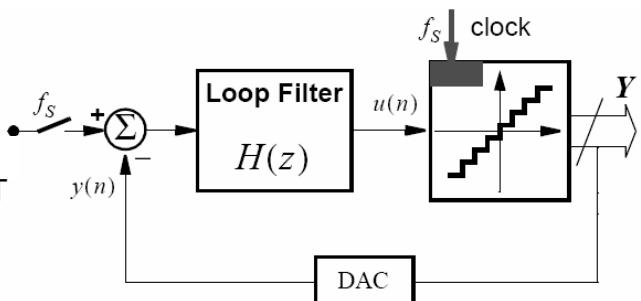
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CT- $\Sigma\Delta$ Ms: Basic Concepts



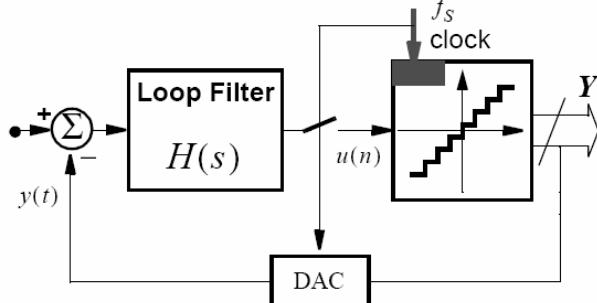
□ Discrete-Time $\Sigma\Delta$ Ms

- ◆ DT loop filter
- ◆ All internal signals are DT
- ◆ Sampling at the input



□ Continuous-Time $\Sigma\Delta$ Ms

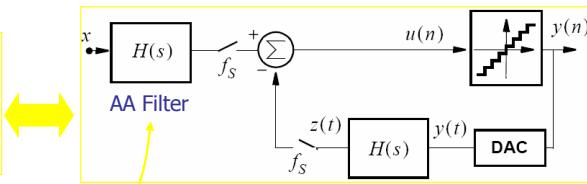
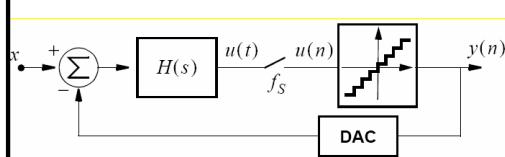
- ◆ CT front (loop filter) part
- ◆ DT back (quantizer) part
- ◆ Sampling inside the loop



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CT- $\Sigma\Delta$ Ms: Basic Concepts



□ Pros of CT- $\Sigma\Delta$ Ms

- ◆ Implicit anti-aliasing filter
- ◆ Less impact of sampling errors
- ◆ No input switches – potentially better for low-voltage supply
- ◆ No “settling” error at the loop filter circuitry
- ◆ Potentially larger operation speed with less power consumption
- ◆ No sampling of the noise at the input capacitors
- ◆ Reduced digital noise coupling

□ Counters of CT- $\Sigma\Delta$ Ms

- ◆ Very involved dynamic due to the combination of non-linearity, CT and DT
- ◆ larger impact of circuit non-linearities
- ◆ Time constant tuning is needed for correct loop filtering
- ◆ Large sensitive to time uncertainty (“jitter”)

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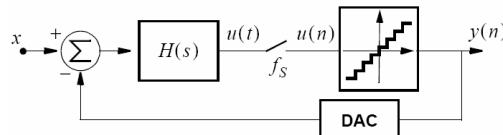
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CT- $\Sigma\Delta$ Ms: Basic Concepts

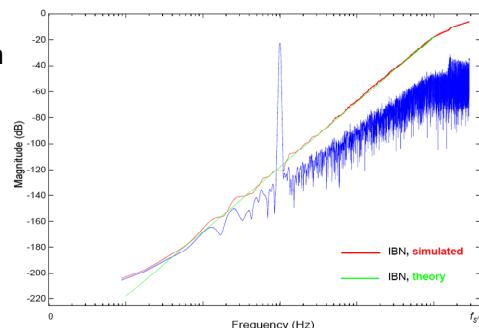


□ Linear analysis of CT- $\Sigma\Delta$ Ms, assuming [Bree01]:

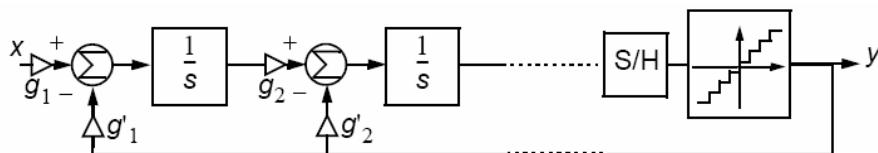
- ◆ Linear model for the quantizer
- ◆ DAC gain is unity in the signal bandwidth



$$Y(f) \equiv \frac{H(f)}{1+H(f)} \cdot X(f) + \frac{1}{1+H(f)} \cdot E(f)$$



□ Example: L th-order, B -bit single-loop architecture



$$Y(f) \equiv \frac{g_1}{g'_1} \cdot X(f) + (2\pi f \tau)^L \cdot E_q(f) \quad \Rightarrow \quad DR = \frac{3(2^B - 1)^2 (2L + 1) M^{2L+1}}{2\pi^{2L}}$$

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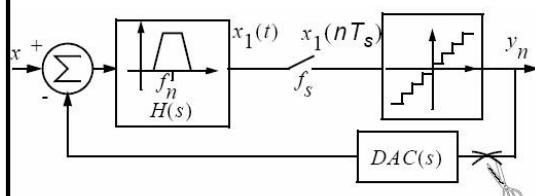
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



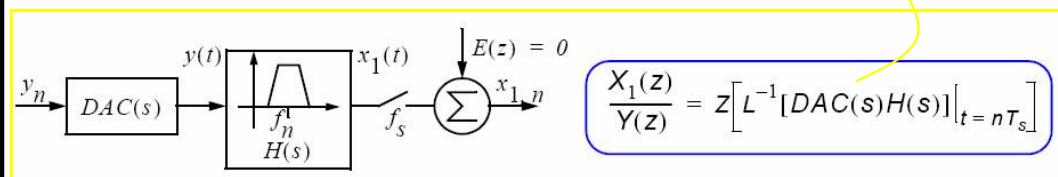
□ DT-to-CT synthesis method: pulse invariant transformation (freq. domain)

- ◆ Find an equivalent DT $\Sigma\Delta$ M that fulfils the required specifications
- ◆ Based on a DT-to-CT equivalence [Cher00]



DAC	$H(z)$	$H(s)$
NRZ	$\frac{z^{-1} \cdot (1-z^{-1})}{1+z^{-2}}$	
RZ	$\frac{\left(1-\frac{\sqrt{2}}{2}\right) \cdot z^{-1} - \left(\frac{\sqrt{2}}{2} \cdot z^{-2}\right)}{1+z^{-2}}$	$\frac{\omega_o \cdot s}{s^2 + \omega_o^2}$
HRZ	$\frac{\frac{\sqrt{2}}{2} \cdot z^{-1} - \left(\left(1-\frac{\sqrt{2}}{2}\right) \cdot z^{-2}\right)}{1+z^{-2}}$	

Open-loop configuration



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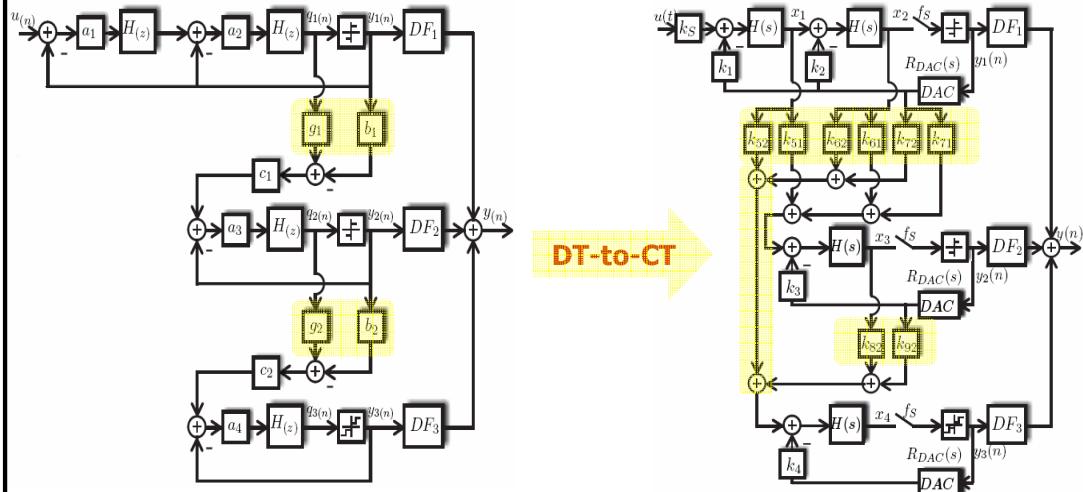
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



□ Application of DT-to-CT method to cascade CT $\Sigma\Delta$ Ms

- ◆ Every state variable and DAC output must be connected to the integrator input of the ulterior stages in the cascade [Ortm01]
- ◆ Increases the number of analog components (transconductors and amplifiers)



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CT- $\Sigma\Delta$ Ms: Synthesis Methods

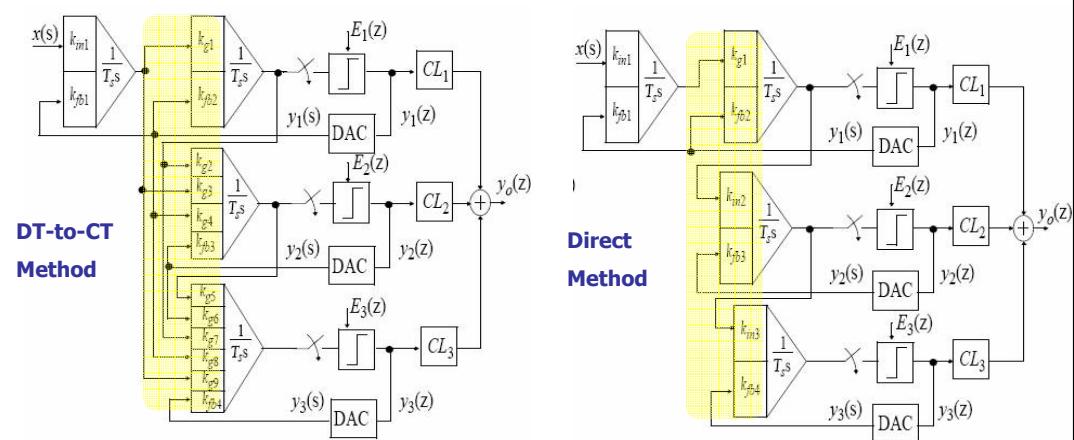


□ Direct synthesis method [Bree01]

- ◆ Uses the desired NTF as a starting point, (as for the DT case)
- ◆ An Inverse Chevichev distribution of the NTF zeros has advantages in terms of SNR and stability

□ Application to cascade architectures [Tort06]

- ◆ Optimum placement of poles/zeroses of the NTF
- ◆ Synthesis of both analog and digital part of the cascade CT $\Sigma\Delta$ Modulator
- ◆ Reduced number number of analog components



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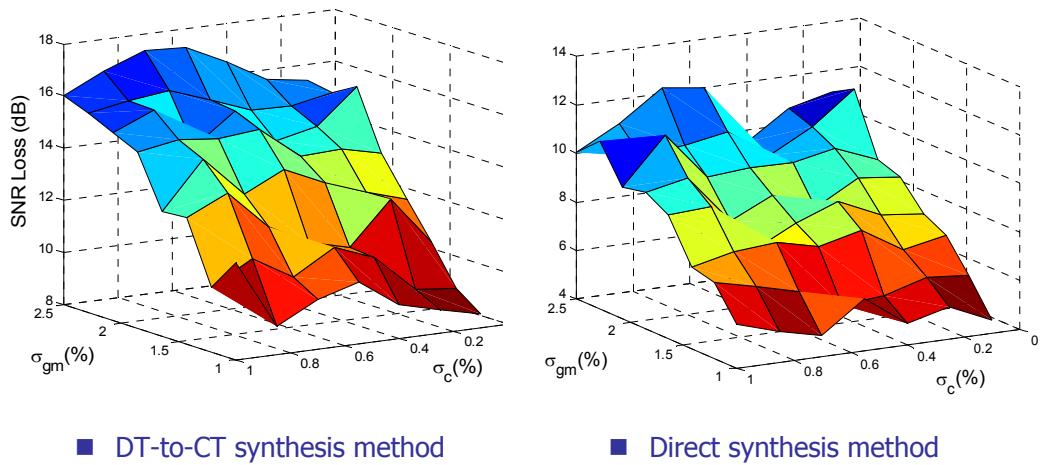
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



□ Direct synthesis of cascade architectures (I) [Tort06]

- ◆ Sensitivity to mismatch (gm , C)
- ◆ A 2-1-1 example



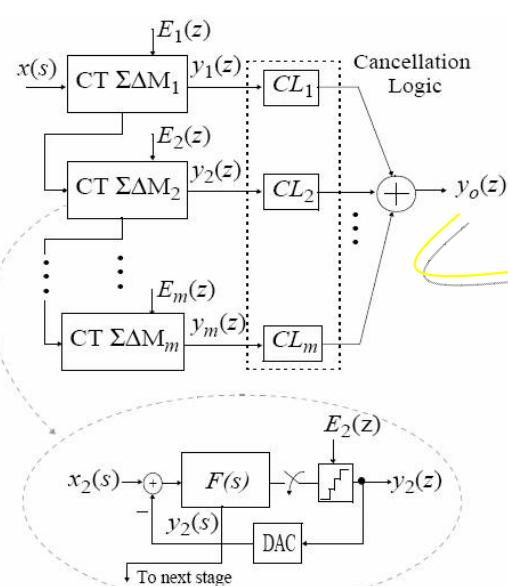
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



□ Direct synthesis of cascade architectures (II) [Tort06]



$$y_o(z) = \sum_{k=1}^m y_k(z) CL_k(z)$$

$$E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)$$

$$y_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{kk}}$$

$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}}$$

$$\left[Z_{km} \equiv Z \left(L^{-1}(H_D F_{km}) \Big|_{n T_s} \right) \right]$$

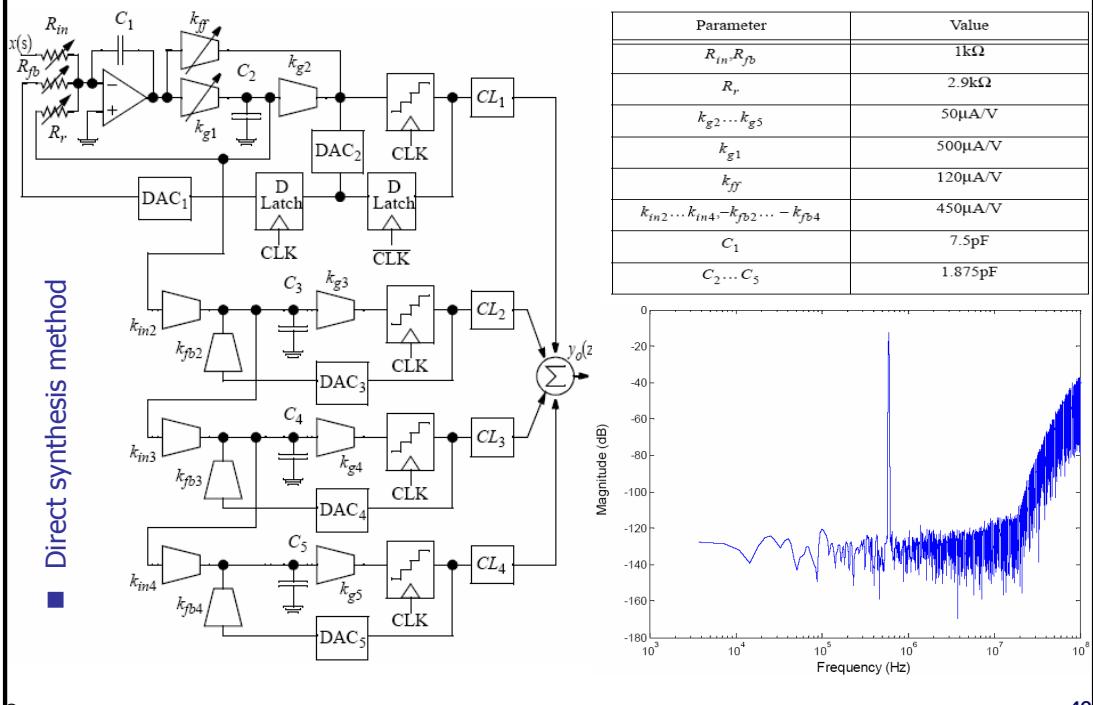
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



□ A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT $\Sigma\Delta$ M for VDSL [Tort06]



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CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Advanced Architectures and State of the Art

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KTH, Stockholm, April 23-27

OUTLINE



1. State of the Art on SC $\Sigma\Delta$ ADCs

2. State of the Art on CT $\Sigma\Delta$ ADCs

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Single-loop Single-bit $\Sigma\Delta$ ICs

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ³
[Kero94]	21.00	8.00E+02	320	4th-ord	3um MS / 10V	2.50E-02	14.90	351.28
[Kash99]	20.00	8.00E+02	320	4th-ord	0.6um MS / 5V	1.60E-02	19.07	137.22
[Wang03]	18.50	4.80E+04	--	6th-ord	0.35um MS / 5V-3.3V	2.30E-01	12.93	71.59
[Yama94]	18.00	2.00E+01	1600	4th-ord	1.2um MS / 5V	1.30E-03	247.96	2.64
[Brid04]	17.20	8.00E+02	320	4th-ord	0.6um MS (2P) / 5V	5.00E-02	415.11	0.91
[Brid02]	17.10	8.00E+02	320	4th-ord	0.6um MS / 5V	5.00E-02	444.90	0.79
[Snoe01]	16.70	2.20E+04	64	4th-ord	0.5um MS / 2.5V	2.50E-03	1.07	248.96
[Mede97]	16.40	9.60E+03	256	2nd-ord	0.7um STD / 5V	1.71E-03	2.06	104.79
[Coba99]	16.00	4.00E+04	64	4th-ord	0.5um STD / 1.5V	1.00E-03	0.38	428.81
[Bran91b]	16.00	5.00E+04	256	2nd-ord	1um MS / 5V	1.38E-02	4.21	38.84
[Grilo96]	15.30	7.00E+03	286	2nd-ord	0.6um STD / 1.8V	2.00E-03	7.08	14.22
[Mau00]	15.30	5.00E+05	64	5th-ord	0.6um STD / 5V	2.10E-01	10.41	9.67
[Rom03]	15.30	5.00E+05	96	5th-ord	0.8um STD / 3.3V	4.30E-02	2.13	47.24
[Bose88]	14.50	1.60E+04	256	2nd-ord	3um MS / 5V	1.20E-02	32.37	1.79
[Yao04]	14.40	4.00E+04	100	3rd-ord	0.18um STD / 1.5V	1.20E-04	0.45	259.04
[Dess01]	14.40	5.00E+04	100	3rd-ord	0.35um MS / 5V	1.20E-04	0.45	259.04
[Klem06]	14.37	2.70E+05	48	4th-ord	0.18um STD / 1.5V	1.20E-04	0.45	259.04
[Send97]	14.30	6.00E+03	128	2nd-ord	0.5um STD / 5V	1.20E-04	0.45	259.04
[Burn96]	14.20	1.95E+04	256	2nd-ord	0.2um MS / 5V	1.20E-04	0.45	259.04
[Bur01]	14.00	4.00E+04	192	3rd-ord (IF-to-BB)	0.25um STD / 5V	1.20E-04	0.45	259.04
[Nade94]	13.80	2.00E+03	250	3rd-ord	0.18um STD / 1.5V	1.20E-04	0.45	259.04
[Goes06]	13.50	2.00E+04	256	2nd-ord	0.18um MS / 5V	1.20E-04	0.45	259.04
[Opt91]	13.50	5.00E+05	64	4th-ord (DFB)	1.5um STD / 5V	1.20E-04	0.45	259.04
[Than97]	13.40	1.95E+05	128	2nd-ord	1.2um STD / 5V	1.20E-04	0.45	259.04
[Chen03]	13.10	2.00E+05	520	2nd-ord	0.13um STD / 5V	1.20E-04	0.45	259.04
[Till01]	13.00	1.60E+04	64	2nd-ord	0.25um STD / 5V	1.20E-04	0.45	259.04
[Sauv03]	13.00	1.60E+04	64	2nd-ord (SO)	0.18um MS (MM) / 0.65V	4.55E-05	0.35	58.90
[Bal02]	13.00	2.20E+04	64	4th-ord	0.5um MS / 1.8V	1.70E-03	9.43	2.17
[Kesk02]	13.00	4.00E+04	256	2nd-ord (RO)	0.35um MS (2P) / 1V	5.60E-03	17.09	1.20
[Pelu98]	12.50	3.20E+04	48	3rd-ord	0.5um STD / 0.9V	4.00E-05	0.22	67.00
[Shim05]	12.37	4.00E+05	16	3rd-ord	0.18um / 1.8V	4.00E-03	1.89	6.99
[Sauv02]	12.20	1.60E+04	64	2nd-ord (SO)	0.18um STD / 0.7V	8.00E-05	1.06	11.05
[Pelu97]	12.00	6.80E+03	74	2nd-ord	0.7um STD / 1.5V	1.01E-04	3.63	2.82
[Au97]	12.00	1.60E+04	64	3rd-ord	1.2um MS / 2V	3.40E-04	5.19	1.97
[Kesk02]	12.00	1.00E+05	102.4	2nd-ord (RO)	0.35um MS (2P) / 1V	5.60E-03	13.67	0.75
[Sauv03]	11.00	3.20E+04	32	2nd-ord (SO)	0.18um MS (MM) / 0.65V	4.55E-05	0.69	7.36
[Chen03]	9.90	1.00E+06	104	2nd-ord	0.13um STD / 1.5V	1.28E-03	1.33	1.79
[Shim05]	8.87	1.00E+07	8	3rd-ord	0.18um / 1.8V	4.00E-03	0.85	1.37
[Burd01]	8.70	7.68E+06	24	3rd-ord (IF-to-BB)	0.25um STD / 2.5V	1.35E-02	4.23	0.25
[Gero03]	8.50	5.00E+02	16	3rd-ord (SWO, LR)	0.8um MS (2P) / 1.8V	2.20E-06	12.15	0.07
[Wismar06]	8.35	4.00E+04	85	1st-order	90nm STD / 0.2V	4.40E-07	0.03	24.01
[Chen03]	8.10	2.00E+06	52	2nd-ord	0.13um STD / 1.5V	1.28E-03	2.32	0.29

- 2nd-order loop ~ 40%
- 3rd-order loop ~ 20%
- 4th-order loop ~ 30%

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Single-loop Multi-bit $\Sigma\Delta$ ICs

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ³
[Bair96]	13.66	5.00E+05	16	4th-ord(4b)	1.2um MS / 5V	5.80E-02	8.96	3.61
[Chen95]	15.65	4.00E+04	64	2nd-ord(3b)	1.2um MS / 5V	6.75E-02	32.82	3.91
[Geer00]	15.80	2.50E+06	24	3rd-ord(4b)	0.65um MS / 5V	2.95E-01	2.07	68.85
[Geer00]	12.00	1.25E+07	24	3rd-ord(4b)	0.65um MS / 5V	3.80E-01	7.42	1.38
[Harr94]	16.00	3.90E+04	128	3rd-ord(1b, 5b) (dual)	2um MS (2P) / 5V	8.50E-02	33.26	4.92
[Leun97]	19.30	9.60E+04	64	7th-ord(1.5b)	0.8um MS / 5V	7.60E-01	12.26	131.36
[Nys97]	19.00	8.00E+02	512	2nd-ord(3b)	2um MS / 5V	2.18E-03	5.19	252.36
[Fras04]	18.04	4.00E+04	153.6	5th-ord (17level)	0.35um MS / 5V	3.00E-01	27.83	24.17
[Yang03]	18.70	4.00E+04	128	5th-ord(17level)	0.35um MS (2P) / 5V-3.3V	6.80E-02	3.99	266.27
[Lei01]	15.99	4.80E+04	128	3rd-order(10level)	0.25um / 5V	1.25E-02	4.01	40.41
[Fool00]	16.22	4.80E+04	64	2nd-ord(5b)	0.5um STD / 3.3V	6.86E-02	18.72	10.18
[Grilo02]	16.70	4.00E+04	64	2nd-ord(5b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	13.00	1.00E+06	32	2nd-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	13.50	4.00E+05	57.5	2nd-ord(6b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	12.83	1.25E+06	18	2nd-ord(6b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	11.67	3.84E+06	12	2nd-ord(6b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Joha03]	16.00	9.00E+01	512	1st-ord (3b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Kuo02]	13.70	1.25E+06	12	4th-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Kuo02]	13.00	2.00E+06	12	4th-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Reut02]	14.00	2.50E+06	32	5th-ord(1.5b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Balm04]	13.70	2.50E+07	8	4th-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Gagg03]	13.80	6.00E+05	96	2nd-ord (3b)	0.13um MS / 1.5V	8.00E-03	1.26	41.96
[Jiang02]	13.80	4.00E+06	8	5th-ord(4b)	0.13um MS / 1.5V	7.00E-03	0.60	43.96
[Kwon06]	14.00	4.40E+06	32.7	2nd-ord (4b)	0.13um MS / 1.5V	2.40E-03	0.82	22.07
[Lee06]	13.90	2.20E+06	60	2nd-ord (5level)	0.13um MS / 1.5V	2.90E-03	2.81	0.23
[Fuji06]	12.75	6.40E+06	12.5	4th-ord(4b) 2S	0.13um MS / 1.5V	3.44E-02	1.18	7.69
[Fuji06]	11.83	8.00E+06	12.5	4th-ord(4b) 2S	0.18um MS / 1.8V	3.44E-02	1.18	7.69
[Gagg04]	14.37	3.00E+05	350	2nd-ord (3b)	0.13um MS / 1.5V	8.00E-03	1.26	41.96
[Gagg04]	13.37	1.10E+06	47	2nd-ord (3b)	0.13um MS / 1.5V	7.00E-03	0.60	43.96
[Gomez02]	12.83	4.00E+05	65	2nd-ord(5b)	0.13um STD / 1.5V	2.40E-03	0.82	22.07
[Gomez02]	8.01	4.00E+06	12	2nd-ord(5b)	0.13um STD / 1.5V	2.90E-03	2.81	0.23
[Yu05]	9.37	4.00E+06	10	2nd-ord(4b-dual)	90nm STD / 1.3V	2.10E-03	0.79	2.08
[Yu05]	10.70	2.00E+06	20	2nd-ord(4b-dual)	90nm STD / 1.3V	2.10E-03	0.63	6.58
[Yu05b]	12.50	4.00E+05	50	2nd-ord(4b-dual)	90nm STD / 1.3V	2.10E-03	0.91	15.95
[Gomez02]	12.00	4.00E+05	65	2nd-ord(5b)	0.13um STD / 1.2V	1.40E-03	0.85	11.96
[Koh05]	10.70	3.88E+06	19.79	2nd-ord(5level)	90nm STD / 1.2V	1.20E-03	0.19	22.33

Multi-bit resolution:

- 3 or 4 bits ~ 70%

Loop order:

- 2nd-order ~ 50%
- + 2nd-order loop ~ 50% (easier to stabilize w/ multi-bit)

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Cascade Single-bit $\Sigma\Delta$ ICs

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁵
[Yoon98]	15.30	6.40E+04	16	2-1-1-2	2um MS / 6.6V	7.90E-02	30.60	3.29
[Fui97]	18.15	4.80E+04	128	2-2	0.7um MS / 5V	5.00E-01	35.91	20.17
[Marg98a]	14.80	2.00E+06	24	2-1-1	1um MS / 5V	2.30E-01	4.03	17.66
[Miac98]	14.82	5.00E+04	64	2-2	3um MS / 5V	7.40E-02	51.03	1.42
[Rebe90]	15.00	1.80E+05	64	1-1-1	1.5um MS / 5V	7.60E-02	12.89	6.35
[Kito94]	16.15	4.40E+04	64	2-2	1.2um BiCMOS / 5V	1.02E-01	31.82	5.72
[Wang01]	18.10	2.50E+04	64	2-2	0.6um MS / 5V	7.50E-02	10.68	65.68
[Will94]	17.00	5.00E+04	128	2-1	1um MS / 5V	4.70E-02	7.17	45.62
[Yin93]	15.70	3.20E+05	64	2-1	1.2um STD / 5V	6.50E-02	3.82	34.82
[Yin94]	15.82	1.50E+06	64	2-1-1	2um BiCMOS / 5V	1.80E-01	2.07	69.61
[David03]	13.00	1.00E+03	256	2-1	1.5um MS / 5V	---	---	---
[Geer99]	15.00	2.20E+06	24	2-1-1	0.5um MS / 3.3V	2.00E-01	2.77	29.48
[Mor00]	14.00	2.20E+06	24	2-2-2	0.35um MS / 3.3V	1.50E-01	4.16	9.83
[Gome00]	16.65	4.40E+04	128	2-1	0.6um MS / 3V	2.20E-02	4.86	52.88
[Lee03]	14.16	1.00E+06	64	2-2	0.35um MS (2P) / 1.8V-2.4V	1.50E-01	8.20	5.57
[Lee03]	12.00	2.00E+06	32	2-2	0.35um MS (2P) / 1.8V	1.50E-01	18.31	0.56
[Olia02]	13.50	3.60E+05	36	2.2	0.4um MS / 1.8V	5.00E-03	1.20	24.12
[Rabi97]	16.10	5.00E+04	80	2-1	0.8um MS / 1.8V	2.50E-03	0.71	246.29
[Saue03]	13.00	1.60E+04	64	2-1	0.18um MS (MiM) / 0.65V	6.18E-05	0.47	43.37
[Saue03]	12.17	3.20E+04	32	2-1	0.18um MS (MiM) / 0.65V	6.18E-05	0.42	27.45
[Ahn05b]	12.70	4.80E+04	64	2-2 (switched-RC int.)	0.35um MS / 0.6V	1.00E-03	3.13	5.30

Most-common cascades:

- 2-1 → 3rd order, 2 stage
- 2-2 → 4th order, 2 stage
- 2-1-1 → 4th order, 3 stage

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Cascade Multi-bit $\Sigma\Delta$ ICs

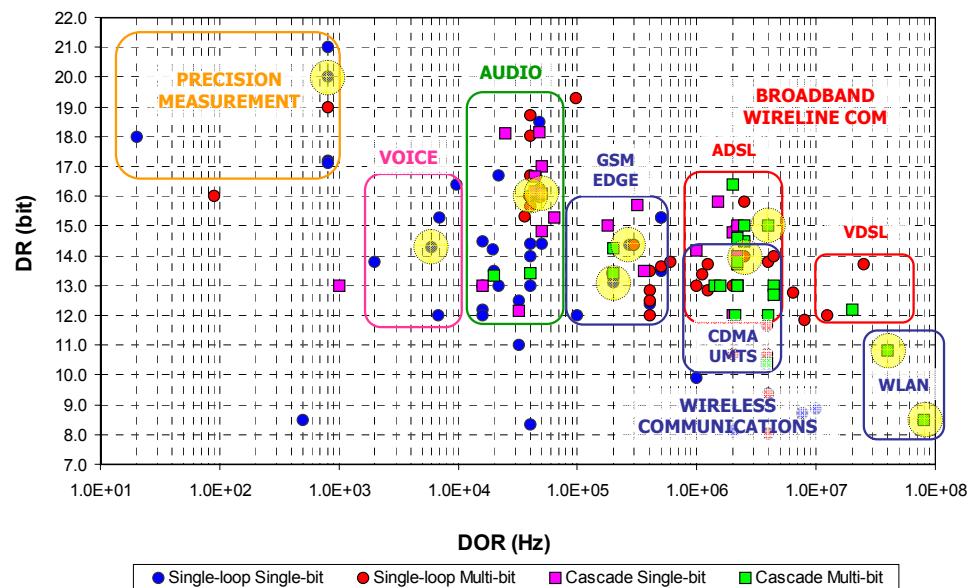
Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁵
[Broo97]	14.50	2.50E+06	8	2-0(5b)	0.6um MS / 5V	5.50E-01	9.49	6.09
[Bran91a]	12.00	2.10E+06	24	2-1(3b)	1um STD / 5V	4.10E-02	4.77	2.14
[Mede99]	13.00	2.20E+06	16	2-1-1(3b)	0.7um STD / 5V	5.50E-02	3.05	6.70
[Fui90]	15.00	2.50E+06	8	2(4b)-1(4b)-1(4b)	0.5um MS / 5V	1.05E-01	1.28	63.81
[Dedi94]	14.25	2.00E+05	16	2(1.5b)-2(1.5b)-2(1.5b)	1.2um MS / 5V	4.00E-02	10.26	4.74
[Mor00]	13.00	2.20E+06	24	2-2(5b)	0.35um MS / 3.3V	9.90E-02	5.49	3.72
[Gupta02]	14.60	2.20E+06	29	2-1-1(2b)	0.35um STD / 3.3V	1.80E-01	3.29	18.81
[Feld98]	13.00	1.40E+06	16	2-2-2(1.5b)	0.7um MS / 3.3V	8.10E-02	7.06	2.90
[Rio01b]	13.00	2.20E+06	16	2-1-1(4b)	0.35um STD / 3.3V	7.37E-02	4.09	5.00
[Rio01b]	12.00	4.00E+06	16	2-1-1(4b)	0.35um STD / 3.3V	7.83E-02	4.78	2.14
[Bosi05]	12.20	2.00E+07	4	2(4b)-pipeline(9b)	0.18um MS/ 3.3V-1.8V	2.40E-01	2.55	4.60
[Lamp01]	13.00	1.56E+06	32	2-2(3b)	0.35um MS / 2.5V	5.00E-02	3.91	5.23
[Rio02b]	13.70	2.20E+06	32	2-1-1(3b)	0.25um STD / 2.5V	7.17E-02	2.45	13.56
[Rio02b]	13.00	4.40E+06	16	2-1-1(3b)	0.25um STD / 2.5V	7.17E-02	1.99	10.28
[Vieu01]	15.00	4.00E+06	16	2(5b)-(2b)-1(3b)	0.5um MS / 2.5V	1.50E-01	1.14	71.47
[Rio03]	13.80	2.20E+06	32	2-1-1(3b)	0.25um MS (MiM) / 2.5V	6.58E-02	2.10	16.98
[Rio03]	12.70	4.40E+06	16	2-1-1(3b)	0.25um MS (MiM) / 2.5V	6.58E-02	2.25	7.39
[Para06]	10.8	4.00E+07	8	2-2 (4b)	90nm STD / 1.4V	7.80E-02	1.09	4.07
[Taba03]	8.50	8.00E+07	4	2(LP1.5b)-2(BP4b)	0.13um MS / 1.2V	1.75E-01	6.04	0.15
[Dezz03]	13.40	2.00E+05	195	2-1 (5-level)	0.13um MS / 1.2V	2.40E-03	1.11	24.30
[Dezz03]	10.40	3.84E+06	100	2-1 (5-level)	0.13um MS / 1.2V	4.30E-03	0.83	4.07
[Reve03]	13.33	2.00E+04	64	2-1(1.5b) (2S)	0.35um MS (2P, low-Vt) / 0.8V	6.00E-05	0.29	88.09
[Ahn05]	13.40	4.00E+04	64	2-2(1.5b)	0.35um MS / 0.6V	1.00E-03	2.31	11.67
[Brew05]	16.40	2.00E+06	8	2-2-0(dual)	0.25um MS (2P) / ?V	4.75E-01	2.75	78.59

Multi-bit quantization is mostly used in the last modulator stage

DT-LP- $\Sigma\Delta$ Ms: State of the Art



DT LPSDMs organized per architecture

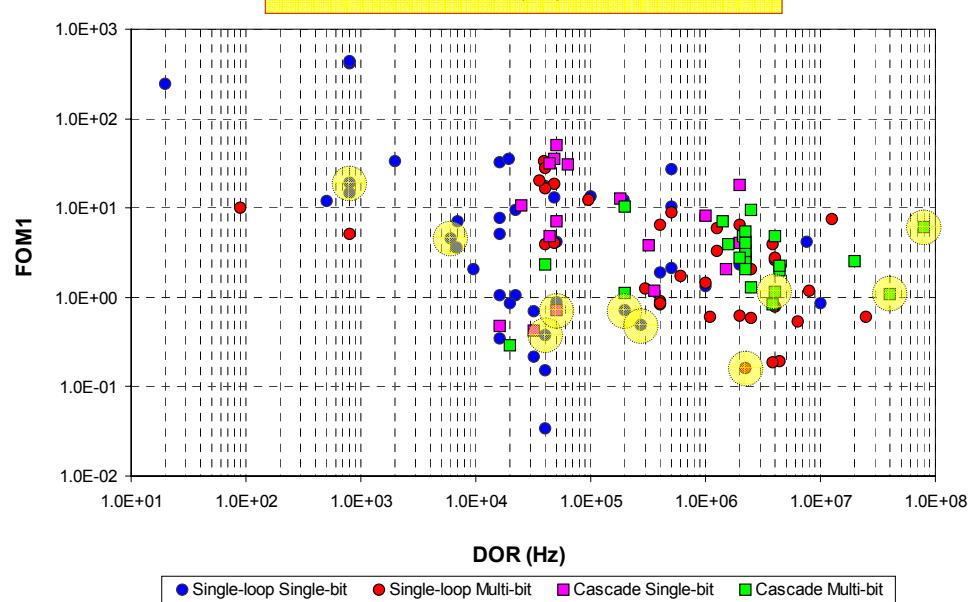


DT-LP- $\Sigma\Delta$ Ms: State of the Art



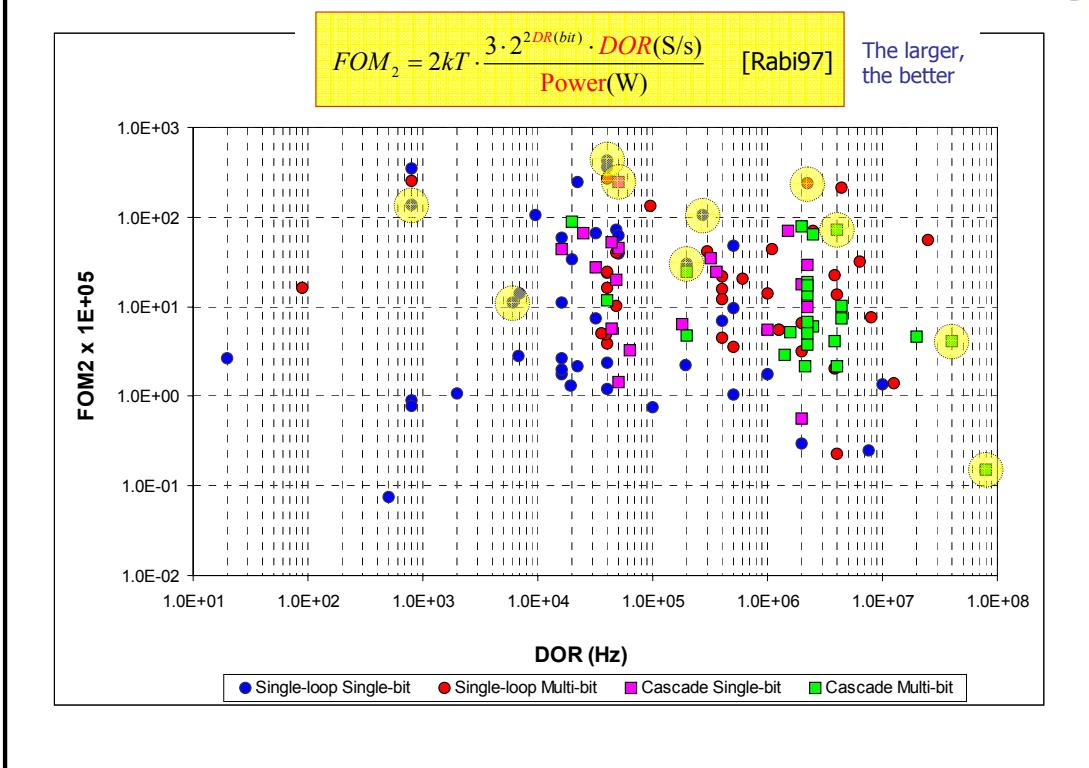
$$FOM_1 = \frac{\text{Power}(W)}{2^{\text{DR}(\text{bit})} \cdot \text{DOR}(\text{s/s})} \times 10^{12} \quad [\text{Good96}]$$

The lower, the better



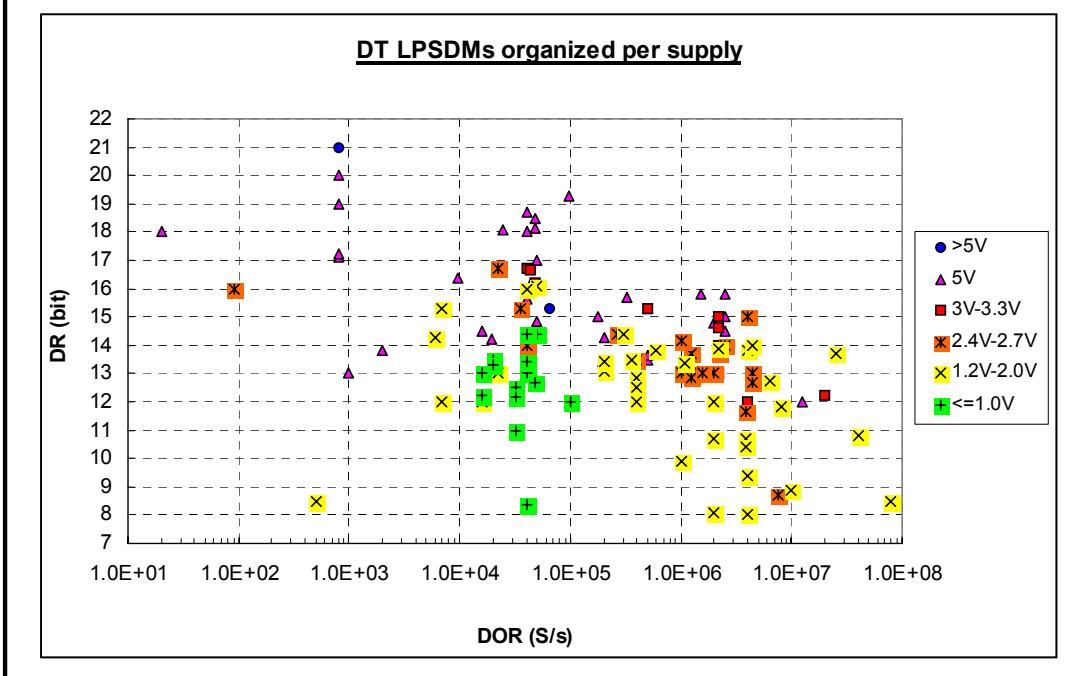
DT-LP- $\Sigma\Delta$ Ms: State of the Art

CNMC



DT-LP- $\Sigma\Delta$ Ms: State of the Art

CNMC

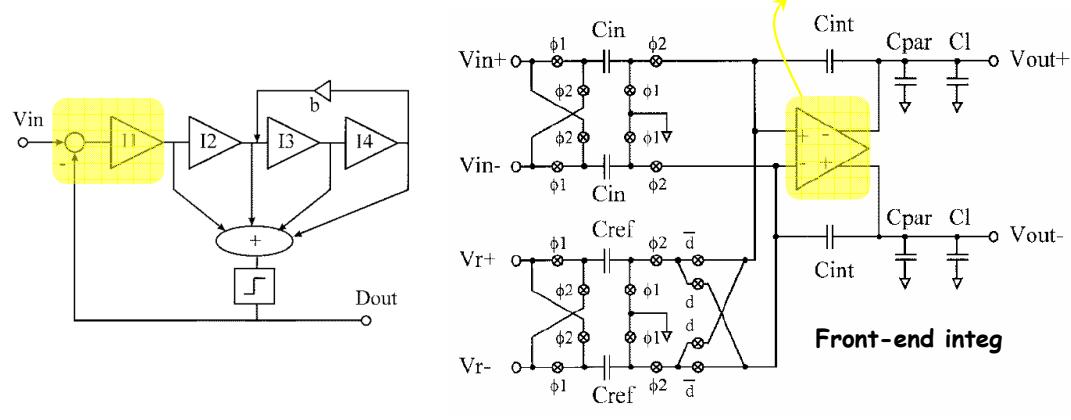
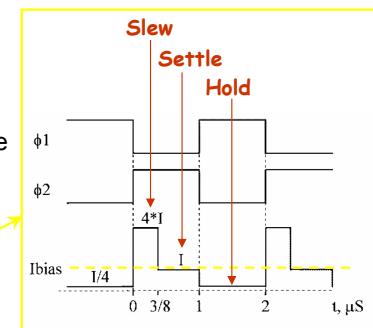


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Precision Apps



Digitization of seismic signals [Kash99]

- Fourth-order feedforward summation architecture
 - Resonation around the two last integrators
 - Chopper at the front-end in order to reduce 1/f noise
- Dynamic biasing of 1st amplifier** for power saving
- 0.6 μ m CMOS tech (2P)
- 122-dB DR within 400Hz bandwidth
- 256kHz sampling rate (OSR=320)
- 16mW, 5V

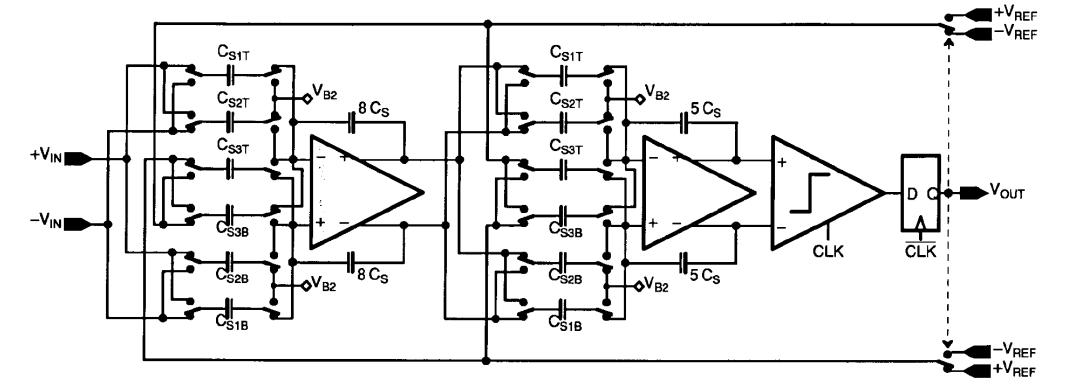
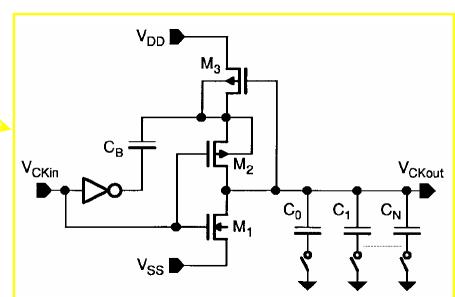


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Voice codecs



Voice-band conversion [Send97]

- Second-order loop
 - Double-sampling \rightarrow 2x effective OSR**
 - Modified NTF
 - Bootstrapped switches
- 0.5 μ m CMOS tech (2P2M)
- 88dB DR within 3kHz bandwidth
- 1MHz clock rate (2MHz effective sampling)
- 0.55mW, 1.5V

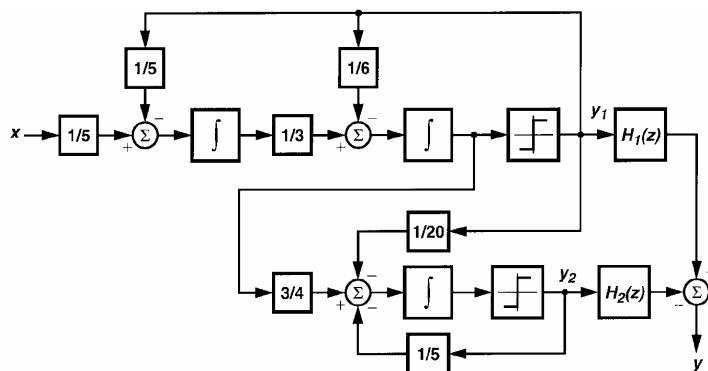
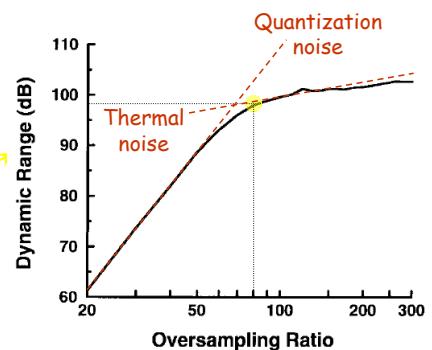


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Audio codecs



☐ Audio conversion [Rabi97]

- ◆ 2-1 cascade topology
- ◆ Resolution limited by kT/C noise
- ◆ Rail-to-rail operation
- ◆ Two-stage class A/AB amplifiers
- ◆ Bootstrapping of switches
- ◆ 0.8 μ m CMOS tech (1P3M)
- ◆ 99dB DR within 25kHz bandwidth
- ◆ 4MHz sampling rate (OSR=80)
- ◆ 2.5mW, 1.8V

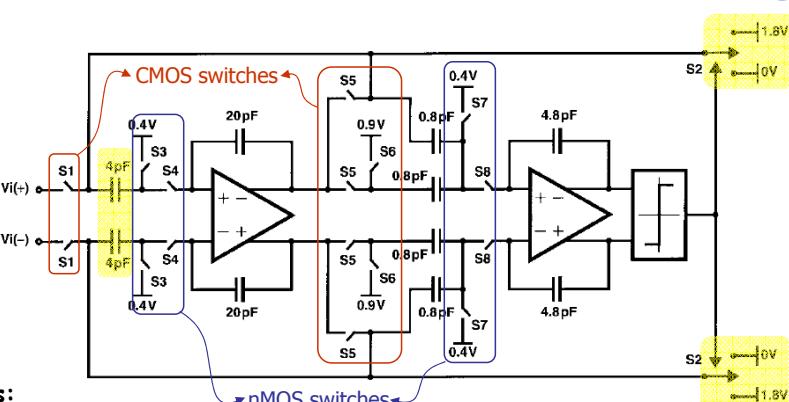


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Audio codecs



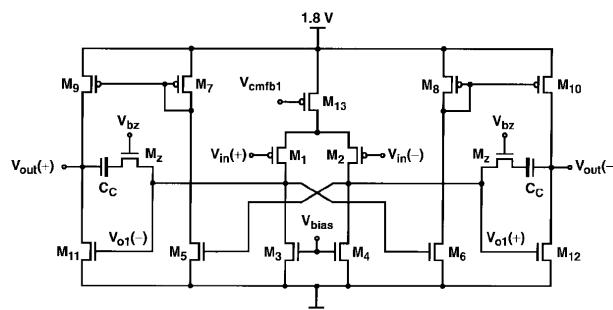
First modulator stage:

- Low input common-mode voltage (400mV)
- CMOS switches only required for sampling large swing signals

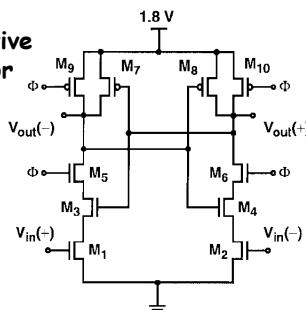


Class A/AB amplifiers:

- 1/f noise relies on pMOS input sizing

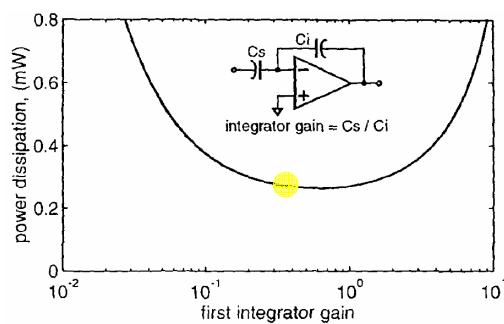
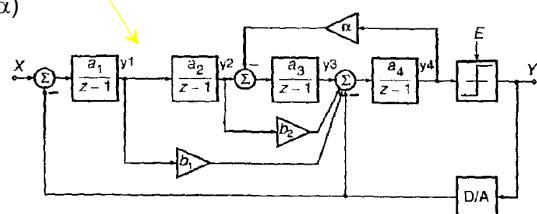


Regenerative comparator



□ Audio conversion [Coba99]

- ◆ Fourth-order single-loop mixed topology
 - Feedforward and feedback paths
 - Resonation around two last integrals (α)
- ◆ Capacitor sizing:
 - Input cap based on kT/C noise
 - Remaining caps based on matching
- ◆ Bootstrapping of switches
- ◆ 0.5 μ m CMOS tech (1P3M)
- ◆ 98.2dB DR within 20kHz bandwidth
- ◆ 2.8MHz sampling rate (OSR=64)
- ◆ 1mW, 1.5V

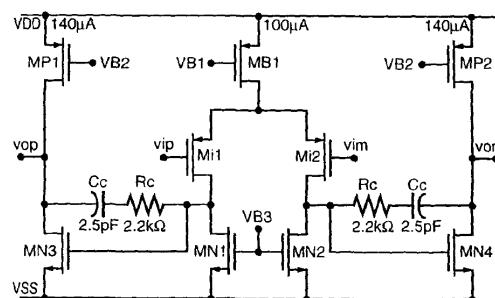


Power dissipation issues:

- 1st-integ gain is fixed to 1/3
- Clock duty-cycle is not 50%:
More time for integration (larger Ceq)
- 1st-integ consumes 72% of power
- Aggressive cap scaling in rest of integs

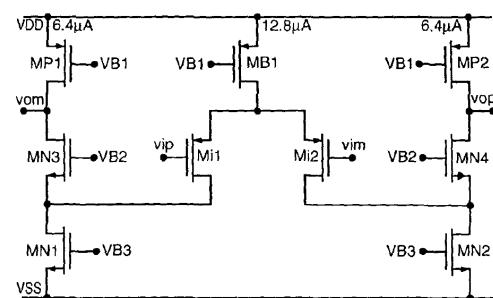
◆ 1st integrator

- Two-stage Miller amplifier
- pMOS input pair with non-minimal lengths to reduce 1/f noise
- Large DC gain



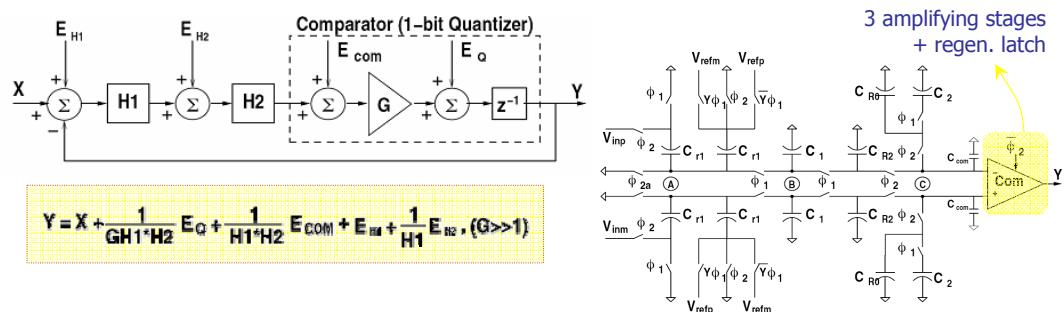
◆ 2nd to 4th integrators

- Folded-cascode amps
- 55-dB DC gain



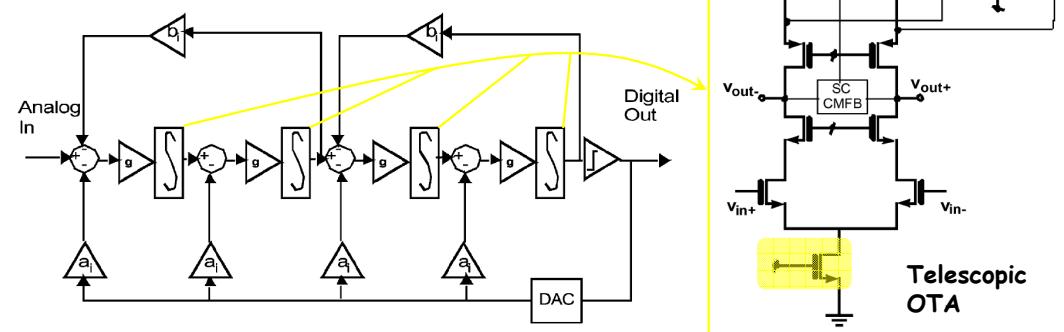
Wireless communications, GSM/BT/WCDMA [Chen03]

- ◆ **Passive 2nd-order modulator → w/o amplifiers**
 - Capacitive voltage dividers reduce the input range
 - Loading effects between passive stages
- ◆ Functionality critically relies in the comparator
 - $H_1 \cdot H_2$ is limited to unity at DC (passive)
 - Eq suppressed within baseband by comparator gain
 - Noise from comparator adds to the input signal
- ◆ 80.5/61.5/50.3dB DR within 0.1/1/2MHz BW
- ◆ 1.3mW, 1.5V, 0.13μm CMOS tech
 - Switching power dominates (104MHz clock)
 - 30% from comparator DC biasing



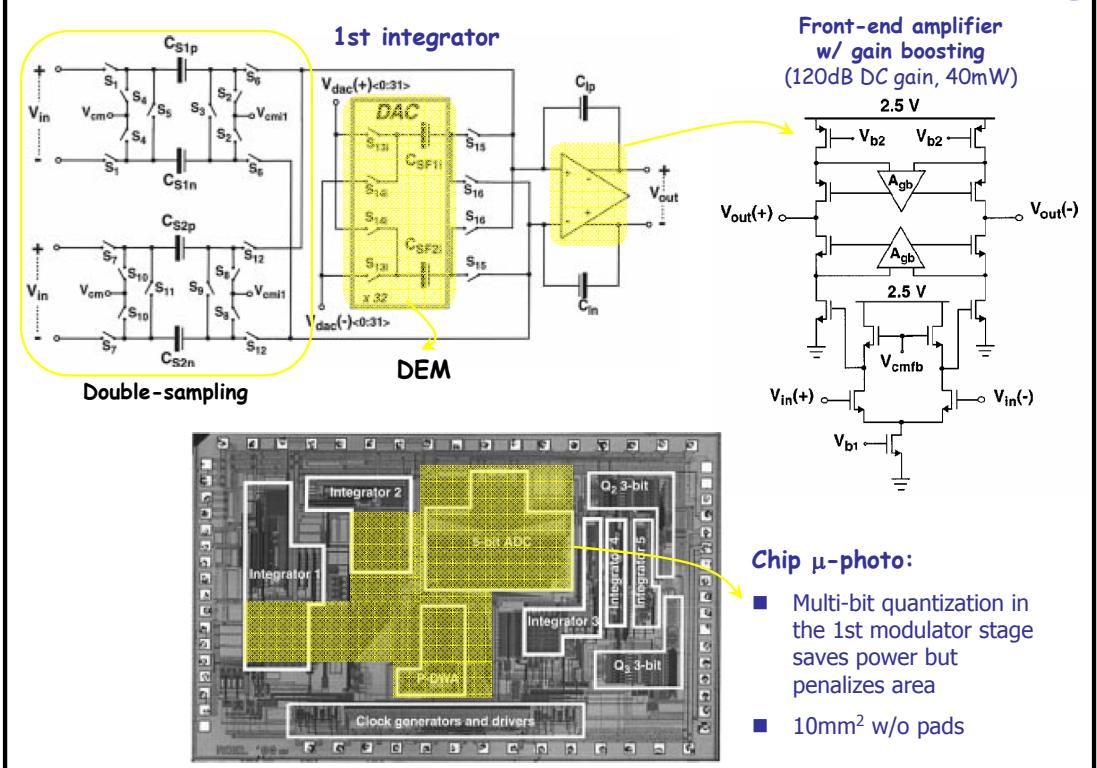
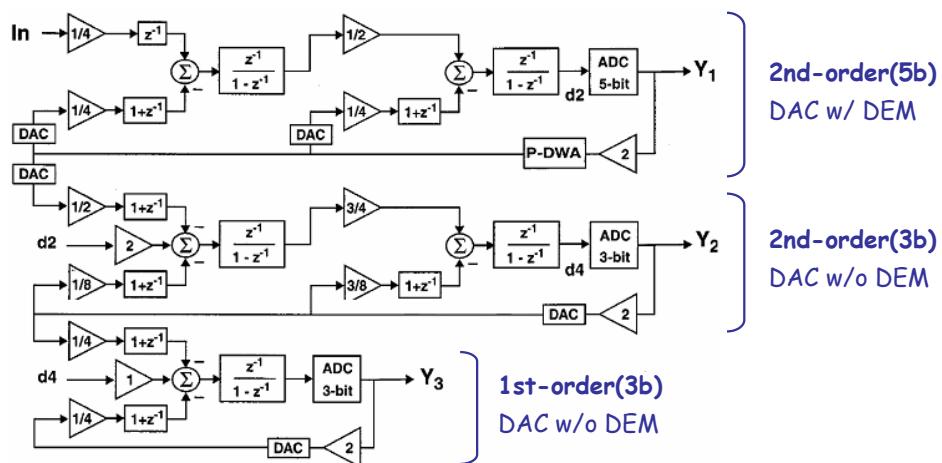
Wireless communications, GSM/GPRS/EDGE [Klem06]

- ◆ Fourth-order distributed feedback topology
 - Inverse Chebyshev approximation
 - NTF w/ two optimized zeros (b_1)
- ◆ Single-stage amplifiers:
 - Telescopic OTAs w/ dynamic biasing
 - Constant slew-rate for power saving under process variations
- ◆ Capacitor scaling → 8:2:1:1 (20pF integrating cap at input)
- ◆ 0.25μm CMOS tech
- ◆ 88dB DR within 270kHz bandwidth
- ◆ 26MHz sampling rate (OSR=48)
- ◆ 2.8mW, 2.7V



Broadband communications, ADSL [Vleu01]

- ◆ 2-2-1 cascade topology w/ multi-bit quantization
 - Limited by K/T/C noise → Multi-bit quantization in all stages to reduce noise leakage
 - Linearization of 1st-stage DAC → partitioned DWA (DEM)
 - Double-sampling [Send97] → OSR=2x8
- ◆ 150mW, 2.5V, 0.5μm CMOS tech (2P3M)
- ◆ 32MHz clock rate (64MHz effective sampling)
- ◆ 95dB DR within 2MHz bandwidth

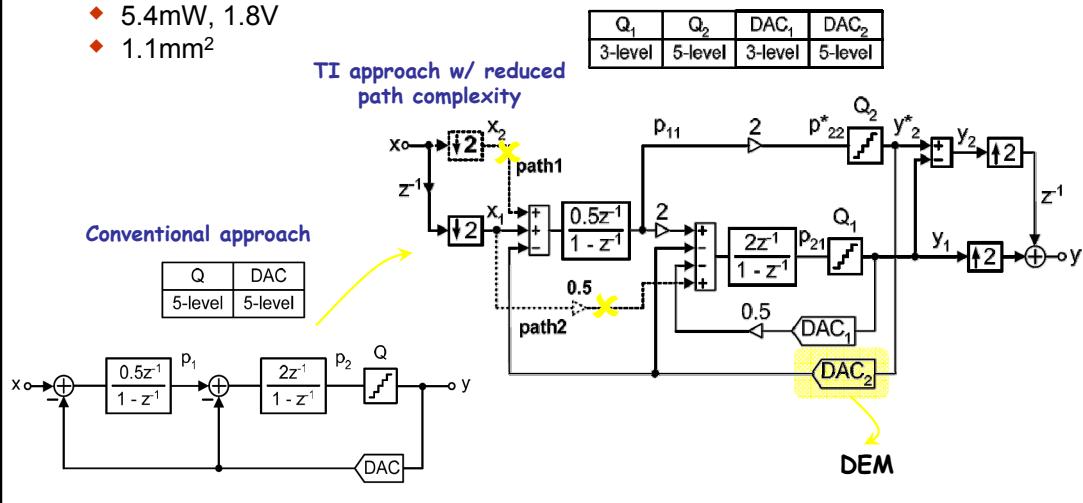


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Broadband com



Broadband communications, ADSL [Lee06]

- 2nd-order topology w/ multi-bit quantization
- 2 channels w/ time interleaving**, but only 2 opamps \rightarrow Reduced complexity
- Linearization of 5-level feedback to 1st integ \rightarrow ILA (DEM)
- 0.18 μ m CMOS tech (MiM caps)
- 66MHz clock rate (132MHz effective sampling, OSR=60)
- 85dB DR within 1.1MHz bandwidth
- 5.4mW, 1.8V
- 1.1mm²

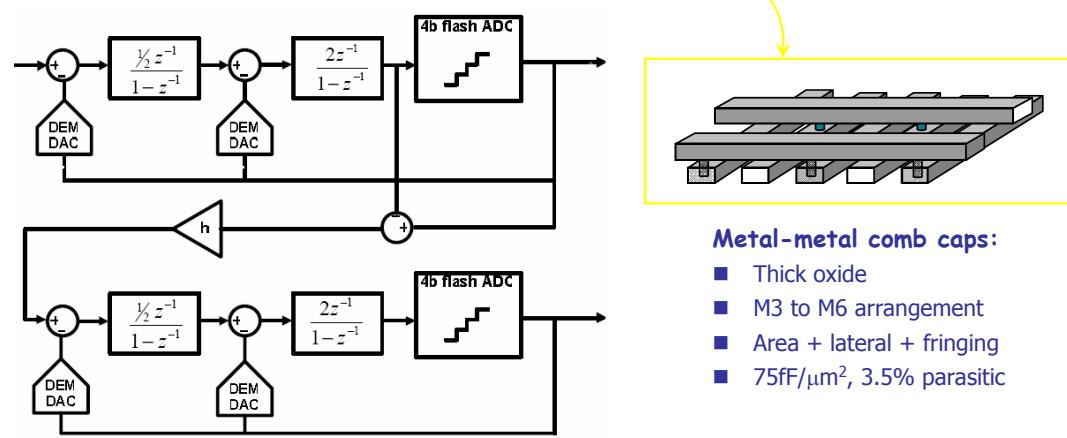


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Wireless com



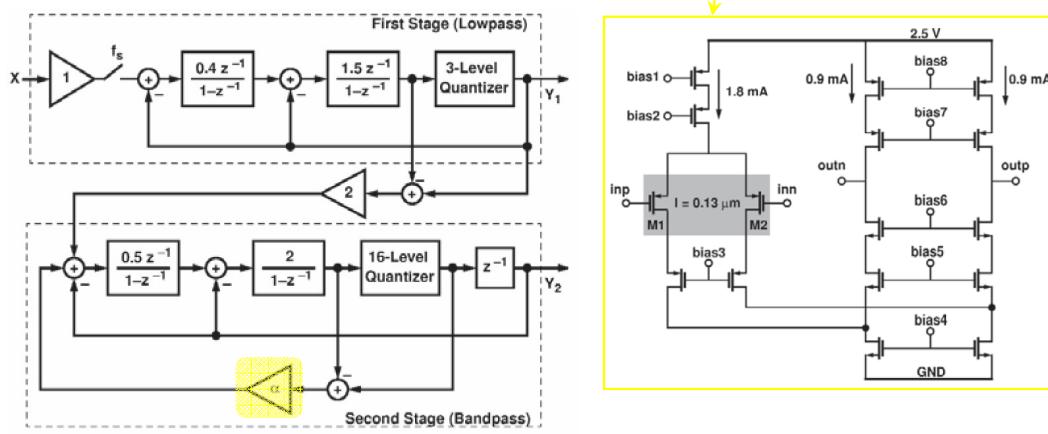
Wireless communications, WLAN [Para06]

- 2-2 cascade topology with 4-bit internal quantizers
 - Linearization of all multi-bit DACs \rightarrow rotational DWA (DEM)
- Two-stage amplifiers \rightarrow pMOS telescopic + nMOS common-source stage
- 90nm CMOS tech (1P7M) \rightarrow metal-metal caps
- 330MHz sampling rate \rightarrow OSR=8
- 67dB DR within **20MHz bandwidth**
- 78mW, 1.4V



Wireless communications, WLAN [Taba03]

- Fourth-order multi-bit cascade topology
 - 1st stage: 2nd-order LP (1.5b)
 - 2nd stage: 2nd-order BP (4b) → local resonance (α) and DAC w/o DEM
- 0.13 μ m 1.2V CMOS tech (1P6M) → 0.25 μ m 2.5V I/O MOST, MiM caps
- Folded-cascode amplifiers with 0.13 μ m input pMOS for fast settling
- 160MHz sampling rate → OSR=4!
- 53dB DR within 40MHz bandwidth
- 175mW power consumption



Band-Pass $\Sigma\Delta$ M ICs

Based on $z^1 \rightarrow -z^2$ transformation

Author	DR (bit)	fs (Hz)	fn (Hz)	Bw (Hz)	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁶
[Cor97]	9.5	1.25E+06	2.50E+05	6.25E+03	4th-ord	2um MS / 5V	---	---	---
[Long93]	15	7.20E+06	1.80E+06	3.00E+04	4th-ord	1um MS / 5V	---	---	---
[Rosa00]	11.5	6.52E+06	1.63E+06	1.00E+04	4th-ord	0.8um STD / 5V	6.00E-02	12.67	5.71
[Baza98]	6.7	4.00E+07	2.00E+07	1.25E+06	2nd-ord	0.5um MS / 5V	6.50E-02	30.31	0.09
[Park99]	12.2	2.00E+07	5.00E+06	2.00E+05	4th-ord	0.65um STD / 4V	1.80E-01	7.50	15.66
[Song95]	9	8.00E+06	2.00E+06	3.00E+04	4th-ord	2um MS / 3.3V	8.00E-04	0.78	16.48
[Andr96]	8	8.00E+06	2.00E+06	6.40E+04	6th-ord	0.5um MS (2P) / 3.3V	8.00E-03	15.38	0.42
[Haire96]	11.7	1.30E+07	3.25E+06	2.00E+05	4-2	0.8um MS (2P) / 3V	1.44E-02	1.29	64.27
[Baza99]	9.4	6.80E+07	1.70E+07	1.25E+06	4-4	0.6um MS (2P) / 3V	4.80E-02	4.03	4.18
[Sal02]	11.7	8.00E+07	2.00E+07	2.70E+05	4th-ord	0.35um / 3V	5.60E-02	0.84	99.34
[Sal02]	6.7	8.00E+07	2.00E+07	3.84E+06	4th-ord	0.35um / 3V	5.60E-02	24.57	0.11
[Sal03]	13.3	8.00E+07	2.00E+07	1.25E+06	4-4	0.35um / 3V	3.70E-02	0.18	1415.26
[Sal03]	11.7	8.00E+07	2.00E+07	1.76E+06	4-4	0.35um / 3V	3.70E-02	0.53	155.92
[Taba99]	13	8.00E+07	2.00E+07	1.25E+06	6th-ord	0.25um MS / 2.5V	9.00E-02	0.53	383.86
[Ueno02]	12.6	1.00E+07	5.66E+05	2.50E+05	2-2(3b)	0.25um MS (2P) / 2.5V	7.70E-02	17.95	8.63
[Cheu01]	6.7	4.28E+07	1.07E+07	2.00E+05	2nd-ord	0.35um STD / 1V	1.20E-02	10.69	0.24
[Cheu02]	6.8	4.28E+07	1.07E+07	2.00E+05	2nd-ord	0.35um MS (2P) / 1V	1.20E-02	9.97	0.28
[Kuo04]	10	7.13E+00	1.07E+07	2.00E+05	4th-ord	0.25um MS / 1V	8.45E-03	0.76	33.45
[Kuo04]	12.04	7.13E+00	1.07E+07	1.00E+05	4th-ord	0.25um MS / 1V	1.00E-01	1.13	563.12
[Kuo04]	12.7	7.13E+00	1.07E+07	6.00E+04	4th-ord	0.25um MS / 1V	1.00E-01	1.13	403.30
[Kuo04]	13.37	7.13E+00	1.07E+07	6.00E+04	4th-ord	0.25um MS / 1V	1.00E-01	1.13	3552.46

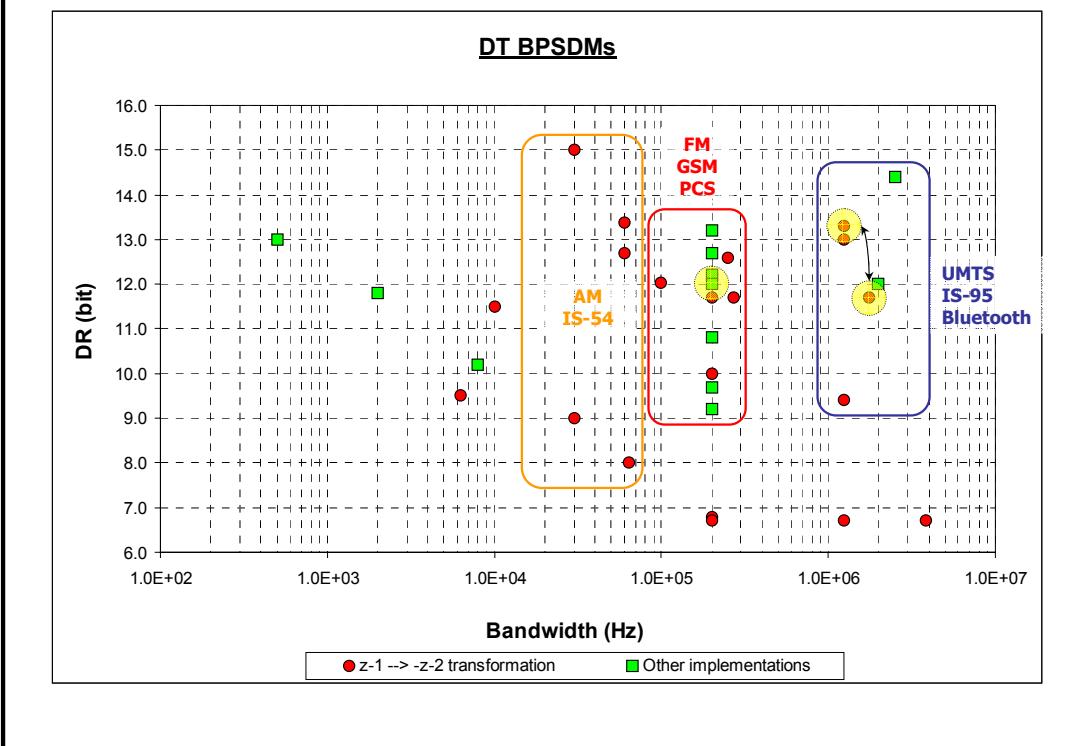
Synthesis method: $z^1 \rightarrow -z^2$ (~50%)

Other BPDSM ICs

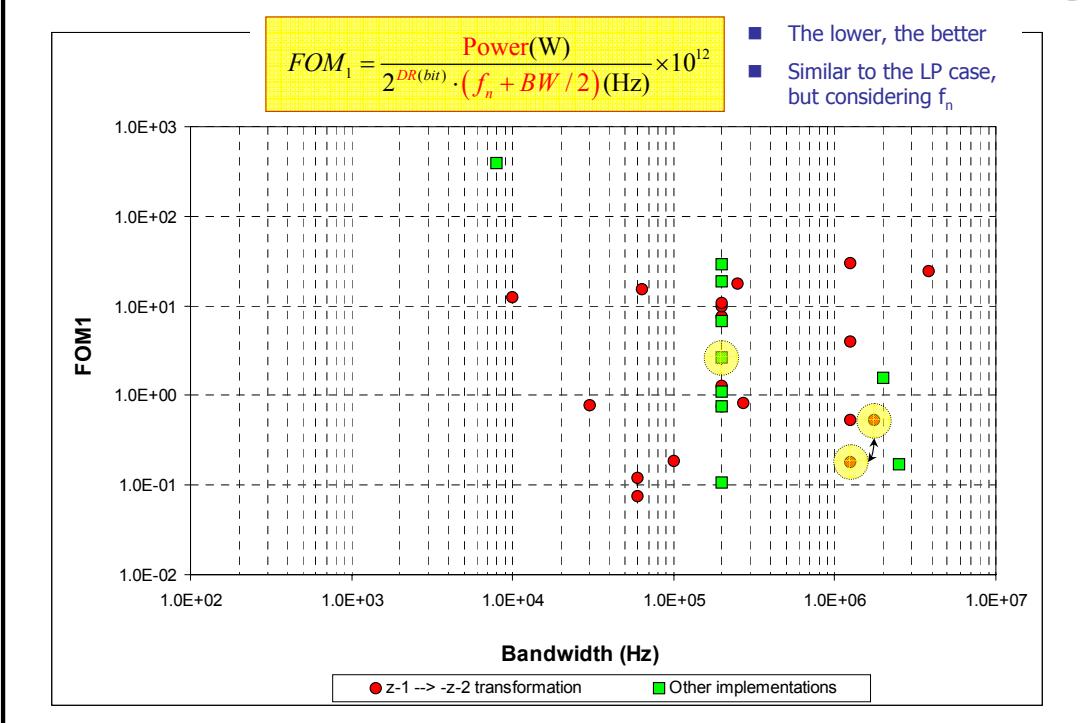
Author	DR (bit)	fs (Hz)	fn (Hz)	Bw	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁶
[Chua98]	13	5.00E+05	1.25E+05	5.00E+04	4th Opt NTF	3um MS (2P) / 3V	2.70E-01	0.08	---
[Jan93]	10.2	1.83E+06	4.55E+05	8.00E+04	4th Opt NTF	3um MS (2P) / 3V	1.30E-01	18.94	2.35
[Jan97]	10.8	1.00E+07	3.75E+06	2.00E+05	4th Quadrature	0.8um STD / 5V	1.30E-01	18.94	2.35
[Liu97]	11.8	8.27E+05	4.13E+05	2.00E+03	4th Opt NTF	2um MS (2P) / 5V	---	---	---
[Cusi01]	12	3.71E+07	1.07E+07	2.00E+05	6th Opt NTF	0.35um STD / 3.3V	1.16E-01	2.62	38.99
[Ong97]	12.2	8.00E+07	2.00E+07	2.00E+05	4th-ord	0.6um STD / 3.3V	7.20E-02	0.76	154.26
[Toni99]	12.7	4.28E+07	1.07E+07	2.00E+05	6th Opt NTF	0.35um STD / 3.3V	8.00E-02	1.11	149.19
[Chen05]	9.7	1.28E+07	3.25E+06	2.00E+05	3rd Quadrature	0.35um STD / 3.3V	1.87E-02	6.71	3.09
[Andr98]	9.2	4.00E+06	1.00E+06	2.00E+05	3rd(3b) Opt NTF	0.5um MS (2P) / 3V	1.90E-02	29.37	0.50
[Taba00]	12	6.40E+07	1.60E+07	2.00E+06	6th 2-path	0.25um STD / 2.5V	1.10E-01	1.58	64.72
[Mauro05]	13.2	1.31E+07	1.00E+07	2.00E+05	2-0 Quadrature	0.25um STD / 2.1V	1.00E-02	0.11	2232.33
[Ying04]	14.4	6.00E+07	4.00E+07	2.50E+06	4th Quadrature	0.18um STD / 1.8V	1.50E-01	0.17	3208.05

Passband location: $f_n = f_s/4$ (~80%)

DT-BP- $\Sigma\Delta$ MJs: State of the Art



DT-BP- $\Sigma\Delta$ MJs: State of the Art

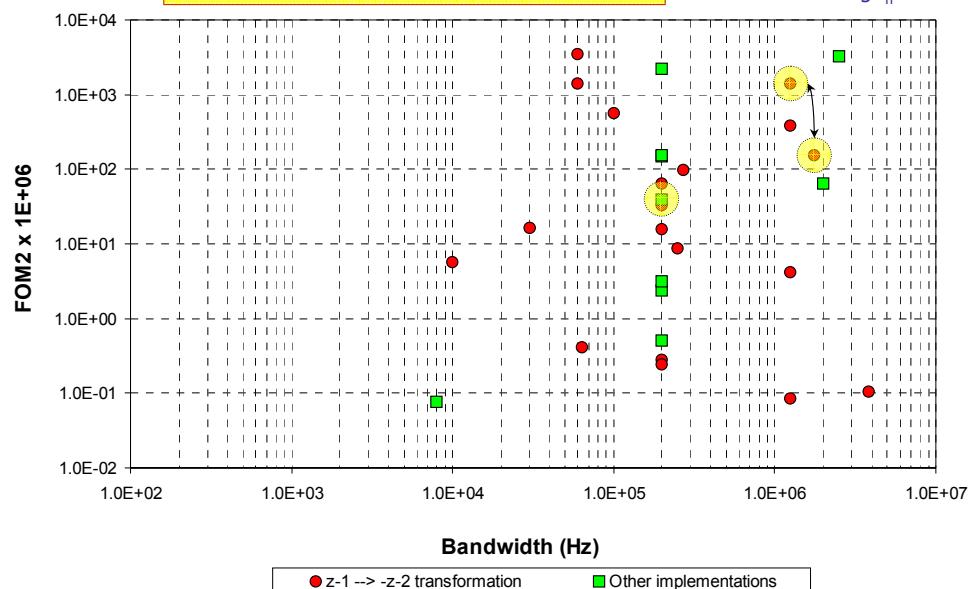


DT-BP- $\Sigma\Delta$ Ms: State of the Art



$$FOM_2 = 2kT \cdot \frac{3 \cdot 2^{2DR(\text{bit})} \cdot (f_n + BW/2) \text{ (Hz)}}{\text{Power (W)}}$$

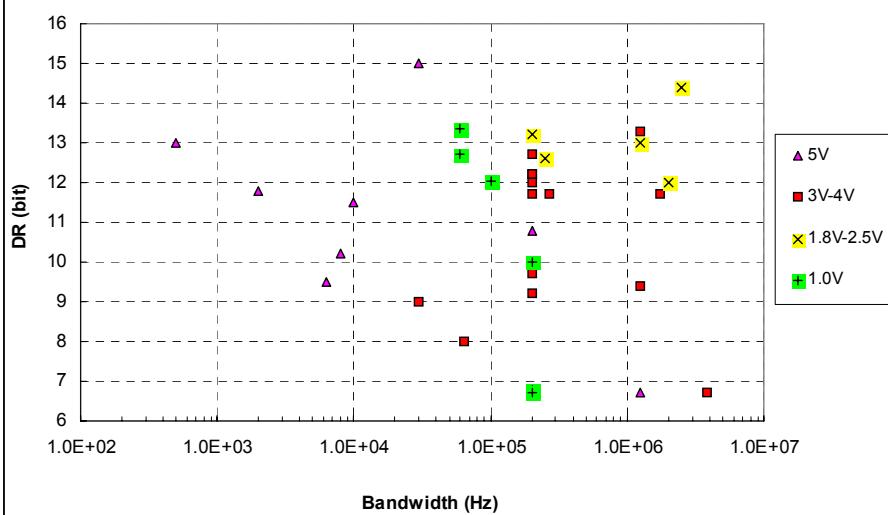
- The larger, the better
- Similar to the LP case, but considering f_n



DT-BP- $\Sigma\Delta$ Ms: State of the Art



DT BPSDMs organized per supply

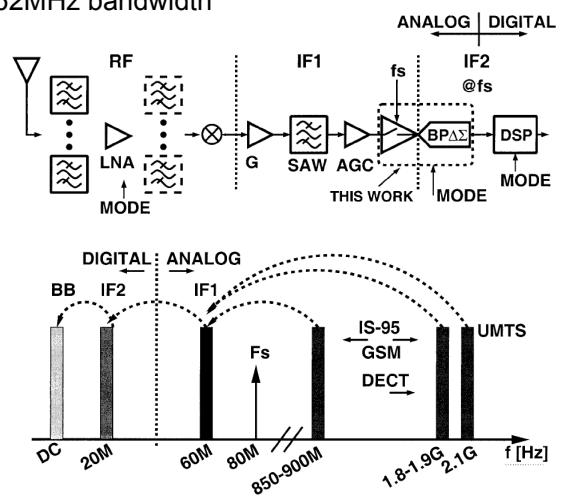
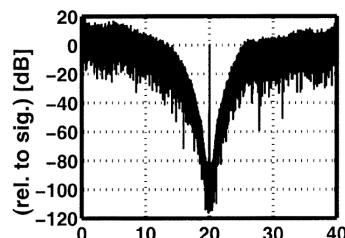


DT-BP- $\Sigma\Delta$ Ms: State of the Art / Wireless com

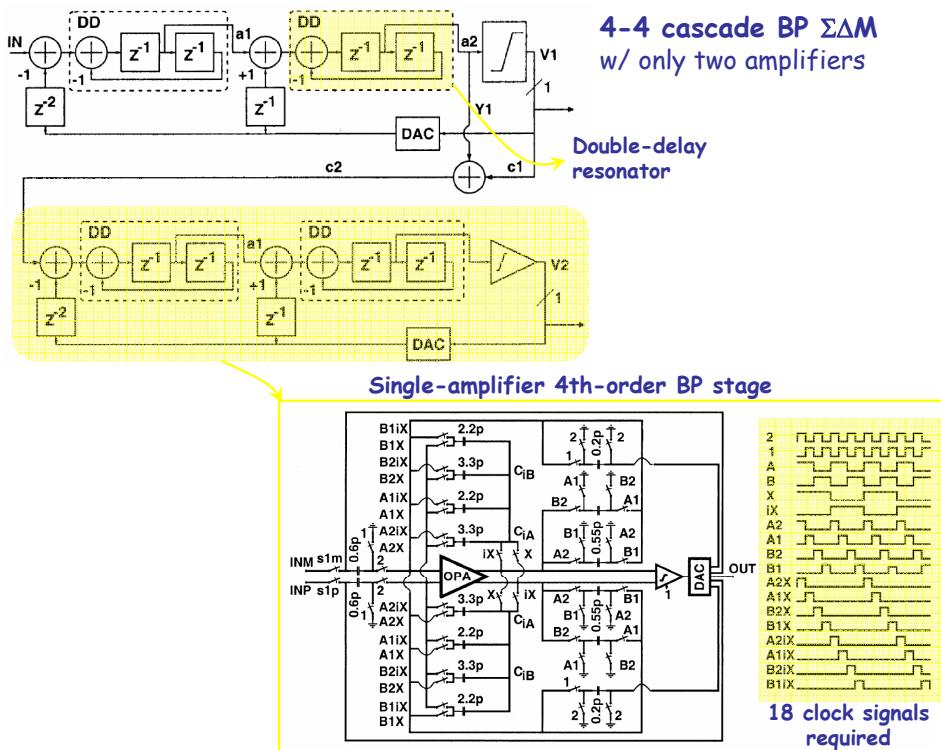


Digital IF receivers, IS-95/DECT [Salo03]

- ◆ Eighth-order bandpass cascade topology
 - 4-4 cascade BP $\Sigma\Delta$ M \rightarrow Equivalent to 2-2 LP $\Sigma\Delta$ M
 - $z^{-1} \rightarrow -z^{-2}$ transformation $\rightarrow f_n = f_s/4 = 80\text{MHz}/4 = 20\text{MHz}$
 - Double-delay (DD) resonators using only one amplifier
 - Based on single-amplifier 4th-order BP $\Sigma\Delta$ M
- ◆ Only two amplifiers required \rightarrow Folded-cascode topology
- ◆ 82/72dB DR within 1.25/1.762MHz bandwidth
- ◆ 0.35 μm CMOS tech
- ◆ 37mW, 3.0V



DT-BP- $\Sigma\Delta$ Ms: State of the Art / Wireless com

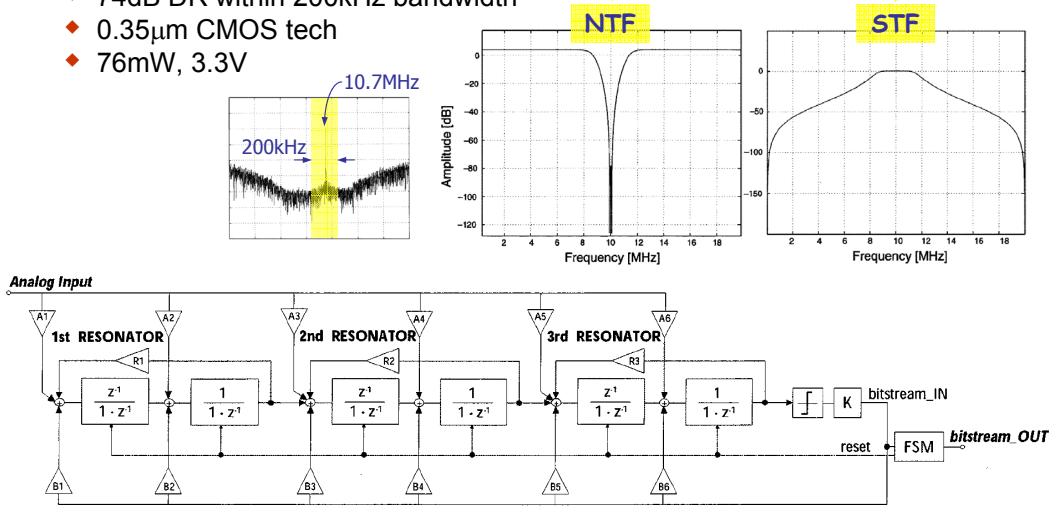


DT-BP- $\Sigma\Delta$ M: State of the Art / Wireless com



Digital IF receivers, FM [Cusi01]

- ◆ Sixth-order single-loop bandpass $\Sigma\Delta$ M
 - Distributed feedback and distributed feedforward topology
 - Optimized NTF and STF \rightarrow NTF w/ spread zeros, STF w/ interferer filtering
 - $f_n = f_s/4 = 42.8\text{MHz}/4 = 10.7\text{MHz}$
- ◆ Limited by kT/C and amplifier noise
- ◆ 74dB DR within 200kHz bandwidth
- ◆ 0.35 μm CMOS tech
- ◆ 76mW, 3.3V



CT- $\Sigma\Delta$ M: State of the Art



Low-Pass Single-bit

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)
[Badj02]	10,00	2,20E+04	64	4th-ord	0.5um CMOS 1.8V	1,70E-03
[Bree00]	13,3	2,00E+05	65	4th-ord	0.35um CMOS 2.5V	1,80E-03
[Gerf02]	11,3	5,00E+04	48	3rd-ord	0.5um CMOS 1.5V	2,50E-04
[Gerf03]	11,8	5,00E+04	48	3rd-ord	0.5um CMOS 1.5V	1,35E-04
[Lin99]	10,5	5,00E+06	16	2nd-ord	1.2um CMOS 3V	1,20E-02
[Luh00]	10	6,20E+06	64	5th-ord	0.6um CMOS 3.3V	1,60E-02
[Luh98a]	8	2,00E+06	25	2nd-ord	2um CMOS 5V	1,50E-02
[Luh98b]	9,6	2,00E+06	25	2nd-ord	2um CMOS 5V	1,66E-02
[Putt04]	12,5	2,00E+06	140	2nd-ord	0.18um CMOS / 1.8V	6,00E-03
[Veld02]	11,3	4,00E+06	38,4	4th-ord	0.18um CMOS 1.8V	6,60E-03
[Zwan96]	13	8,00E+03	64	4th-ord	0.5um CMOS 2.2V	2,00E-04
[Zwan99]	10,4	1,00E+06	10	2nd-ord	0.5um CMOS 5V	7,20E-03
[Ortm03]	10	5,00E+04	48	3rd-ord	0.5um CMOS 1.5V	7,50E-04
[Sami03]	9,4	1,00E+05	32	3rd-ord	0.5um CMOS 1.5V	7,50E-05
[Phil03]	12,3	1,00E+06	64	5th-ord	0.18um CMOS	4,40E-03
[Phil04]	14,5	2,00E+06	32	4th-ord	0.18um ST 1.8V	2,00E-03
[Blan02]	11,30	1,60E+04	62,5	4th-ord	0.35um STD/2.5V	7,50E-05
[Dagh04]	12,40	2,46E+06	813	2nd-ord	0.18um CMOS / 1.8V	1,80E-02
[Das05]	14,00	1,20E+06	213	4th-ord	90nm CMOS / 1.3V	5,40E-03
[Muñ05]	14,60	2,00E+06	32	4th-ord	0.18um CMOS / 1.8V	4,70E-03
[Naga05]	11,37	8,56E+05	150	4th-ord	0.11um CMOS / 1.2V	3,42E-03
[Naga05]	10,37	2,60E+06	50	4th-ord	0.11um CMOS / 1.2V	3,42E-03
[Pun07]	12,00	5,00E+04	64	3rd-ord	0.18um CMOS / 0.5V	3,70E-04

CT- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Multi-bit

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)
[Dorr03]	10	4,00E+06	26	3rd-ord (3b) - DEM	0.13um CMOS 1.2V	3,00E-03
[Gian03]	11	3,00E+07	10	4th-ord (4b)	0.13um CMOS 1.5V	7,50E-02
[Pato04]	11	3,00E+07	10	4th-ord (4b) - DEM	0.13um CMOS 1.5V	7,00E-02
[Yan03]	14	2,00E+06	16	3rd-ord (5b)	0.5um CMOS MS /	6,20E-02
[Yan04]	14,4	2,00E+06	16	3rd-ord (5b) - Calib.	0.5um CMOS MS /	6,20E-02
[Moya03]	13	2,40E+07	10	3rd-ord (6b) - Calib.	0.5um CMOS MS/2.5V	7,50E-02
[Schi04]	14	2,40E+05	54	4th-ord (3b) - ??	0.13um CMOS /1.25V	3,00E-03
[Dorr05]	12	4,00E+06	26	3rd-ord (4b) - Tracking quant	0.13um CMOS /1.5V	3,00E-03
[Font05]	12,5	1,20E+06	42	3rd-ord (2b)	90nm CMOS / 1.5V	6,00E-03
[Morr05]	16,7	4,00E+04	128	2nd-ord(4b) - DEM	0.18um CMOS /3.3V	3,73E-02
[Nguy05]	15,9	9,60E+04	128	4th-ord (4b) - DEM	0.35um (2P) /3.3V	1,80E-02
[Cald05]	8,9	4,00E+07	5	3rd-ord (4b) - time-interleav	0.18um CMOS /1.8V	1,03E-01
[Aria06]	8,70	4,00E+07	16	2nd-order (3b) - Complex	0.25um CMOS /2.5V	3,20E-02
[Mitt06]	13	4,00E+07	16	3rd-order (4b)	0.13um CMOS / 1.2V	2,00E-02
Bree04	10,87	2,00E+07	8	2-2 (4b)	0.18um ST/1.8V	1,22E-01
Bree04	10,87	4,00E+07	8	2-2 (4b) I/Q	0.18um ST/1.8V	2,16E-01

■ Band-Pass

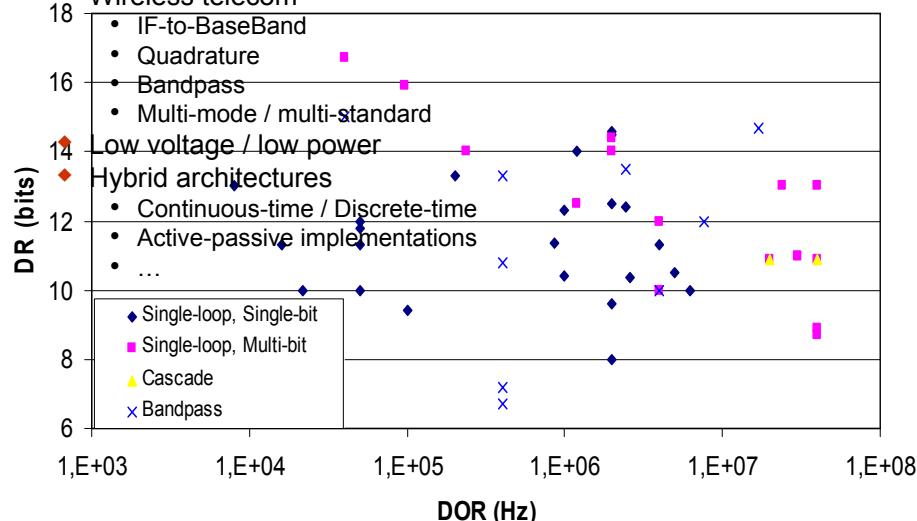
Author	DR (bit)	fs (Hz)	fn (Hz)	Bw (Hz)	DOR(Hz)	Architecture	Process	Power (W)
[Copp02]	10	1,28E+08	4,00E+06	2,00E+06	4,00E+06	2nd-ord (Complex)	0.25um CMOS 2V	1,42E-02
[Enge99]	10,8	4,00E+07	1,07E+07	2,00E+05	4,00E+05	6th-ord	0.5um CMOS 5V	6,00E-02
[Hsu00]	6,7	2,80E+08	7,00E+07	2,00E+05	4,00E+05	2nd-ord	0.5um CMOS 2.5V	3,90E-02
[Tao99]	7,2	4,00E+08	1,00E+08	2,00E+05	4,00E+05	4th-ord	0.35um CMOS 3.3V	1,65E-01
[Zwan00]	13,3	2,11E+07	1,07E+07	2,00E+05	4,00E+05	5th-ord	0.25um CMOS 2.5V	1,10E-02
[Veld03b]	15	2,60E+07	1,00E+05	2,00E+04	4,00E+04	5th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	9,10E-03
[Veld03b]	13,5	7,88E+07		1,23E+06	2,46E+06	5th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	1,31E-02
[Veld03b]	12	1,54E+08		3,84E+06	7,68E+06	5th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	1,41E-02
[Schr06]	14,7	2,64E+08	4,40E+07	8,50E+06	1,70E+07	4th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	3,75E-01

CT- $\Sigma\Delta$ Ms: State of the Art



□ A Large number of different topologies and applications

- ◆ Broadband (15-20MHz) telecom
- ◆ Wireless telecom

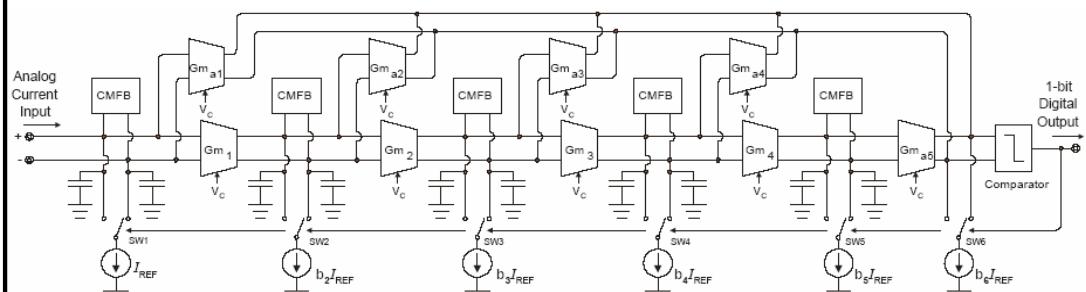
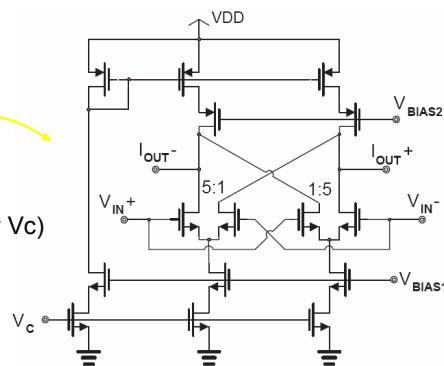


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



□ Gm-C 5th-order single-loop [Luh00]

- ◆ Fifth-order feedforward loop filter
 - Butterworth approximation
 - Gm-C implementation
 - Cross-coupled asymmetric differential pairs
 - Tunable transconductance gain (controlled by V_c)
- ◆ 0.6 μ m CMOS technology
- ◆ 62-dB DR within 3.1MHz bandwidth
- ◆ 400MHz sampling rate
- ◆ 16mW, 3.3V

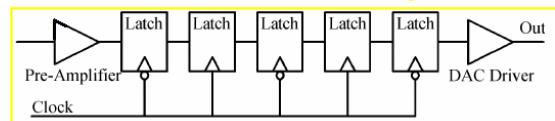
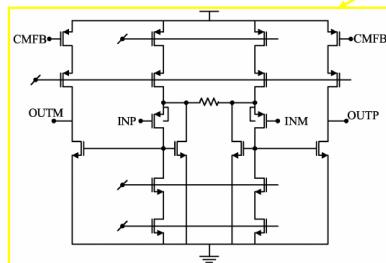
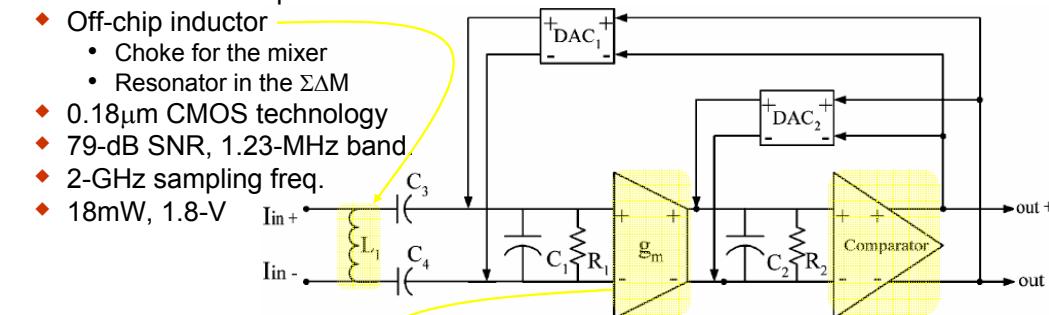


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



□ Gm-C 2nd-order single-loop for CDMA [Dagh04]

- ◆ Second-order loop filter
- ◆ Off-chip inductor
 - Choke for the mixer
 - Resonator in the $\Sigma\Delta$ M
- ◆ 0.18 μ m CMOS technology
- ◆ 79-dB SNR, 1.23-MHz band
- ◆ 2-GHz sampling freq.
- ◆ 18mW, 1.8-V

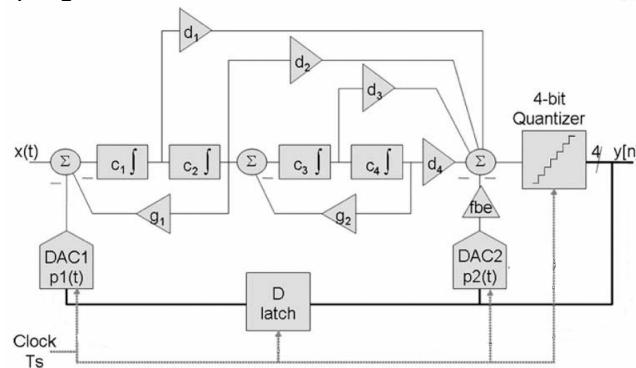
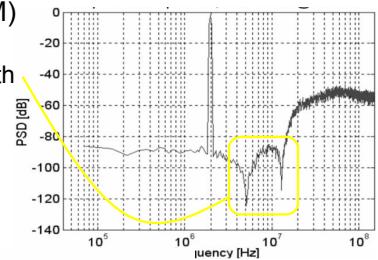


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



RC-active 4th-order (4-b) single-loop (I) [Pato04]

- 4th-order loop filter, 4-bit internal quantizer (+DEM)
- Direct synthesis method to optimize NTF
 - NTF-zero optimized to achieve the largest bandwidth
 - Robustness (stability) against process variations
- DAC2 used to compensate the excess loop delay
- 0.13 μ m CMOS technology
- 67-dB DR within 15-MHz bandwidth
- 300-MHz sampling rate
- 70mW, 1.5V

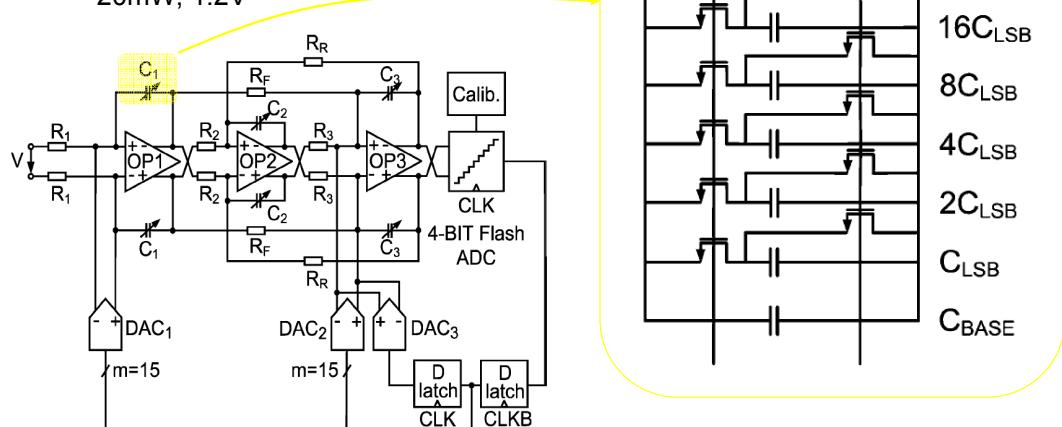


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



RC-active 3rd-order (4-b) single-loop [Mitt06]

- 3rd-order 4-bit
- Active-RC integrators
- Trimming of time-constants
- 0.13- μ m CMOS
- 12-bit ENOB within 20-MHz band
- 640-MHz sampling rate
- 20mW, 1.2V

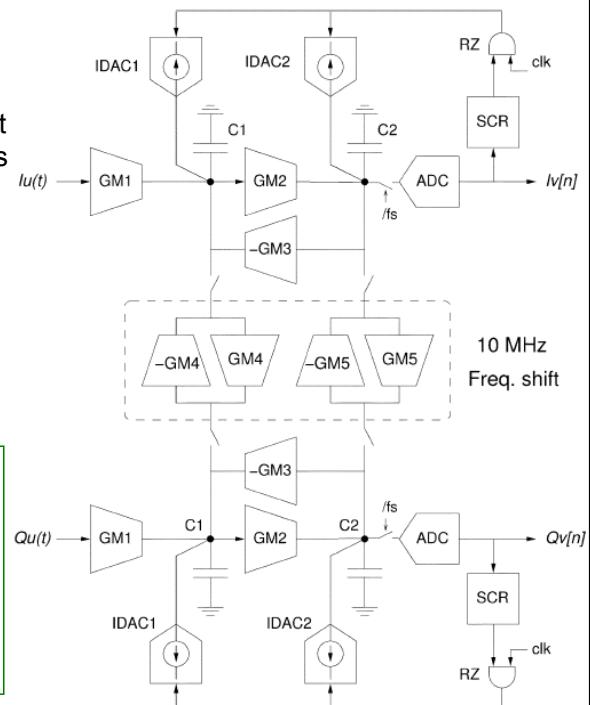
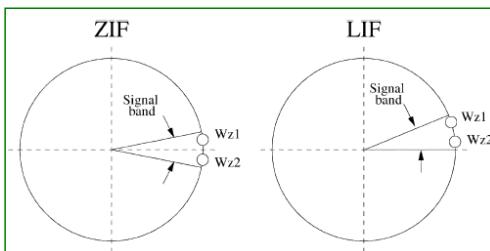


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



Complex architecture for WLAN (IEEE 802.11 a/b/g) [Aria06]

- First Complex (2x2nd-order) 3-bit
- NTF poles for ZIF and LIF modes
- Gm-C integrators
- 0.25 μ m CMOS standard technology (MOS caps)
- 8.7-bit ENOB within 20-MHz bandwidth
- 320-MHz sampling rate
- 32mW, 2.5V



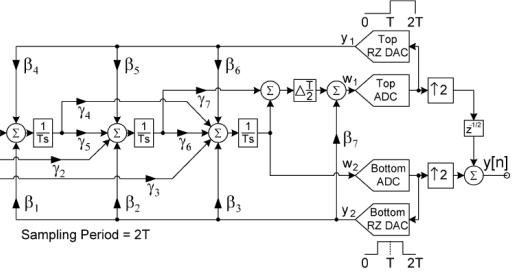
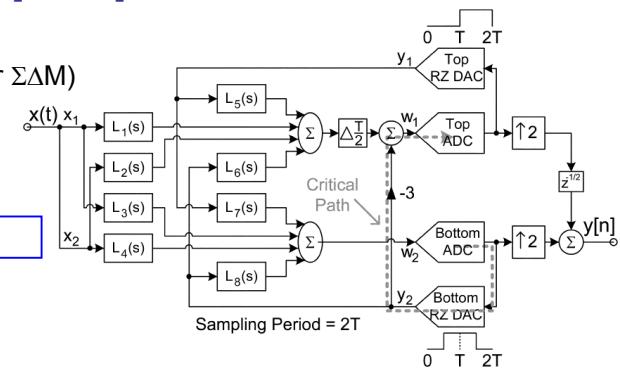
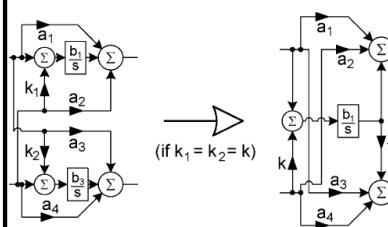
CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



Time-Interleaved architecture [Cald06]

- Time-interleaved (2x3rd-order $\Sigma\Delta$)
- 0.18- μ m CMOS
- 8.7-bit ENOB within 20-MHz
- 200-MHz sampling rate
- 103mW, 1.8V

Equivalence for integrator reduction

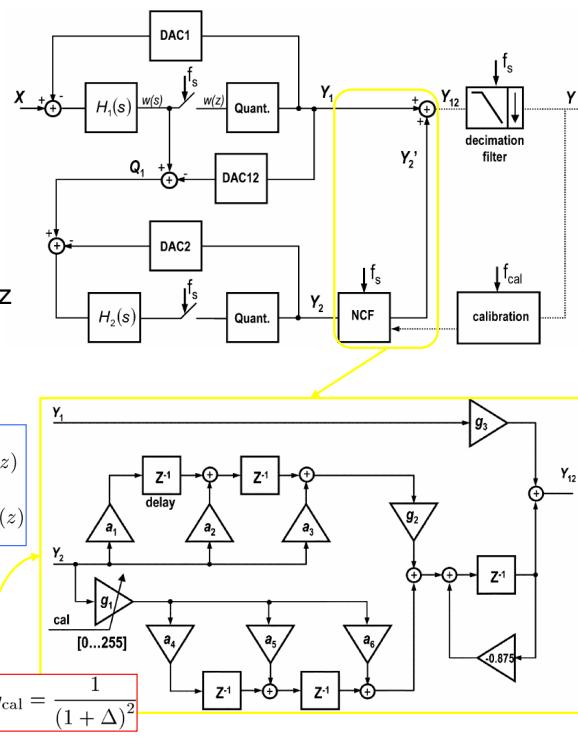


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



Cascade architecture [Bree04]

- ◆ 2-2 cascade topology
- ◆ Each stage with 4-bit quantizer
- ◆ DT-to-CT synthesis method
- ◆ 0.18 μ m CMOS technology
- ◆ 67-dB DR, 10-MHz bandwidth
- ◆ Quadrature configuration, 20-MHz
- ◆ 120mA, 1.8-V supply
- ◆ Digital calibration of NCF



$$Y_1(z) = \frac{D_1(z)}{1 + N_1(z) \cdot z^{-1}} \cdot Q_1(z) + \frac{N_1(z)}{1 + N_1(z) \cdot z^{-1}} \cdot X(z)$$

$$Y_2(z) = \frac{N_2(z)}{1 + N_2(z) \cdot z^{-1}} \cdot Q_1(z) + \frac{D_2(z)}{1 + N_2(z) \cdot z^{-1}} \cdot Q_2(z)$$

$$H_{NCF}(z) = -\frac{D_1(z)}{N_2(z)} \cdot \frac{1 + N_2(z) \cdot z^{-1}}{1 + N_1(z) \cdot z^{-1}}$$

$$g_{cal} = \frac{1}{(1 + \Delta)^2}$$

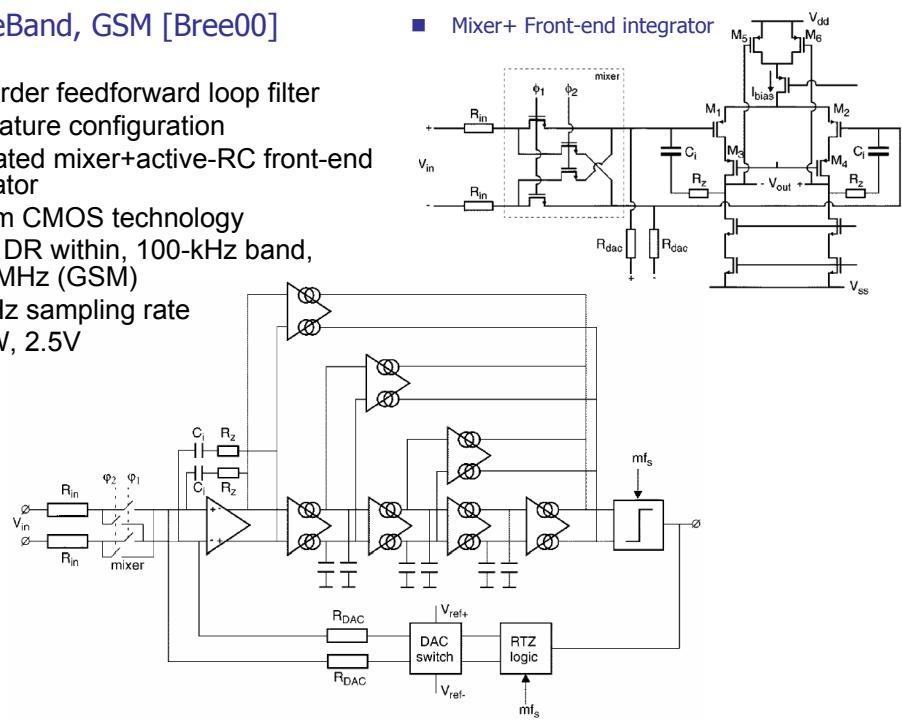
CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



IF-to-BaseBand, GSM [Bree00]

- ◆ Fifth-order feedforward loop filter
- ◆ Quadrature configuration
- ◆ Integrated mixer+active-RC front-end integrator
- ◆ 0.35 μ m CMOS technology
- ◆ 82-dB DR within, 100-kHz band, IF=50MHz (GSM)
- ◆ 13-MHz sampling rate
- ◆ 1.8mW, 2.5V

Mixer+ Front-end integrator

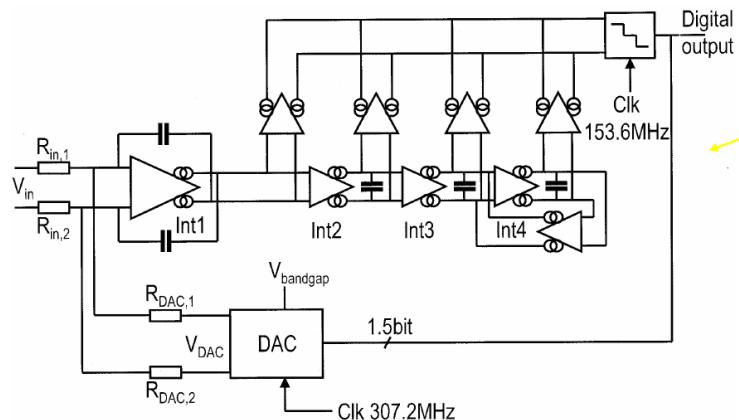
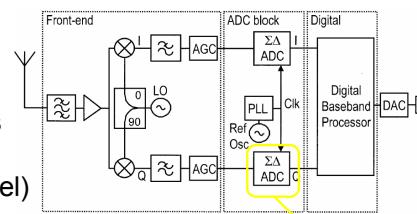


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



□ Quadrature architecture (I) [Veld02]

- ◆ Quadrature 4th-order, 1.5-bit topology
- ◆ Double loop to minimize internal signal swings
- ◆ 0.18 μ m CMOS technology
- ◆ 70-dB DR within 2-MHz bandwidth (per channel)
- ◆ 153.6MHz sampling rate
- ◆ 11.5mW, 1.8V

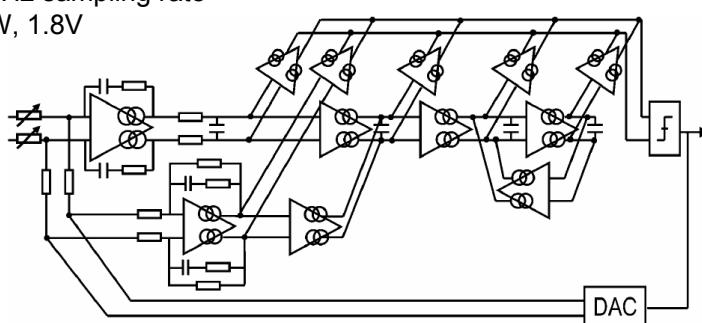
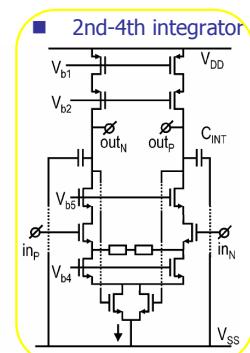
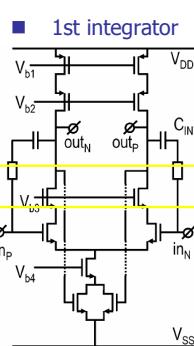


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



□ Programmable-gain, Merged filtering architecture [Phil04]

- ◆ Fourth-order loop filter
- ◆ Programmable gain functionality
 - Switchable input resistors (1,10,100k Ω)
- ◆ Compensating high-pass filtering
- ◆ Telescopic cascode opamps
- ◆ 0.18 μ m CMOS technology
- ◆ 89-dB DR, 1-MHz bandwidth
- ◆ 46-59 dB SNR-peak
- ◆ 64MHz sampling rate
- ◆ 2mW, 1.8V

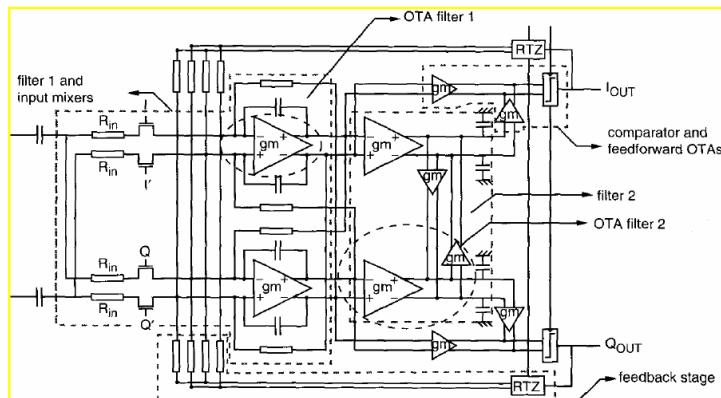
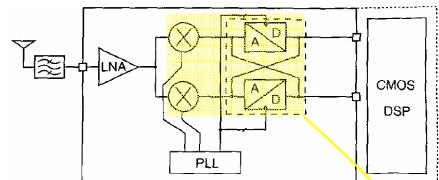


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



□ BP modulator + input mixer [Copp02]

- ◆ 1-bit, quadrature bandpass modulator
 - Second-order complex BP filter
 - Input mixing stage
- ◆ Downconversion of RF signals (0.3-1.6GHz)
- ◆ 0.25 μ m CMOS technology
- ◆ 62-dB DR, 2-MHz bandwidth, 4MHz IF
- ◆ 128-MHz sampling rate
- ◆ 14mW, 2-V

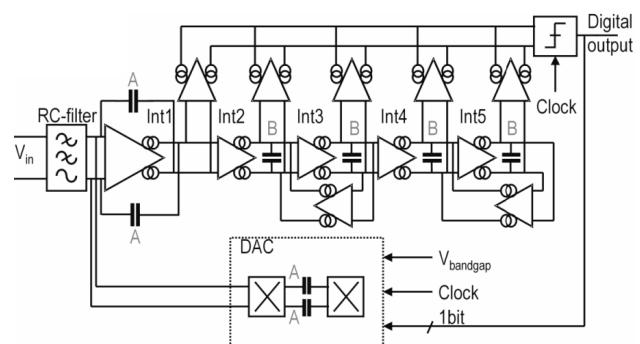
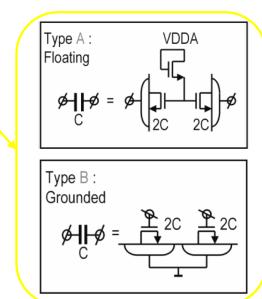
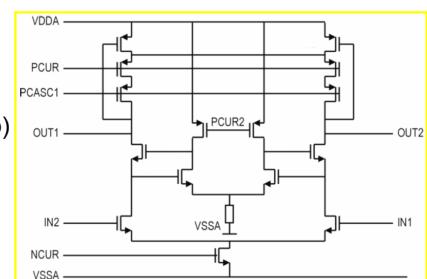


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



□ MultiMode/MultiStandard applications [Veld03]

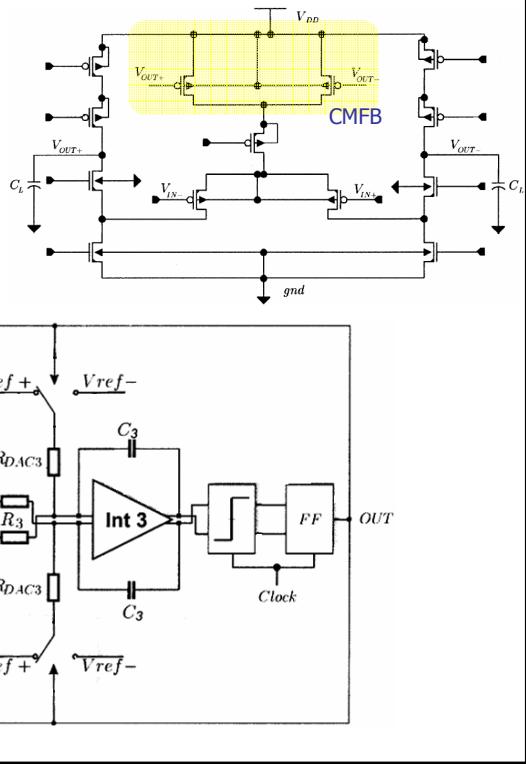
- ◆ 1-bit, complex fifth-order loop filter
 - SC DAC to reduce sensitivity to clock jitter
 - NMOS in NWELL (switchable) capacitors
 - Active RC 1st stage (regulated-cascode opamp)
 - Gm-C integrators for the remaining stages
- ◆ 0.18 μ m CMOS technology
- ◆ GSM/CDMA2000/UMTS modes
 - 92/83/72-dB DR, 200/1228/3840-kHz
 - 26/76.8/153.6-MHz sampling rate
 - 3.8/4.1/4.5mW, 1.8-V



CT- $\Sigma\Delta$ Ms: State of the Art / Low-power, low-voltage

□ Low-power Modulator [Gerb03]

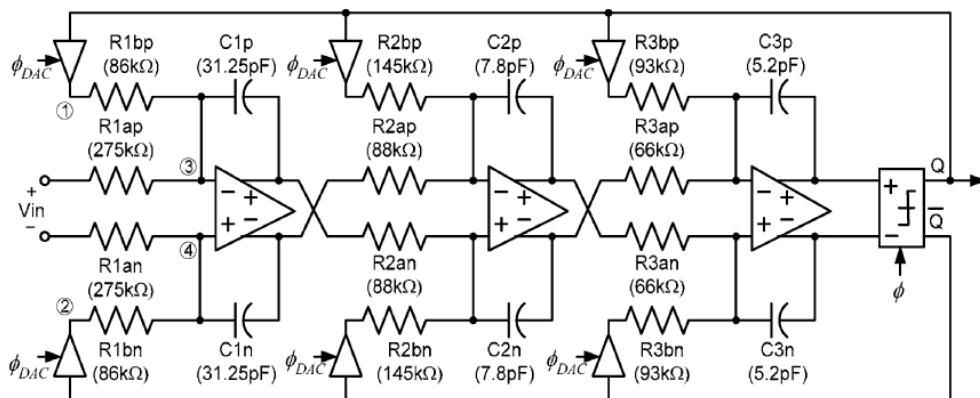
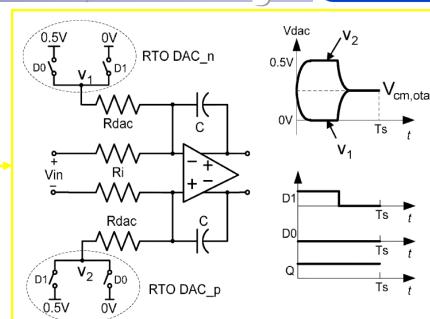
- ◆ Third-order loop filter
 - RC-active implementation
 - Folded-cascode opamps ($40\mu\text{W}$)
- ◆ 0.5 μm CMOS technology
- ◆ 80-dB DR within 25-kHz bandwidth
- ◆ 2.4MHz sampling rate
- ◆ $135\mu\text{W}$, 1.5V



CT- $\Sigma\Delta$ Ms: State of the Art / Low-power, low-voltage

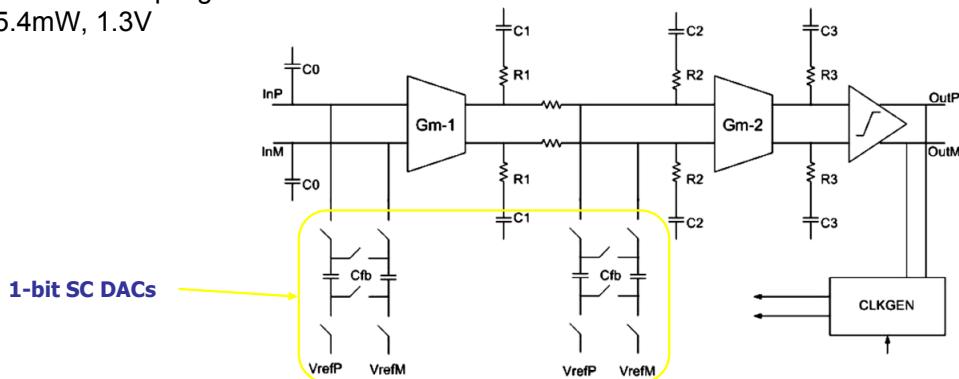
□ Low-power/Low-Voltage (0.5V) [Pun07]

- ◆ Third-order loop filter
 - RC-active integrators
 - Body-input OTAs and comparators
- ◆ Return-to-Open DAC
- ◆ 0.18 μm CMOS technology
- ◆ 74-dB DR within 25-kHz bandwidth
- ◆ $300\mu\text{W}$, 0.5V



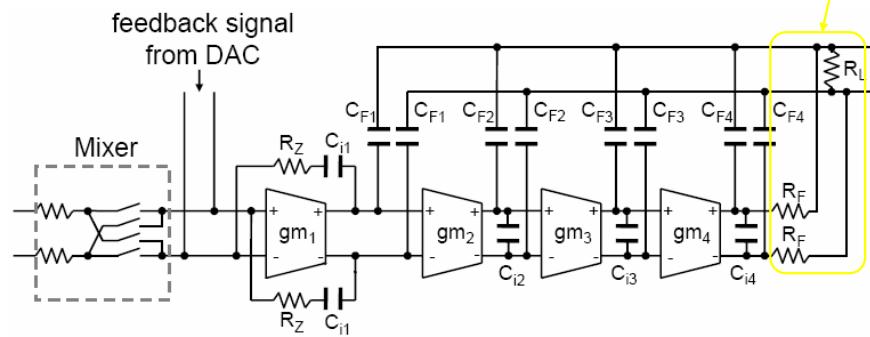
□ Active-passive implementations (I) [Das05]

- ◆ 4th-order loop filter
- ◆ Two (folded-cascode) amplifiers plus passive components
 - N-well resistors
 - PMOS capacitors
- ◆ Double loop to minimize internal signal swings
- ◆ 90nm CMOS technology
- ◆ 86-dB SNR-peak within 600-kHz bandwidth
- ◆ 256MHz sampling rate
- ◆ 5.4mW, 1.3V



□ Active-passive implementations (II) [Naga05]

- ◆ 4th-order loop filter
- ◆ Passive current-summing network in the feedforward path
 - Phase compensation
 - Reduce power consumption
- ◆ 0.11 μ m, dual- V_t CMOS technology
- ◆ Variable gain implemented by varying the DAC output power
- ◆ 57-dB DR within 1.3-MHz bandwidth
- ◆ 132-MHz sampling rate
- ◆ 3.42mW, 1.2V

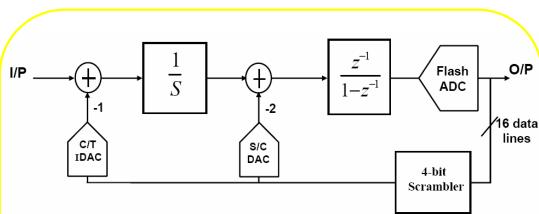


CT- $\Sigma\Delta$ Ms: State of the Art / Hybrid architectures



□ Hybrid lowpass (CT-DT) architectures [Morr05][Nguy05]

- ◆ CT front-end integrator
 - Potentially faster with less power consumption
 - Anti-aliasing filtering
 - Avoids the use of bootstrapping
- ◆ Problems
 - Sensitivity to clock jitter
 - Chopper stabilization techniques with CT filters
 - Hybrid tuning circuit required

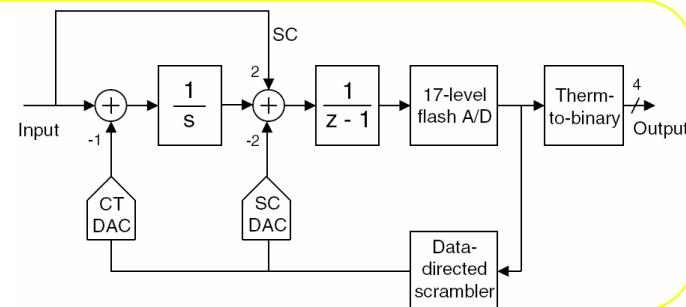


□ [Morr05]

- ◆ 0.18 μ m CMOS technology
- ◆ 102-dB DR, 20-kHz signal bandwidth
- ◆ 11.3mA, 3.3-V

□ [Nguy05]

- ◆ 0.35 μ m CMOS technology
- ◆ 106-dB DR, 192-kHz
- ◆ 36mW

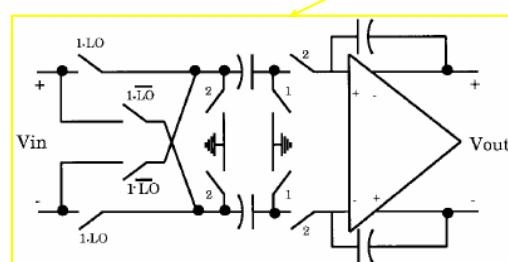
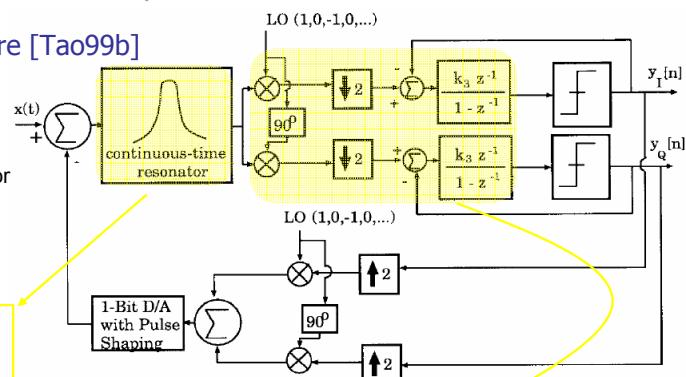
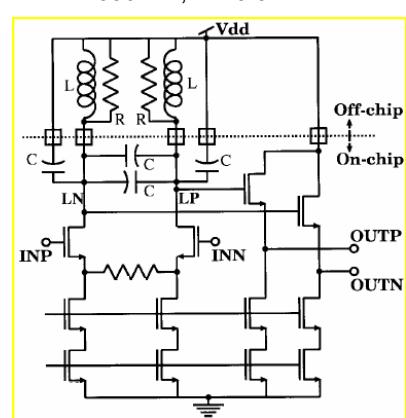


CT- $\Sigma\Delta$ Ms: State of the Art / Hybrid architectures



□ Hybrid BP (CT-DT) architecture [Tao99b]

- ◆ Fourth-order loop filter
 - IF=100MHz
 - CT front-end resonator
 - In-loop mixer+DT integrator
- ◆ 50-dB DR, 200-kHz band
- ◆ 0.35 μ m CMOS technology
- ◆ 330mW, 2.7/3.3V



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CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Circuits and Errors

Rocío del Río, Belén Pérez-Verdú and José M. de la Rosa



{rocio,belen,jrosa}@imse.cnm.es



KTH, Stockholm, April 23-27

OUTLINE



1. Circuits and Errors in DT $\Sigma\Delta$ Modulators

- Errors degrading NTF
- Additive noise sources
- Harmonic distortion
- Case study

2. Circuits and Errors in CT $\Sigma\Delta$ Modulators

- CT $\Sigma\Delta$ M subcircuits
- Building-block errors
- Architectural timing errors
- Case study

3. Layout & Prototyping

- Layout floorplanning
- Chip package
- Test PCB and Set-up

DT- $\Sigma\Delta$ Ms: Overview of Non-idealities



- Depending on their effect:

ERRORS DEGRADING NTF

- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
 - ▼ Amplifier GB
 - ▼ Amplifier SR
 - ▼ Switch R_{on}

Impact depends on topology

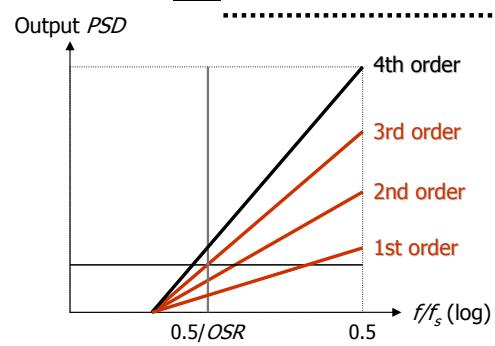
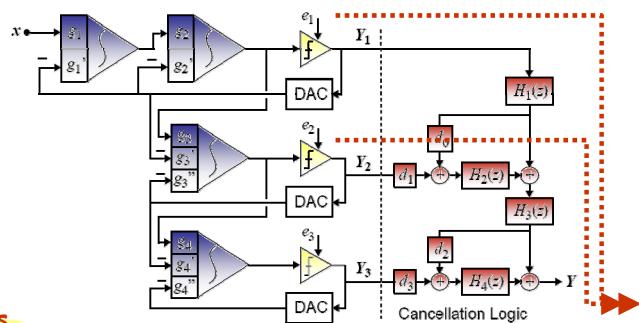
😊 SINGLE-LOOP $\Sigma\Delta$ Ms

→ Low sensitivity

😢 CASCADE $\Sigma\Delta$ Ms

→ **Noise leakages**

Imperfect cancellation of low-order quantization errors



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DT- $\Sigma\Delta$ Ms: Overview of Non-idealities



- Depending on their effect:

ERRORS DEGRADING NTF

- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
 - ▼ Amplifier GB
 - ▼ Amplifier SR
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Impact depends on topology

😊 SINGLE-LOOP $\Sigma\Delta$ Ms

→ Low sensitivity

😢 CASCADE $\Sigma\Delta$ Ms

→ **Noise leakages**

Imperfect cancellation of low-order quantization errors

MODELED AS ADDITIVE ERRORS

- CIRCUIT NOISE
 - ▼ Thermal noise (switches, opamps, refs)
 - ▼ 1/f noise (opamps, refs)
- CLOCK JITTER
- DISTORTION
 - ▼ Non-linear amplifier gain
 - ▼ Non-linear capacitors
 - ▼ Non-linear settling
 - ▼ Non-linear switches

Front-end
dominates

**Similar impact on
different topologies**

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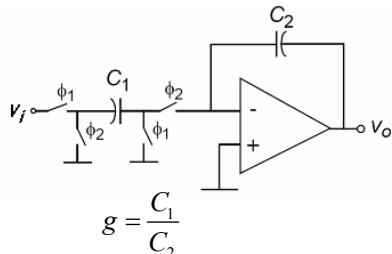
6

DT- $\Sigma\Delta$ Ms: Integrator Leakage

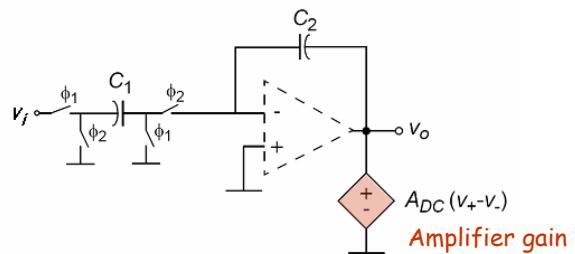


- Effect of amplifier gain on the integrator transfer function:

Ideal SC integrator



SC integrator considering amplifier finite gain



$$v_{o,n} = v_{o,n-1} + g \cdot v_{i,n-1} \rightarrow v_{o,n} = \frac{1}{1 + \frac{1}{A_{DC}}} \left[\left(1 + \frac{1}{A_{DC}} \right) \cdot v_{o,n-1} + g \cdot v_{i,n-1} \right]$$

$$H(z) = g \frac{z^{-1}}{1 - z^{-1}}$$

$$H(z) \approx g \frac{z^{-1}}{1 - z^{-1} \left(1 - \frac{g}{A_{DC}} \right)} = g \frac{z^{-1}}{1 - z^{-1} (1 - g\mu)}$$

Shift of the pole from DC ($z=1$)

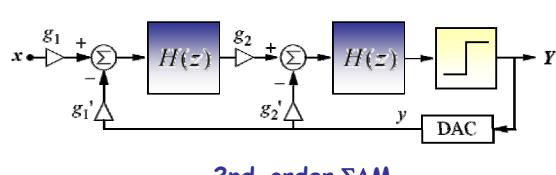
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DT- $\Sigma\Delta$ Ms: Integrator Leakage



- Effect on single-loop $\Sigma\Delta$ Ms:



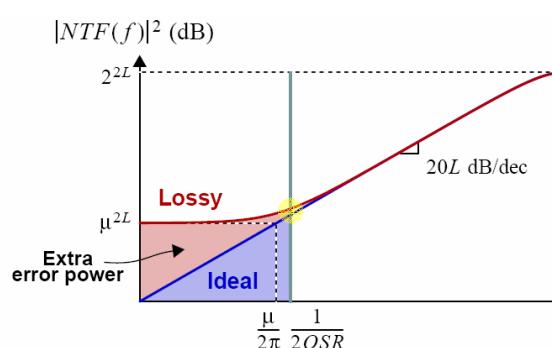
- Ideally: $H(z) = \frac{z^{-1}}{1 - z^{-1}}$

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z)$$

- In practice: $H(z) = \frac{z^{-1}}{1 - z^{-1}(1 - \mu)}$

$$\begin{aligned} NTF(z) &= [1 - z^{-1}(1 - \mu)]^2 \\ &= (1 - z^{-1})^2 + 2\mu z^{-1}(1 - z^{-1}) + \mu^2 z^{-2} \end{aligned}$$

$$P_Q(\mu) \approx \frac{\Delta^2}{12} \left(\frac{\pi^4}{5OSR^5} + \frac{2\mu^2}{3OSR^3} + \frac{\mu^4}{OSR} \right)$$



Lth-order $\Sigma\Delta$:

$$\Delta P_Q \approx \frac{\Delta^2}{12} \frac{L\mu^2 \pi^{2L-2}}{(2L-1)OSR^{(2L-1)}}$$

Quite insensitive to leakages ($\mu^2, L-1$ shaping)



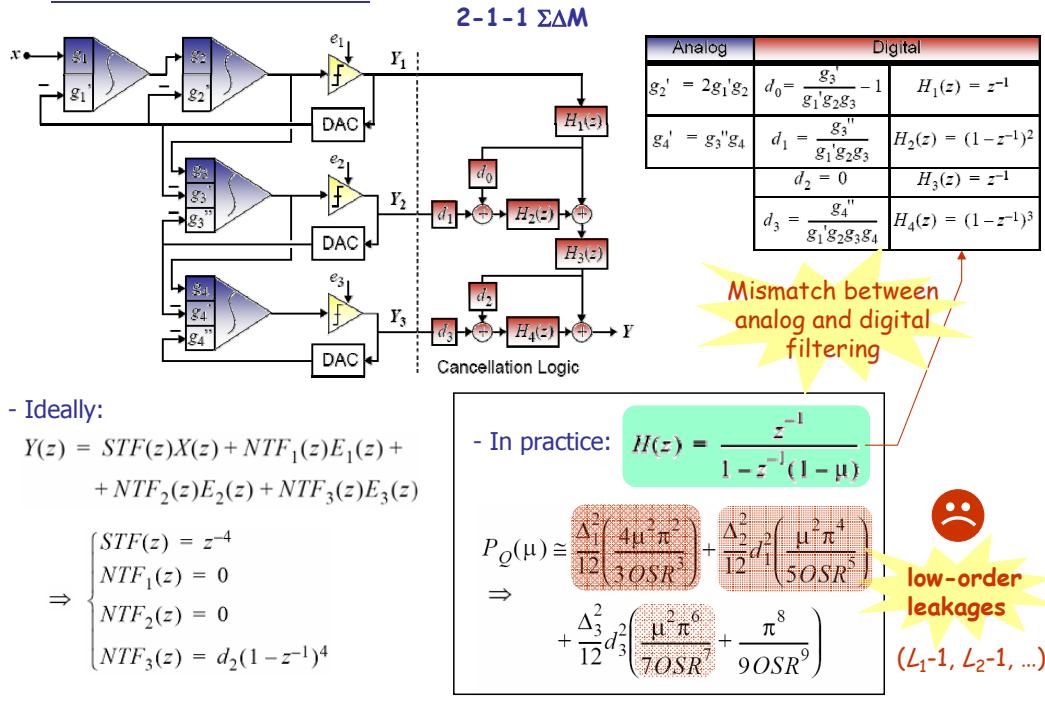
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DT- $\Sigma\Delta$ Ms: Integrator Leakage



Effect on cascade $\Sigma\Delta$ s:



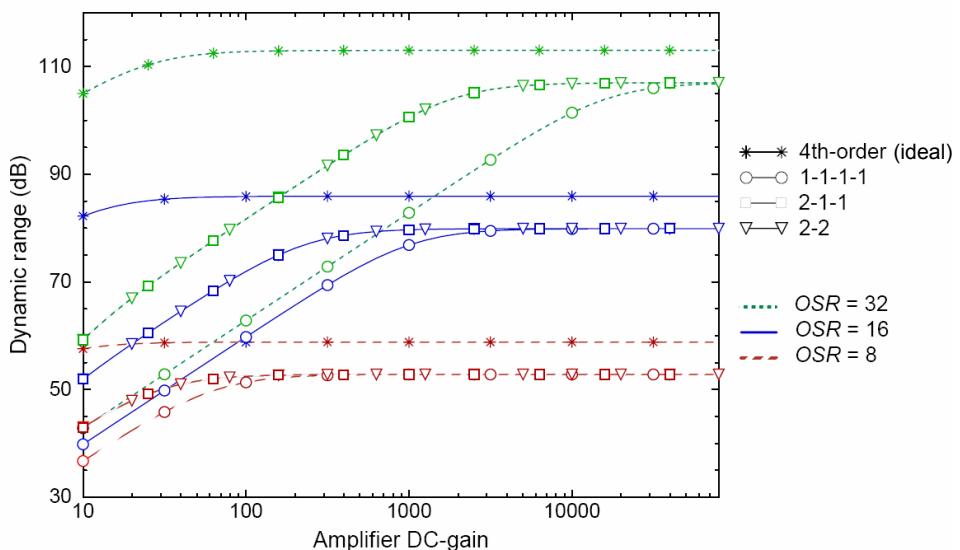
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DT- $\Sigma\Delta$ Ms: Integrator Leakage



Comparison of integrator leakage effect on 4th-order $\Sigma\Delta$ s



→ Sensitivity to integ leakages of cascades increases with OSR and L
→ 1st-stage leakages dominate (L_1-1 shaping)

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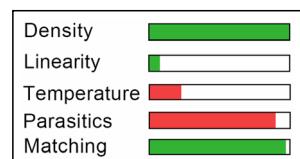
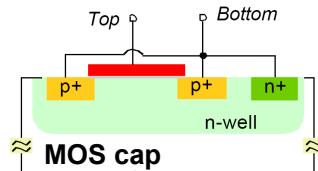
DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



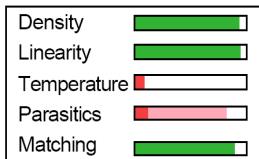
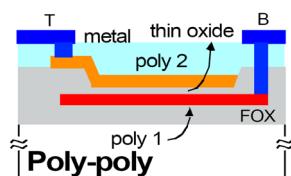
Circuit primitive:



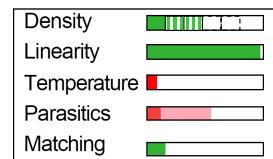
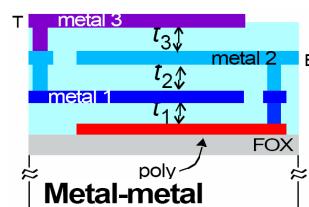
Physical implementations:



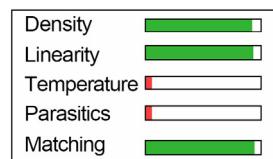
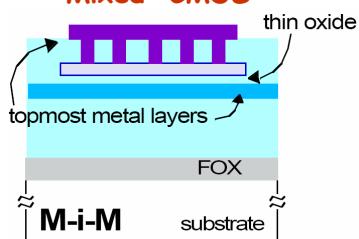
"Analog" CMOS



"Digital" CMOS



"Mixed" CMOS



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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch

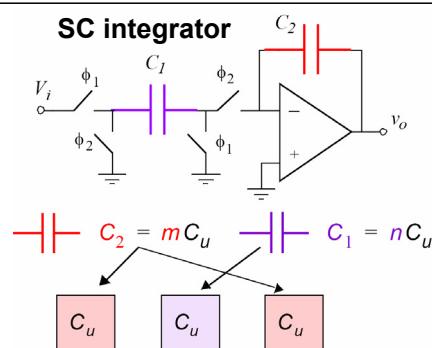
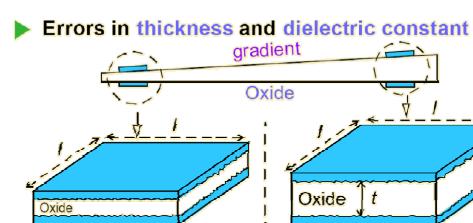
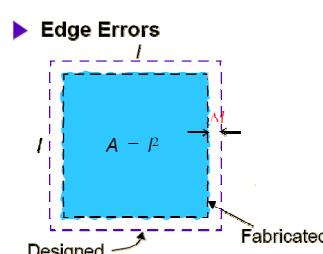


$$C = C_{oxc}^* \cdot (W \cdot L)$$

Actual \neq Ideal

Local and global errors in:

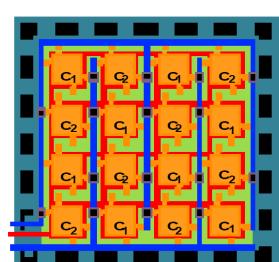
- ▶ Area
- ▶ Capacitance per Unit Area



$$g = \frac{C_1}{C_2} = \frac{nC_u}{mC_u}$$

$$\frac{\sigma_g}{g} = \sqrt{\frac{1}{n} + \frac{1}{m}} \cdot \frac{\sigma_{Cu}}{C_u}$$

$\sigma_C \sim 0.05\% - 0.1\%$
using good quality caps and adequate layout strategies



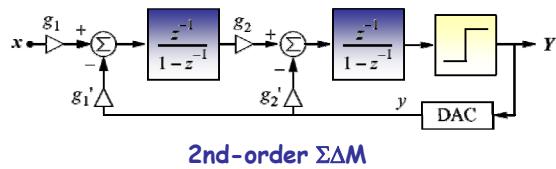
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch

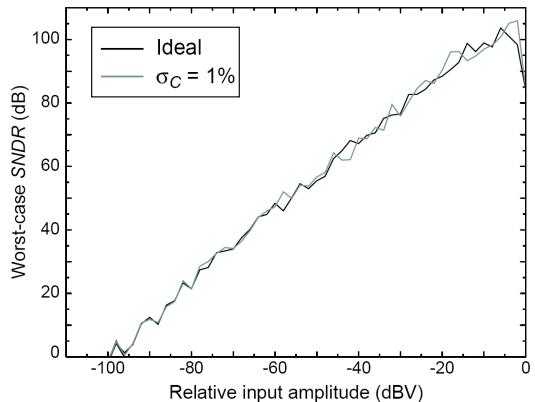
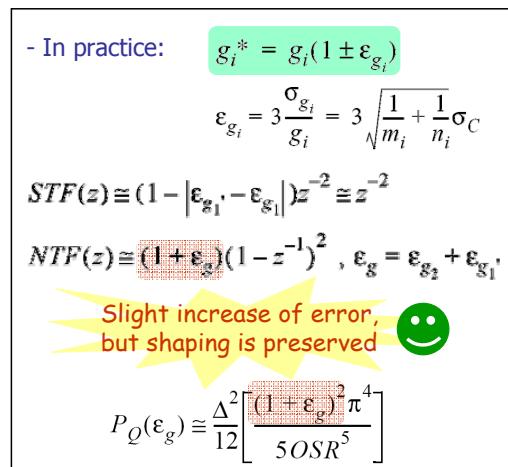


Effect on single-loop $\Sigma\Delta$ Ms:



- Ideally: $g_1 = g_1'$
 $g_2 = 2g_1'g_2$

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z)$$



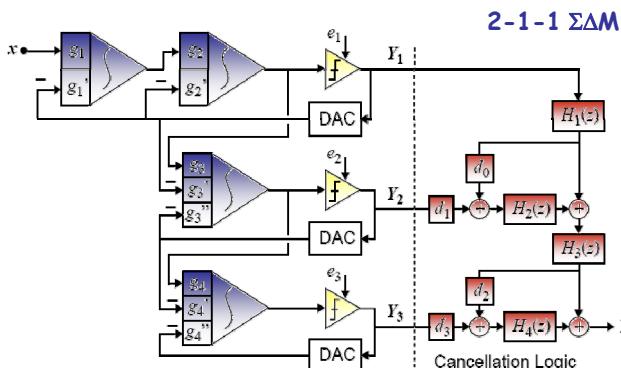
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



Effect on cascade $\Sigma\Delta$ Ms:



Analog	Digital
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$ $H_1(z) = z^{-1}$
$g_4'' = g_3''g_4$	$d_1 = \frac{g_3''}{g_1'g_2g_3}$ $H_2(z) = (1 - z^{-1})^2$
$d_2 = 0$	$H_3(z) = z^{-1}$
$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$	$H_4(z) = (1 - z^{-1})^3$

Mismatch between analog and digital coeffs

- Ideally:

$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z)$$

$$\Rightarrow \begin{cases} STF(z) = z^{-4} \\ NTF_1(z) = 0 \\ NTF_2(z) = 0 \\ NTF_3(z) = d_2(1 - z^{-1})^4 \end{cases}$$

- In practice: $g_i^* = g_i(1 \pm \varepsilon_{g_i})$

$$STF(z) \approx z^{-4}$$

$$NTF_1(z) \approx d_1 z^{-2} (1 - z^{-1})^2$$

$$NTF_2(z) \approx d_1 \varepsilon_2 z^{-1} (1 - z^{-1})^3$$

$$NTF_3(z) \approx d_2 (1 + \varepsilon_3) (1 - z^{-1})^4$$



low-order leakages
 (L_1, L_2, \dots)

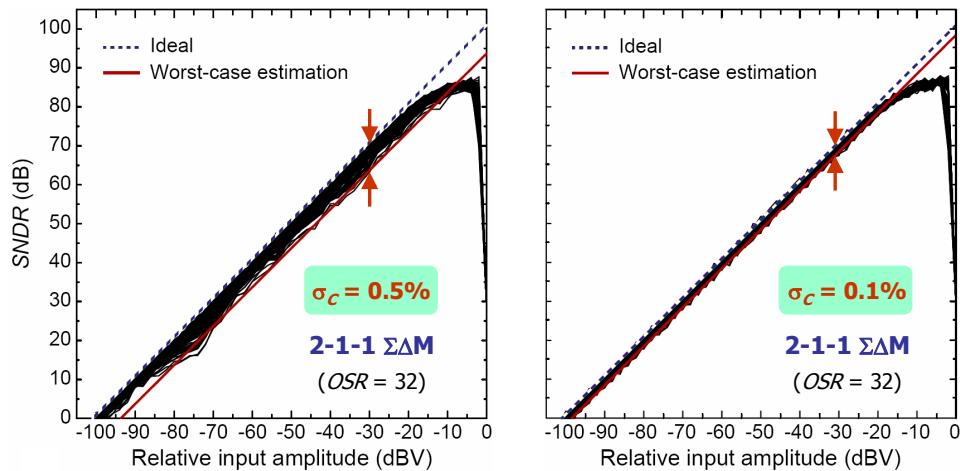
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



■ Effect on cascade $\Sigma\Delta$ Ms:



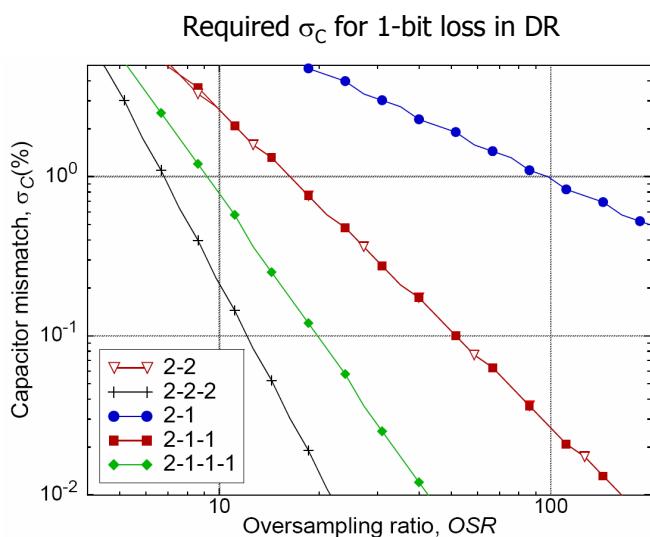
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



■ Effect on cascade $\Sigma\Delta$ Ms:



Sensitivity to mismatch rapidly increases with:
 - Oversampling ratio (OSR)
 - Cascade order (L)

1st-stage leakages dominate (L_1 shaping)

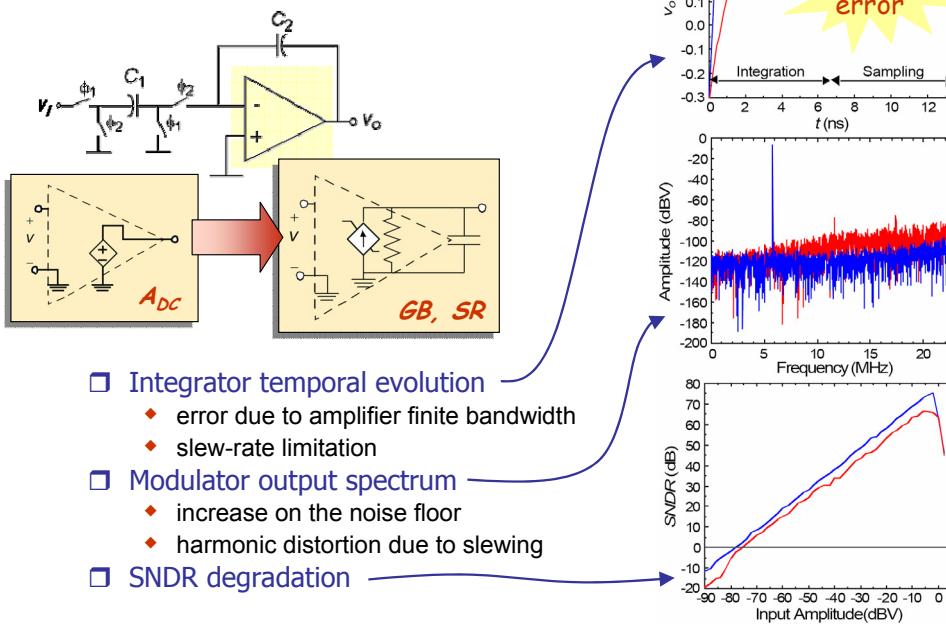
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DT- Σ Ms: Integrator Incomplete Settling



- If only amplifier gain is considered, the relation between v_o and virtual ground is assumed to be independent on time
- In practice, this relation depends is non-linear on time



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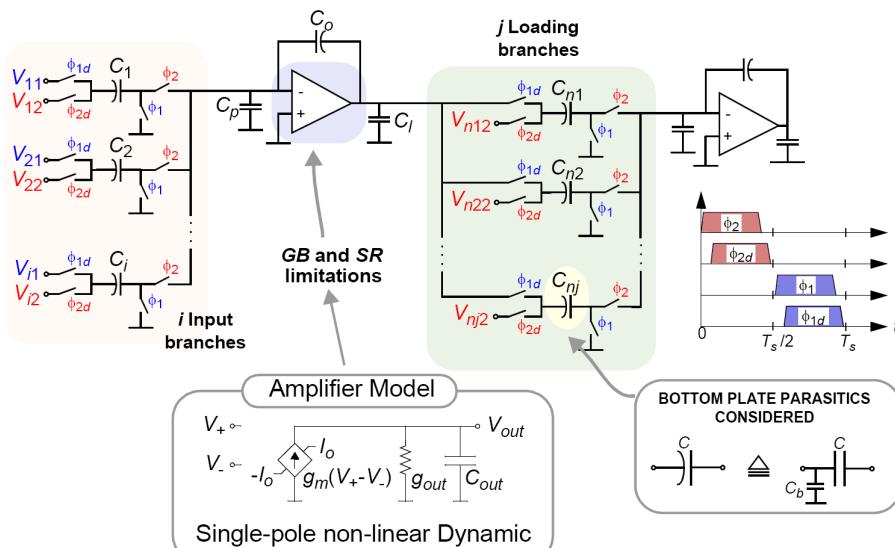
17

DT- Σ Ms: Integrator Incomplete Settling



Integrator temporal evolution: [Rio00]

- ♦ Both integration and sampling dynamics considered
- ♦ 1 pole model + SR limitation in amplifiers
- ♦ All parasitic caps taken into account



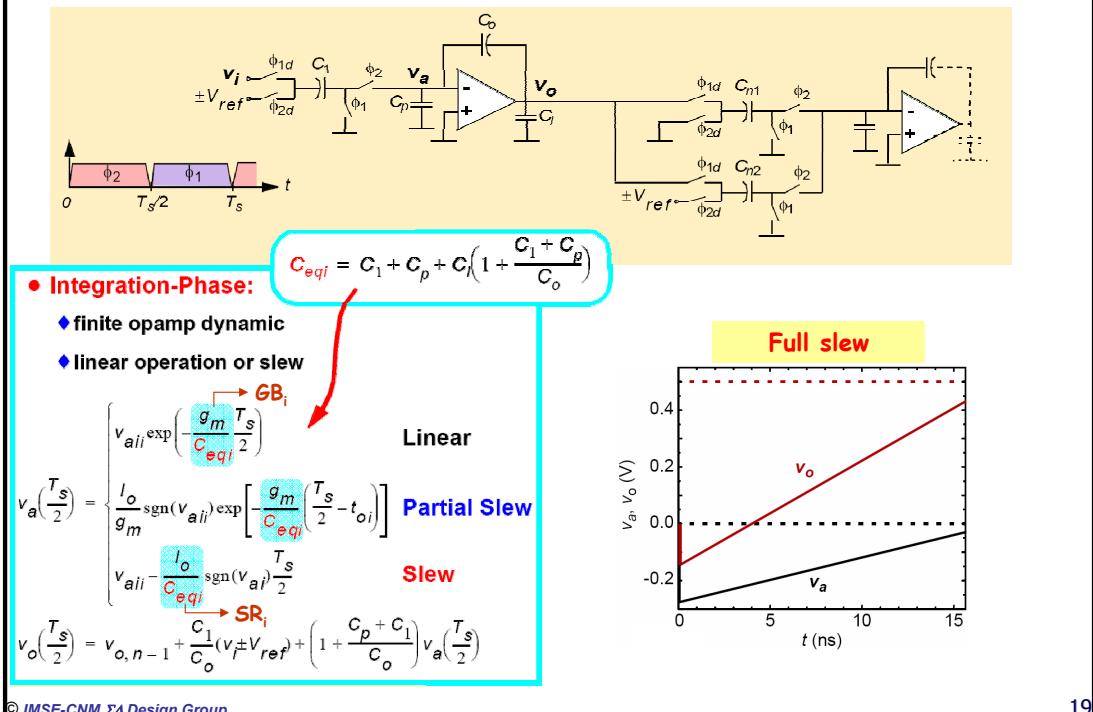
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



Integrator temporal evolution: [Rio00]



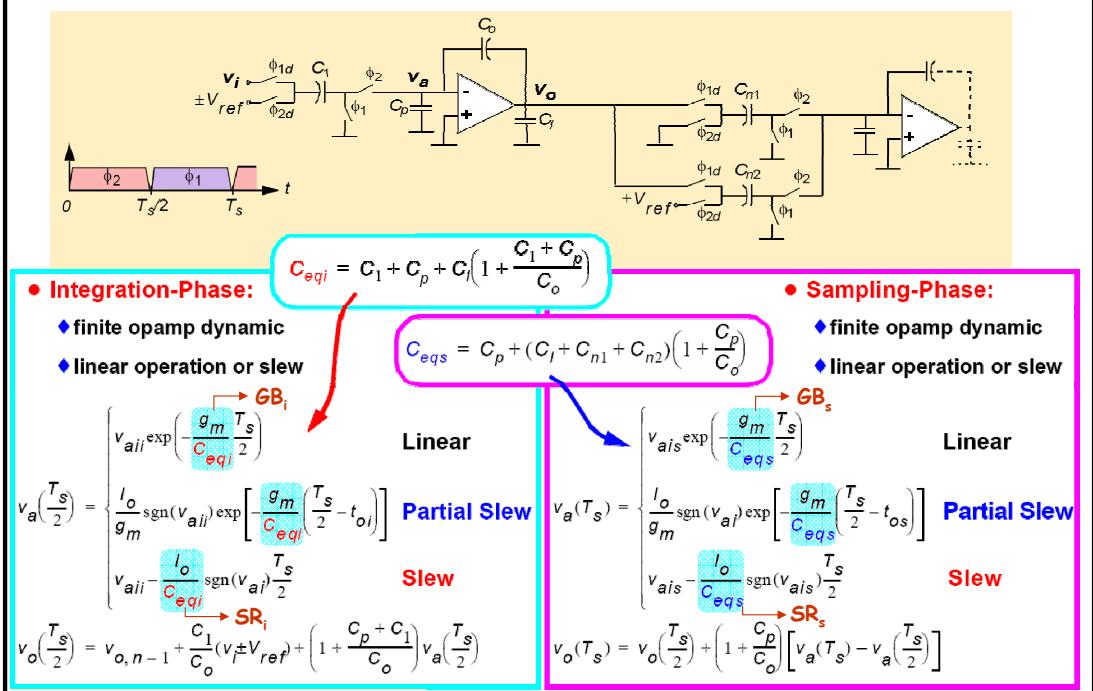
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



Integrator temporal evolution: [Rio00]



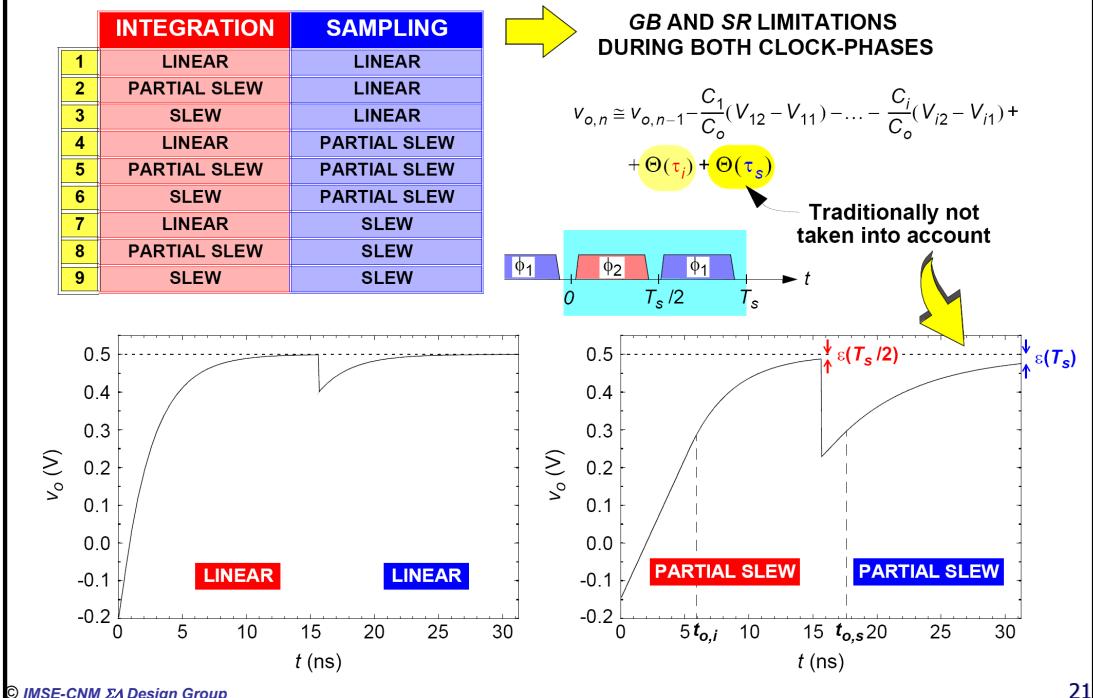
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



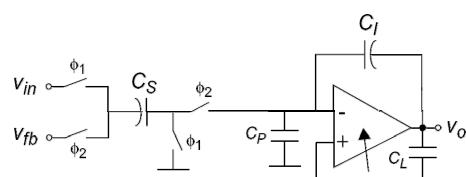
Integrator temporal evolution: [Rio00]



DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



Effect of the amplifier GB:

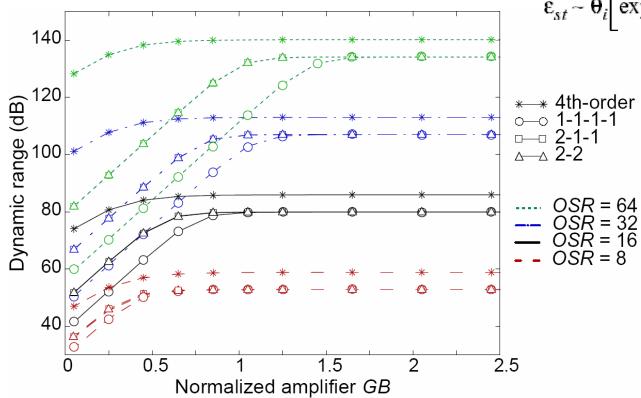


→ If only amplifier GB is considered (assuming no SR limitation)

$$GB_i = \frac{g_m}{C_{eq,i}} \quad GB_s = \frac{g_m}{C_{eq,s}}$$

$$v_o(z) = \frac{C_S}{C_I} \left(1 - \epsilon_{st} \right) \frac{z^{-1}v_{in}(z) - z^{-1/2}v_{fb}(z)}{1 - z^{-1}}$$

$$\epsilon_{st} \sim \theta_i \left[\exp \left(-GB_i \frac{T_s}{2} \right) \right] + \theta_s \left[\exp \left(-GB_s \frac{T_s}{2} \right) \right] + \theta_i \cdot \theta_s$$



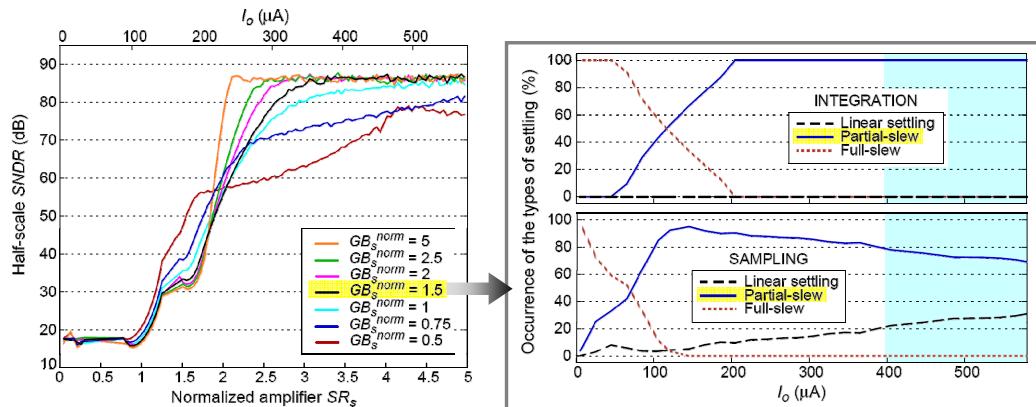
- Can be viewed as a systematic error in the integrator weight
- Effect on $\Sigma\Delta$ Ms similar to a mismatch between analog and digital coeffs
- It causes low-order noise leakages in cascade $\Sigma\Delta$ Ms

DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



■ Additional effect of the amplifier SR (+ GB):

- "Dominant" linear dynamics are not mandatory in order to fulfill specs
- SR can trade for GB
- It can be used to optimize the power consumption of amplifiers



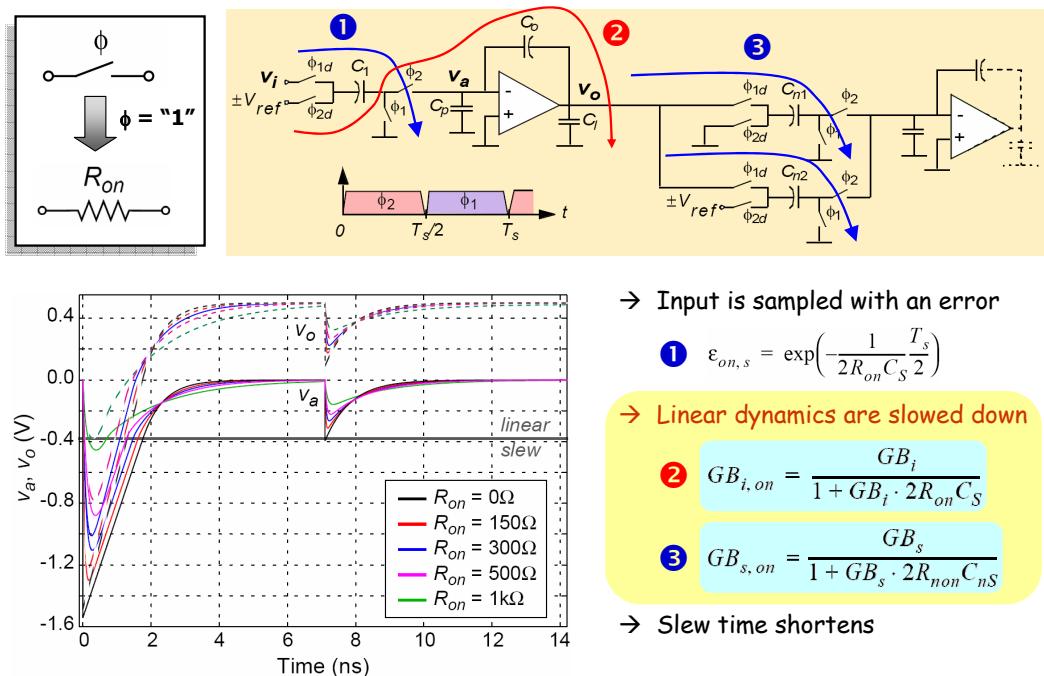
Non-linear dynamics cause distortion!

SR at the front-end integ must be carefully tackled

DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



■ Additional effect of the switches Ron (+ GB + SR):

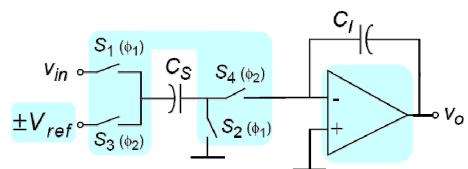
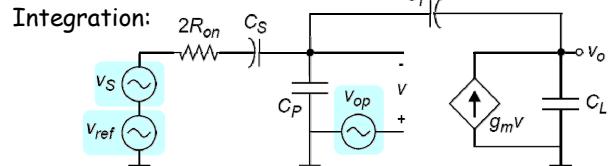
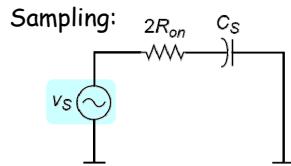


DT-ΣΔMs: Circuit Noise



Main noise sources in SC integrators:

- Switches → Thermal noise
- Amplifiers → Thermal and flicker noise
- References → Thermal and flicker noise



■ Noise contribution of the switches (input-referred):

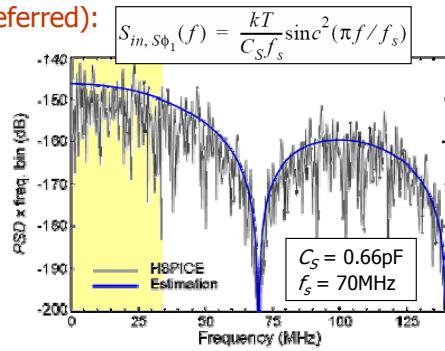
$$\text{Switches for sampling } S_S = 2kT \cdot 2R_{on}$$

$$H_{S\phi_1}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$$

$$BW_{n,S\phi_1} = \int_0^{+\infty} |H_{S\phi_1}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$$

$$S_{in,S\phi_1}(f) \cong \frac{2BW_{n,S\phi_1}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

← Aliased component [Fisc82]



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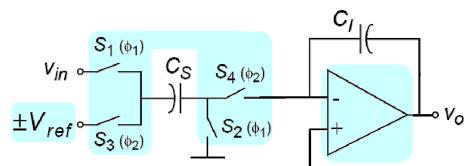
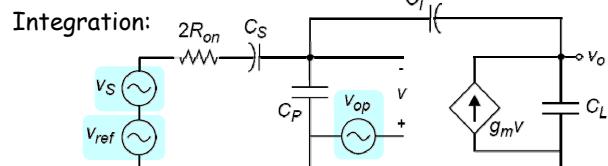
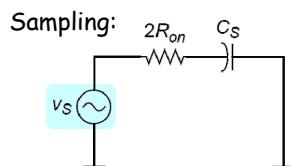
25

DT-ΣΔMs: Circuit Noise



Main noise sources in SC integrators:

- Switches → Thermal noise
- Amplifiers → Thermal and flicker noise
- References → Thermal and flicker noise



■ Noise contribution of the switches (input-referred):

$$\text{Switches for sampling } S_S = 2kT \cdot 2R_{on}$$

$$\text{Switches for integration } S_S = 2kT \cdot 2R_{on}$$

$$H_{S\phi_1}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$$

$$H_{S\phi_2}(s) = \frac{1 + s/z_1}{(1 + s/p_1)(1 + s/p_2)} \quad z_1 = \frac{g_m}{C} \quad p_1 \equiv \frac{g_m}{C_{eq,i}} \quad p_2 \equiv \frac{C_{eq,i}}{C} \cdot \frac{1}{2R_{on}C_S}$$

$$BW_{n,S\phi_1} = \int_0^{+\infty} |H_{S\phi_1}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$$

$$BW_{n,S\phi_2} = \int_0^{+\infty} |H_{S\phi_2}(f)|^2 df \cong \frac{p_2}{4} \approx \frac{1}{4 \cdot 2R_{on}C_S}$$

$$S_{in,S\phi_1}(f) \cong \frac{2BW_{n,S\phi_1}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

$$S_{in,S\phi_2}(f) \cong \frac{2BW_{n,S\phi_2}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

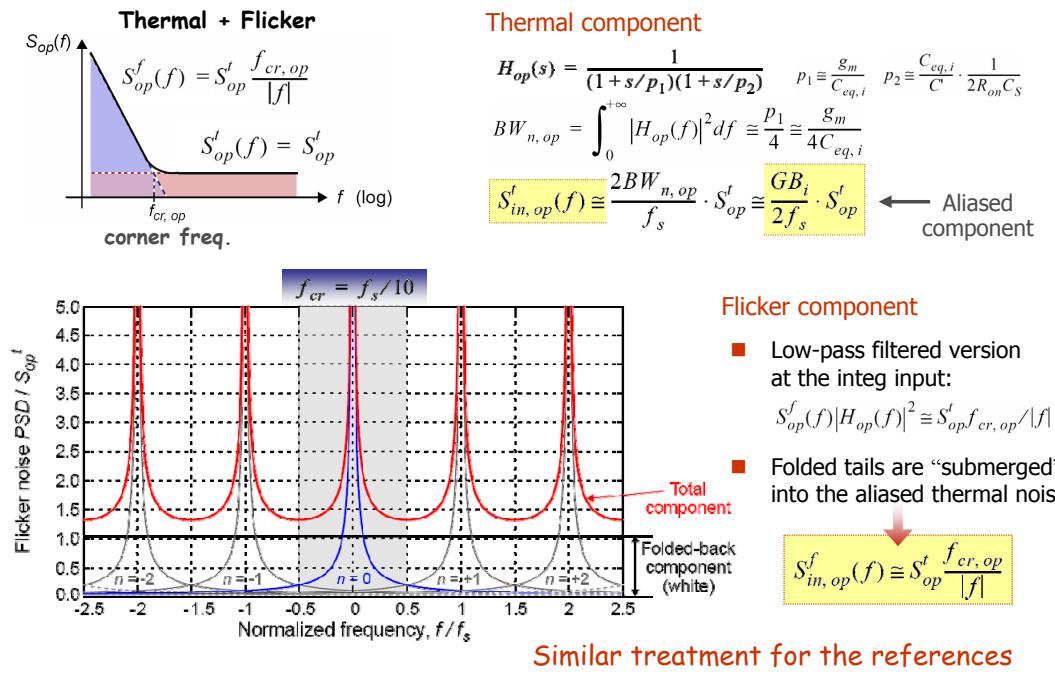
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DT- $\Sigma\Delta$ Ms: Circuit Noise



- Noise contribution of the amplifier (input-referred):



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DT- $\Sigma\Delta$ Ms: Circuit Noise



Total noise PSD for the front-end integ:

$$S_{eq, in}(f) \approx \underbrace{\frac{2kT}{C_S f_s}}_{\text{switches}} + \underbrace{S_{op}^t \left(\frac{GB_i}{2f_s} + \frac{f_{cr, op}}{|f|} \right)}_{\text{amplifier}} + \underbrace{S_{ref}^t \left(\frac{GB_{ref}}{2f_s} + \frac{f_{cr, ref}}{|f|} \right)}_{\text{references}}$$

Switches:

- kT/C is the ultimate limitation on the converter resolution
- It can only be decreased by increasing C_S and/or f_s (it does not depend on R_{on} !)
- $\times 2$ in fully-diff implementations (3-dB increase, but signal power is 6dB larger!)

Amplifiers & References:

- GBs should be as low as settling errors allow (reduces folding!)
- 1/f contributions decrease with the corner frequency
- Adequate techniques can be applied in low-freq apps: CDS, chopper, ... [Enz96]

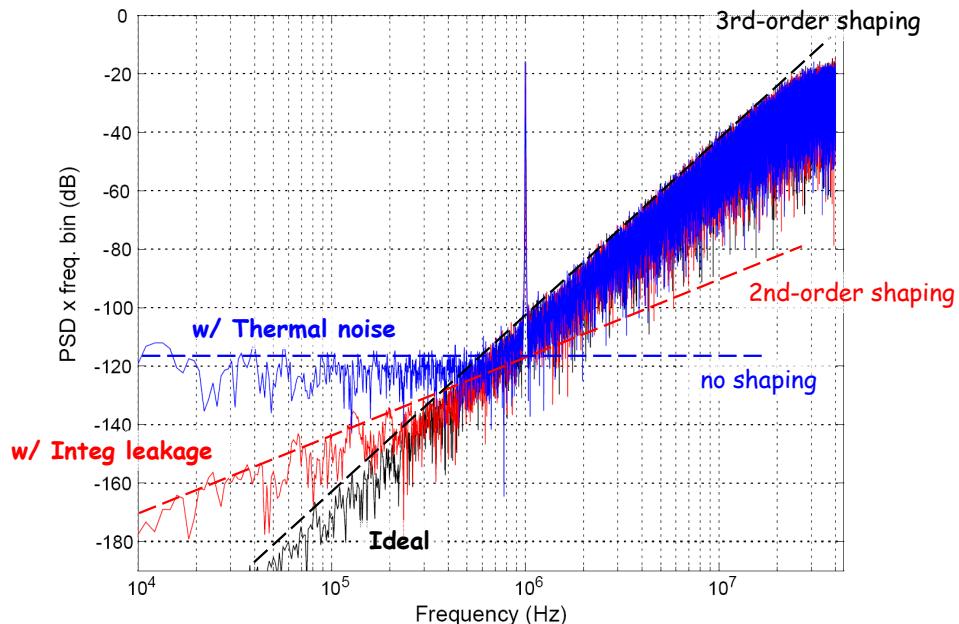
$$P_{CN, in} \approx \left[\frac{2kT}{C_S} + S_{op}^t \frac{GB_i}{2} + S_{ref}^t \frac{GB_{ref}}{2} \right] \frac{1}{OSR} + 2 \ln \left(\frac{f_b}{f_o} \right) (S_{op}^t f_{cr, op} + S_{ref}^t f_{cr, ref})$$

In-band error power due to circuit noise in the $\Sigma\Delta$ M

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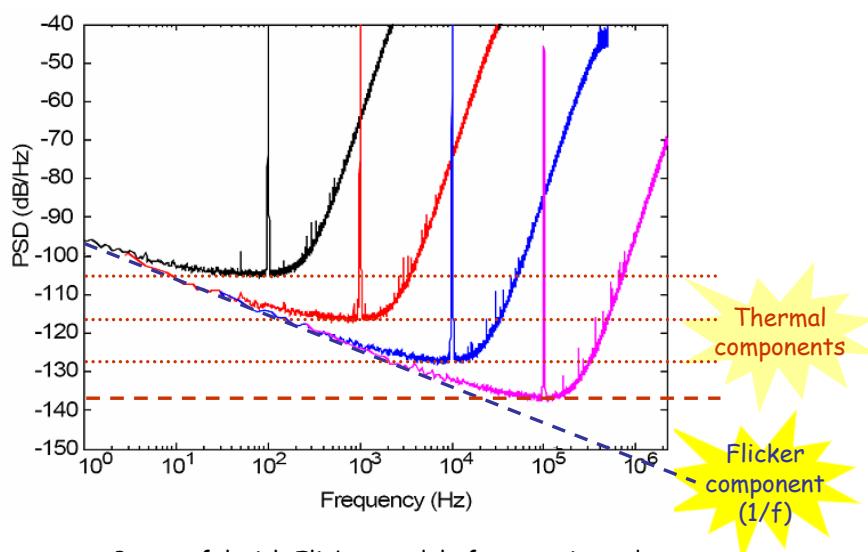
Effect of noise leakages and thermal noise on a 2-1 cascade



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Effect of 1/f and thermal noise on the spectra of a 4th-order $\Sigma\Delta$ M
(silicon results for several fs)



Be careful with Flicker models for transistors!
Front-end amplifier needed redesign!

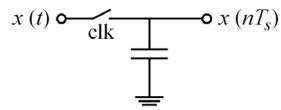
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DT-ΣΔMs: Clock Jitter



- Sampling time uncertainty [Boser88]:

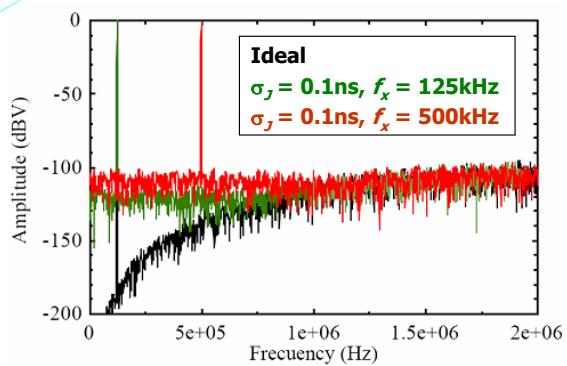
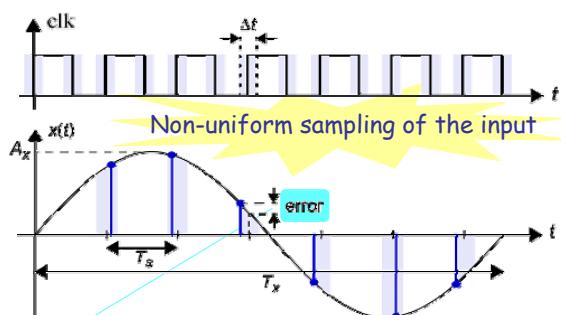


→ If jitter is modeled as random:

$$S_J = \frac{A_x^2 (2\pi f_x \sigma_j)^2}{2 f_s}$$

$$P_J = \frac{A_x^2 (2\pi f_x \sigma_j)^2}{2 OSR}$$

Error is larger, the larger input freq (wideband apps!)



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DT-ΣΔMs: Non-linearity of Capacitors



- In an ideal capacitor: $dq = Cdv$
- In practice: $dq = C(v)dv$, with C being voltage-dependent

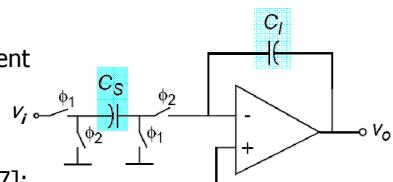
$$C(v) = C(1 + a_1 v + a_2 v^2 + \dots)$$

→ Considering the effect of the sampling cap only [Bran97]:

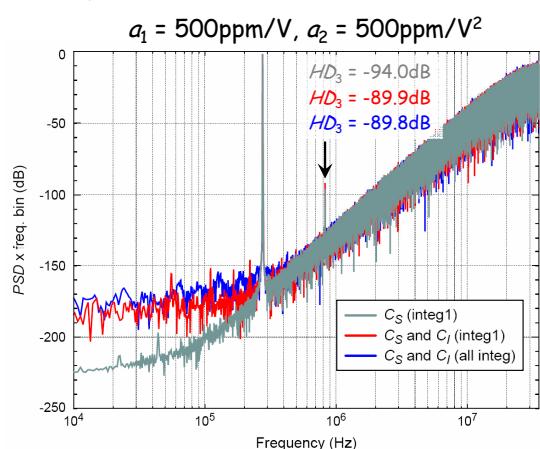
$$v_{o,n} \approx v_{o,n-1} + g_1 v_{in,n-1} \left(1 + \frac{a_1}{2} v_{in,n-1} + \frac{a_2}{3} v_{in,n-1}^2 \right)$$

$$A_2 \approx \frac{1}{2} \left(\frac{a_1}{2} A_x^2 \right) \Rightarrow HD_2 \approx 20 \log_{10} \left(\frac{a_1}{4} A_x \right)$$

$$A_3 \approx \frac{1}{4} \left(\frac{a_2}{3} A_x^3 \right) \Rightarrow HD_3 \approx 20 \log_{10} \left(\frac{a_2}{12} A_x^2 \right)$$



- Even-order distortion cancels w/ fully-diff
- Non-linearity of sampling cap dominates
- Valid for weak non-linearities (MOS caps are very non-linear!)



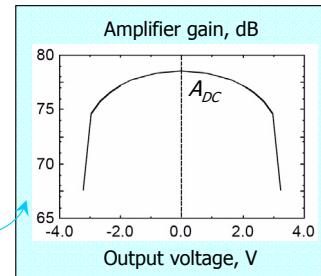
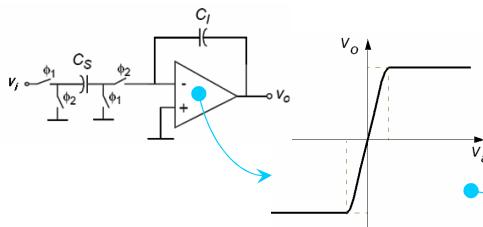
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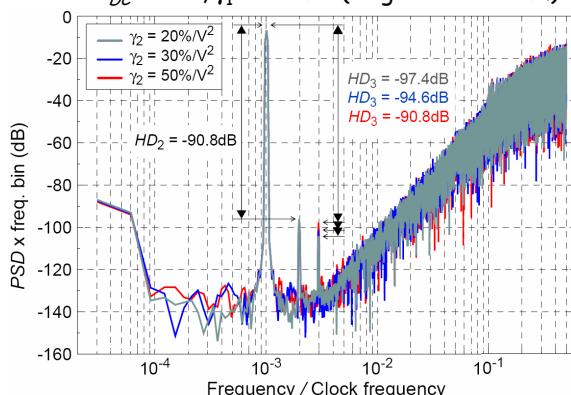
DT- $\Sigma\Delta$ M: Non-linear Amplifier Gain



→ Actual amplifier gain depends on output voltage:



$$A_{DC} = 500, \gamma_1 = 10\%/\text{V} \text{ (single-ended } \Sigma\Delta\text{M)}$$



$$A_{DC}(v_o) = A_{DC}(1 + \gamma_1 v_o + \gamma_2 v_o^2 + \dots)$$

$$HD_2 \cong 20 \log_{10} \left(\frac{\gamma_1 (1+g)}{2} g A_x \right)$$

$$HD_3 \cong 20 \log_{10} \left(\frac{\gamma_2 (1+g)}{4} g^2 A_x^2 \right) \quad [\text{Yin94}]$$

- Increasing A_{DC} helps a lot!
- A_{DC} at the front-end larger than noise leakages require

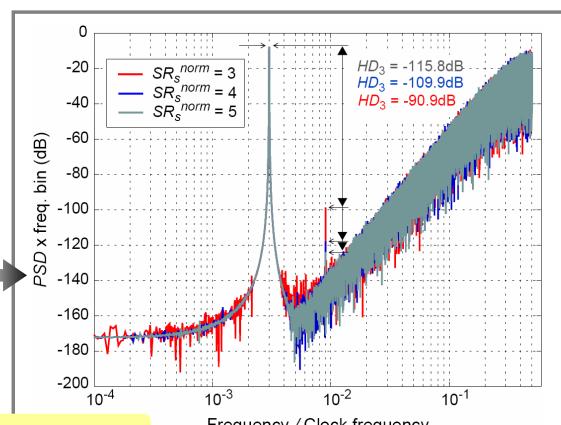
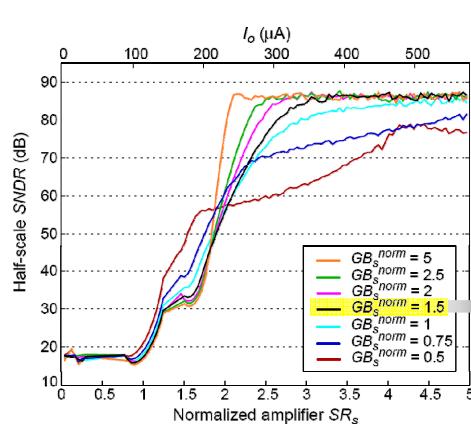
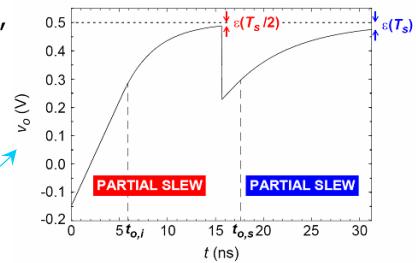
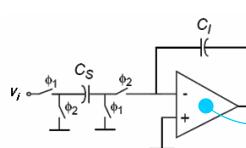
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DT- $\Sigma\Delta$ M: Non-linear Settling



→ SR can trade for GB in the integrator settling, but non-linear dynamics cause distortion:



SR at the front-end larger than settling requires

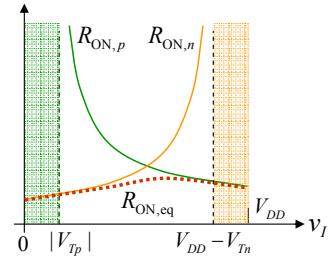
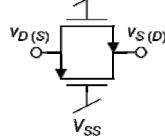
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DT- $\Sigma\Delta$ Ms: Non-linear Switch Resistance



→ Switches exhibit a finite R_{ON} which is also non-linear:

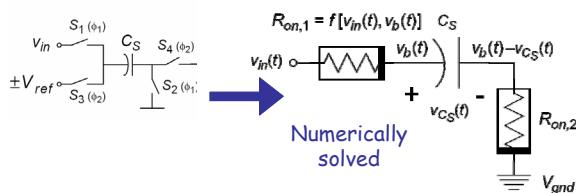


$$R_{ON,n} = \frac{1}{k'_n \left(\frac{W}{L}\right)_n (V_{DD} - v_I - V_{Th})}$$

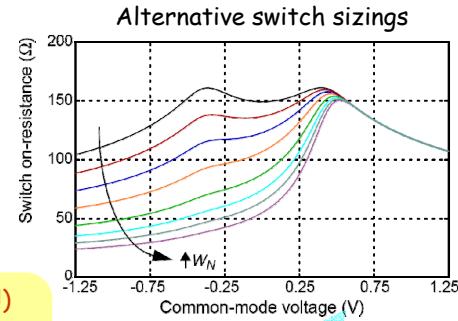
$$R_{ON,p} = \frac{1}{k'_p \left(\frac{W}{L}\right)_p (v_I - |V_{Tp}|)}$$

$$R_{ON,eq} = R_{ON,n} // R_{ON,p}$$

■ Non-linear sampling [Geer02]:



- Distortion is dynamic (increases with input freq!)
- Front-end switch dominates
- R_{ON} at the front-end smaller than settling requires
- Very important in low-voltage!



Most suited sizing depends on parasitics, Vref/Vsupply, ...

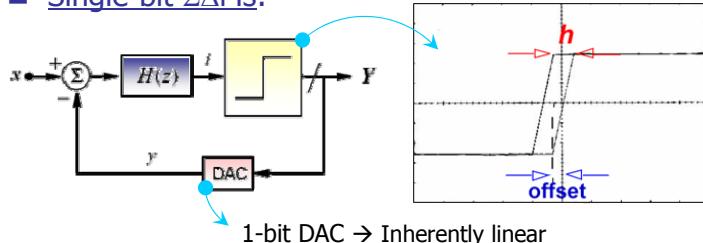
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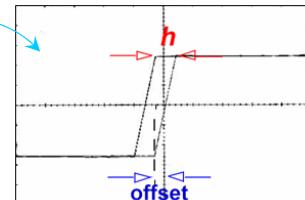
DT- $\Sigma\Delta$ Ms: Comparators and Multi-bit Quantizers



■ Single-bit $\Sigma\Delta$ Ms:



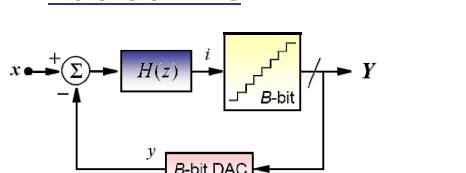
Comparator:



- **Offset** → Attenuated by the integrator DC gain
- **Hysteresis** → Shaped similarly to quantization error [Boser88]

$$P_h = 4h^2 \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

■ Multi-bit $\Sigma\Delta$ Ms:



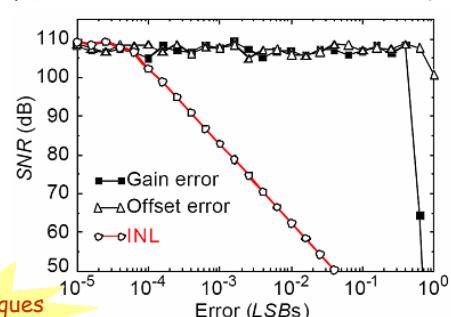
Multi-bit ADC → Errors attenuated/shaped

Multi-bit DAC → Non-linearity directly added to the input!

$$[\text{Mede99}]: \sigma_D^2 = \frac{1}{2} \left(\frac{\Delta}{2^B - 1} \right)^2 \text{INL}_{\text{LSB}}^2$$

DEM techniques
Dual quantization

Effect of DAC errors on a 2nd-order 3-bit $\Sigma\Delta$ M



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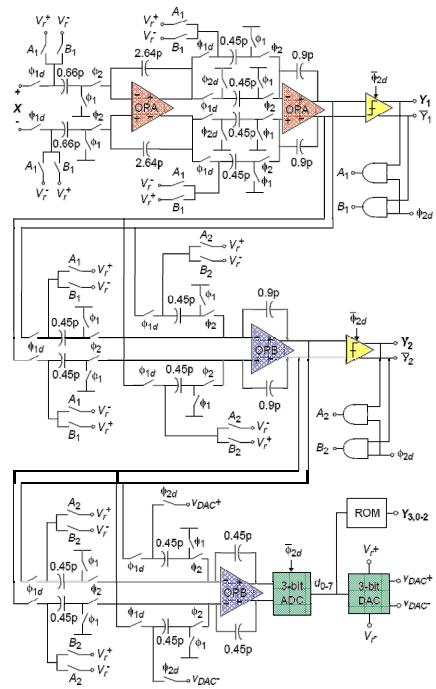
DT- $\Sigma\Delta$ Ms: Case Study



- A case study: A 2.5-V Cascade $\Sigma\Delta$ M in CMOS 0.25um for ADSL/ADSL+

2-1-1 w/ dual quantization

- Two different amplifiers: 2-stage OA in the 1st stage, and 1-stage OA in 2nd and 3rd stages.
- Standard CMOS switches (no clock-boosting).
- Only 2-branch integrators and 2x16 unit capacitors (MiM).
- Comparators: regenerative latch + preamplification stage.
- 3-bit quantizer in the last stage:
 - Resistive-ladder DAC (no calibration).
 - Flash ADC: Static differential input stage + latched comparators.
- Power-down control.



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DT- $\Sigma\Delta$ Ms: Case Study



Blocks Specs

EQUATION DATABASE

	Typical	Worst Case
Quantization noise	-88.1dB	-86.2dB
Id corner analysis:	-90.3dB	
DC gain	16dB	
Cap. mismatch leakage	-95.4dB	-89.4dB
($\sigma_C = 0.05\%$) variation in the 2.5-V supply		
DAC error	-96.4dB	
Thermal noise	-84.8dB	-82.2dB
kT/C noise	-88.1dB	-86.0dB
Amplifier noise	-87.5dB	-84.5dB
Clock jitter	-90.1dB	
In-band error power	-82.3dB	-80.3dB
Dynamic range	82.8dB (13.5bit)	80.8dB (13.1bit)

MODULATOR	Topology	2-1-1(3b)
	Oversampling ratio	16
	Reference voltage	1.5V
	Clock frequency	70.4MHz
	Clock jitter	15ps (0.1%)
FRONT-END INTEGRATOR	Sampling capacitor	0.66pF
	Cap. sigma (MiM, 1pF)	0.05%
	Cap. tolerance	$\pm 20\%$
	Bottom parasitic cap.	1%
	Switch on-resistance	150 Ω
AMPLIFIER	DC gain	3000 (70dB)
	GB (1.5pF)	265MHz
	Slew rate (1.5pF)	800V/ μ s
	Output swing	$\pm 1.8V$
	Input equivalent noise	6nV/sqrt(Hz)
COMPARATORS	Hysteresis	20mV
	Offset	$\pm 10mV$
	Resolution time	3ns
3-bit QUANTIZER	DAC I/NL	0.5%FS

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DT- $\Sigma\Delta$ Ms: Case Study

	Typical	Worst Case
Quantization noise	-88.1dB	-86.2dB
Ideal	-90.3dB	
DC gain leakage	-99.8dB	
Cap. mismatch leakage ($\sigma_C = 0.05\% \mid 0.1\%$)	-95.4dB	-89.4dB
DAC error	-96.4dB	
Thermal noise	-84.8dB	-82.2dB
kT/C noise	-88.1dB	-86.0dB
Amplifier noise	-87.5dB	-84.5dB
Clock jitter	-90.1dB	
In-band error power	-82.3dB	-80.3dB
Dynamic range	82.8dB (13.5bit)	80.8dB (13.1bit)

MODULATOR	Topology	2-1-1(3b)
	Oversampling ratio	16
	Reference voltage	1.5V
	Clock frequency	70.4MHz
	Clock jitter	15ps (0.1%)
FRONT-END INTEGRATOR	Sampling capacitor	0.66pF
	Cap. sigma (MiM, 1pF)	0.05%
	Cap. tolerance	$\pm 20\%$
	Bottom parasitic cap.	1%
	Switch on-resistance	150 Ω
AMPLIFIER	DC gain	3000 (70dB)
	GB(1.5pF)	265MHz
	Slew rate (1.5pF)	800V/ μ s
	Output swing	$\pm 1.8V$
	Input equivalent noise	6nV/sqrt(Hz)
COMPARATORS	Hysteresis	20mV
	Offset	$\pm 10mV$
	Resolution time	3ns
3-bit QUANTIZER	DAC I/NL	0.5%FS

DT- $\Sigma\Delta$ Ms: Case Study

Integrator Dynamics

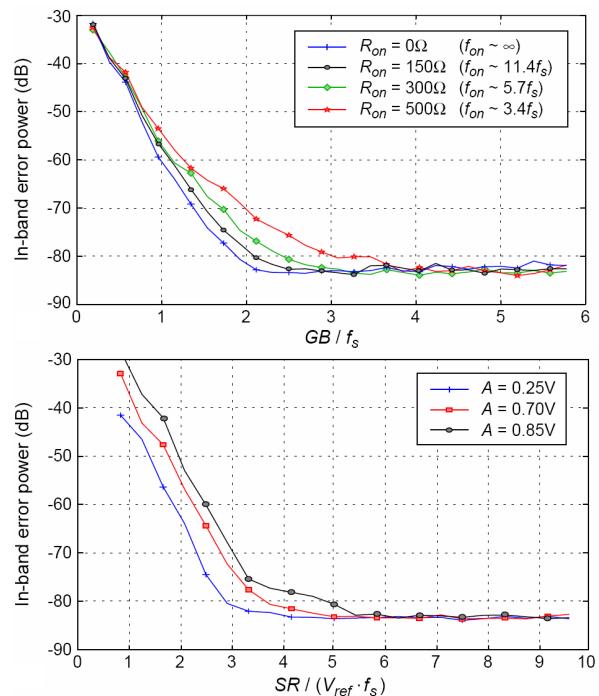
- $GB > 2.5f_s$ is ideally enough to limit settling errors (this architecture w/ OSR = 16).
- Switch on-resistance slows down the effective amplifier response:

$$GB_{eff} \cong \frac{GB}{1 + GB/f_{on}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_{on}C_S}$$

$R_{on} \sim 150\Omega$ requires just $GB > 3.2f_s$

Standard switches $GB = 265MHz$
(no clock-boosting) (assuming that 85% of the clock cycle is useful)

- Slew rate must be large enough to let the linear dynamic to correctly settle.
 $SR/(V_{ref} \cdot f_s) = 6.5 \rightarrow SR = 800V/\mu s$
- Partially slew-rate limited operation of the front-end integrator introduces distortion.



DT- $\Sigma\Delta$ Ms: Case Study

Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)		265MHz	210MHz	
Slew rate (1.5pF)		800V/ μ s	350V/ μ s	
Output swing		$\pm 1.80V$	$\pm 1.60V$	
Input equivalent noise	6nV/sqrt(Hz)		50nV/sqrt(Hz)	

OPA

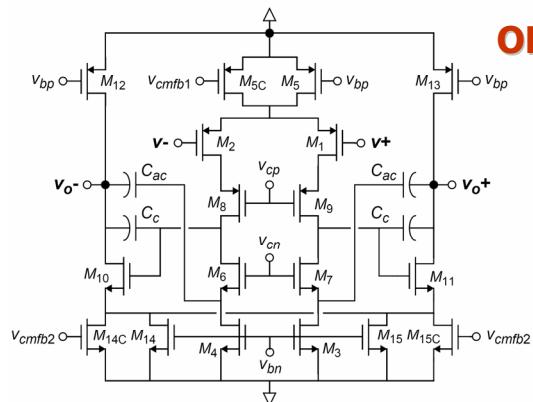
OPB

- SC CMFB nets
- pMOS input scheme
Cancelled body effect
(substrate noise coupling)
- Smaller 1/f noise

DT- $\Sigma\Delta$ Ms: Case Study

Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)		265MHz	210MHz	
Slew rate (1.5pF)		800V/ μ s	350V/ μ s	
Output swing		$\pm 1.80V$	$\pm 1.60V$	
Input equivalent noise	6nV/sqrt(Hz)		50nV/sqrt(Hz)	



OPA 2-stage amplifier Telescopic 1st stage
2-path compensation

	Typical	Worst Case
DC gain	78.6dB	73.5dB
GB (1.5pF)	446.8MHz	331.5MHz
PM (1.5pF)	64.0°	57.9°
SR (1.5pF)	1059V/ μ s	883V/ μ s
Output swing	$\pm 2.09V$	$\pm 1.86V$
Input eq. noise	5.1nV/sqrt(Hz)	5.5nV/sqrt(Hz)
Input capacitance	126fF	129fF
Power consumption	17.2mW	19.4mW

DT- $\Sigma\Delta$ Ms: Case Study



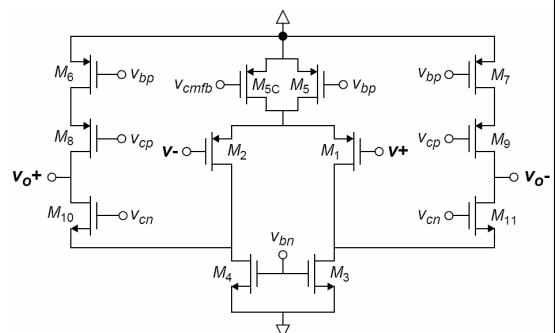
Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)		265MHz	210MHz	
Slew rate (1.5pF)		800V/ μ s	350V/ μ s	
Output swing		$\pm 1.80V$	$\pm 1.60V$	
Input equivalent noise		6nV/sqrt(Hz)	50nV/sqrt(Hz)	

- SC CMFB nets
- pMOS input scheme
- Cancelled body effect
(substrate noise coupling)
- Smaller 1/f noise

OPB folded-cascode amplifier

	Typical	Worst Case
DC gain	58.0dB	56.8dB
GB (1.5pF)	393.5MHz	331.7MHz
PM (1.5pF)	70.3°	67.7°
SR (1.5pF)	377V/ μ s	373V/ μ s
Output swing	$\pm 1.97V$	$\pm 1.72V$
Input eq. noise	4.1nV/sqrt(Hz)	5.1nV/sqrt(Hz)
Input capacitance	300fF	343fF
Power consumption	6.6mW	6.9mW



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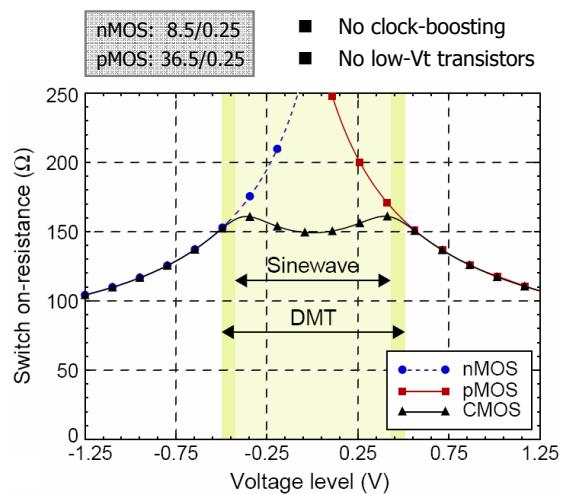
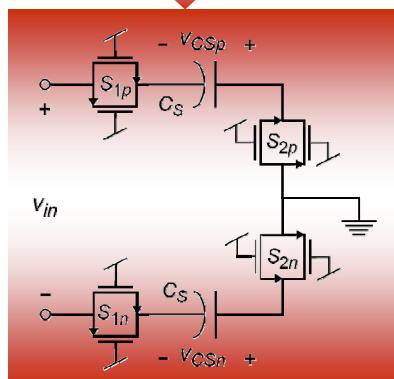
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Switch on-resistance

- Slow-down of the integrators dynamics
- Incomplete sampling (RC time constant)
- Dynamic distortion (front-end integrator)

Standard CMOS switches



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DT- $\Sigma\Delta$ Ms: Case Study

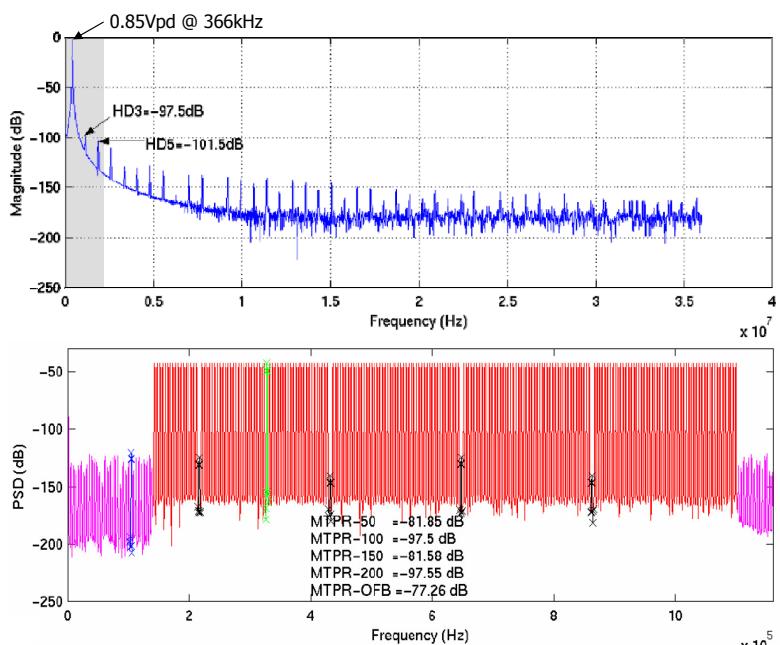
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Switch on-resistance

Dynamic distortion
evaluated through
electrical simulation

■ Sinewave input

THD < -96dB



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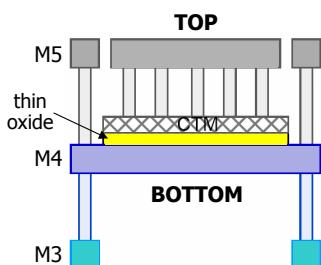
DT- $\Sigma\Delta$ Ms: Case Study

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MiM capacitors

CMOS tech with
mixed-signal facilities

Thin oxide between
metal 4 and metal 5



Cap. matching	0.05% (1pF)
Bottom plate parasitic	1%
Cap. spread	$\pm 20\%$

→ Very good matching (0.1% assumed for 6- σ design)

→ Helps to limit the capacitive load to integrators

→ Integrators weights:

- Front-end integ, 0.66pF: $27\mu\text{m} \times 27\mu\text{m}$
- Remaining integs, 0.45pF: $22\mu\text{m} \times 22\mu\text{m}$

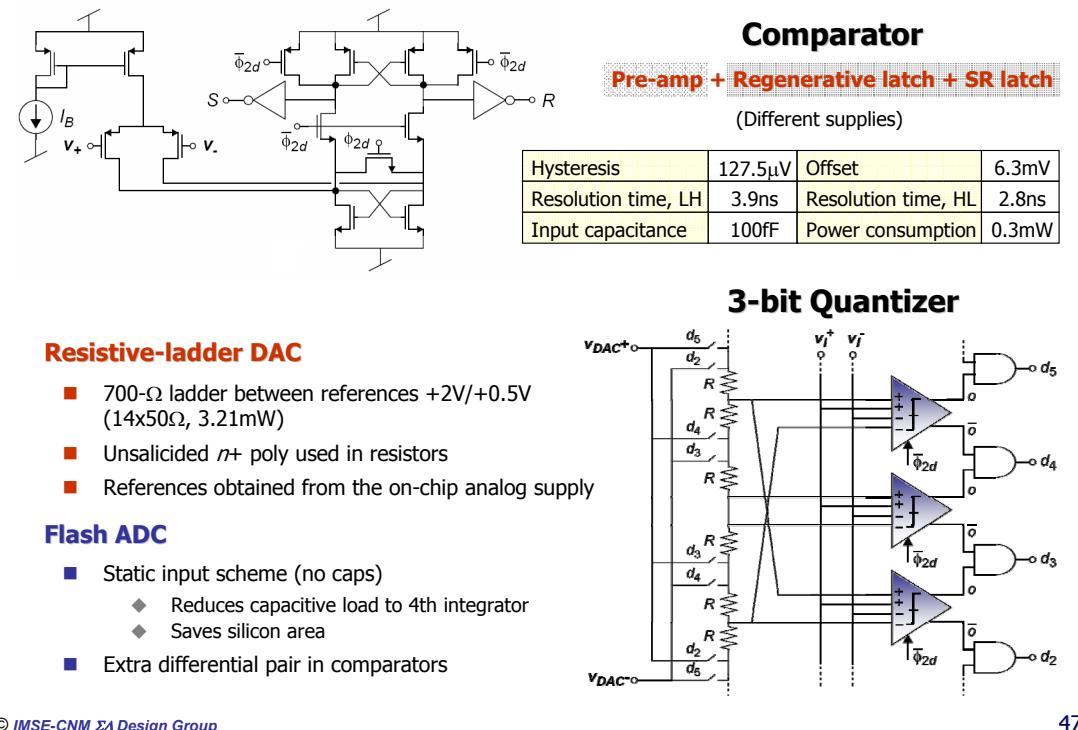
→ Also MiM caps in OPA, in the SC CMFB nets, and in the anti-aliasing filter

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DT- $\Sigma\Delta$ Ms: Case Study

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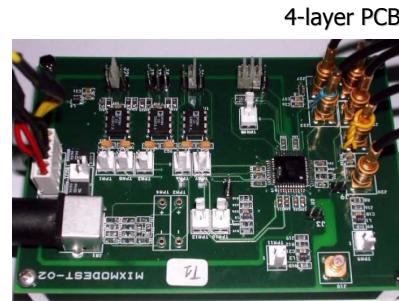
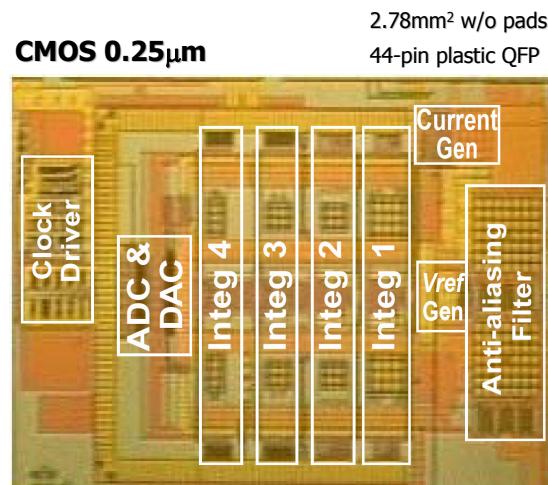
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DT- $\Sigma\Delta$ Ms: Case Study

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CENTRO INVESTIGACIONES Y ESTUDIOS AVANZADOS

Layout & Prototyping



- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

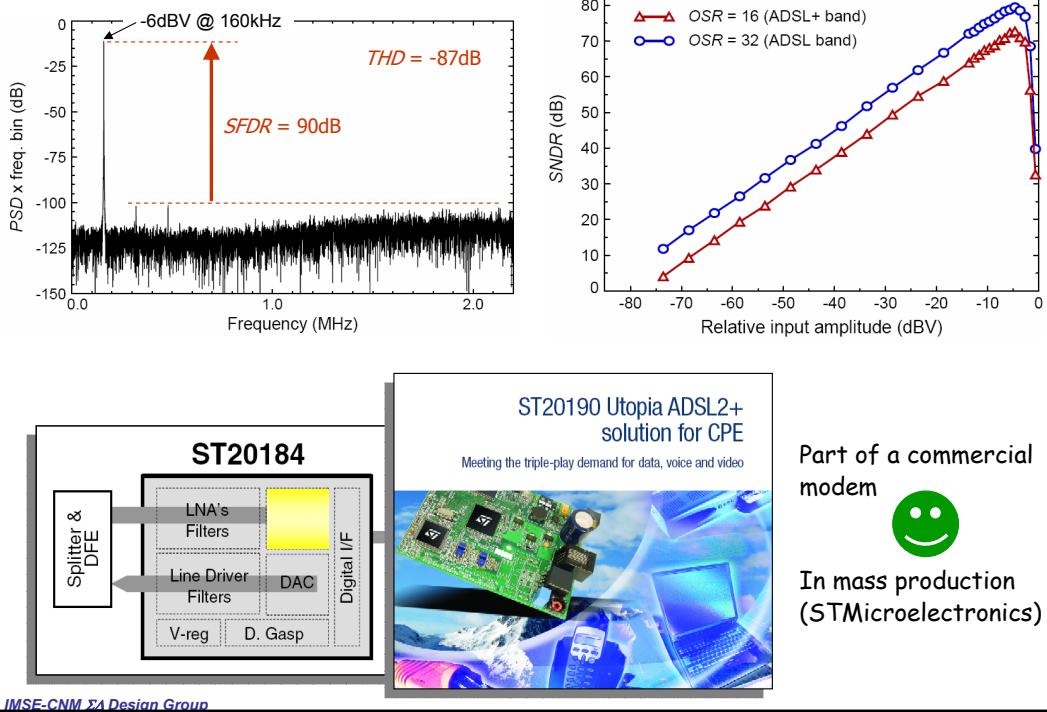
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DT- $\Sigma\Delta$ M: Case Study

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Experimental results



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CT- $\Sigma\Delta$ M : Overview of CT- $\Sigma\Delta$ M Non-idealities

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CT- $\Sigma\Delta$ M Non-Idealities

Building-block Errors

- Opamp finite (non-linear) DC gain
- Integrator transient response
- Element tolerances
- Time-constant error
- Non-linearity (Front-end V-I and DAC)
- Noise

Architectural Timing Errors

- Quantizer metastability
- Excess loop delay
- Clock jitter

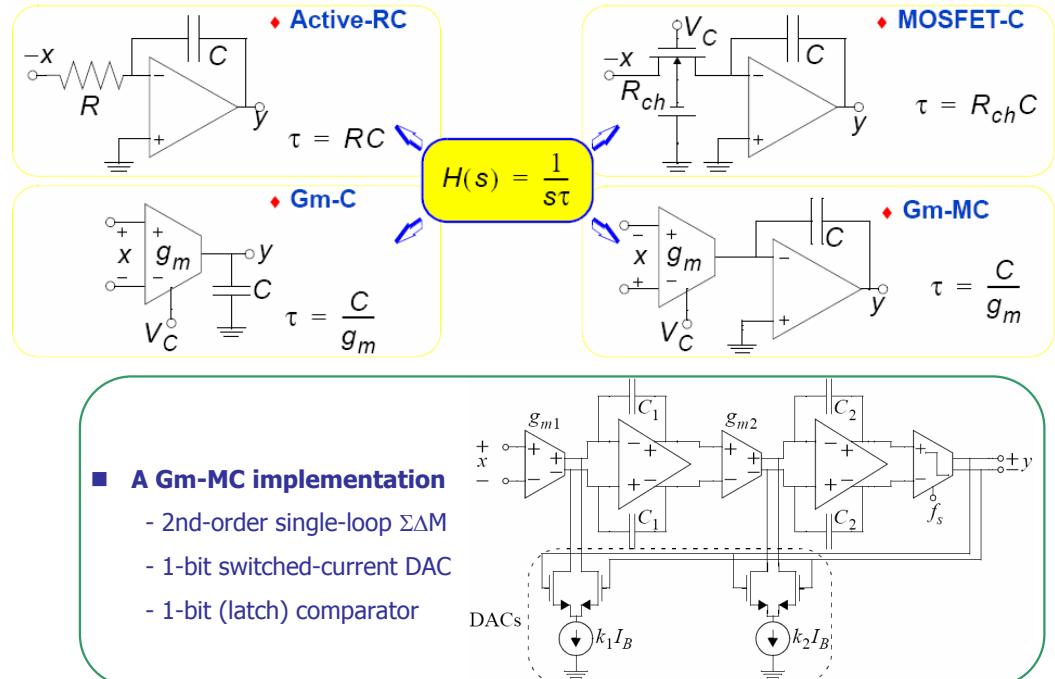
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CT- $\Sigma\Delta$ Ms: Basic building blocks



□ Basic building blocks – CT Integrators



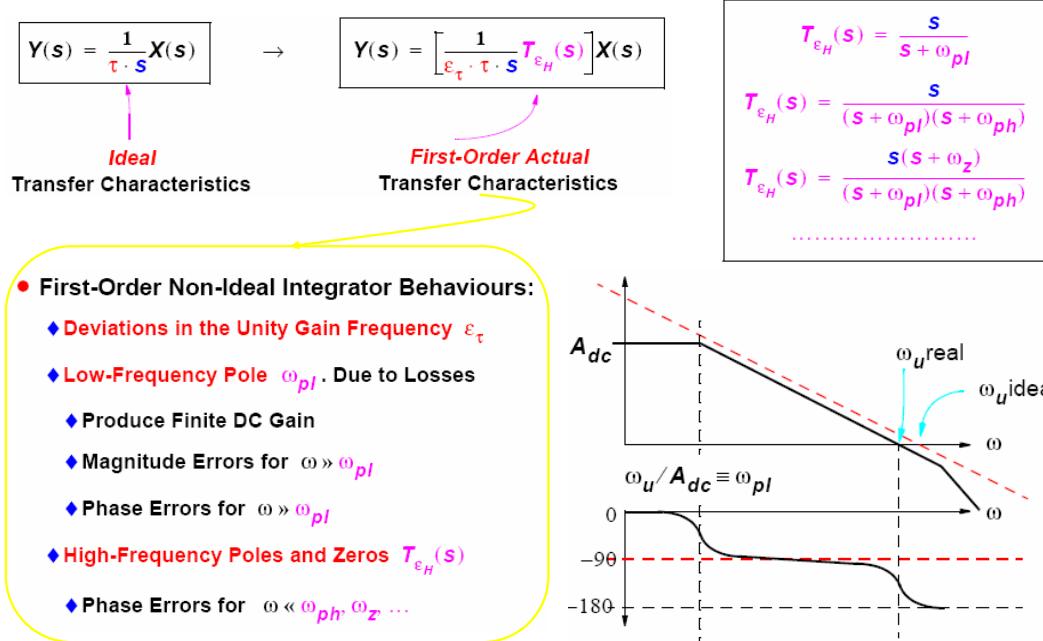
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CT- $\Sigma\Delta$ Ms: Non-ideal Integrator Transfer Function



□ Integrator Transfer Function (ITF) degraded by circuit non-idealities



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CT- $\Sigma\Delta$ M: Effect of finite DC gain error



Opamp finite DC gain (I)

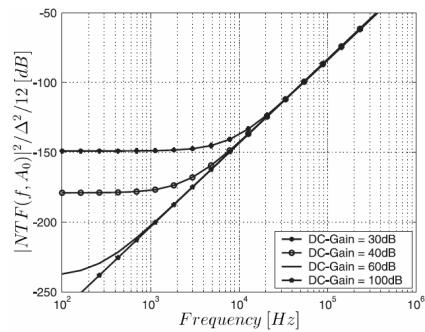
RC	MOSFET-C	Gm-C	Gm-MC
$\omega_{pl} < \frac{G}{C \cdot A_0} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{G_{ch}}{C \cdot A_0} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{\omega_u G_{go}}{\varepsilon_T G_m} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{G_{go}}{C \cdot A_0} = \frac{\omega_u G_{go}}{A_0 G_m} = \frac{\omega_u}{A_0}$

RC integrators [Gerd03]

$$\text{ITF}(s) = \frac{\alpha/\tau}{s + \gamma} \quad \alpha = \frac{A_0}{1 + A_0} \quad \gamma = \frac{1/\tau}{1 + A_0}$$

- Same IBN degradation as in SC $\Sigma\Delta$ Ms ($\tau = 1/f_s$)

$$P_{A_0} = \frac{\Delta^2}{12k_1^2 k_q^2} \left[\frac{1}{A_0^{2L} M} + \sum_{m=1}^L \frac{\pi^{2L} L(L-1)\dots(L-m+1)}{(2m+1)M^{2L+1} A_0^{2(L-m)} m!} \right]$$



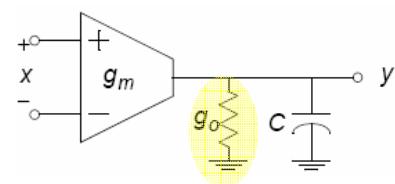
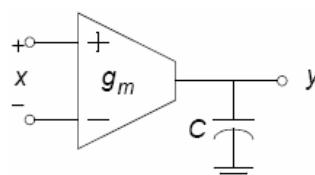
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CT- $\Sigma\Delta$ M: Effect of finite DC gain error



Opamp finite DC gain (II) – Gm-C integrators

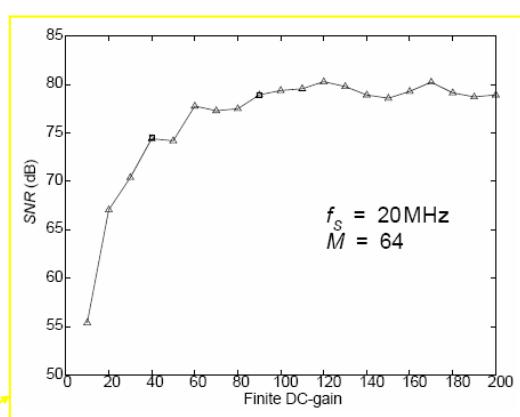


Power Spectral Density of an L th-order $\Sigma\Delta$ M

$$S_Q(f) = \left[\sum_{i=0}^{L-1} \binom{L}{i} \left(\frac{j\omega}{\omega_{pl}} \right)^i \right]^2 \cdot \frac{\Delta^2}{12 \cdot A_{dc}^{2L} \cdot f_s}$$

Relative increase of P_Q in a 2nd-order $\Sigma\Delta$ M

$$\frac{P_Q}{P_Q|_{A_{dc} \rightarrow \infty}} \approx \frac{5}{\pi^2} \left(\frac{M}{A_{dc}} \right)^4 + \frac{10}{3\pi^2} \left(\frac{M}{A_{dc}} \right)^2 + 1$$



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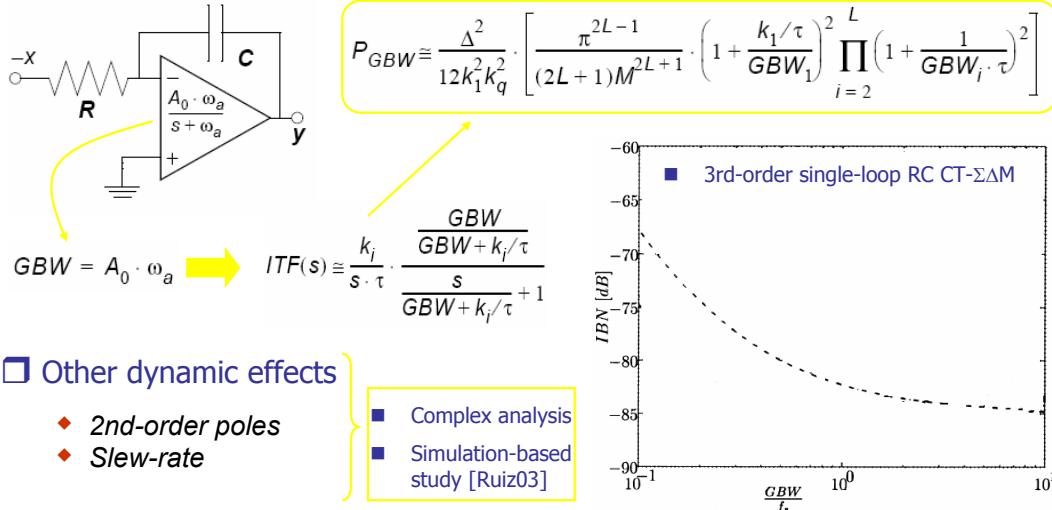
CT- $\Sigma\Delta$ Ms: Integrator transient response



☐ Integrator transient response (I)

- ♦ Less critical than in DT $\Sigma\Delta$ Ms
- ♦ Need to be taken into account, specially in broadband applications

☐ Influence of GBW [Geff03]



☐ Other dynamic effects

- ♦ 2nd-order poles
- ♦ Slew-rate

- Complex analysis
- Simulation-based study [Ruiz03]

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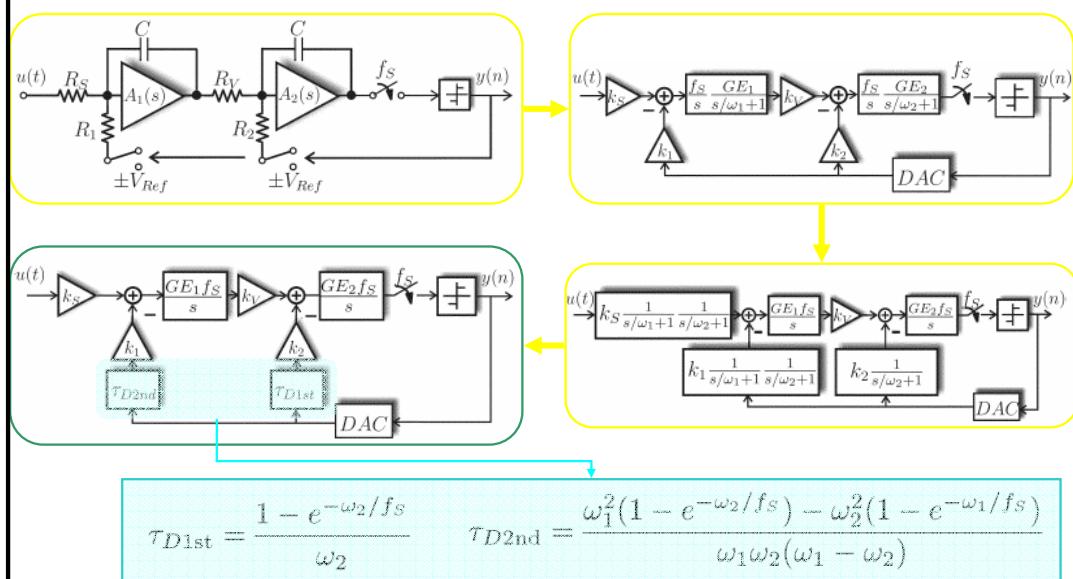
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CT- $\Sigma\Delta$ Ms: Integrator transient response



☐ Model of GBW for RC-active based CT- $\Sigma\Delta$ Ms [Ortm04]

- ♦ Modeled as a gain error (GE) and extra loop delay
- ♦ Each delay is different for each feedback path



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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Element tolerances

- ◆ Scaling coefficients accuracy limited by random errors in resistors/capacitors

$$\frac{\Delta \tau}{\tau} = \frac{\Delta C}{C} - \frac{\Delta g_m}{g_m} \quad \Rightarrow \quad \sigma_\tau = \sqrt{\sigma_C^2 + \sigma_{g_m}^2}$$

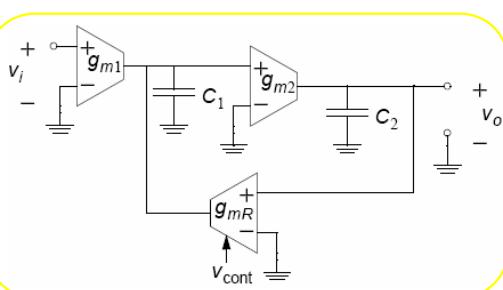
- ◆ Especially critical in:

- High-order single-loop architectures (instability)
- Cascade architectures (analog/digital coefficient ratios)

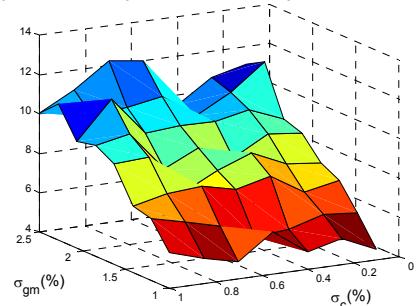
- ◆ Two types of random errors:

- Absolute tolerances: variations from chip to chip (10-20%)
- Relative mismatches: variations from device to device on one chip (0.5-1%)

■ Electrical control of frequency tuning



■ System-level optimization and synthesis method



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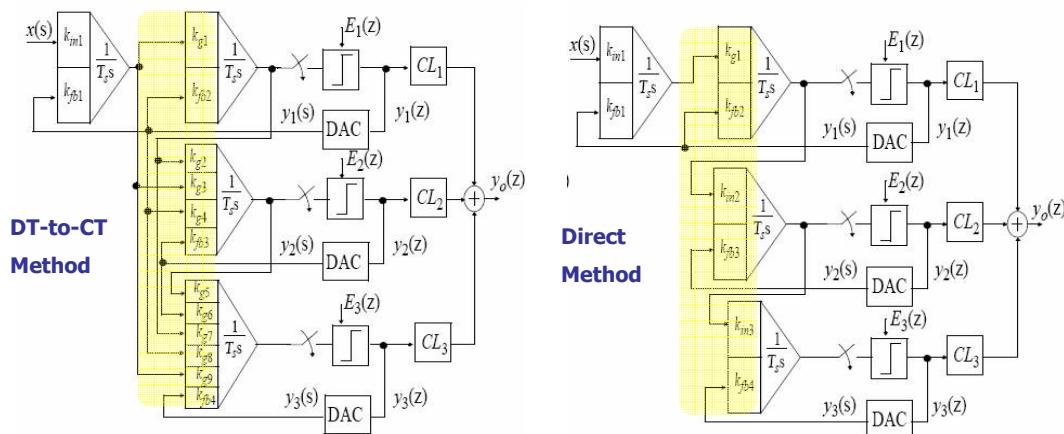
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Direct synthesis method of CT cascade architectures [Tort06]:

- ◆ Optimum placement of poles/zeroes of the NTF
- ◆ Synthesis of both analog and digital part of the cascade CT $\Sigma\Delta$ Modulator
- ◆ Reduced number number of analog components
- ◆ Reduced sensitivity to element tolerances



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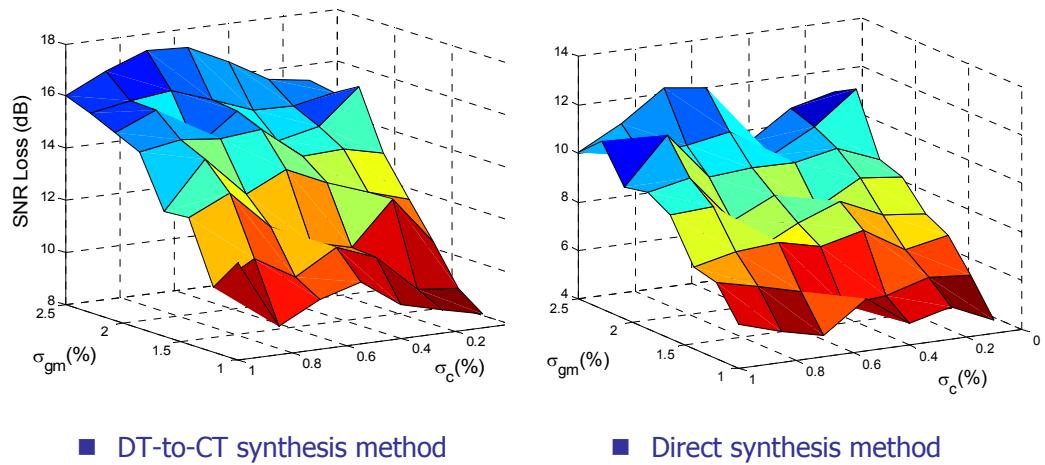
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Direct synthesis of cascade architectures (I) [Tort06]

- ◆ Sensitivity to mismatch (gm, C)
- ◆ A 2-1-1 example



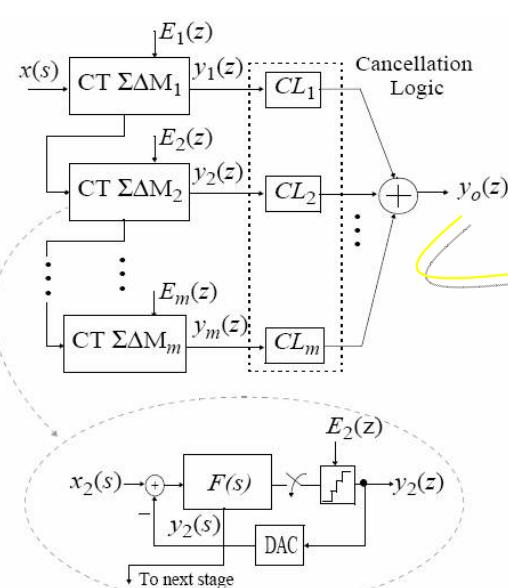
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Direct synthesis of cascade architectures (II) [Tort06]



$$y_o(z) = \sum_{k=1}^m y_k(z) CL_k(z)$$

$$E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)$$

$$y_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{kk}}$$

$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}}$$

$$\left[Z_{km} \equiv Z \left(L^{-1} (H_D F_{km}) \Big|_{n T_s} \right) \right]$$

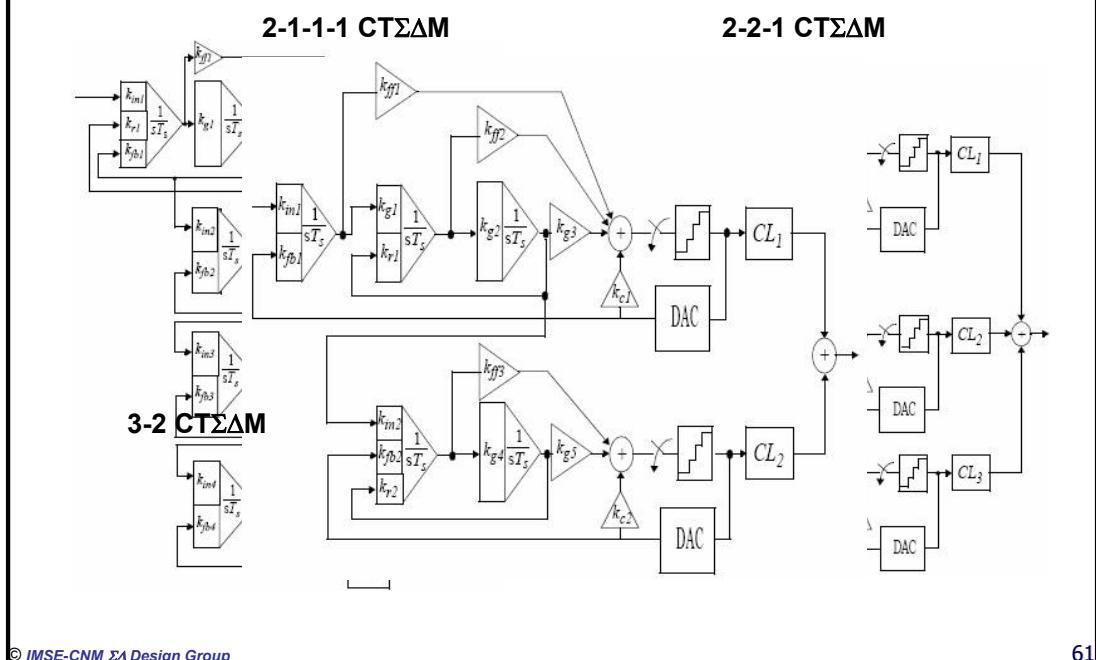
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



- Synthesized cascaded CT $\Sigma\Delta$ Ms to cope with 12-bit@20-MHz



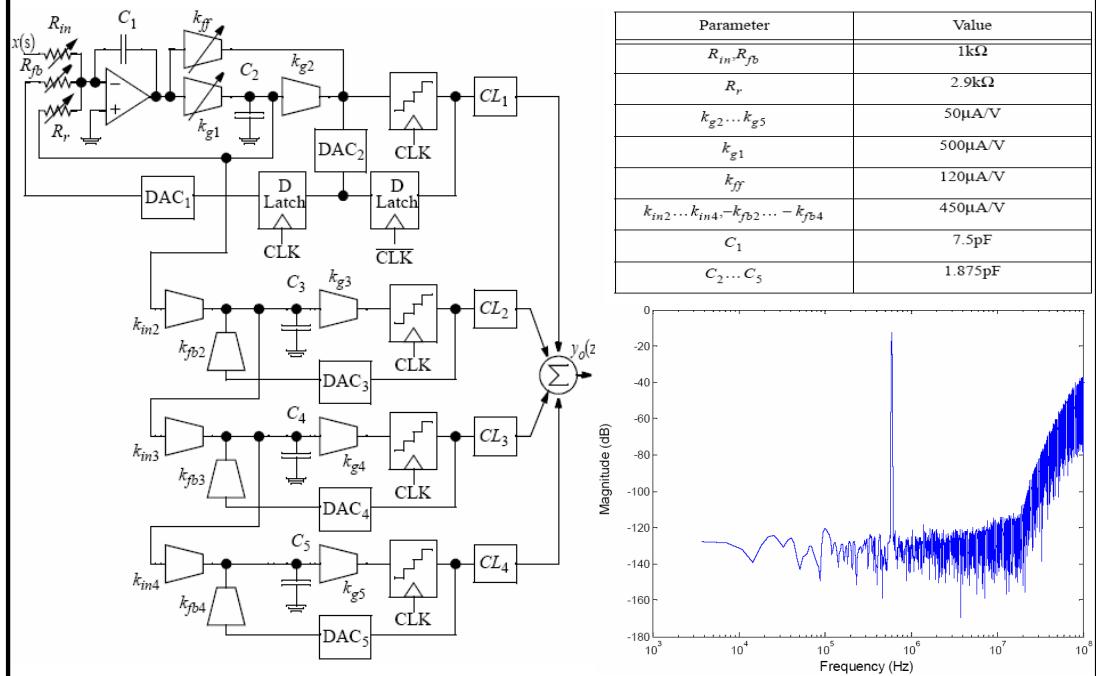
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



- A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT $\Sigma\Delta$ M (RC/Gm Integrators)



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CT- $\Sigma\Delta$ Ms: Integrator time-constant error

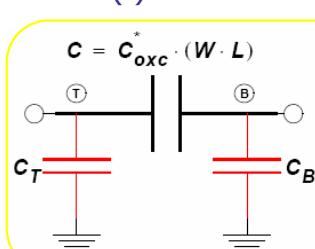


☐ Integrator time-constant error (I)

$$ITF(s) = \frac{A_0}{1 + sC(1 + \varepsilon_\tau)/g_o}$$

$$\varepsilon_\tau = C_p/C$$

$$C = C_{oxc}^* \cdot (W \cdot L)$$



- ♦ Capacitor plate parasitic capacitances
- ♦ Parasitic capacitances of the interconnection lines
- ♦ Parasitic input capacitances of the circuits connected to the node
- ♦ Parasitic output capacitances of the circuits connected to the node

RC ε_τ	MOSFET-C ε_τ	Gm-C ε_τ	Gm-MC ε_τ
$1 + \frac{G}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$	$1 + \frac{G_{ch}}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$	$1 + \frac{C_T}{C}$	$1 + \frac{G_{go}}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$

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CT- $\Sigma\Delta$ Ms: Integrator time-constant error

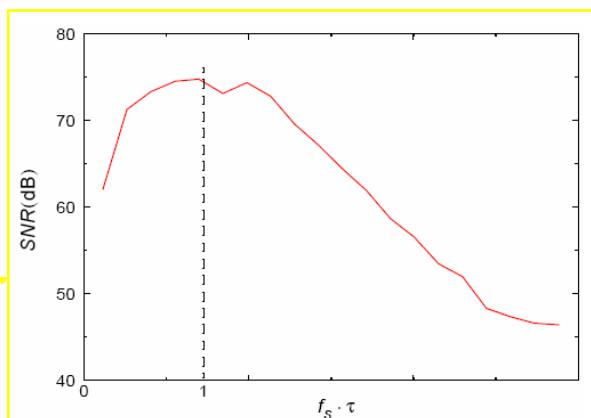


☐ Integrator time-constant error (II)

$$\Delta P_{Q_{A_0 \cdot \varepsilon_\tau}} \Big|_{\text{dB}} \cong \begin{cases} \frac{3M^2}{\pi^2} \cdot \frac{1}{A_o^2} + (1 + \varepsilon_\tau)^2 & \text{(1st-order modulator)} \\ (1 + \varepsilon_\tau)^4 + \frac{10}{3\pi^2} \cdot \frac{(1 + \varepsilon_\tau)^2}{A_o^2} M^2 + \frac{5}{\pi^4 A_o^4} M^4 & \text{(2nd-order modulator)} \end{cases}$$

Optimum SNR for:

$$\tau = 1/f_s$$



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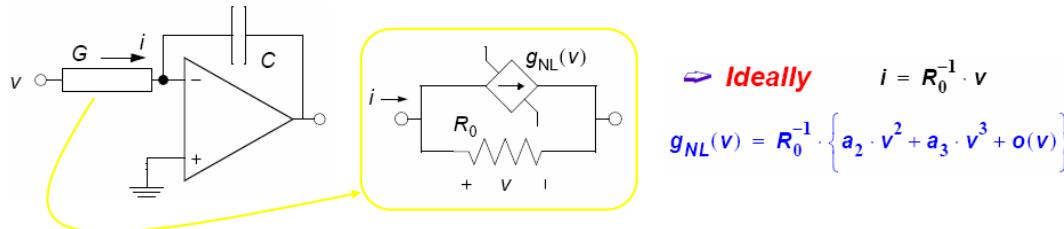
CT- $\Sigma\Delta$ Ms: Non-linear errors



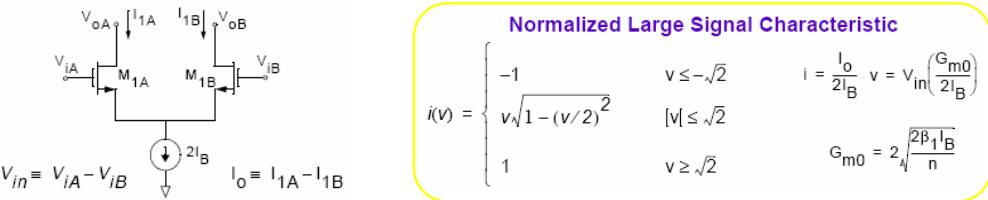
□ Non-linearity (I): Causes

- ◆ Intrinsic non-linearity of the resistor material
- ◆ Modulation of thickness of the conductive layer with resistor voltage

□ V-I transformation in RC integrators



□ V-I transformation in Gm-C integrators



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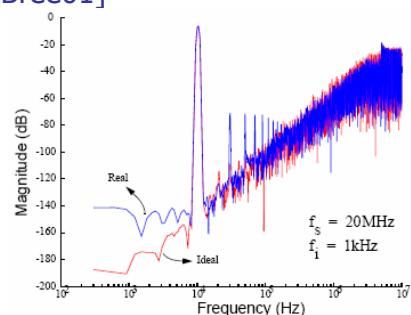
CT- $\Sigma\Delta$ Ms: Non-linear errors



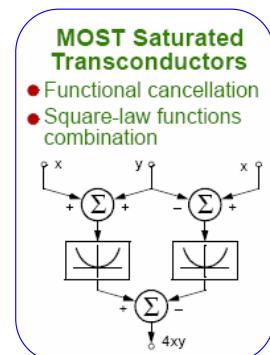
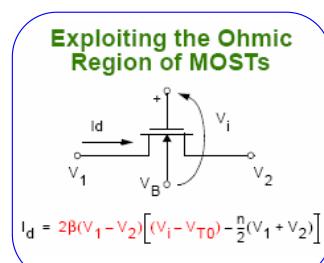
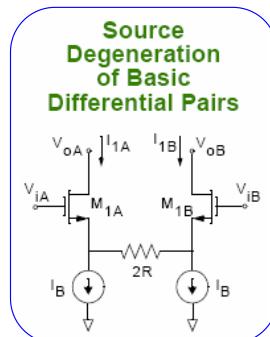
□ Non-linearity (II): Effect on Gm-C CT- $\Sigma\Delta$ Ms [Bree01]

$$\left. \begin{aligned} i(v) &= \beta v \sqrt{2I_B/\beta - v} \approx \sum_{k=1}^{\infty} g_{m_k} v^k \\ i(v) &\equiv g_{m_1} v + g_{m_3} v^3 \end{aligned} \right\}$$

$$THD \equiv HD_3 \equiv \frac{g_{m_3}}{g_{m_1}} V_i^2$$



□ Linearization strategies



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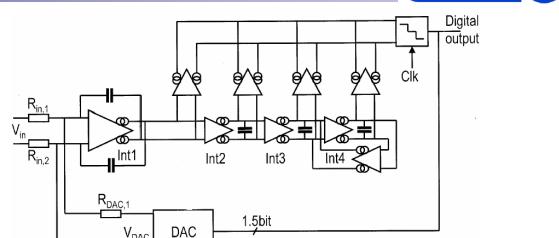
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CT- $\Sigma\Delta$ Ms: Non-linear errors



□ Non-linearity (III) – Commonplace architecture

- RC-active front-end integrator
- Gm-C subsequent integrators



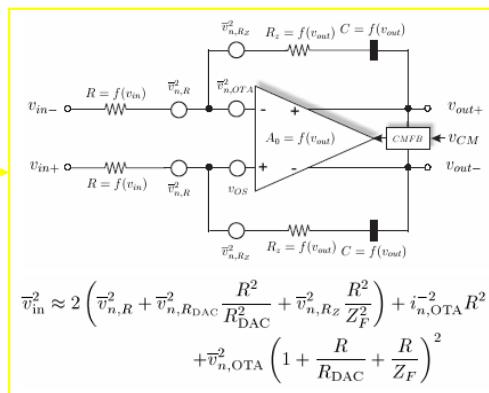
□ Other sources of non-linearity

- Multi-bit DACs
- Linearity must be the same or lower than the required resolution
- Corrected by same techniques as those employed in SC $\Sigma\Delta$ Ms
 - DEM
 - Calibration

□ Circuit noise

- Dominated by noise sources from the front-end integrator and DAC
- Flicker noise reduced by proper sizing and/or chopper techniques
- Unsampled noise – effect of sampling reduced by the loop gain

$$P_{Th} \approx \frac{KT}{4C} \frac{\pi^{2L}}{(2L+1)M}$$



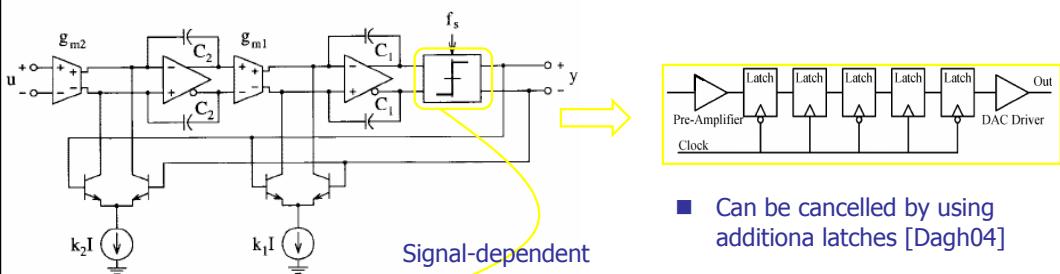
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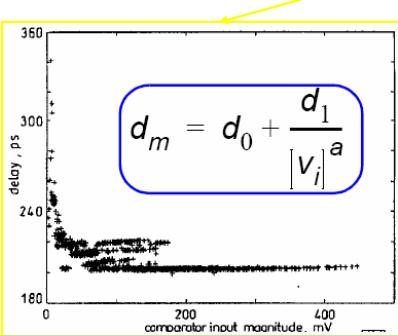
CT- $\Sigma\Delta$ Ms: Comparator metastability



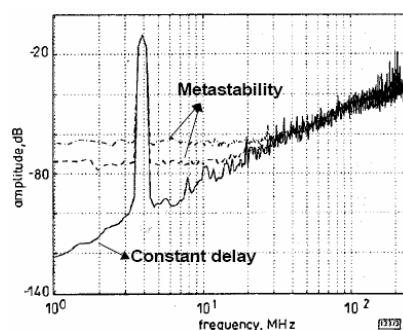
□ Comparator metastability



- Can be cancelled by using additional latches [Dagh04]



- Modeled as a jitter noise [Cher00]



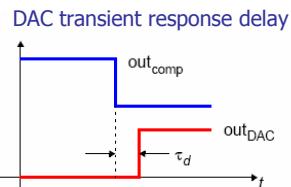
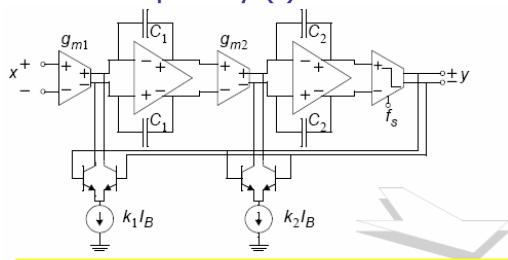
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CT- $\Sigma\Delta$ Ms: Excess loop delay



☐ Excess loop delay (I)

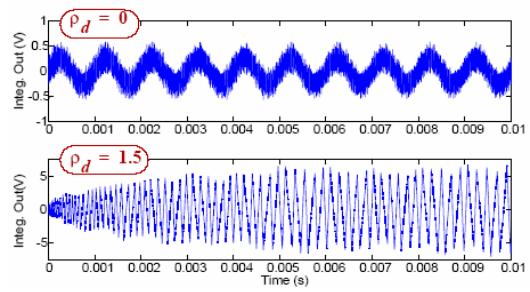


$$Y(f) = \frac{g_q g_1 g_2}{(st)^2 + g_q g_1' g_2' e^{-\tau_d s} + g_q g_2' e^{-(st)} e^{-\tau_d s}} X(f) + \frac{(st)^2}{(st)^2 + g_q g_1' g_2' e^{-\tau_d st} + g_q g_2' \cdot (st) e^{-\tau_d s}} E(f)$$

- ◆ Adds additional poles to STF/NTF
- ◆ Causes instability
- ◆ Stability condition:

• 2nd-order $\rho_d \leq \frac{g'_2}{2g'_1 g_2}$

• L th-order $\rho_d \propto \frac{1}{|H(f)|}_{\text{outband}}$



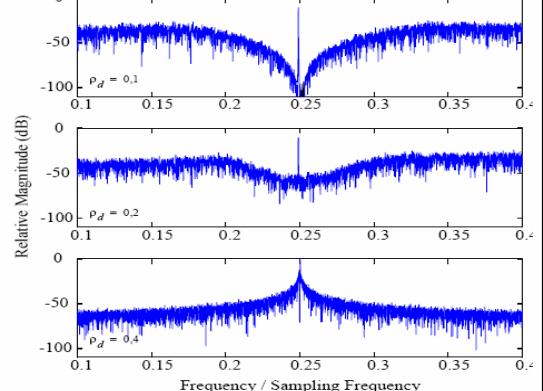
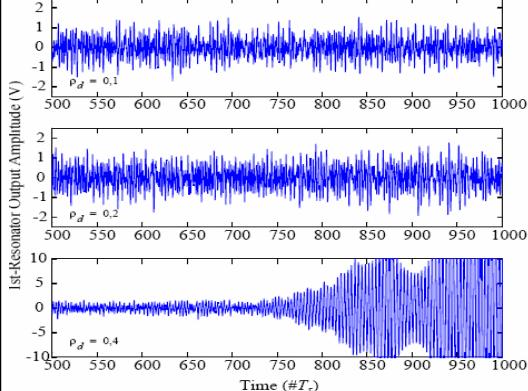
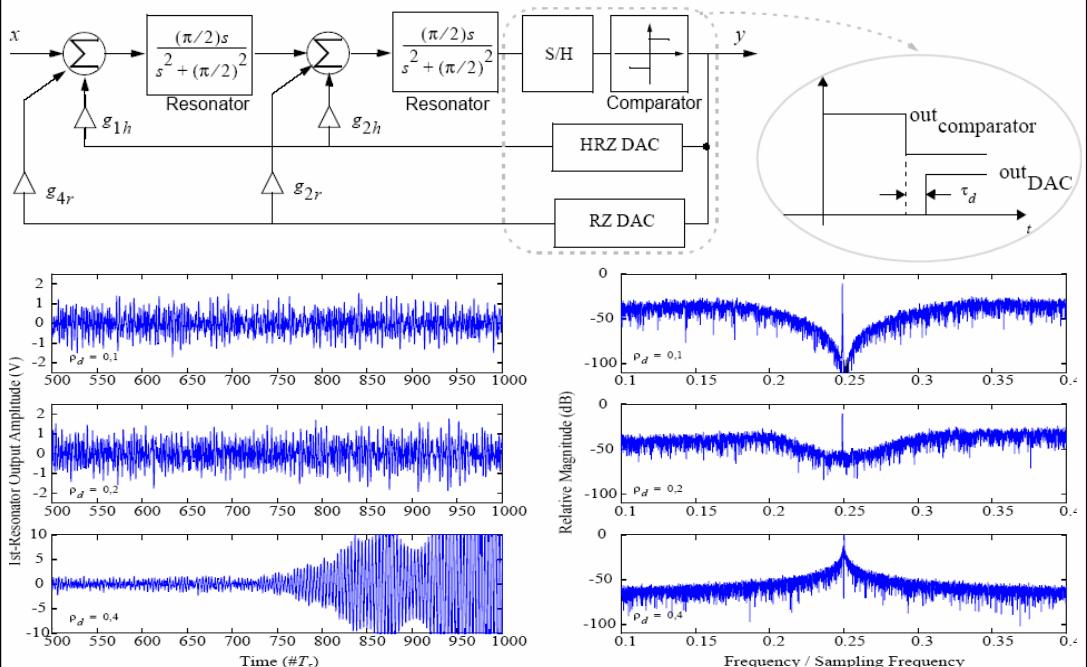
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CT- $\Sigma\Delta$ Ms: Excess loop delay



☐ Excess loop delay (II) – an example of instability



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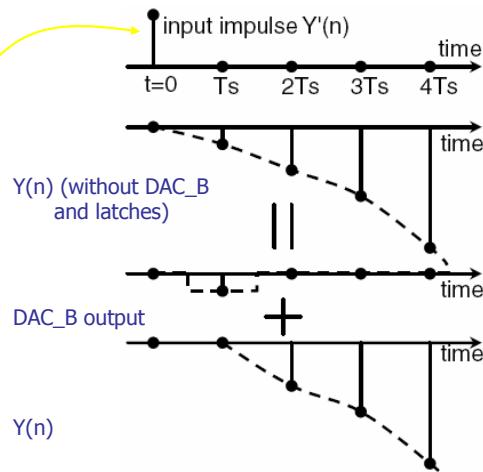
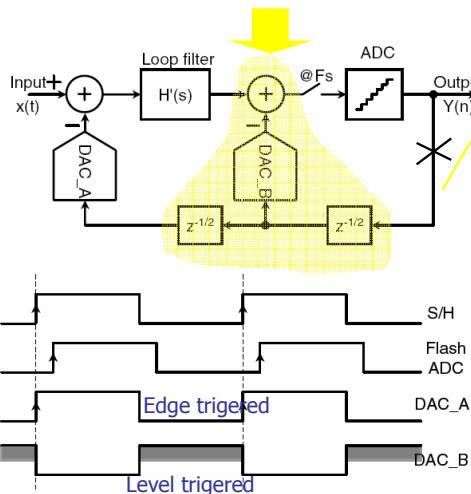
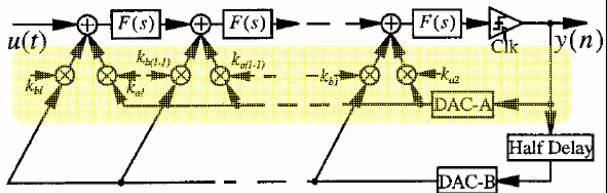
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CT- $\Sigma\Delta$ Ms: Excess loop delay



Excess loop delay (III) – cancellation techniques

- Extra feedback paths (DACs) with tunable gains [Cher00]
- Additional DAC and two latches [Yan04]



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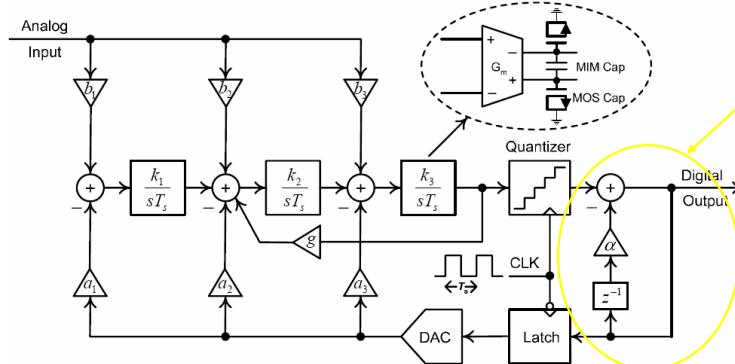
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CT- $\Sigma\Delta$ Ms: Excess loop delay



Excess loop delay (IV) - Digital compensation [Font05]

- Implemented in a 3rd-order single loop architecture with 5-level quantizer
- 90nm CMOS
- 74-dB SNDR-peak, 600kHz bandwidth
- 6.0mW, 1.5V
- Excess loop delay compensated in the digital domain
- Half-a-clock-cycle delay
 - Relax comparators speed
 - Provide maximum isolation between quantizer and DAC switch events



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CT- $\Sigma\Delta$ Ms: Clock jitter error



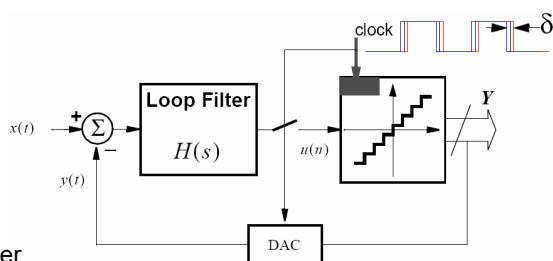
☐ Clock jitter (I)

◆ S/H

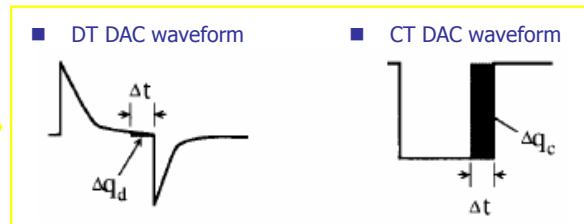
- Shaped by the modulator NTF
- Can be neglected

◆ DAC

- Directly adds with the input
- Increases the in-band noise power



CT $\Sigma\Delta$ Ms are more sensitive to clock jitter than DT $\Sigma\Delta$ Ms



☐ White noise model approximation (NRZ DAC) [Cher00][Zwan96]

◆ Standard deviation of jitter error: $\sigma_j^2 \approx \sigma_j^2 I_{\text{DAC}}^2$

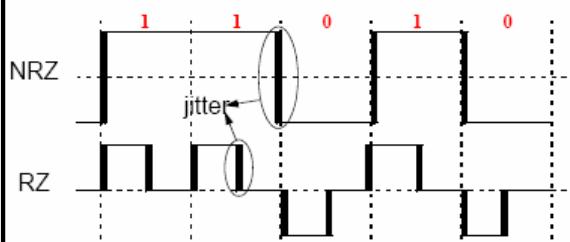
◆ SNR degradation: $SNR_J = 10 \log \left(\frac{1}{16MB_w^2 \sigma_j^2} \right)$

$$\frac{\sigma_{j_{\text{CT}}}}{\sigma_{j_{\text{DT}}}} = \left(\frac{\pi}{2M} \right)^2$$

CT- $\Sigma\Delta$ Ms: Clock jitter error



☐ Clock Jitter (II) – White noise model approximation (NRZ/RZ DAC) [Tao99a]

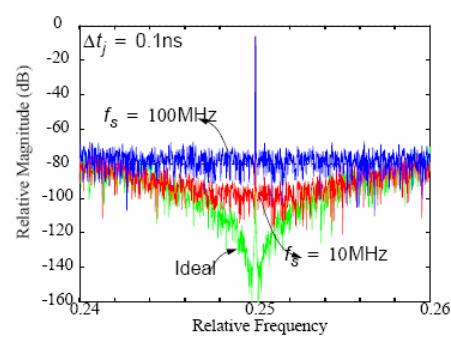


■ Lowpass CT- $\Sigma\Delta$ Ms

$$P_{\text{jitter}}|_{\text{RZ}} \approx \left(\frac{T_s}{T_0} \right)^2 P_{\text{jitter}}|_{\text{NRZ}}$$

■ Bandpass CT- $\Sigma\Delta$ Ms

$$SNR_J \approx \begin{cases} 10 \log \left[\frac{\text{sinc}(\pi f_n T_s)}{64 \sigma_j^2 B_w^2 M} \right] & \text{NRZ} \\ 10 \log \left[\frac{\text{sinc}(\pi f_n T_s)}{64 \left(\frac{T_s}{T_0} \right)^2 \sigma_j^2 B_w^2 M} \right] & \text{RZ} \end{cases}$$



CT- $\Sigma\Delta$ Ms: Clock jitter error



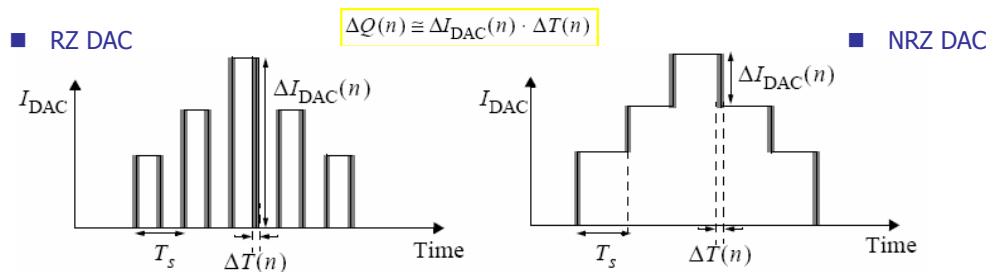
□ Clock Jitter (III) – lingering effect [Olia03a]

- ◆ Jitter-induced noise includes both **white** and **shaped** components
- ◆ State-space analysis of CT- $\Sigma\Delta$ Ms with RZ DAC shows that:

$$S_\varepsilon(z) = (\sigma_s^2 T) \sum_{m_2=1}^N \sum_{j_2=1}^{m_2-1} \sum_{m_1=1}^N \sum_{j_1=1}^{m_1-1} a_{m_1} a_{m_2} z^{j_1-j_2} \times \mathbf{C} \mathbf{A}^{m_1-j_1-1} \mathbf{\Lambda} \mathbf{A}_T^{m_2-j_2-1} \mathbf{C}_T$$

□ Multi-bit NRZ DACs

- ◆ Commonly used in CT- $\Sigma\Delta$ Ms for broadband telecom applications
- ◆ Less sensitive to clock jitter



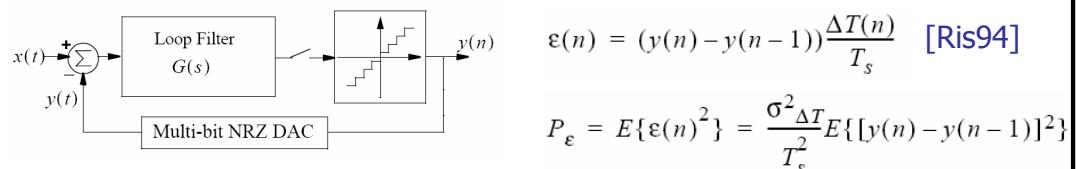
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CT- $\Sigma\Delta$ Ms: Clock jitter error



□ Clock Jitter (IV) – Multi-bit NRZ DACs [Tort05]



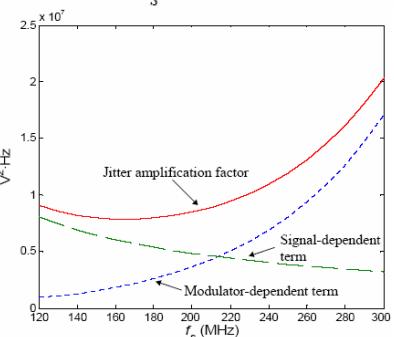
$$\varepsilon(n) = (y(n) - y(n-1)) \frac{\Delta T(n)}{T_s} \quad [\text{Ris94}]$$

$$P_\varepsilon = E\{\varepsilon(n)^2\} = \frac{\sigma_{\Delta T}^2}{T_s^2} E\{(y(n) - y(n-1))^2\}$$

- Using state-space formulation of NTF:

$$P_\varepsilon = \frac{\sigma_{\Delta T}^2}{T_s^2} \cdot \left(\frac{T_s^2 A^2 \omega_{in}^2}{2} + \frac{X_{FS}^2}{6(2^B - 1)^2} \cdot \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right)$$

$$\psi(\bar{g}, \bar{p}, \bar{\lambda}, L) = 1 - \bar{g}^T \bar{p} + \sum_{k=1}^L \sum_{j=1}^L g_k p_k g_j p_j \frac{\lambda_k^{-1} - \lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}}$$



$$SNR_{\text{jitter}} \equiv \frac{A^2}{2 \cdot P_{\varepsilon_{\text{band}}}} = \frac{A^2}{2 \cdot B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2 \omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3(2^B - 1)^2} \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right]}$$

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CT- $\Sigma\Delta$ Ms: Clock jitter error



- ☐ Clock Jitter (V): Comparison of [Tort05] with previous approaches

Assuming that SNR_{jitter} is dominated by the signal-dependent term:

$$SNR_{MAX} = 10\log\left(\frac{M}{4\pi^2\sigma_{\Delta T}^2 B_w^2}\right) \quad [\text{Boser, JSSC, 1988}]$$

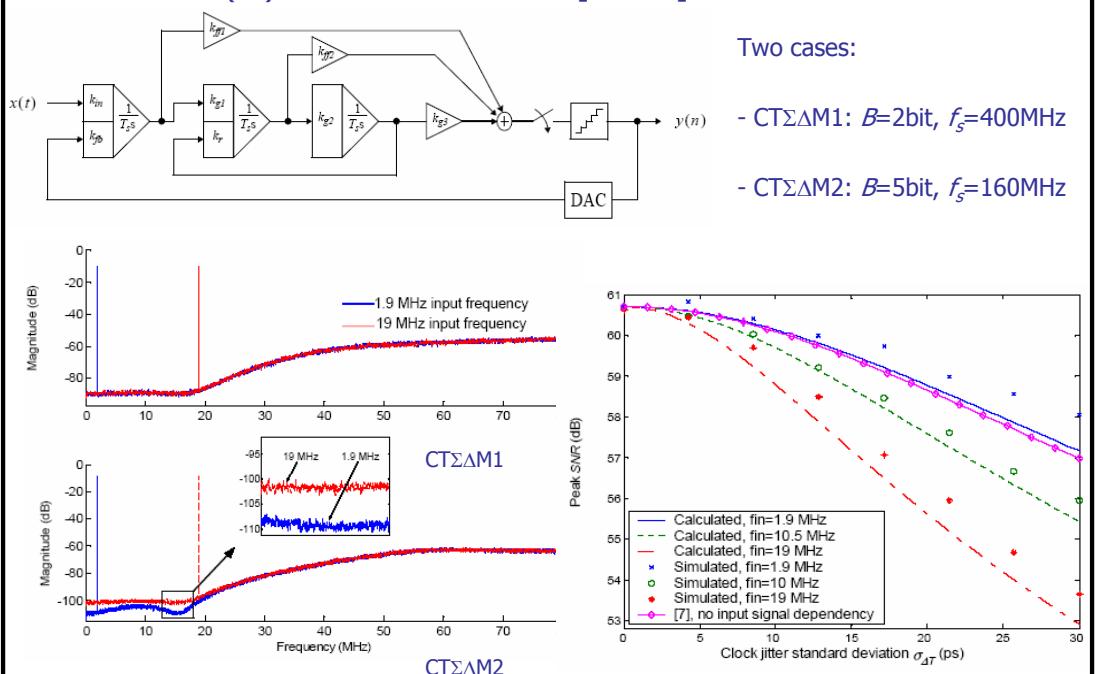
If the modulator-dependent term dominates (single-bit quantization):

$$SNR_{jitter} = 10\log\left(\frac{1}{16M\sigma_{\Delta T}^2 B_w^2}\right) \quad [\text{Van der Zwan, JSSC, 1996}]$$

CT- $\Sigma\Delta$ Ms: Clock jitter error



- ☐ Clock Jitter (VI) – Multi-bit NRZ DACs [Tort05]

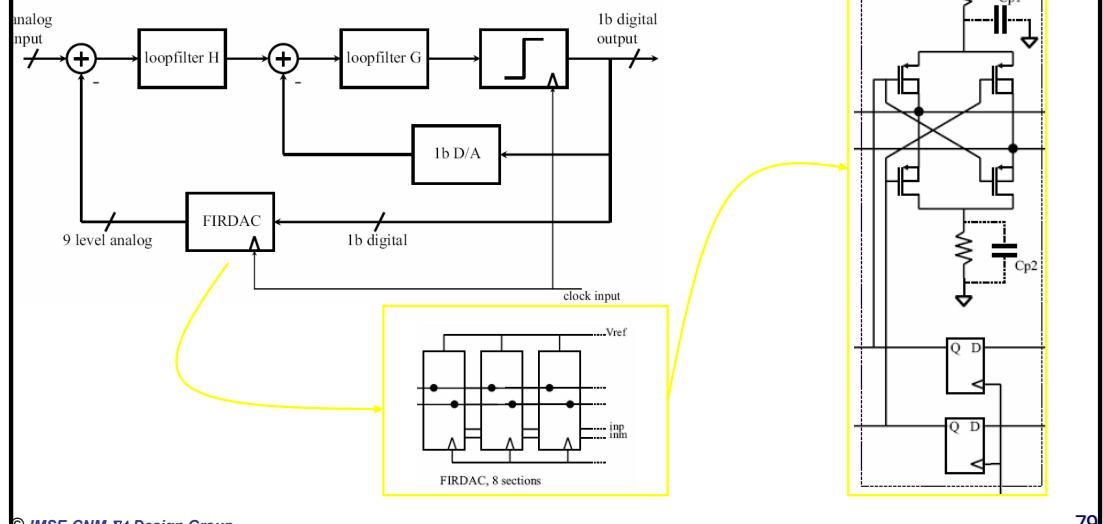


CT- $\Sigma\Delta$ Ms: Clock jitter error



□ Clock Jitter (VII) – Compensation techniques

- ◆ Multi-bit quantization (non-linear DAC)
- ◆ Switched-capacitor DAC [Veld03]
 - Voltage-mode operation (proper for active RC integrators)
 - Slower than switched-current (current steering) DAC
- ◆ FIRDAC to generate a multilevel signal [Putt04]



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CT- $\Sigma\Delta$ Ms: Case Study

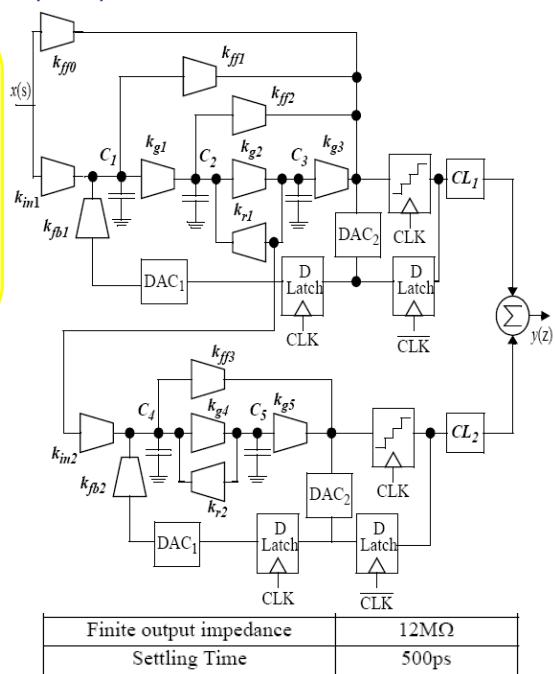


□ A case study: A Gm-C 12-bit@20MHz, 4-b, 3-2 CT $\Sigma\Delta$ M

- ◆ 130nm mixed-signal CMOS, 1P8M
- ◆ Cascade 3-2 multi-bit (4b) CT $\Sigma\Delta$
- ◆ Gm-C loop-filter implementation
- ◆ Current-steering feedback DACs + DEM
- ◆ 12-bit effective resolution
- ◆ 40MS/s output rate (20MHz bandwidth)
- ◆ 240MHz clock frequency
- ◆ 1.2V \pm 10% analog/digital power supply
- ◆ On-chip tuning of analog components
- ◆ Estimated power consumption is 45mW

Loop-filter coefficients

$C_u = 3.65 \text{ pF}$	$k_u = 190 \mu\text{A/V}$
$C_1 = C_2 = C_3 = C_u$	$C_4 = C_5 = 2C_u$
$k_{in1} = 852 \mu\text{A/V}$	$k_{fb1} = 730 \mu\text{A/V}$
$k_{ff0} = 2k_u$	$k_{ff1} = 4k_u$
$k_{ff2} = 2k_u$	$k_{ff3} = 5k_u$
$k_{g1} = k_{g5} = 3k_u$	$k_{g2} = 5k_u$
$k_{g3} = k_u$	$k_{g4} = 7k_u$
$k_{in2} = 5k_u$	$k_{fb2} = 6k_u$
$k_{r1} = k_{r2} = k_u$	



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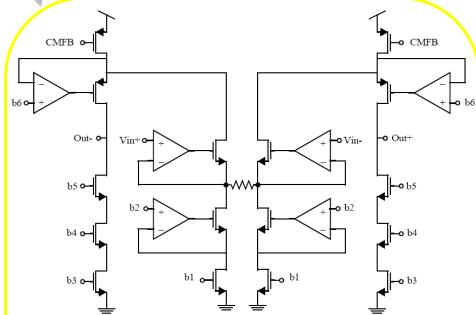
80

CT- $\Sigma\Delta$ Ms: Case Study



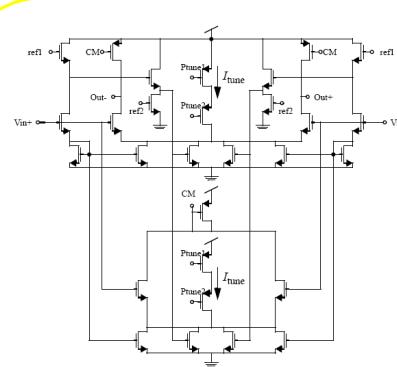
□ Transconductors

- ◆ Resistive source degenerated front-end transconductor
- ◆ Loop-filter transconductors based on quadratic term cancellation



Transistor-level performance

DC Gain	78.3 dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
HD3	-89dB
Power consumption	8.8mW



DC Gain	52dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
HD3	-60dB
Power consumption	622μW

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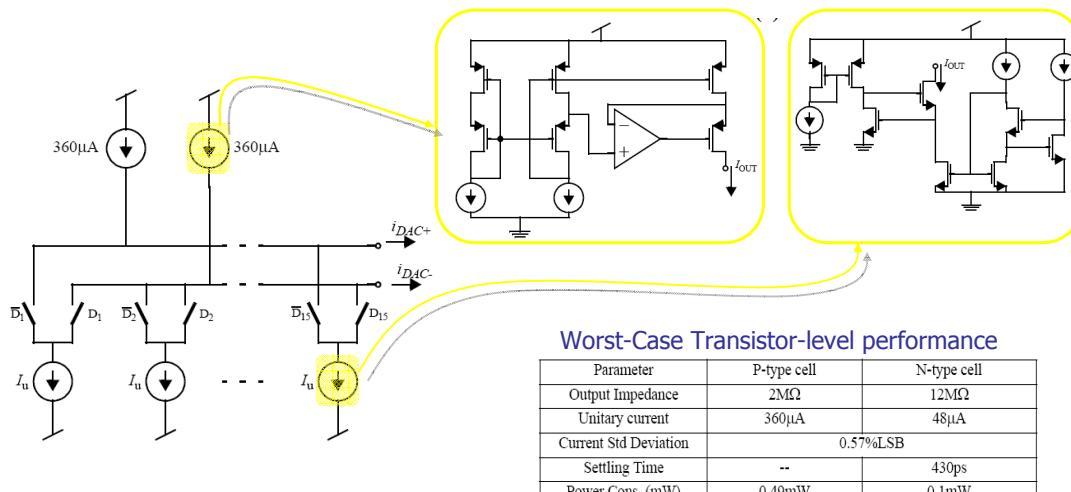
81

CT- $\Sigma\Delta$ Ms: Case Study



□ Current-steering DACs

- ◆ 2 360- μ A P-type gain-boosted current sources
- ◆ 15 N-type regulated-cascode current cells



Worst-Case Transistor-level performance

Parameter	P-type cell	N-type cell
Output Impedance	2MΩ	12MΩ
Unitary current	360μA	48μA
Current Std Deviation	0.57%LSB	--
Settling Time	--	430ps
Power Cons. (mW)	0.49mW	0.1mW

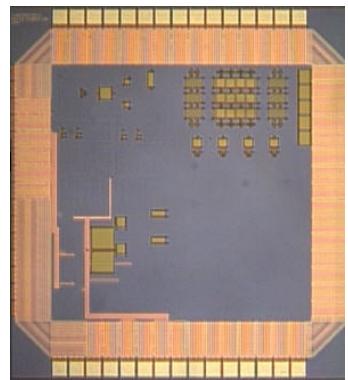
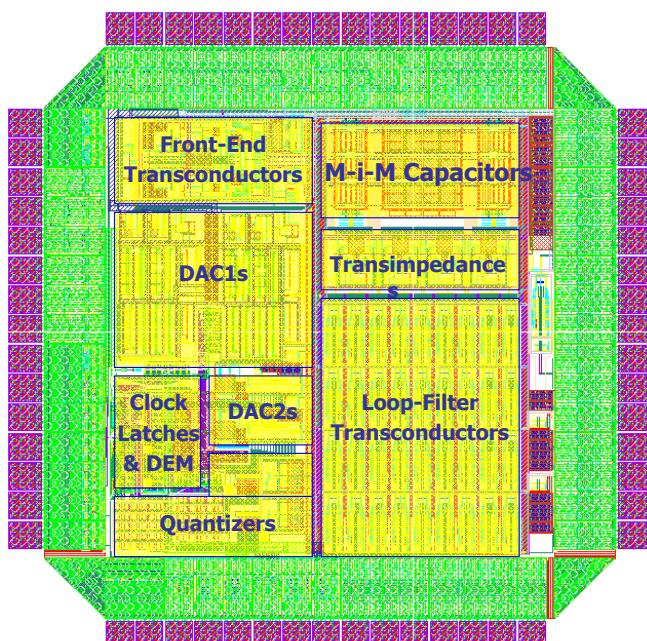
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CT- $\Sigma\Delta$ Ms: Case Study



Chip implementation



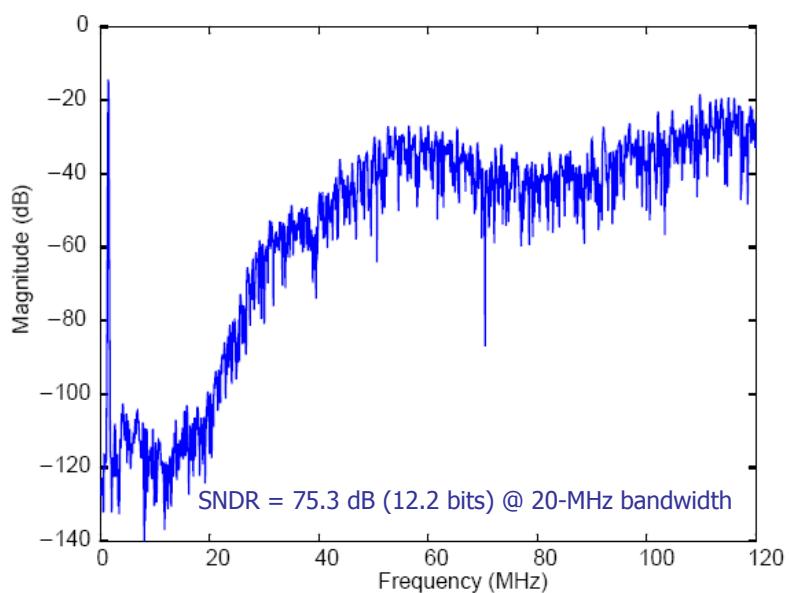
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CT- $\Sigma\Delta$ Ms: Case Study



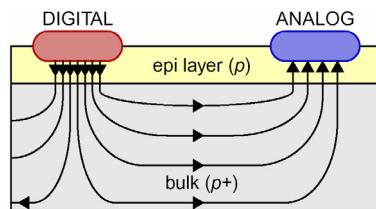
Transistor-level simulation results



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Low-resistive bulk

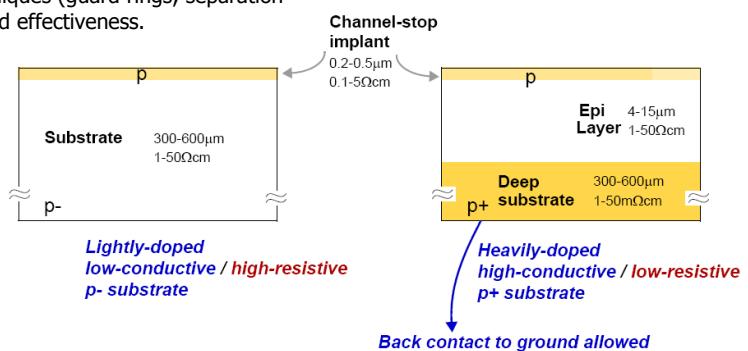


Most Standard CMOS technologies

Epitaxial process with heavily-doped bulk

Impact of the on-chip switching activity

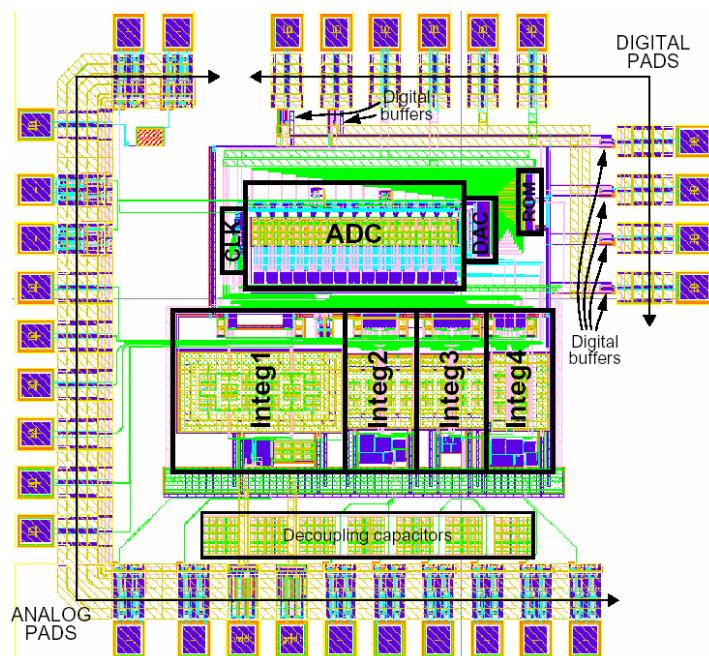
- The deep-substrate is a low-impedance path for injected disturbances.
- Traditional layout techniques (guard rings, separation of blocks) have a limited effectiveness.



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Typical $\Sigma\Delta M$ layout example

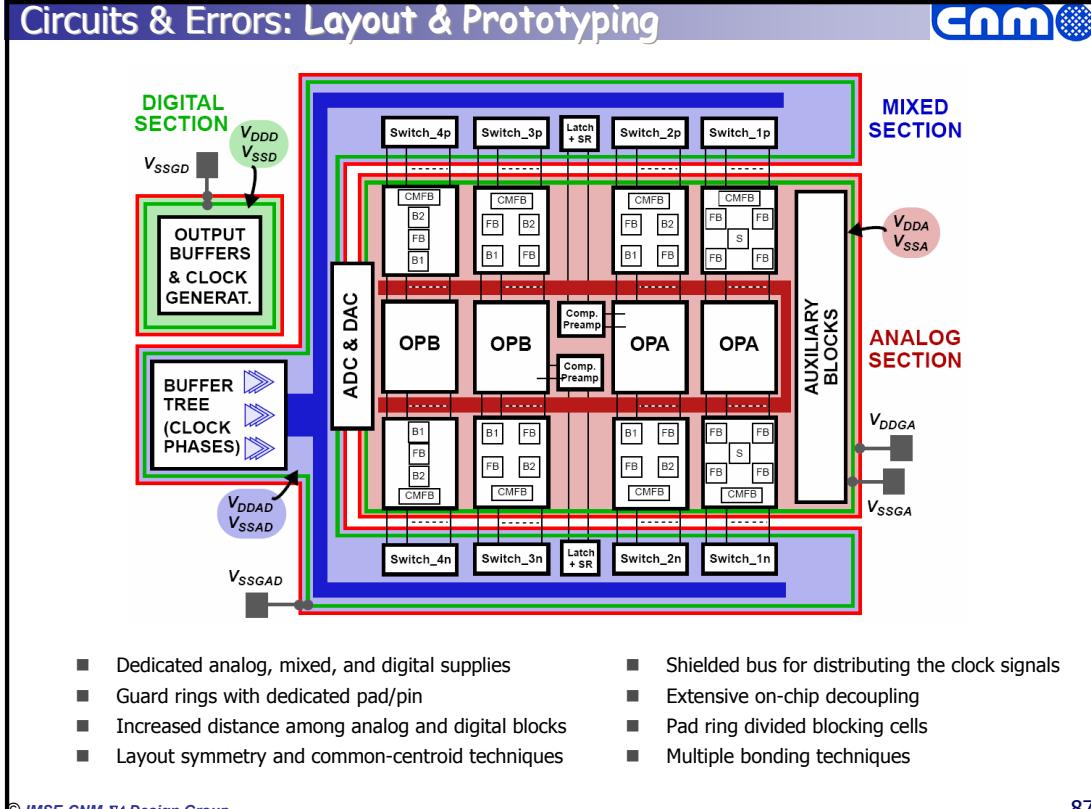


- Dedicated analog and digital supplies:
 - Analog core
 - Digital core
 - Digital output buffers
- Open pad ring
- Common-centroid layout techniques
- Guard rings
- Increased distance among analog and digital blocks

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Circuits & Errors: Layout & Prototyping



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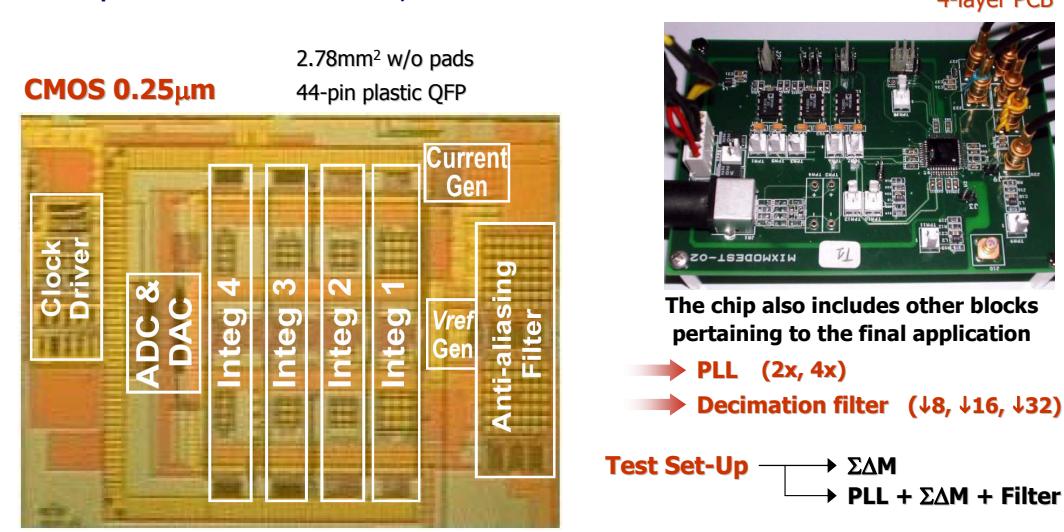
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Circuits & Errors: Layout & Prototyping



Example: A $\Sigma\Delta M$ in $0.25\mu m$ for ADSL/ADSL+

4-layer PCB

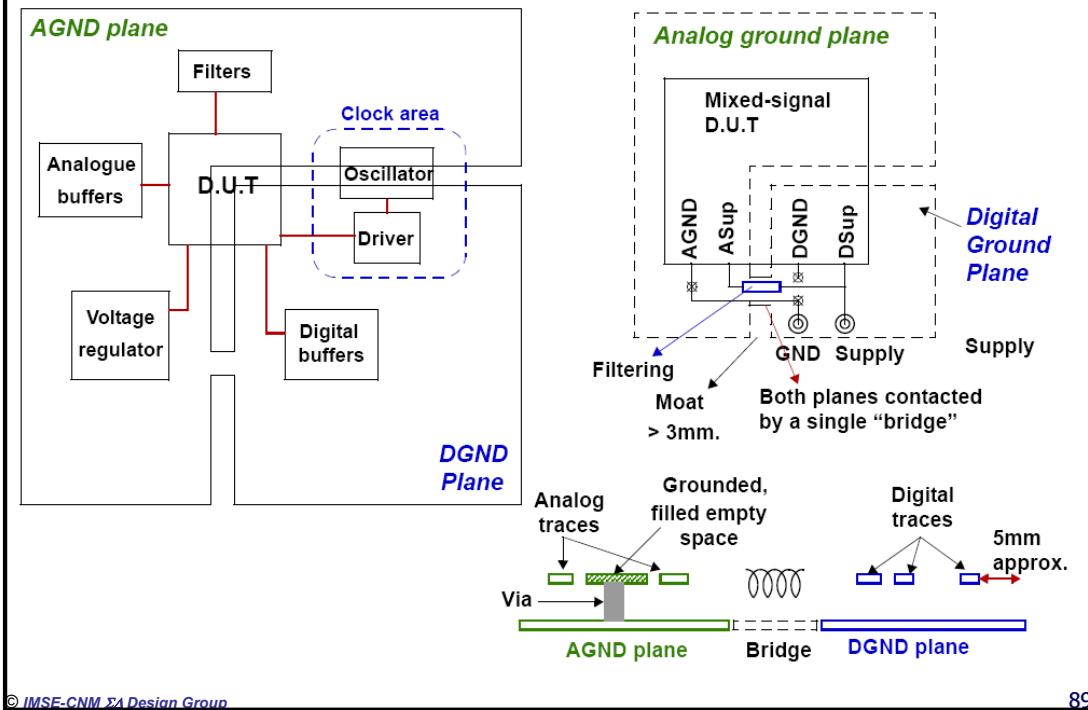


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- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

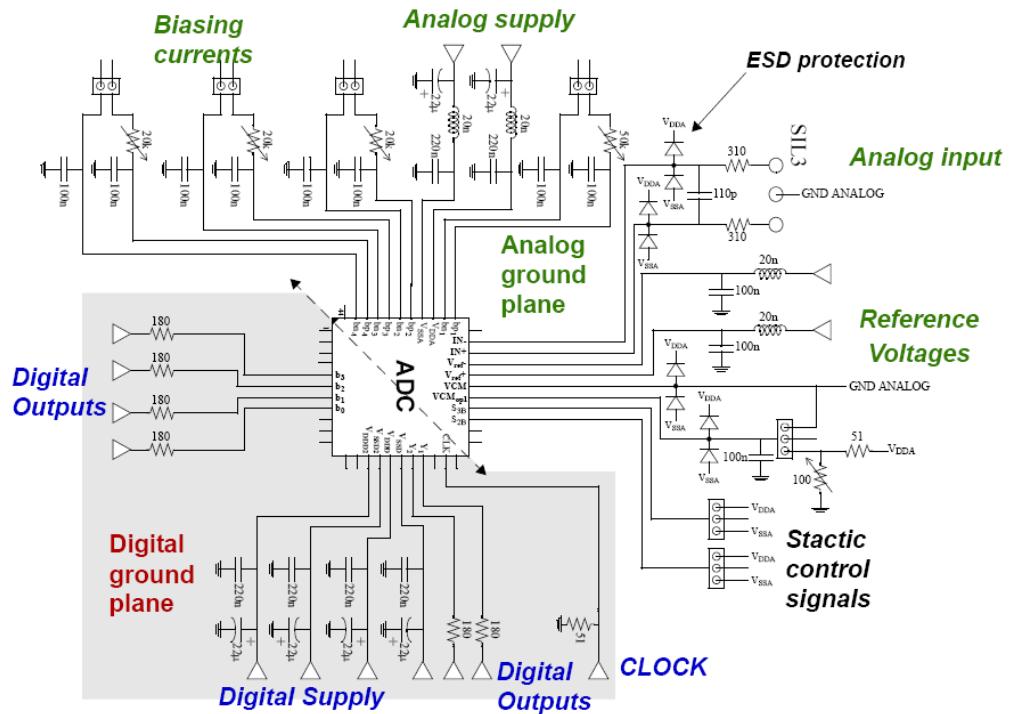
Circuits & Errors: Test PCB



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Circuits & Errors: Test PCB



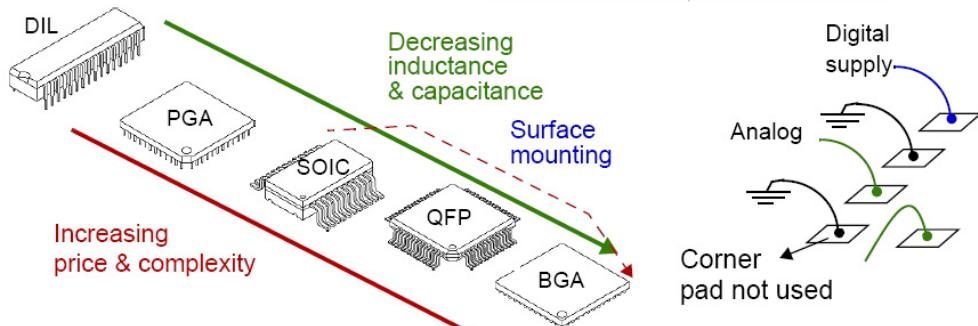
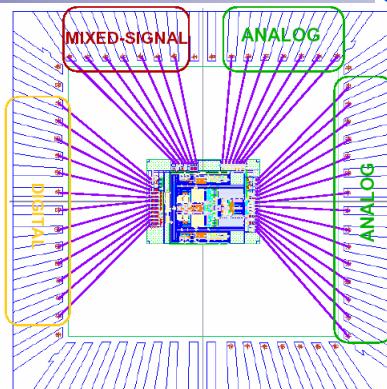
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Circuits & Errors: Chip Package



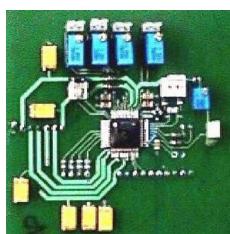
- Double-bonding and multiple pins for supplies
- Different pin assignment for analog, mixed and digital



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Circuits & Errors: Test Set-up

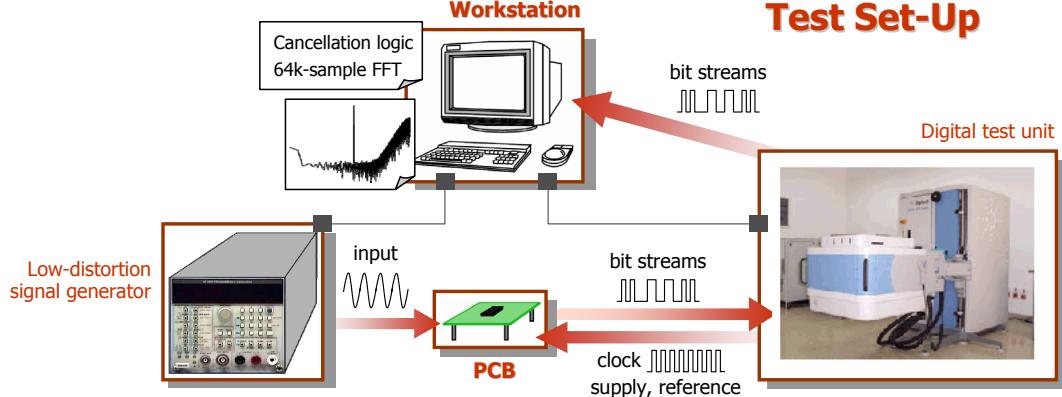


Two-layer PCB

- Soldered samples (in order to avoid socket parasitics)
- Anti-aliasing filter (passive, 1st order)
- Independent control of amplifier bias currents
- Decoupling
- Impedance termination

Novel tech (characterization not yet confirmed by silicon results)

Test Set-Up



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DT- $\Sigma\Delta$ Ms: References



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CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Systematic Design Methodology

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KTH, Stockholm, April 23-27

OUTLINE



1. Introduction

- Digital vs. Analog/Mixed-signal design
- Simulation approaches
- Hierarchical synthesis approach

2. Top-down design methodology

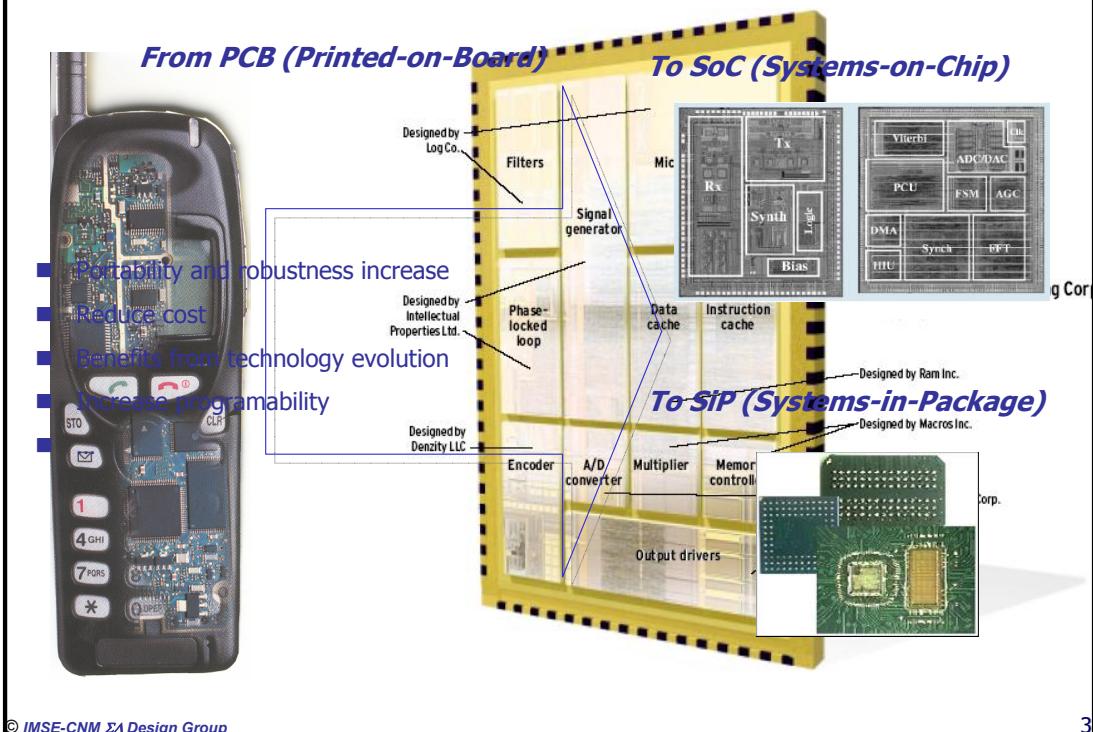
- Top-down/Bottom-up approach
- Optimization engine
- Behavioral simulation

3. Introduction to SIMSIDES

- Description of the toolbox
- Behavioral modeling of building blocks

4. DEMO & Tutorial examples

Introduction: Tendency to System Integration

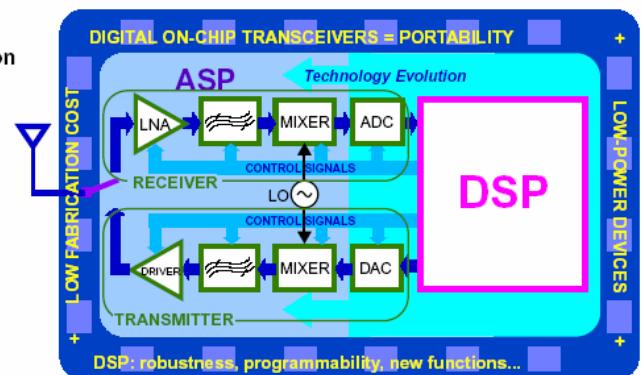
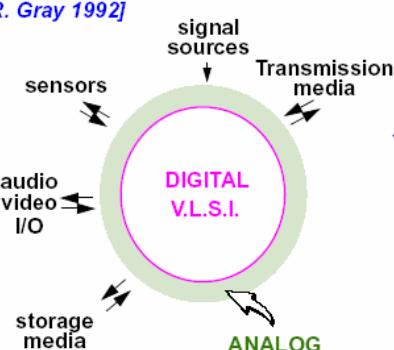


3

Introduction: Digital vs. Analog&Mixed-Signal design



[P.R. Gray 1992]



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Introduction: Digital vs. Analog&Mixed-Signal design



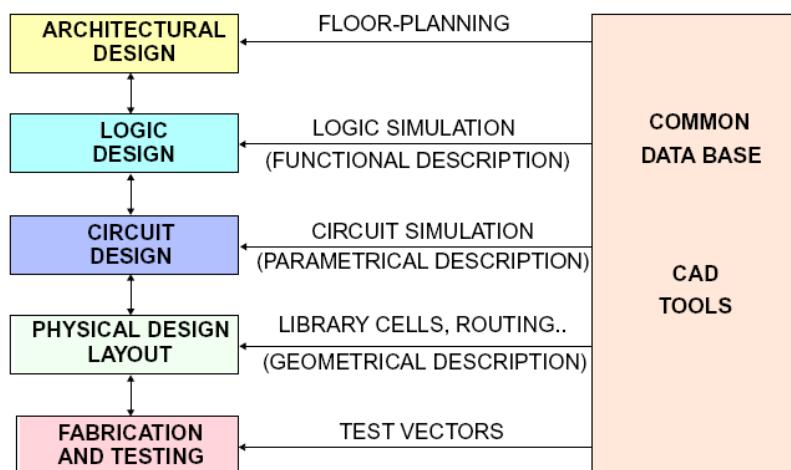
Digital Circuits

- Robustness , programmability and adaptability to different standards and protocols
- Increased performance with technology scaling
- Simplicity of the design and testing
 - ◆ Clear hierarchy leading to well-defined levels of abstraction
 - ◆ Circuit blocks are largely independent of each other
- Automatic top-down design from specs to silicon

A/D/A Interface = Bottle Neck of the Design Process

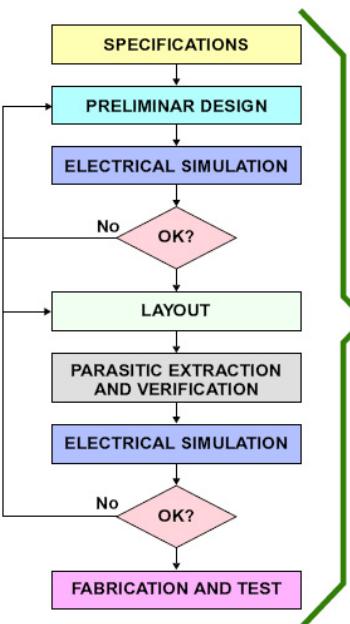
- Technology evolution demands for faster, precise and low-power A/D/A Interfaces
- Analog Circuits in Technologies dedicated to Digital Design (standard ULSI CMOS)
 - ◆ Continuously decreasing supply voltages
 - ◆ Reduced channel length and large threshold voltage in MOS transistors
 - ◆ Poor matching properties and linearity
 - ◆ Incomplete models for the analog design needs
- Proximity of noisy digital circuits
- Need of Design Automation (DA)

Introduction: Digital CAD tools



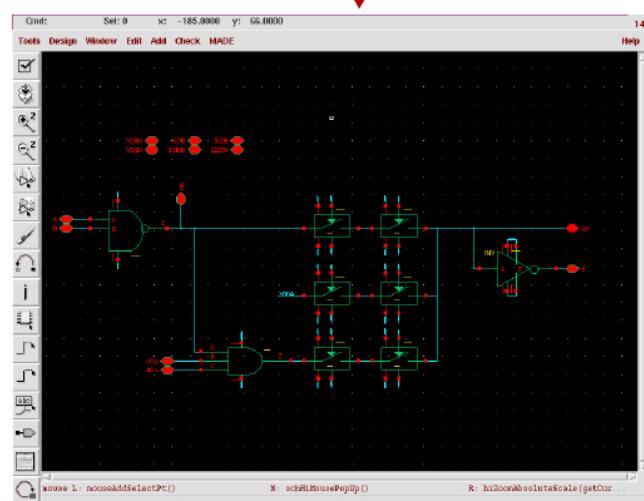
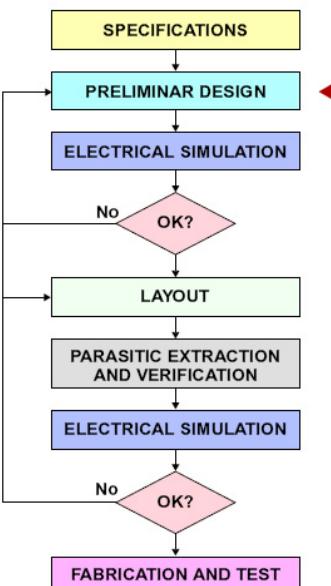
- At each design-flow level:
 - ◆ Generation of a solution
 - ◆ Simulation and verification
- Properly supported by CAD tools:
 - ◆ Simulators, verification tools,
 - ◆ Graphical interfaces: schematic and layout editors,

Introduction: Analog CAD tools

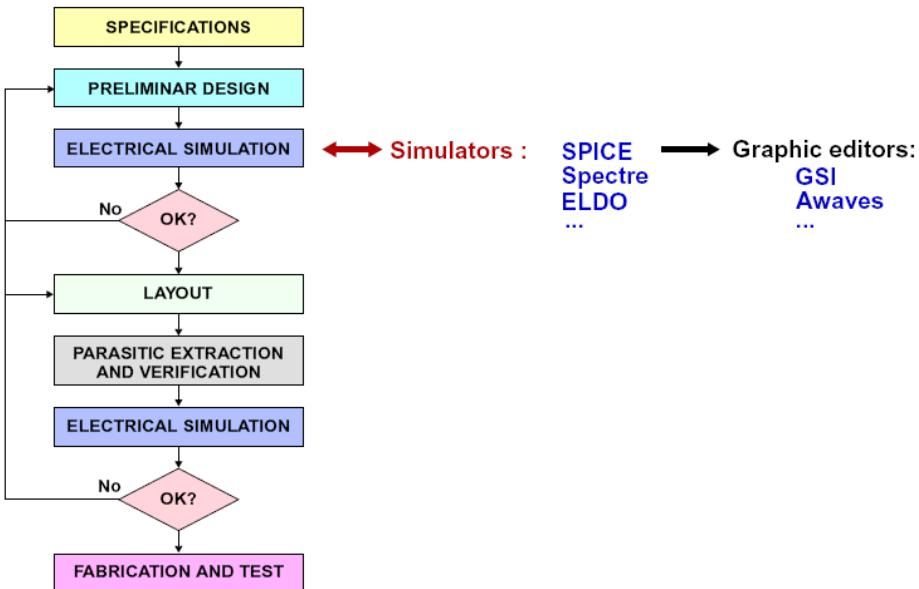


Until a few years ago: only SPICE-like simulators and post-layout verification tools

Introduction: Analog CAD tools



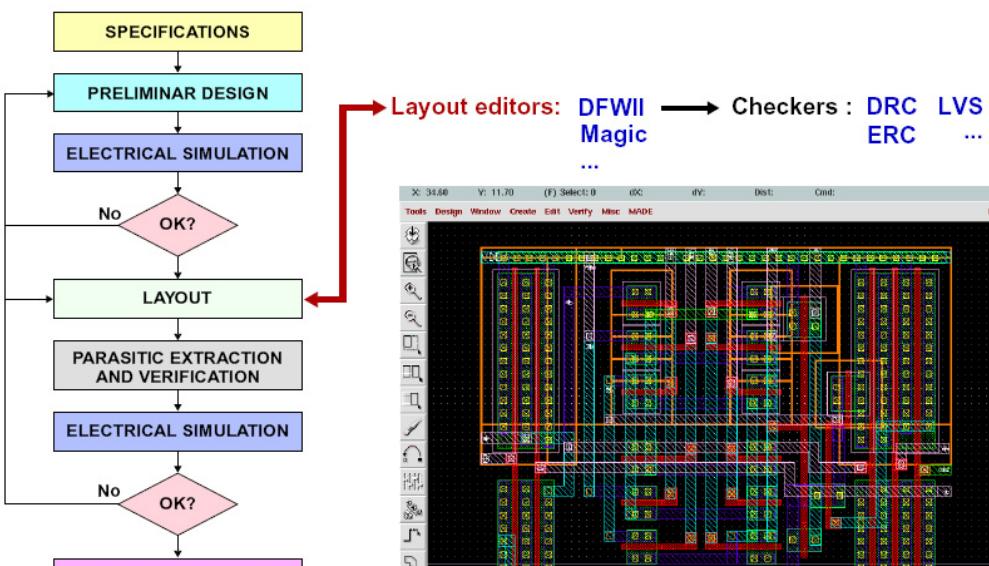
Introduction: Analog CAD tools



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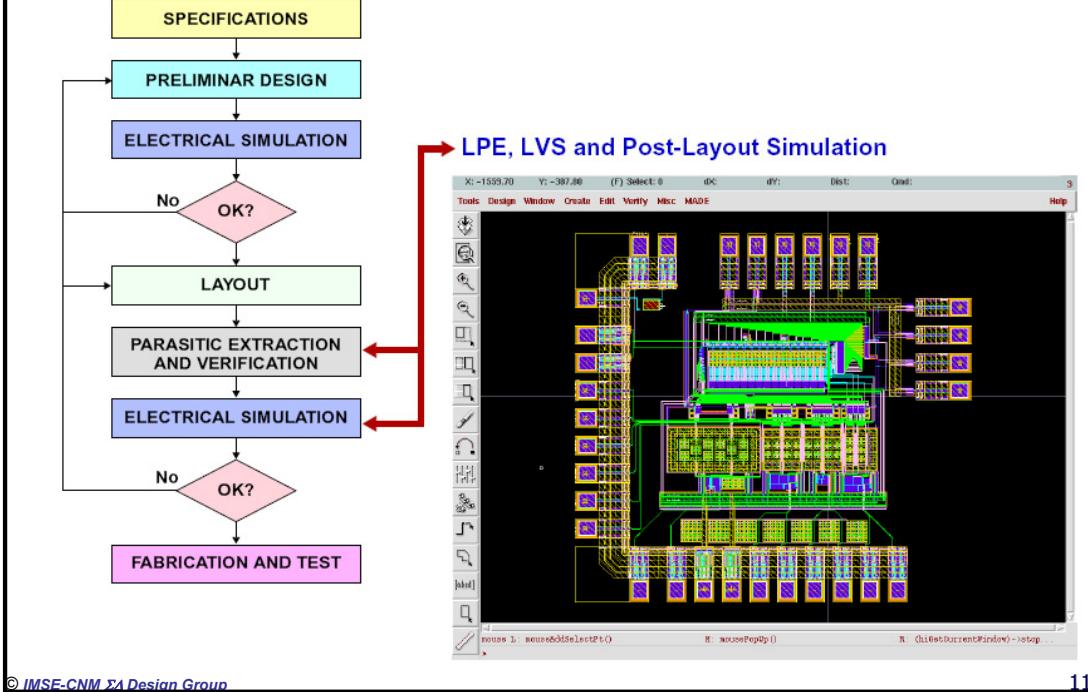
Introduction: Analog CAD tools



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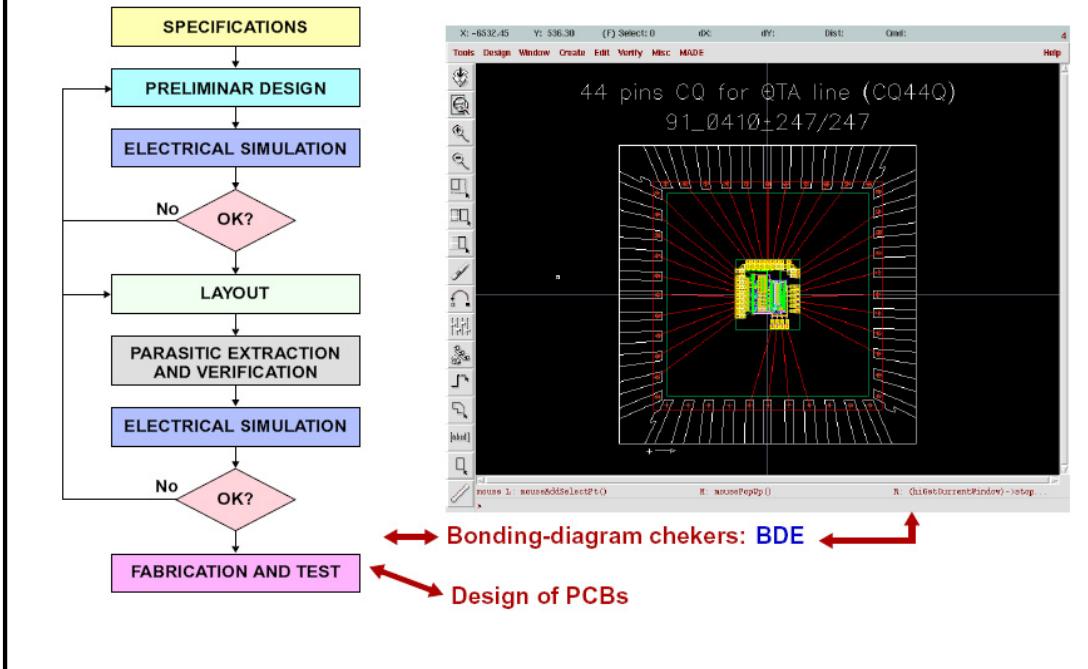
Introduction: Analog CAD tools



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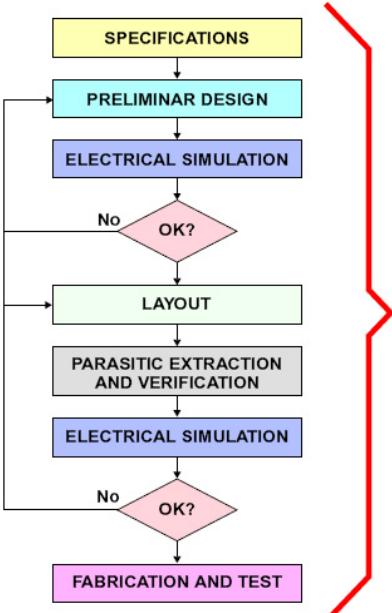
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Introduction: Analog CAD tools

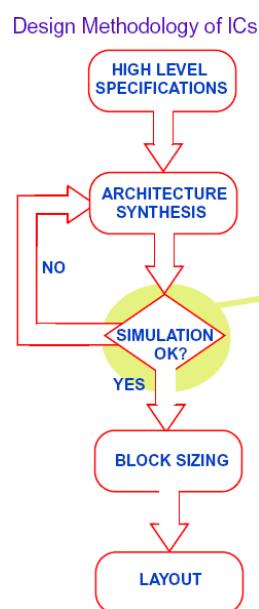


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- ➡ Clearly inefficient for the design of complex systems
- ➡ Excessive consumption of computational resources

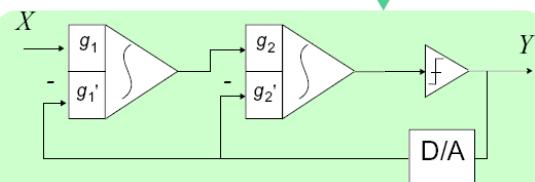


SIMULATION: CRUCIAL PART FOR DESIGN AND VERIFICATION

➡ Electrical simulation of relatively simple discrete-time (SC, SI) circuits is **COMPLETELY INEFFICIENT**

- ♦ Need of time-domain analysis
- ♦ Several thousands of clock cycles required

Example: A 2nd-order ΣΔ ADC



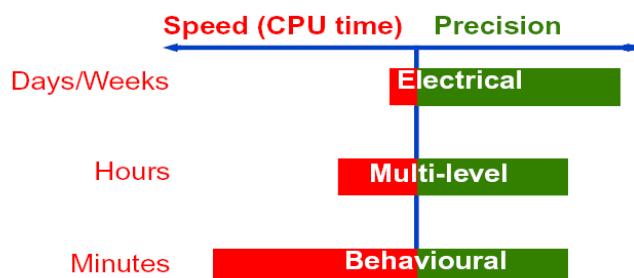
Several weeks of CPU time to obtain SNR

➡ Need of searching other simulation approaches

Introduction: Simulation approaches



- **Electrical simulation with macromodels:** Uses numerical algorithms to solve the differential equations that result from the analysis of a circuit, thus resulting in long CPU times.
- **Multi-level simulation:** The critical parts of the system are simulated numerically while behavioural models are incorporated to emulate the rest of the system. (**ELDO, SABER...**)
- **Behavioural simulation (event-driven):** The system is broken up into a set of subcircuits, often called building blocks or basic blocks. These blocks are described by explicit equations that relate the outputs in terms of the inputs and the internal state variables. Thus, the accuracy of the simulation depends on how precisely those equations describe the real behaviour of each block. The transient evolution of the voltages and currents is not important, only the final value. (**TOSCA, ASIDES, MATLAB-BASED SIMULATORS...**)



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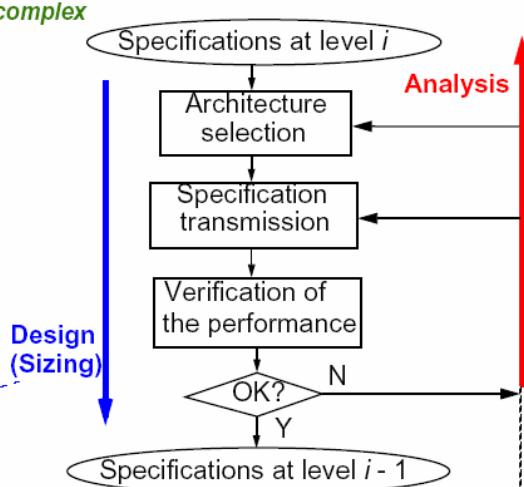
Introduction: Hierarchical synthesis approach



☞ A very popular strategy to synthesize complex blocks is to hierarchize the design

- The complex system is partitioned in simpler blocks with relatively independent functionality.
- In each level of the hierarchy the sizing process involves selecting the architecture and transmitting the specifications to the lower level.

(Mapping specs. on design parameters)



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Introduction: Synthesis methods



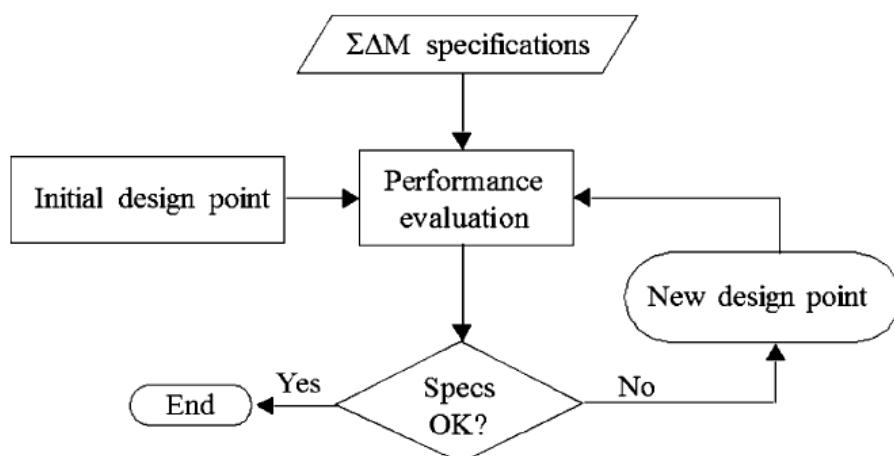
■ Knowledge-based tools: capture the knowledge of experienced designers

- Short execution times
- Not optimized: design procedures usually based on approximate equations and models
- Closed tools
 - Limited to a reduced number of topologies
 - Addition of new ones usually restricted to the tool developers

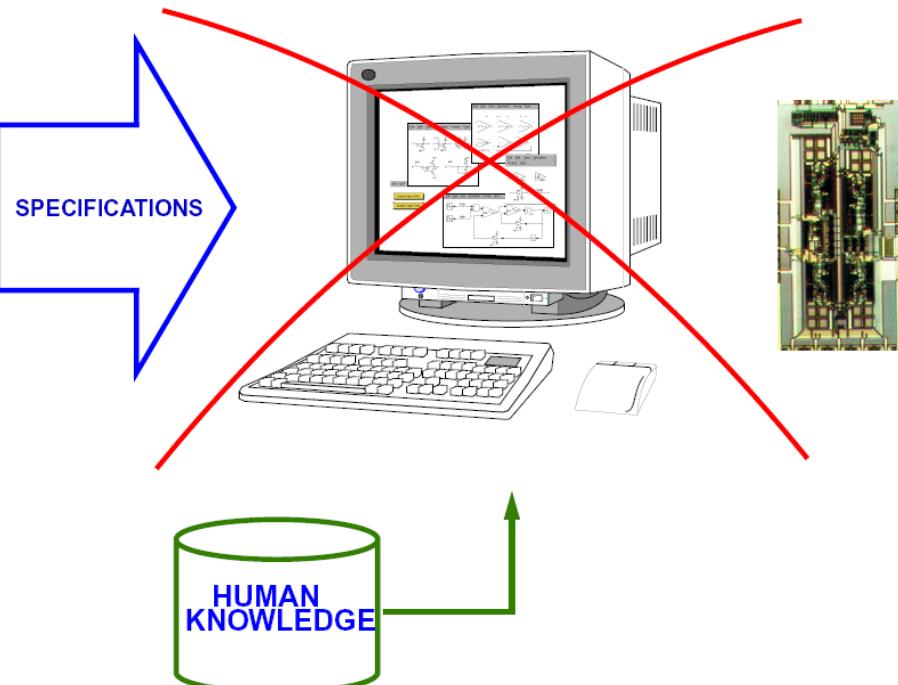
■ Optimization-based tools: based on an iterative optimization procedure

- Cost function evaluation by numerical methods: **equations** or **simulations**
- Two main optimization techniques:
 - **Deterministic:** parameter updating needs information on the cost function and on their derivatives
 - Optimization process may be trapped in a local minimum of the cost function
 - Useful for fine tuning of suboptimal designs
 - **Statistical:** parameters are changed randomly
 - Avoid local minima
 - Appropriate for global optimization
 - No good initial design point is needed
 - Requires larger computational cost

Introduction: Optimization-based synthesis approach



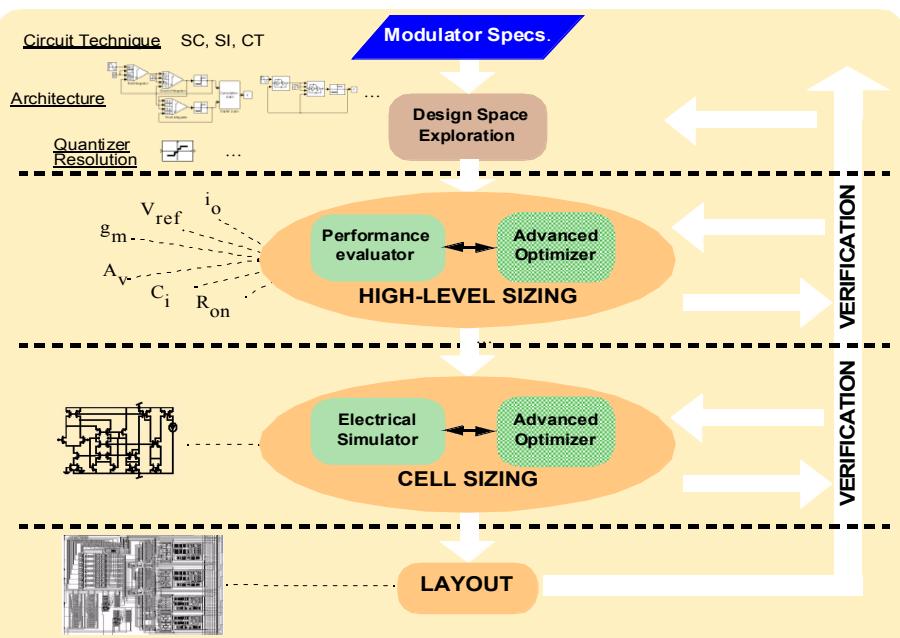
Introduction



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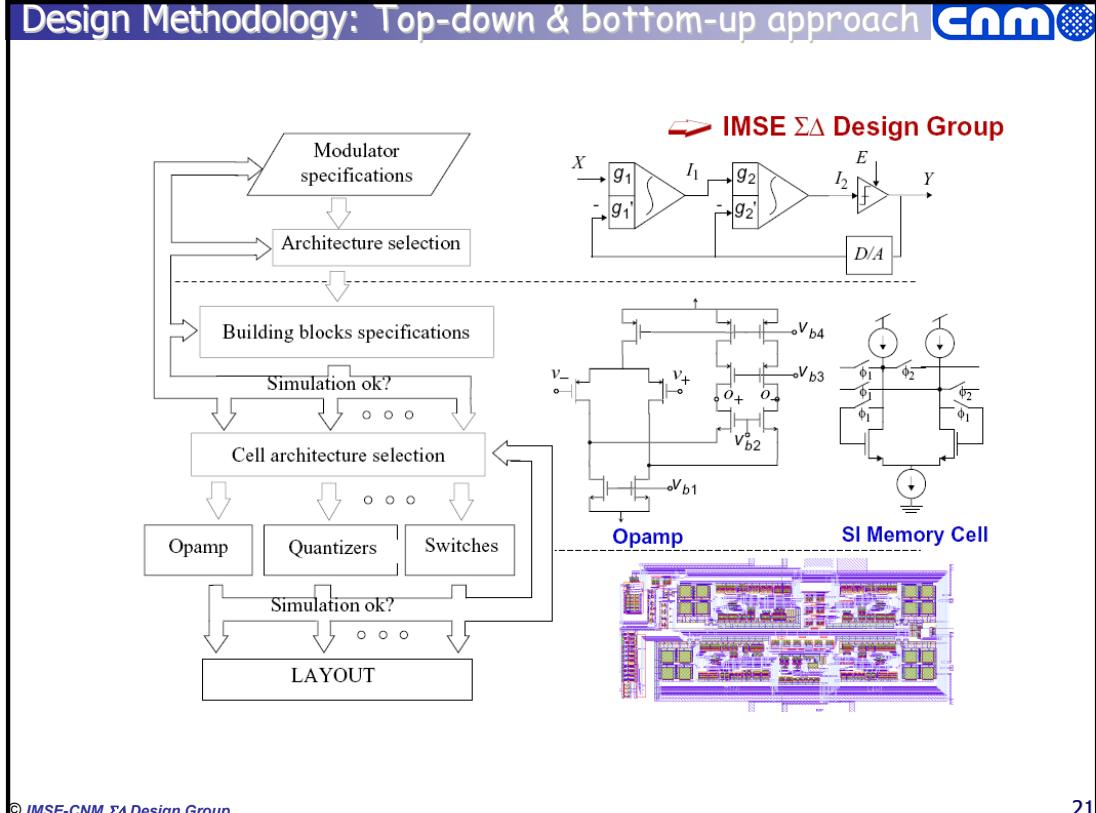
Design Methodology: Top-down & bottom-up approach



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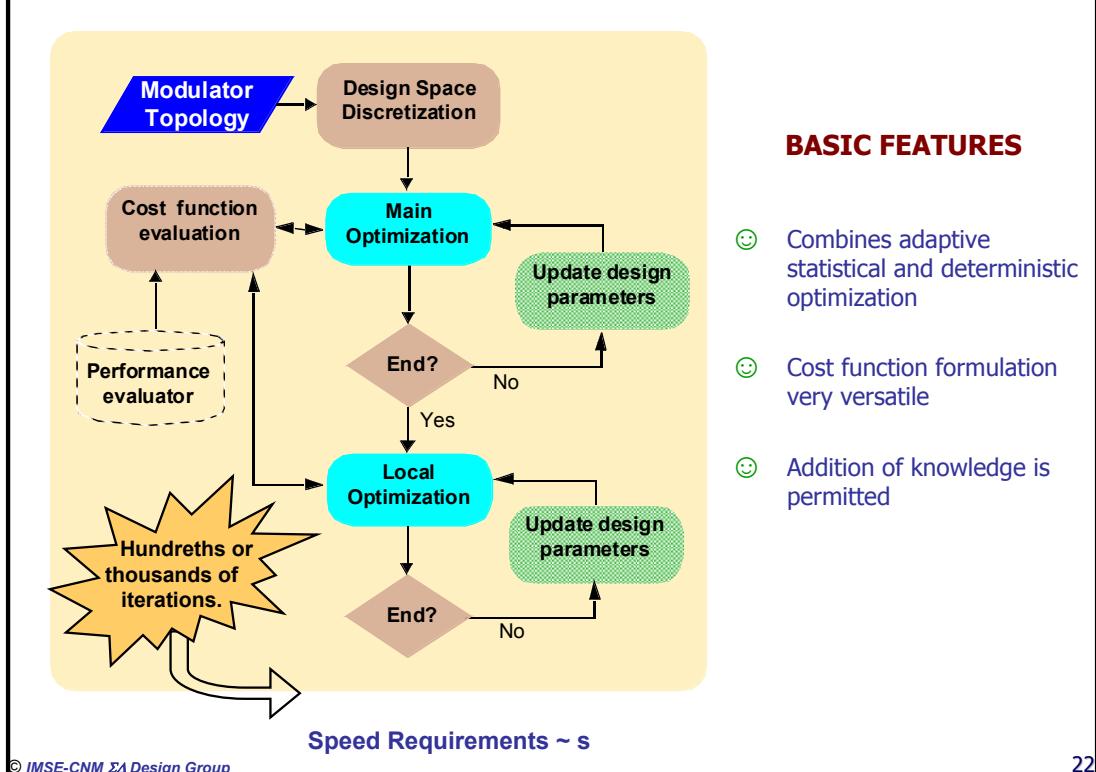
Design Methodology: Top-down & bottom-up approach



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Design Methodology: Optimization



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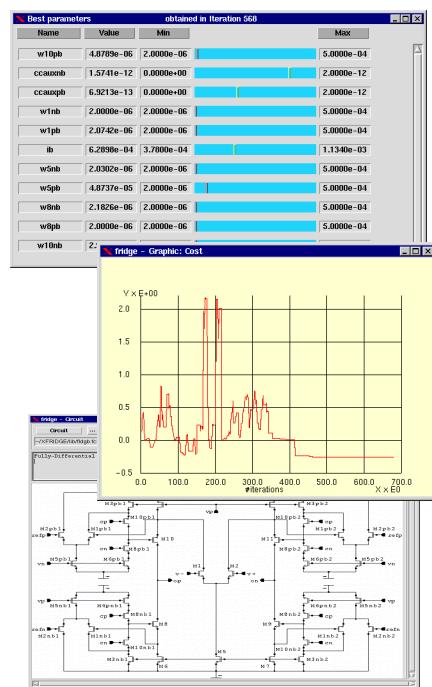
Design Methodology: Optimization



OPTIMIZATION-BASED ENGINE (FRIDGE)

- Interacts with any kind of performance evaluation approach
- Statistical + Deterministic techniques
- Designer's expertise can be added through powerful tools (embedded C++)
- Between Optimization and Knowledge-based approaches, taking the best from both worlds
- Used both for spec transmission and for cell-level sizing
- In process of being complemented with Evolutionary Algorithms

▪ Intese internal use



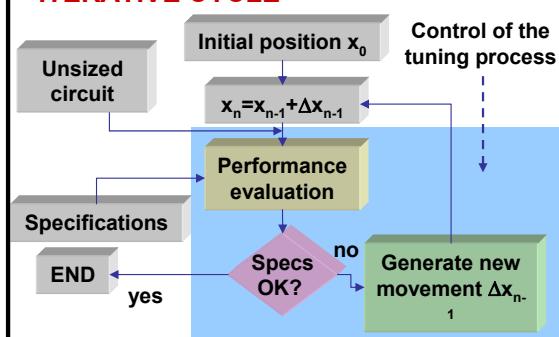
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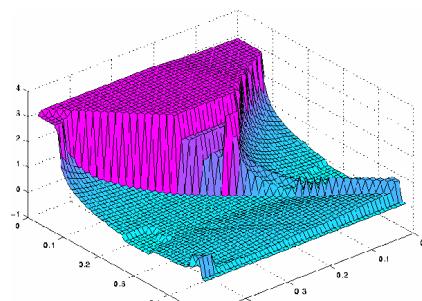
Design Methodology: Optimization



ITERATIVE CYCLE



EXAMPLE OF A COST FUNCTION



FORMULATION OF THE COST FUNCTION

Problem: minimize $y_{oi}(x)$, $1 \leq i \leq P$
 subjected to $y_{rk}(x) \geq Y_{rk}$ or $y_{rk}(x) \leq Y_{rk}$, $1 \leq k \leq R$

Target Specification
P design objectives
R restrictions
Cost Function

Weights used to give priority to the fulfillment of their corresponding specifications

$$\Psi(x) = \begin{cases} \left(-\sum_i w_i \log(y_{oi}) \right) & \text{if } x \in R_A \\ \max_k \left[-w_k \log\left(\frac{y_{rk}}{Y_{rk}}\right) \right] & \text{if } x \notin R_A \end{cases}$$

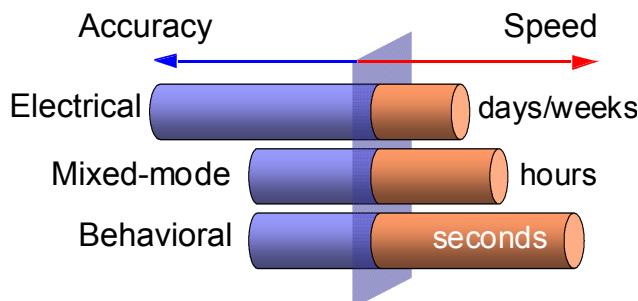
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Simulation of $\Sigma\Delta$ Ms:

- ◆ Strongly non-linear circuits
- ◆ Oversampling → long time-domain simulation

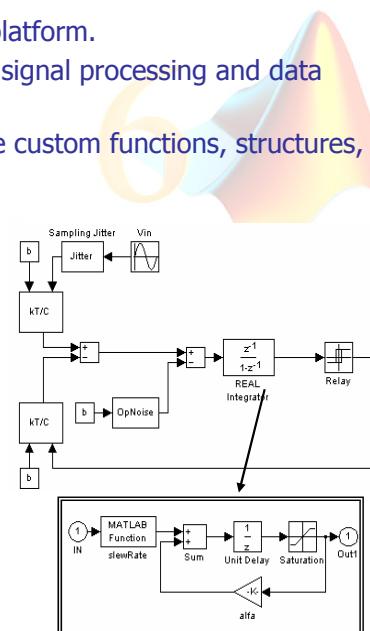
Techniques



- MATLAB-SIMULINK is a widely spread platform.
- Direct access to very powerful tools for signal processing and data manipulation.
- Provides a high-level language to create custom functions, structures, Graphical User Interfaces (GUIs), etc.

Simulink block libraries
(Malcovati et al., IEEE Trans. CAS, 2003)

- Limited to SC circuits.
- Limited accuracy:
 - Transient response in both clock-phases not considered.
 - Non-linear opamp DC gain, non-linear switch-on resistance, non-linear capacitors not included.
- Models based on MATLAB functions → excessive CPU time.



SIMSIDES: Description of the toolbox



Graphical User Interface

SC, SI and CT techniques

Global and efficient optimization techniques

Collection of post-processing routines

Precise behavioural models

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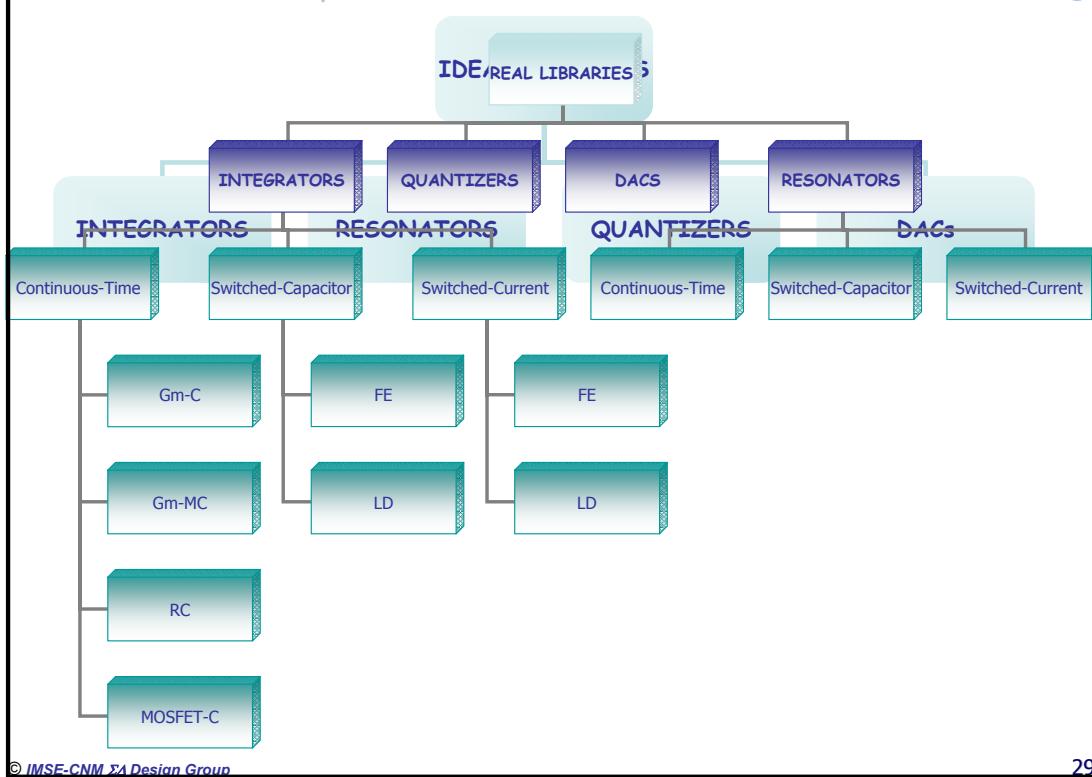
SIMSIDES: Description of the toolbox



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SIMSIDES: Description of the toolbox



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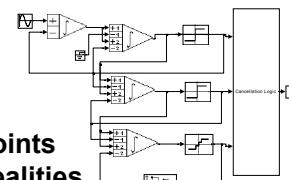
SIMSIDES: Behavioral modeling using S-functions



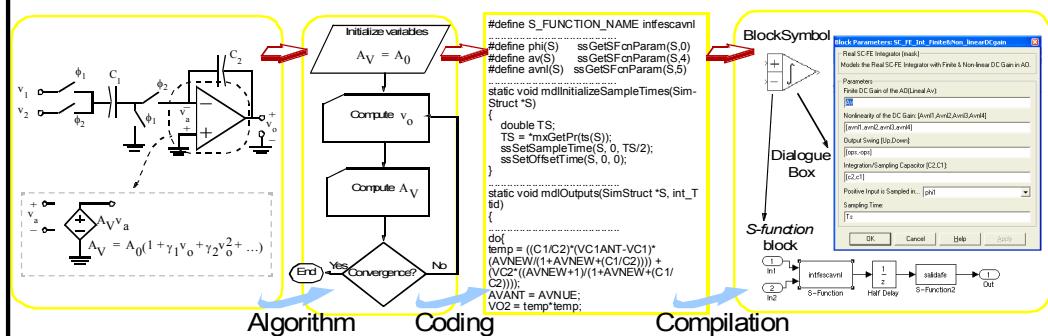
S-functions

- Precise models:
 - All major non-idealities included
 - Time-domain models
- Models based on C-code → fast!!

65536 points
All non-idealities



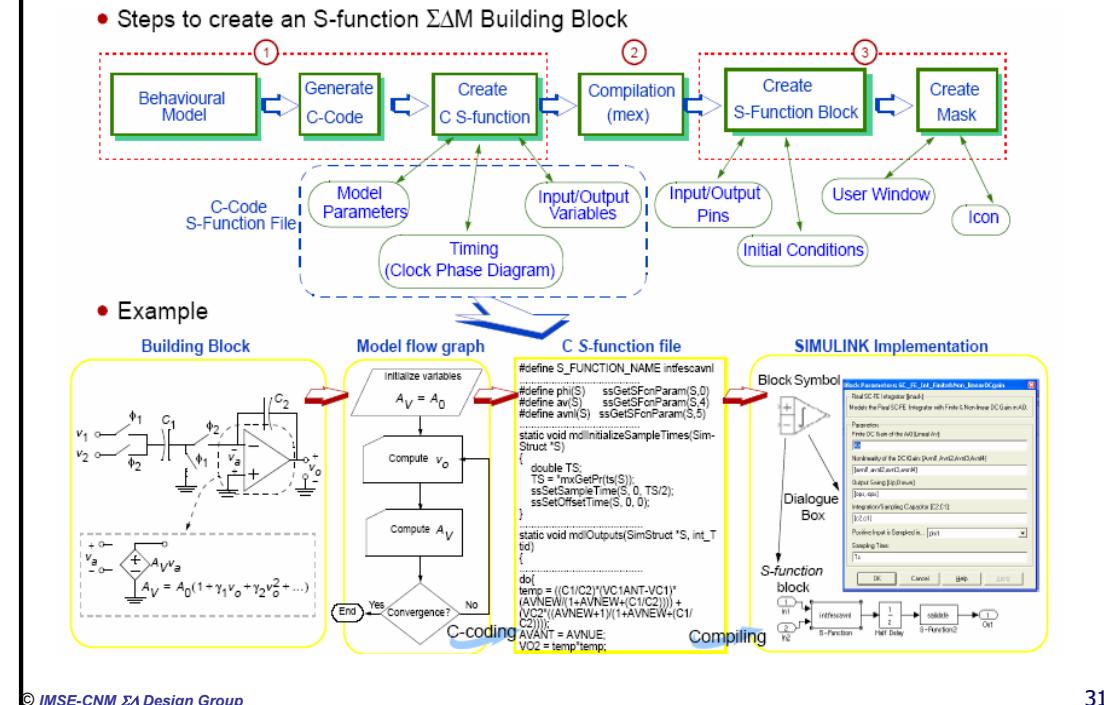
S-functions	M-functions
3 s.	141 s.



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SIMSIDES: Creating S-functions



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SIMSIDES: Behavioral models included in the toolbox

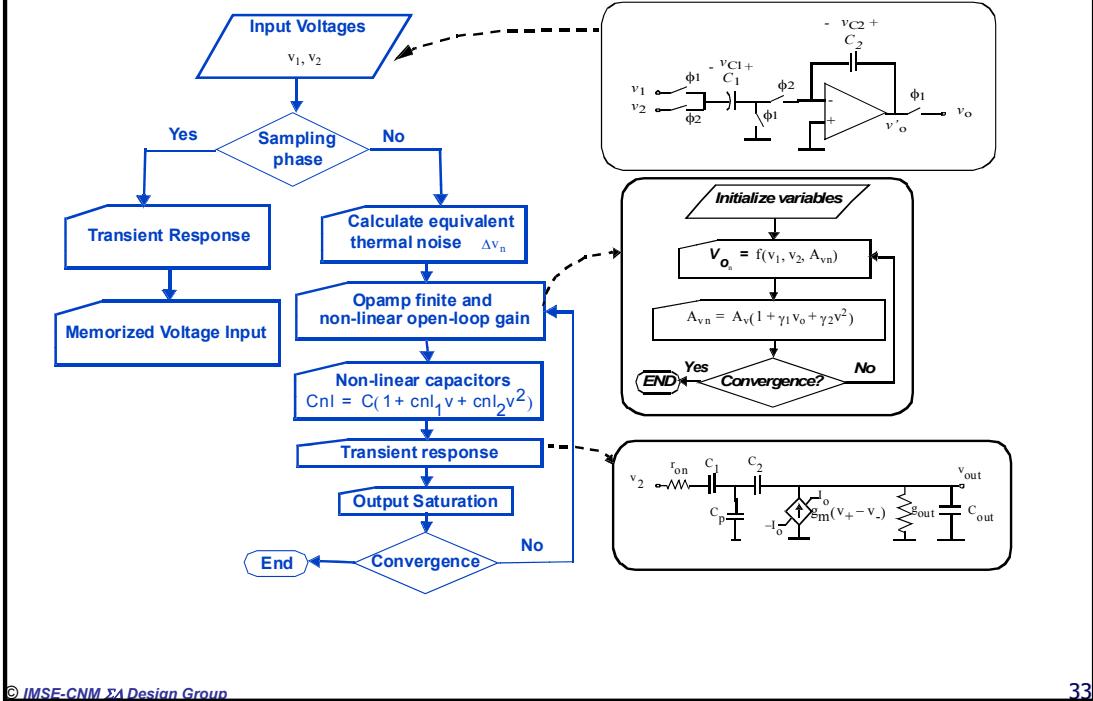


Circuit Tec.	Building Block	Non-ideality	
		Integrators	Opamps
SC	Opamps	Finite and non-linear open-loop DC gain Incomplete settling error (both clock phases considered) Output swing limit Thermal noise	
	Switches	Thermal noise, switch-on (non-linear) resistance	
	Capacitors	Mismatch, non-linearity	
	Resonators	Gain and integrator errors	
SI	Integrators	Linear and non-linear gain error Finite output-input conductance ratio error Charge injection error Incomplete settling error	
	Resonators	Gain and integrator errors	
	Opamps		
	Switches		
CT	Integrators	Finite and non-linear DC gain Non-linear transconductance Thermal noise Output swing limit Transient response	
	Resonators	Gain and integrator errors	
	Opamps		
	Switches		
Clock	Jitter		
	Comparators	Hysteresis and Offset	
	Quantizers	Non-linearity, gain error, loop delay, offset	
DACs	DACs		

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SIMSIDES: Behavioral modeling of SC FE Integrators



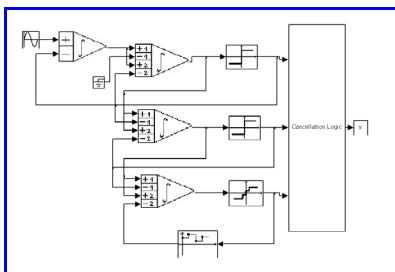
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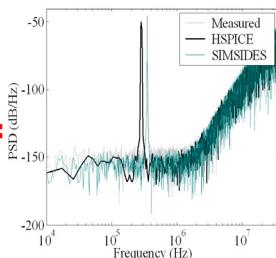
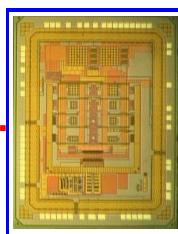
SIMSIDES: Model accuracy



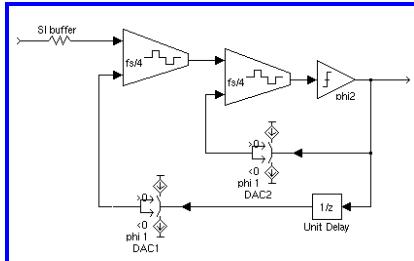
A 0.25μm CMOS 2-1-1 cascade ΣΔ Modulator for ADSL



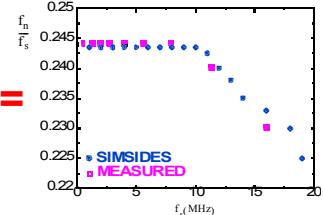
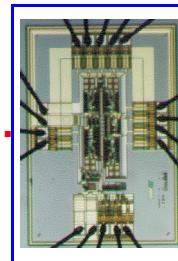
VS.



A 0.8μm CMOS 4th-order bandpass SI ΣΔ Modulator for digital radio



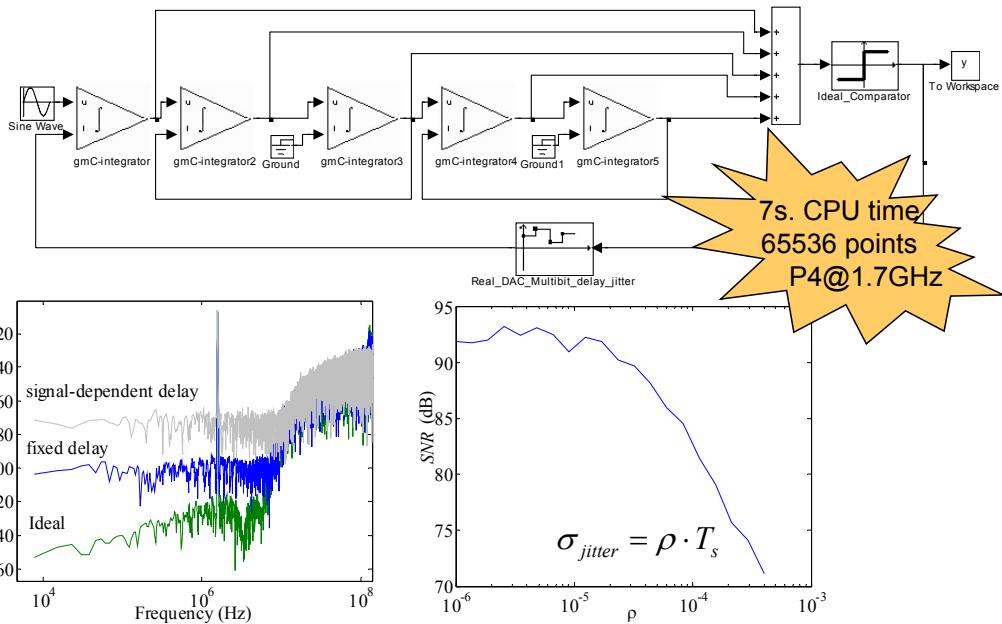
VS.



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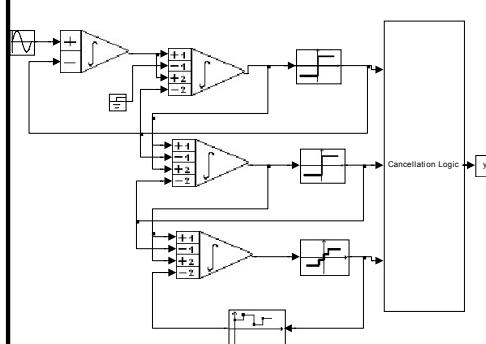
SIMSIDES: Simulating a CT 5th-order LP SL $\Sigma\Delta M$



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SIMSIDES: Sizing a SC 2-1-1 cascade $\Sigma\Delta M$



Specifications

- 13bits@4.4Ms/s
- Minimum area and power consumption

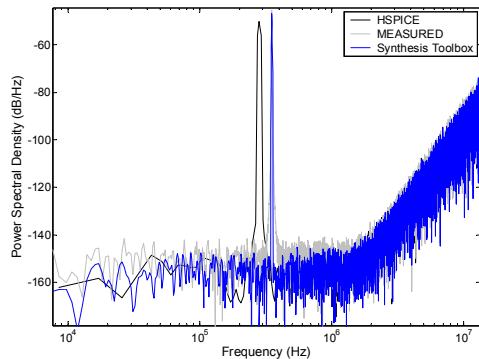
SPECIFICATIONS FOR:		I Int.	II Int.	III Int.	IV Int.
Modulator	Sampling frequency (MHz)	70.4			
	Oversampling ratio	16			
	Reference Voltage (V)	1.5			
Integrators	Feed-back capacitor (pF)	2.64	0.9	0.9	0.45
	Cap. Non-linearity (ppm/V ²)	15			
	Switch on-resistance (Ω)	≤ 150			
Opamps	DC-gain (dB)	≥ 81	≥ 65	≥ 54	≥ 54
	Input noise PSD (nV/Hz ^{1/2})	≤ 1.6	≤ 1.5	≤ 2.9	≤ 2.9
	Transconductance (mA/V)	≥ 6.4	≥ 7	≥ 3.4	≥ 3.4
	Max. Output Current (mA)	≥ 1.5	≥ 2.2	≥ 1.6	≥ 1.6
Comps.	Offset (mV)	≤ 10			
	Hysteresis (mV)	≤ 20			
A/D/A converter	Resolution (bits)	3			
A/D/A converter	DAC INL	$\leq 0.5\%FS$			

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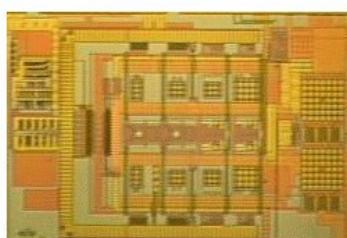
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Synthesis
All non-idealities
40.8 minutes

SIMSIDES: Sizing a SC 2-1-1 cascade $\Sigma\Delta M$



	Synthesis Toolbox	Measured
Clock frequency (MHz)	70.4	
Digital output rate (Ms/s)	4.4	
Oversampling ratio	16	
Reference voltage (V)	1.5	
Technology	0.25μm CMOS@2.5V	
Power consumption (mW)	-	55
Area (mm ²)	-	2.78
Resolution (bits)	13.3	12.7



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SIMSIDES: Conclusions

- SIMSIDES is a $\Sigma\Delta M$ Synthesis Toolbox in the Matlab/Simulink environment.
 - ◆ It allows to efficiently map the modulator specifications into building-block specifications.
 - ◆ It deals with the synthesis of $\Sigma\Delta M$ s using both DT and CT circuit techniques.
- The implementation platform brings numerous advantages with a relatively low penalty in computation time.

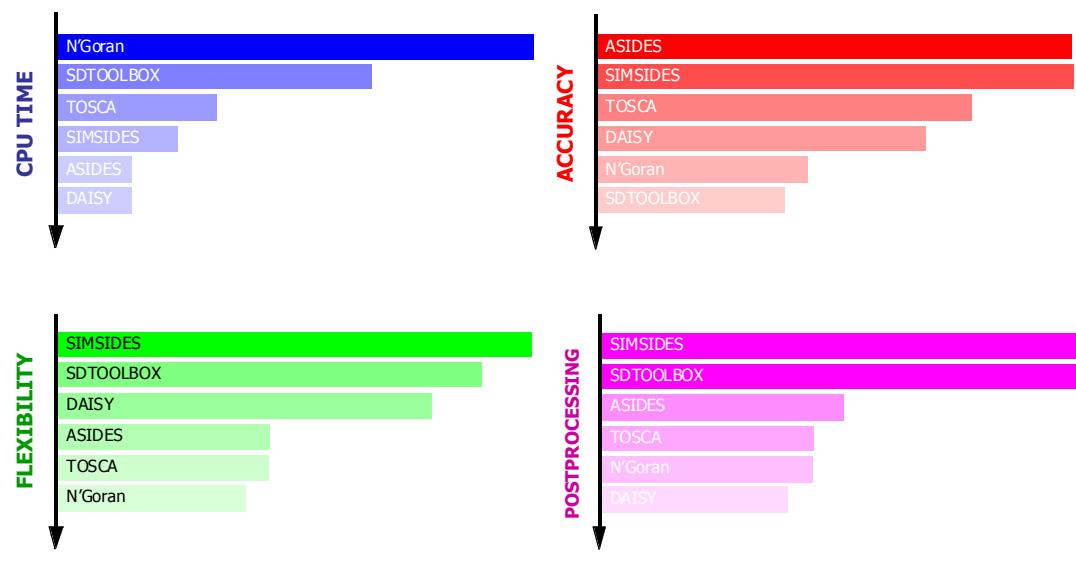
SIMULATOR	CPU-time	Flexibility	User Interface	Accuracy
ASIDES	Secs	Low	Netlist	High
DAISY	Secs	Medium	Graphical	Moderate
SDTOOLBOX (Brigati)	Secs- mins	High	Graphical	Moderate/
SIMSIDES (This work)	Secs	High	Graphical	High

Simulation Approach	CPU Time (s)
Using MATLAB-functions (Brigati, ISCAS99)	415
Using S-functions (This work)	4-5

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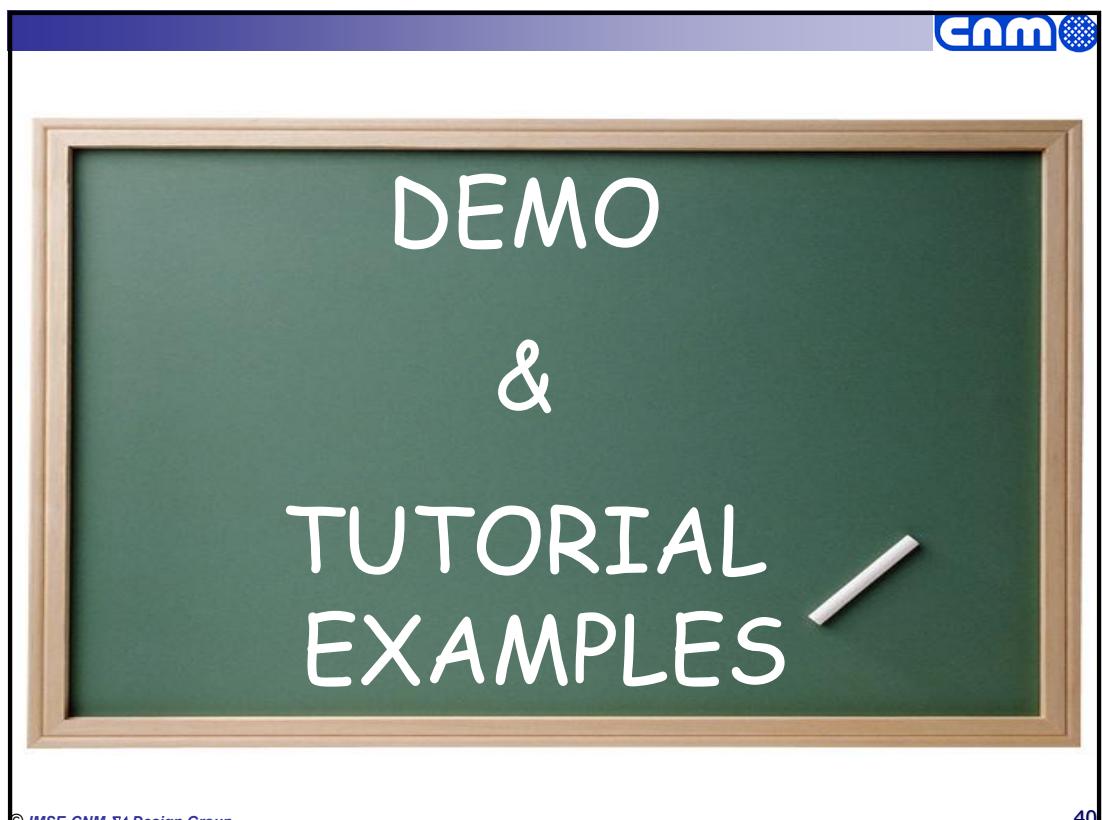
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SIMSIDES: Conclusions



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