

CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Advanced Architectures and State of the Art

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KTH, Stockholm, April 23-27

OUTLINE



1. State of the Art on SC $\Sigma\Delta$ ADCs

2. State of the Art on CT $\Sigma\Delta$ ADCs

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Single-loop Single-bit $\Sigma\Delta$ ICs

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ³
[Kero94]	21.00	8.00E+02	320	4th-ord	3um MS / 10V	2.50E-02	14.90	351.28
[Kash99]	20.00	8.00E+02	320	4th-ord	0.6um MS / 5V	1.60E-02	19.07	137.22
[Wang03]	18.50	4.80E+04	--	6th-ord	0.35um MS / 5V-3.3V	2.30E-01	12.93	71.59
[Yama94]	18.00	2.00E+01	1600	4th-ord	1.2um MS / 5V	1.30E-03	247.96	2.64
[Brid04]	17.20	8.00E+02	320	4th-ord	0.6um MS (2P) / 5V	5.00E-02	415.11	0.91
[Brid02]	17.10	8.00E+02	320	4th-ord	0.6um MS / 5V	5.00E-02	444.90	0.79
[Snoe01]	16.70	2.20E+04	64	4th-ord	0.5um MS / 2.5V	2.50E-03	1.07	248.96
[Mede97]	16.40	9.60E+03	256	2nd-ord	0.7um STD / 5V	1.71E-03	2.06	104.79
[Coba99]	16.00	4.00E+04	64	4th-ord	0.5um STD / 1.5V	1.00E-03	0.38	428.81
[Bran91b]	16.00	5.00E+04	256	2nd-ord	1um MS / 5V	1.38E-02	4.21	38.84
[Grilo96]	15.30	7.00E+03	286	2nd-ord	0.6um STD / 1.8V	2.00E-03	7.08	14.22
[Mau00]	15.30	5.00E+05	64	5th-ord	0.6um STD / 5V	2.10E-01	10.41	9.67
[Romb03]	15.30	5.00E+05	96	5th-ord	0.8um STD / 3.3V	4.30E-02	2.13	47.24
[Bose88]	14.50	1.60E+04	256	2nd-ord	3um MS / 5V	1.20E-02	32.37	1.79
[Yao04]	14.40	4.00E+04	100	3rd-ord	0.18um STD / 1.5V	1.20E-04	0.45	259.04
[Dess01]	14.40	5.00E+04	100	3rd-ord	0.35um MS / 5V	1.20E-04	0.45	259.04
[Klem06]	14.37	2.70E+05	48	4th-ord	0.18um STD / 1.5V	1.20E-04	0.45	259.04
[Send97]	14.30	6.00E+03	128	2nd-ord	0.5um STD / 5V	1.20E-04	0.45	259.04
[Burn96]	14.20	1.95E+04	256	2nd-ord	0.2um MS / 5V	1.20E-04	0.45	259.04
[Bur01]	14.00	4.00E+04	192	3rd-ord (IF-to-BB)	0.25um STD / 5V	1.20E-04	0.45	259.04
[Nade94]	13.80	2.00E+03	250	3rd-ord	0.18um STD / 1.5V	1.20E-04	0.45	259.04
[Goes06]	13.50	2.00E+04	256	2nd-ord	0.18um MS / 5V	1.20E-04	0.45	259.04
[Opt91]	13.50	5.00E+05	64	4th-ord (DFB)	1.5um STD / 5V	1.20E-04	0.45	259.04
[Than97]	13.40	1.95E+05	128	2nd-ord	1.2um STD / 5V	1.20E-04	0.45	259.04
[Chen03]	13.10	2.00E+05	520	2nd-ord	0.13um STD / 5V	1.20E-04	0.45	259.04
[Till01]	13.00	1.60E+04	64	2nd-ord	0.25um STD / 5V	1.20E-04	0.45	259.04
[Sauv03]	13.00	1.60E+04	64	2nd-ord (SO)	0.18um MS (MM) / 0.65V	4.55E-05	0.35	58.90
[Bal02]	13.00	2.20E+04	64	4th-ord	0.5um MS / 1.8V	1.70E-03	9.43	2.17
[Kesk02]	13.00	4.00E+04	256	2nd-ord (RO)	0.35um MS (2P) / 1V	5.60E-03	17.09	1.20
[Pelu98]	12.50	3.20E+04	48	3rd-ord	0.5um STD / 0.9V	4.00E-05	0.22	67.00
[Shim05]	12.37	4.00E+05	16	3rd-ord	0.18um / 1.8V	4.00E-03	1.89	6.99
[Sauv02]	12.20	1.60E+04	64	2nd-ord (SO)	0.18um STD / 0.7V	8.00E-05	1.06	11.05
[Pelu97]	12.00	6.80E+03	74	2nd-ord	0.7um STD / 1.5V	1.01E-04	3.63	2.82
[Au97]	12.00	1.60E+04	64	3rd-ord	1.2um MS / 2V	3.40E-04	5.19	1.97
[Kesk02]	12.00	1.00E+05	102.4	2nd-ord (RO)	0.35um MS (2P) / 1V	5.60E-03	13.67	0.75
[Sauv03]	11.00	3.20E+04	32	2nd-ord (SO)	0.18um MS (MM) / 0.65V	4.55E-05	0.69	7.36
[Chen03]	9.90	1.00E+06	104	2nd-ord	0.13um STD / 1.5V	1.28E-03	1.33	1.79
[Shim05]	8.87	1.00E+07	8	3rd-ord	0.18um / 1.8V	4.00E-03	0.85	1.37
[Burd01]	8.70	7.68E+06	24	3rd-ord (IF-to-BB)	0.25um STD / 2.5V	1.35E-02	4.23	0.25
[Gero03]	8.50	5.00E+02	16	3rd-ord (SWO, LR)	0.8um MS (2P) / 1.8V	2.20E-06	12.15	0.07
[Wismar06]	8.35	4.00E+04	85	1st-order	90nm STD / 0.2V	4.40E-07	0.03	24.01
[Chen03]	8.10	2.00E+06	52	2nd-ord	0.13um STD / 1.5V	1.28E-03	2.32	0.29

- 2nd-order loop ~ 40%
- 3rd-order loop ~ 20%
- 4th-order loop ~ 30%

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Single-loop Multi-bit $\Sigma\Delta$ ICs

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ³
[Bair96]	13.66	5.00E+05	16	4th-ord(4b)	1.2um MS / 5V	5.80E-02	8.96	3.61
[Chen95]	15.65	4.00E+04	64	2nd-ord(3b)	1.2um MS / 5V	6.75E-02	32.82	3.91
[Geer00]	15.80	2.50E+06	24	3rd-ord(4b)	0.65um MS / 5V	2.95E-01	2.07	68.85
[Geer00]	12.00	1.25E+07	24	3rd-ord(4b)	0.65um MS / 5V	3.80E-01	7.42	1.38
[Harr94]	16.00	3.90E+04	128	3rd-ord(1b, 5b) (dual)	2um MS (2P) / 5V	8.50E-02	33.26	4.92
[Leun97]	19.30	9.60E+04	64	7th-ord(1.5b)	0.8um MS / 5V	7.60E-01	12.26	131.36
[Nys97]	19.00	8.00E+02	512	2nd-ord(3b)	2um MS / 5V	2.18E-03	5.19	252.36
[Fras04]	18.04	4.00E+04	153.6	5th-ord (17level)	0.35um MS / 5V	3.00E-01	27.83	24.17
[Yang03]	18.70	4.00E+04	128	5th-ord(17level)	0.35um MS (2P) / 5V-3.3V	6.80E-02	3.99	266.27
[Lei01]	15.99	4.80E+04	128	3rd-order(10level)	0.25um / 5V	1.25E-02	4.01	40.41
[Fool00]	16.22	4.80E+04	64	2nd-ord(5b)	0.5um STD / 3.3V	6.86E-02	18.72	10.18
[Grilo02]	16.70	4.00E+04	64	2nd-ord(5b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	13.00	1.00E+06	32	2nd-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	13.50	4.00E+05	57.5	2nd-ord(6b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	12.83	1.25E+06	18	2nd-ord(6b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Mille03]	11.67	3.84E+06	12	2nd-ord(6b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Joha03]	16.00	9.00E+01	512	1st-ord (3b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Kuo02]	13.70	1.25E+06	12	4th-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Kuo02]	13.00	2.00E+06	12	4th-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Reut02]	14.00	2.50E+06	32	5th-ord(1.5b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Balm04]	13.70	2.50E+07	8	4th-ord(4b)	0.35um STD / 3.3V	6.86E-02	18.72	10.18
[Gagg03]	13.80	6.00E+05	96	2nd-ord (3b)	0.13um MS / 1.5V	8.00E-03	1.26	41.96
[Jiang02]	13.80	4.00E+06	8	5th-ord(4b)	0.13um MS / 1.5V	7.00E-03	0.60	43.96
[Kwon06]	14.00	4.40E+06	32.7	2nd-ord (4b)	0.13um MS / 1.5V	2.40E-03	0.82	22.07
[Lee06]	13.90	2.20E+06	60	2nd-ord (5level)	0.13um MS / 1.5V	2.90E-03	2.81	0.23
[Fuji06]	12.75	6.40E+06	12.5	4th-ord(4b) 2S	0.13um MS / 1.5V	3.44E-02	1.18	7.69
[Fuji06]	11.83	8.00E+06	12.5	4th-ord(4b) 2S	0.18um MS / 1.8V	3.44E-02	1.18	7.69
[Gagg04]	14.37	3.00E+05	350	2nd-ord (3b)	0.13um MS / 1.5V	8.00E-03	1.26	41.96
[Gagg04]	13.37	1.10E+06	47	2nd-ord (3b)	0.13um MS / 1.5V	7.00E-03	0.60	43.96
[Gomez02]	12.83	4.00E+05	65	2nd-ord(5b)	0.13um STD / 1.5V	2.40E-03	0.82	22.07
[Gomez02]	8.01	4.00E+06	12	2nd-ord(5b)	0.13um STD / 1.5V	2.90E-03	2.81	0.23
[Yu05]	9.37	4.00E+06	10	2nd-ord(4b-dual)	90nm STD / 1.3V	2.10E-03	0.79	2.08
[Yu05]	10.70	2.00E+06	20	2nd-ord(4b-dual)	90nm STD / 1.3V	2.10E-03	0.63	6.58
[Yu05b]	12.50	4.00E+05	50	2nd-ord(4b-dual)	90nm STD / 1.3V	2.10E-03	0.91	15.95
[Gomez02]	12.00	4.00E+05	65	2nd-ord(5b)	0.13um STD / 1.2V	1.40E-03	0.85	11.96
[Koh05]	10.70	3.88E+06	19.79	2nd-ord(5level)	90nm STD / 1.2V	1.20E-03	0.19	22.33

Multi-bit resolution:

- 3 or 4 bits ~ 70%

Loop order:

- 2nd-order ~ 50%
- + 2nd-order loop ~ 50% (easier to stabilize w/ multi-bit)

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Cascade Single-bit $\Sigma\Delta$ ICs

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁵
[Yoon98]	15.30	6.40E+04	16	2-1-1-2	2um MS / 6.6V	7.90E-02	30.60	3.29
[Fui97]	18.15	4.80E+04	128	2-2	0.7um MS / 5V	5.00E-01	35.91	20.17
[Marg98a]	14.80	2.00E+06	24	2-1-1	1um MS / 5V	2.30E-01	4.03	17.66
[Miac98]	14.82	5.00E+04	64	2-2	3um MS / 5V	7.40E-02	51.03	1.42
[Rebe90]	15.00	1.80E+05	64	1-1-1	1.5um MS / 5V	7.60E-02	12.89	6.35
[Kito94]	16.15	4.40E+04	64	2-2	1.2um BiCMOS / 5V	1.02E-01	31.82	5.72
[Wang01]	18.10	2.50E+04	64	2-2	0.6um MS / 5V	7.50E-02	10.68	65.68
[Will94]	17.00	5.00E+04	128	2-1	1um MS / 5V	4.70E-02	7.17	45.62
[Yin93]	15.70	3.20E+05	64	2-1	1.2um STD / 5V	6.50E-02	3.82	34.82
[Yin94]	15.82	1.50E+06	64	2-1-1	2um BiCMOS / 5V	1.80E-01	2.07	69.61
[David03]	13.00	1.00E+03	256	2-1	1.5um MS / 5V	---	---	---
[Geer99]	15.00	2.20E+06	24	2-1-1	0.5um MS / 3.3V	2.00E-01	2.77	29.48
[Mor00]	14.00	2.20E+06	24	2-2-2	0.35um MS / 3.3V	1.50E-01	4.16	9.83
[Gome00]	16.65	4.40E+04	128	2-1	0.6um MS / 3V	2.20E-02	4.86	52.88
[Lee03]	14.16	1.00E+06	64	2-2	0.35um MS (2P) / 1.8V-2.4V	1.50E-01	8.20	5.57
[Lee03]	12.00	2.00E+06	32	2-2	0.35um MS (2P) / 1.8V	1.50E-01	18.31	0.56
[Olia02]	13.50	3.60E+05	36	2.2	0.4um MS / 1.8V	5.00E-03	1.20	24.12
[Rabi97]	16.10	5.00E+04	80	2-1	0.8um MS / 1.8V	2.50E-03	0.71	246.29
[Saue03]	13.00	1.60E+04	64	2-1	0.18um MS (MiM) / 0.65V	6.18E-05	0.47	43.37
[Saue03]	12.17	3.20E+04	32	2-1	0.18um MS (MiM) / 0.65V	6.18E-05	0.42	27.45
[Ahn05b]	12.70	4.80E+04	64	2-2 (switched-RC int.)	0.35um MS / 0.6V	1.00E-03	3.13	5.30

Most-common cascades:

- 2-1 → 3rd order, 2 stage
- 2-2 → 4th order, 2 stage
- 2-1-1 → 4th order, 3 stage

DT-LP- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Cascade Multi-bit $\Sigma\Delta$ ICs

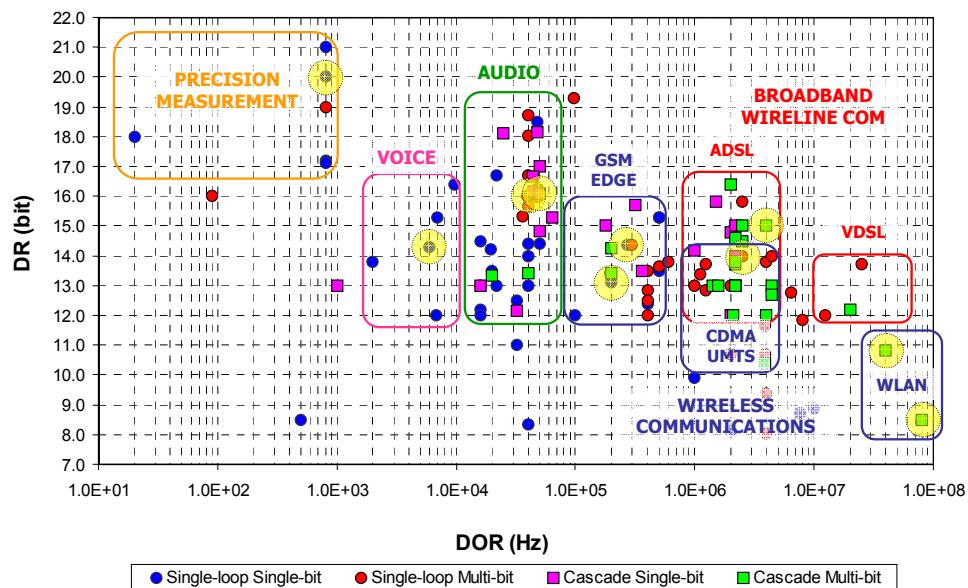
Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁵
[Broo97]	14.50	2.50E+06	8	2-0(5b)	0.6um MS / 5V	5.50E-01	9.49	6.09
[Bran91a]	12.00	2.10E+06	24	2-1(3b)	1um STD / 5V	4.10E-02	4.77	2.14
[Mede99]	13.00	2.20E+06	16	2-1-1(3b)	0.7um STD / 5V	5.50E-02	3.05	6.70
[Fui90]	15.00	2.50E+06	8	2(4b)-1(4b)-1(4b)	0.5um MS / 5V	1.05E-01	1.28	63.81
[Dedi94]	14.25	2.00E+05	16	2(1.5b)-2(1.5b)-2(1.5b)	1.2um MS / 5V	4.00E-02	10.26	4.74
[Mor00]	13.00	2.20E+06	24	2-2(5b)	0.35um MS / 3.3V	9.90E-02	5.49	3.72
[Gupta02]	14.60	2.20E+06	29	2-1-1(2b)	0.35um STD / 3.3V	1.80E-01	3.29	18.81
[Feld98]	13.00	1.40E+06	16	2-2-2(1.5b)	0.7um MS / 3.3V	8.10E-02	7.06	2.90
[Rio01b]	13.00	2.20E+06	16	2-1-1(4b)	0.35um STD / 3.3V	7.37E-02	4.09	5.00
[Rio01b]	12.00	4.00E+06	16	2-1-1(4b)	0.35um STD / 3.3V	7.83E-02	4.78	2.14
[Bosi05]	12.20	2.00E+07	4	2(4b)-pipeline(9b)	0.18um MS/ 3.3V-1.8V	2.40E-01	2.55	4.60
[Lamp01]	13.00	1.56E+06	32	2-2(3b)	0.35um MS / 2.5V	5.00E-02	3.91	5.23
[Rio02b]	13.70	2.20E+06	32	2-1-1(3b)	0.25um STD / 2.5V	7.17E-02	2.45	13.56
[Rio02b]	13.00	4.40E+06	16	2-1-1(3b)	0.25um STD / 2.5V	7.17E-02	1.99	10.28
[Vieu01]	15.00	4.00E+06	16	2(5b)-(2b)-1(3b)	0.5um MS / 2.5V	1.50E-01	1.14	71.47
[Rio03]	13.80	2.20E+06	32	2-1-1(3b)	0.25um MS (MiM) / 2.5V	6.58E-02	2.10	16.98
[Rio03]	12.70	4.40E+06	16	2-1-1(3b)	0.25um MS (MiM) / 2.5V	6.58E-02	2.25	7.39
[Para06]	10.8	4.00E+07	8	2-2 (4b)	90nm STD / 1.4V	7.80E-02	1.09	4.07
[Taba03]	8.50	8.00E+07	4	2(LP1.5b)-2(BP4b)	0.13um MS / 1.2V	1.75E-01	6.04	0.15
[Dezz03]	13.40	2.00E+05	195	2-1 (5-level)	0.13um MS / 1.2V	2.40E-03	1.11	24.30
[Dezz03]	10.40	3.84E+06	100	2-1 (5-level)	0.13um MS / 1.2V	4.30E-03	0.83	4.07
[Reve03]	13.33	2.00E+04	64	2-1(1.5b) (2S)	0.35um MS (2P, low-Vt) / 0.8V	6.00E-05	0.29	88.09
[Ahn05]	13.40	4.00E+04	64	2-2(1.5b)	0.35um MS / 0.6V	1.00E-03	2.31	11.67
[Brew05]	16.40	2.00E+06	8	2-2-0(dual)	0.25um MS (2P) / ?V	4.75E-01	2.75	78.59

Multi-bit quantization is mostly used in the last modulator stage

DT-LP- $\Sigma\Delta$ Ms: State of the Art



DT LPSDMs organized per architecture

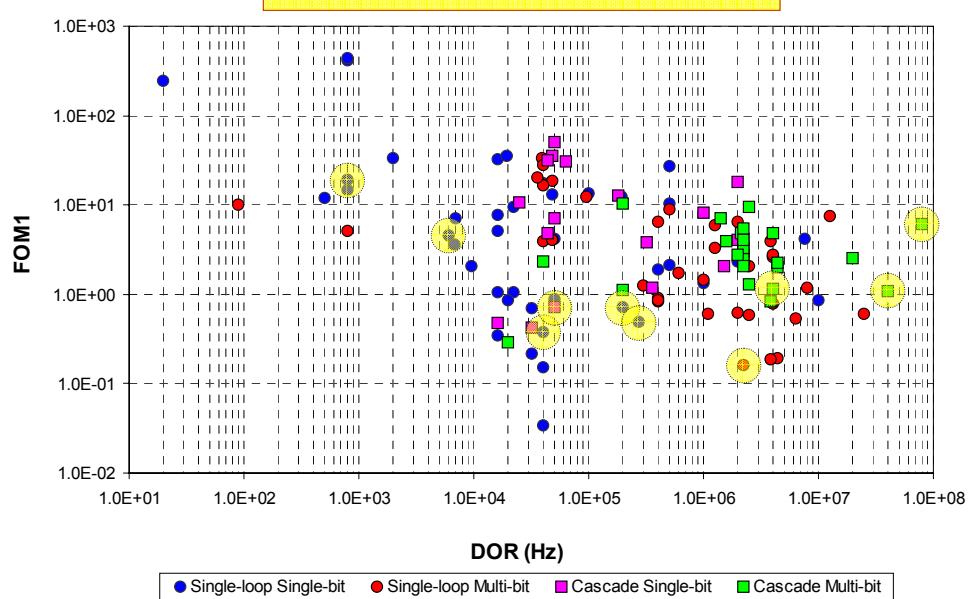


DT-LP- $\Sigma\Delta$ Ms: State of the Art



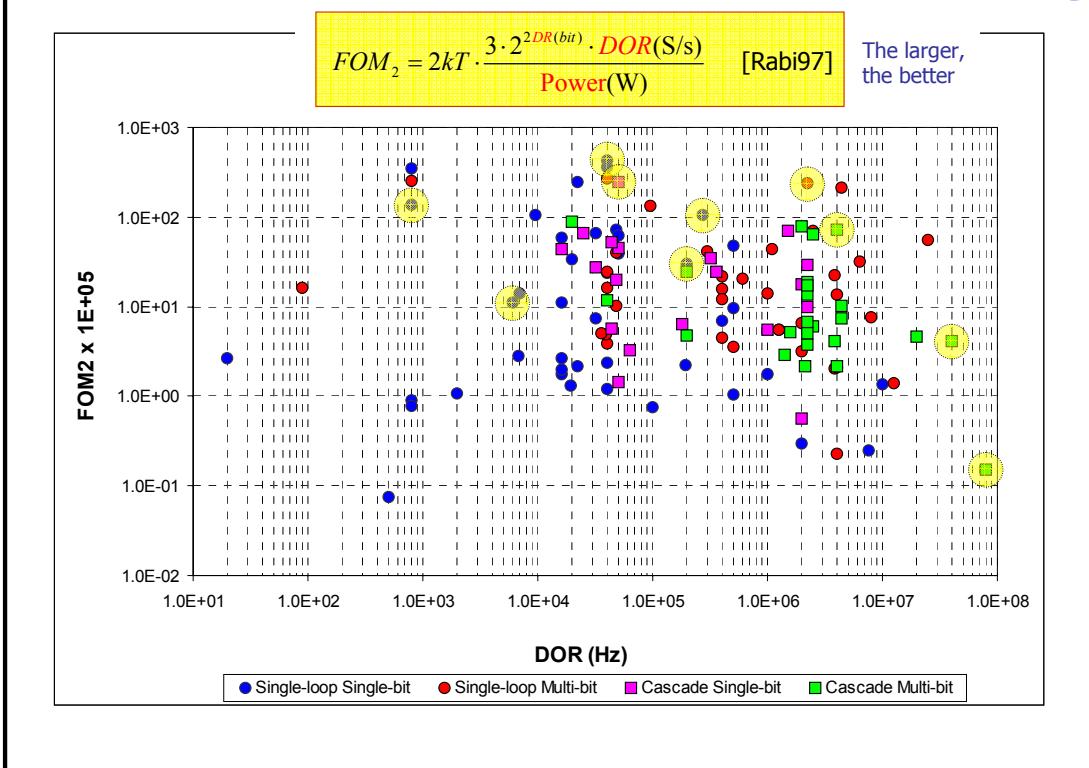
$$FOM_1 = \frac{\text{Power}(W)}{2^{\text{DR}(\text{bit})} \cdot \text{DOR}(\text{s/s})} \times 10^{12} \quad [\text{Good96}]$$

The lower, the better



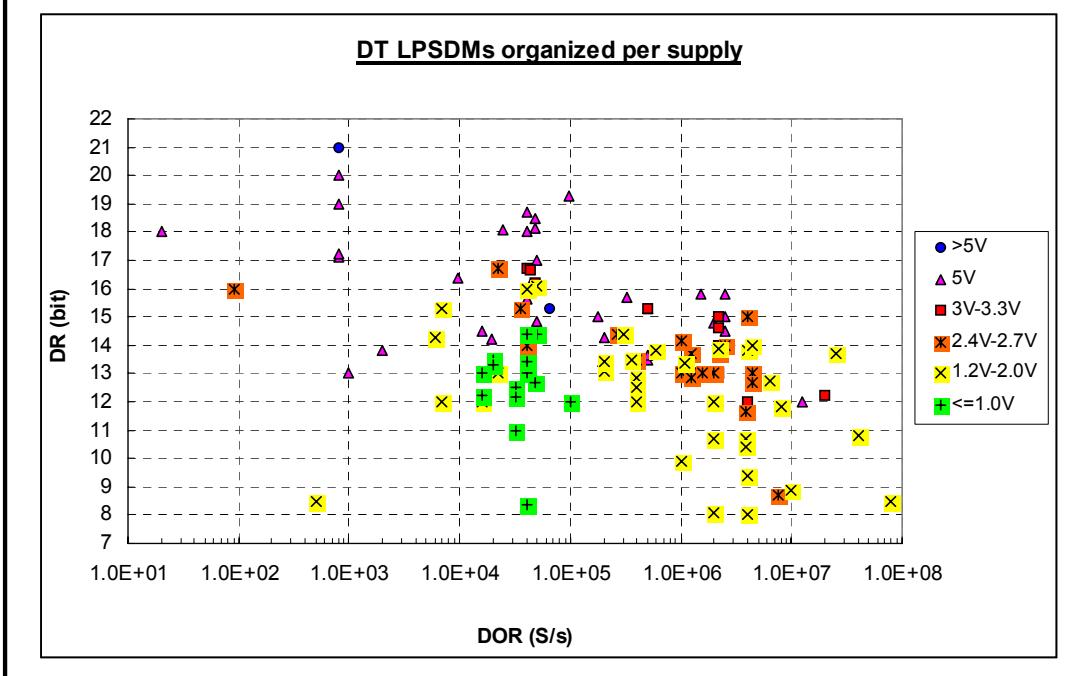
DT-LP- $\Sigma\Delta$ Ms: State of the Art

CNMC



DT-LP- $\Sigma\Delta$ Ms: State of the Art

CNMC

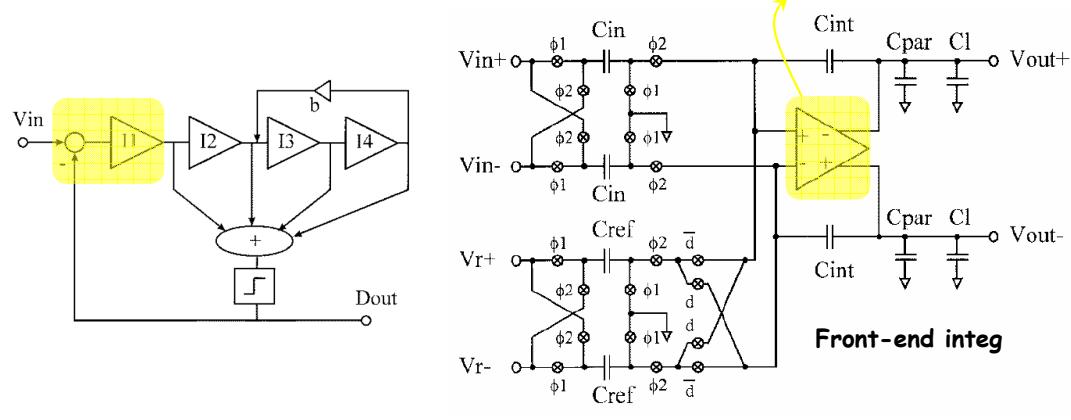
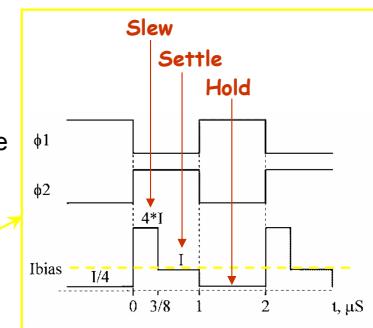


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Precision Apps



Digitization of seismic signals [Kash99]

- Fourth-order feedforward summation architecture
 - Resonation around the two last integrators
 - Chopper at the front-end in order to reduce 1/f noise
- Dynamic biasing of 1st amplifier** for power saving
- 0.6 μ m CMOS tech (2P)
- 122-dB DR within 400Hz bandwidth
- 256kHz sampling rate (OSR=320)
- 16mW, 5V

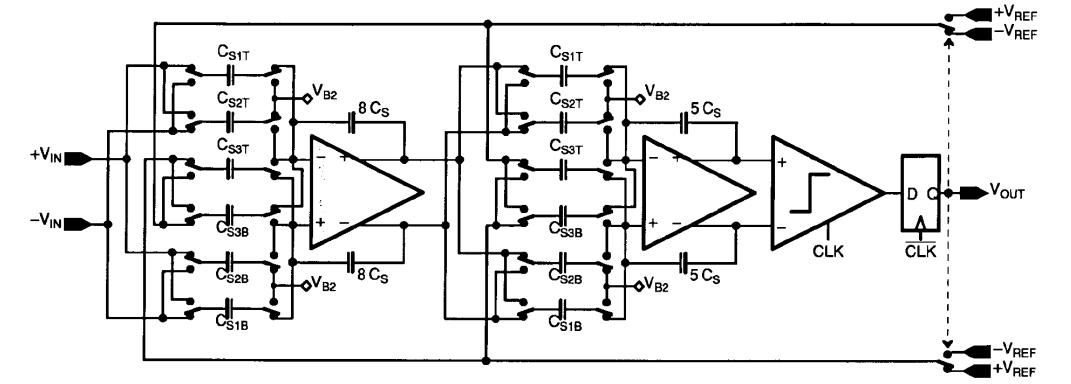
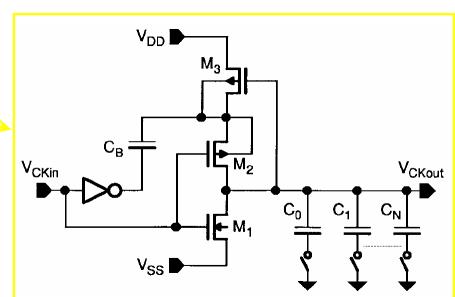


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Voice codecs



Voice-band conversion [Send97]

- Second-order loop
 - Double-sampling \rightarrow 2x effective OSR**
 - Modified NTF
 - Bootstrapped switches
- 0.5 μ m CMOS tech (2P2M)
- 88dB DR within 3kHz bandwidth
- 1MHz clock rate (2MHz effective sampling)
- 0.55mW, 1.5V

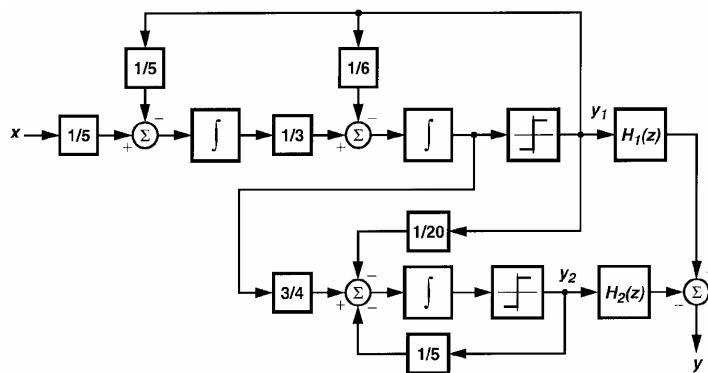
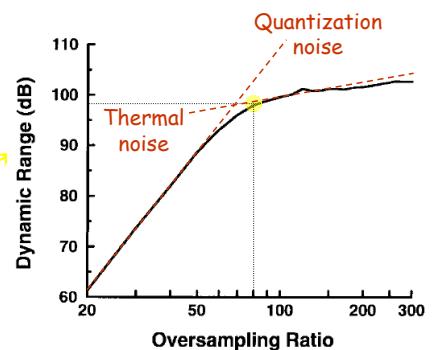


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Audio codecs



□ Audio conversion [Rabi97]

- ◆ 2-1 cascade topology
- ◆ Resolution limited by kT/C noise
- ◆ Rail-to-rail operation
- ◆ Two-stage class A/AB amplifiers
- ◆ Bootstrapping of switches
- ◆ 0.8 μ m CMOS tech (1P3M)
- ◆ 99dB DR within 25kHz bandwidth
- ◆ 4MHz sampling rate (OSR=80)
- ◆ 2.5mW, 1.8V

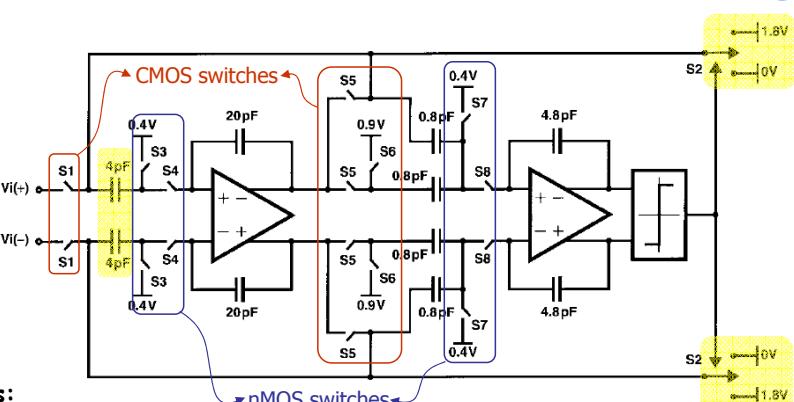


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Audio codecs



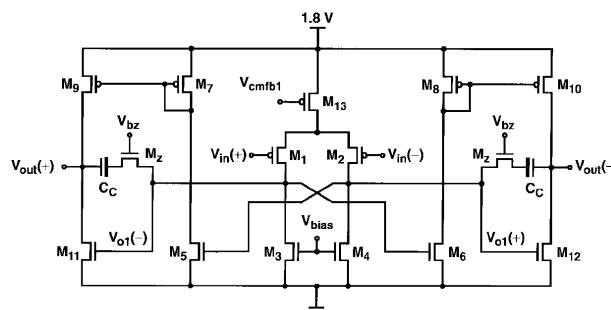
First modulator stage:

- Low input common-mode voltage (400mV)
- CMOS switches only required for sampling large swing signals

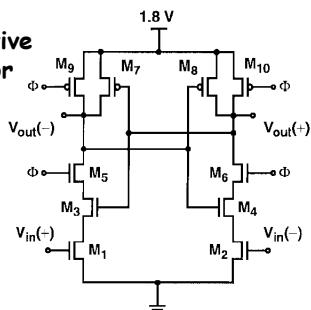


Class A/AB amplifiers:

- 1/f noise relies on pMOS input sizing

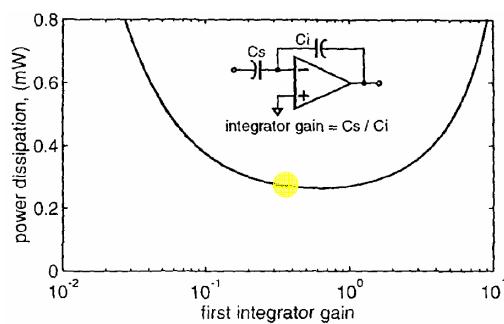
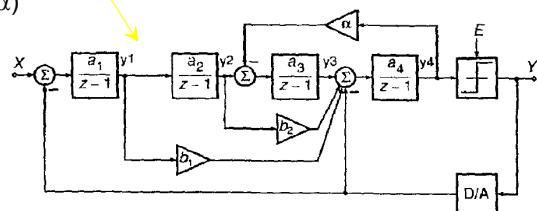


Regenerative comparator



□ Audio conversion [Coba99]

- ◆ Fourth-order single-loop mixed topology
 - Feedforward and feedback paths
 - Resonation around two last integrals (α)
- ◆ Capacitor sizing:
 - Input cap based on kT/C noise
 - Remaining caps based on matching
- ◆ Bootstrapping of switches
- ◆ 0.5 μ m CMOS tech (1P3M)
- ◆ 98.2dB DR within 20kHz bandwidth
- ◆ 2.8MHz sampling rate (OSR=64)
- ◆ 1mW, 1.5V

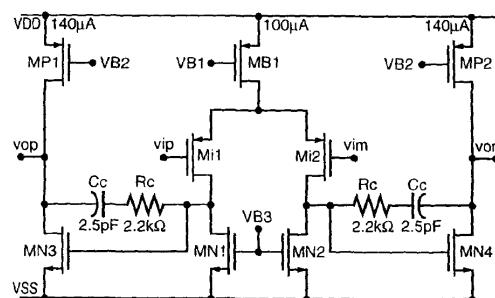


Power dissipation issues:

- 1st-integ gain is fixed to 1/3
- Clock duty-cycle is not 50%:
More time for integration (larger Ceq)
- 1st-integ consumes 72% of power
- Aggressive cap scaling in rest of integs

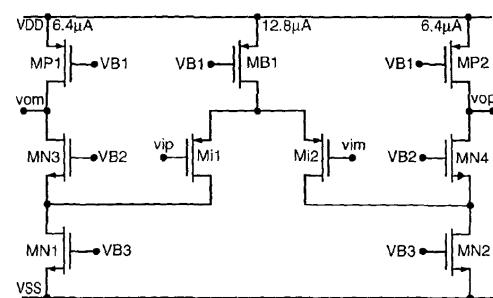
◆ 1st integrator

- Two-stage Miller amplifier
- pMOS input pair with non-minimal lengths to reduce 1/f noise
- Large DC gain



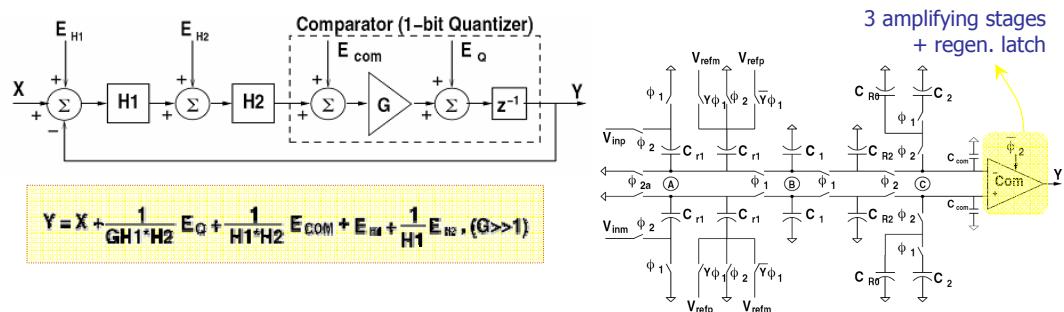
◆ 2nd to 4th integrators

- Folded-cascode amps
- 55-dB DC gain



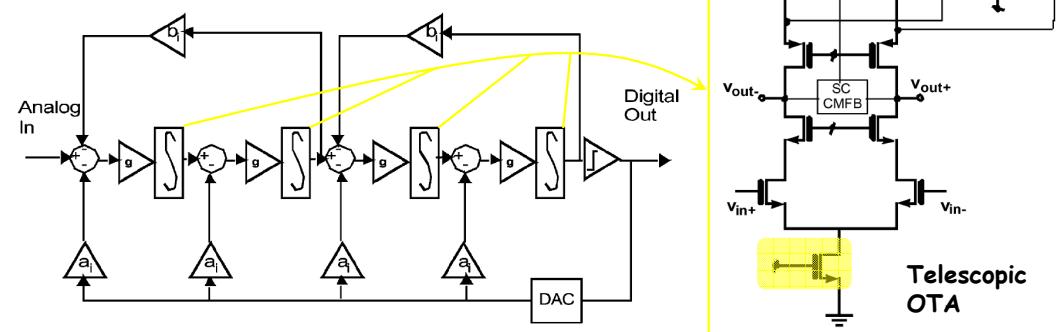
☐ Wireless communications, GSM/BT/WCDMA [Chen03]

- ◆ **Passive 2nd-order modulator → w/o amplifiers**
 - Capacitive voltage dividers reduce the input range
 - Loading effects between passive stages
- ◆ Functionality critically relies in the comparator
 - $H_1 \cdot H_2$ is limited to unity at DC (passive)
 - Eq suppressed within baseband by comparator gain
 - Noise from comparator adds to the input signal
- ◆ 80.5/61.5/50.3dB DR within 0.1/1/2MHz BW
- ◆ 1.3mW, 1.5V, 0.13μm CMOS tech
 - Switching power dominates (104MHz clock)
 - 30% from comparator DC biasing



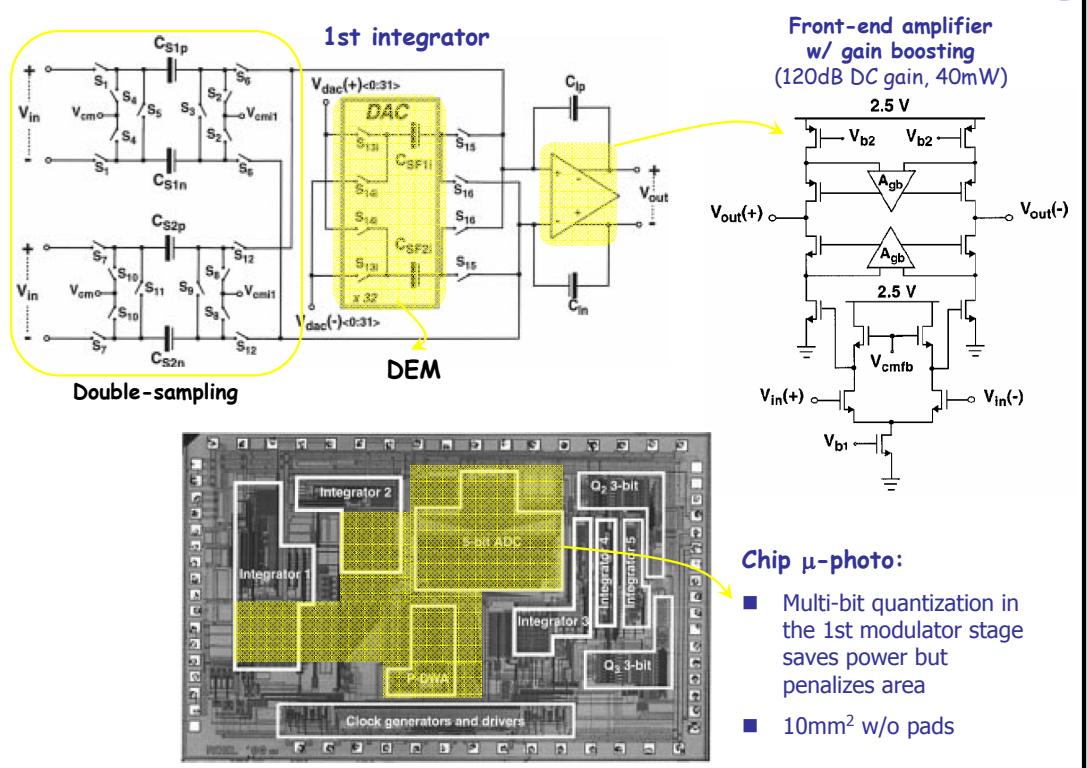
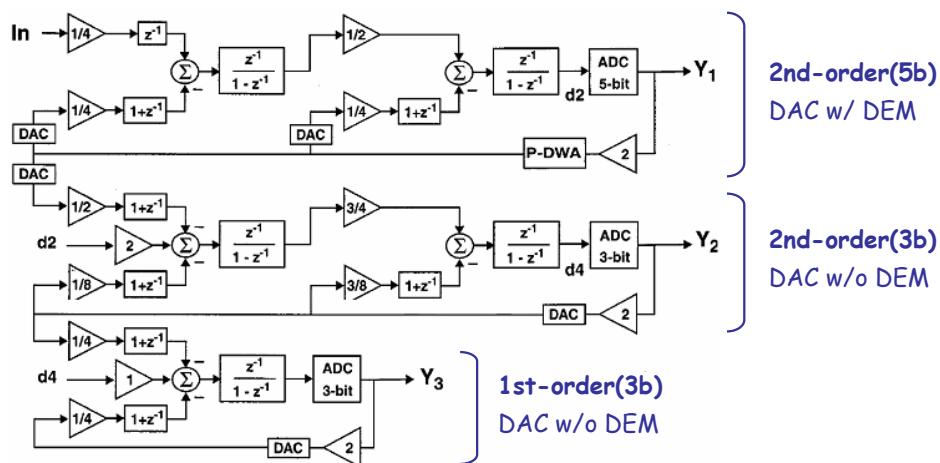
☐ Wireless communications, GSM/GPRS/EDGE [Klem06]

- ◆ Fourth-order distributed feedback topology
 - Inverse Chebyshev approximation
 - NTF w/ two optimized zeros (b_1)
- ◆ Single-stage amplifiers:
 - Telescopic OTAs w/ dynamic biasing
 - Constant slew-rate for power saving under process variations
- ◆ Capacitor scaling → 8:2:1:1 (20pF integrating cap at input)
- ◆ 0.25μm CMOS tech
- ◆ 88dB DR within 270kHz bandwidth
- ◆ 26MHz sampling rate (OSR=48)
- ◆ 2.8mW, 2.7V



Broadband communications, ADSL [Vleu01]

- ◆ 2-2-1 cascade topology w/ multi-bit quantization
 - Limited by K/T/C noise → Multi-bit quantization in all stages to reduce noise leakage
 - Linearization of 1st-stage DAC → partitioned DWA (DEM)
 - Double-sampling [Send97] → OSR=2x8
- ◆ 150mW, 2.5V, 0.5μm CMOS tech (2P3M)
- ◆ 32MHz clock rate (64MHz effective sampling)
- ◆ 95dB DR within 2MHz bandwidth

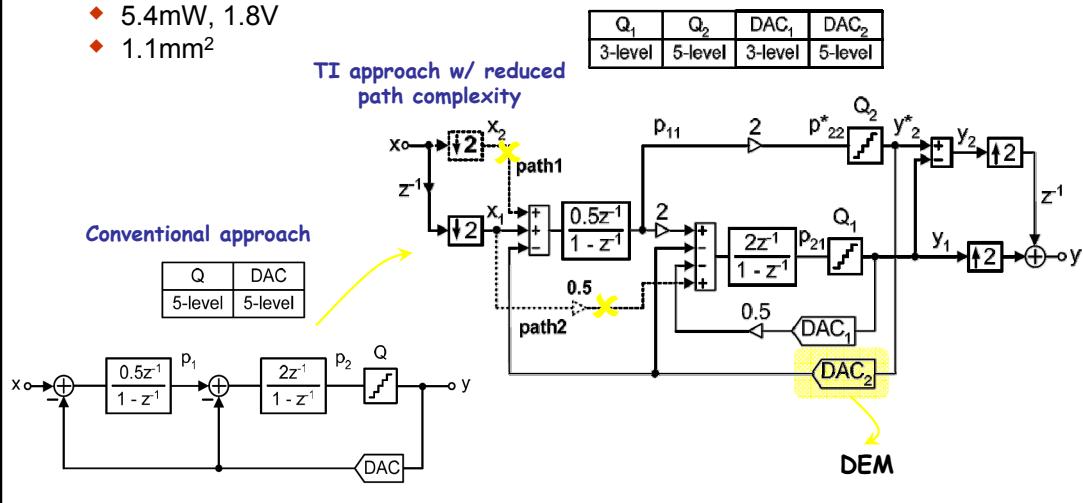


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Broadband com



Broadband communications, ADSL [Lee06]

- 2nd-order topology w/ multi-bit quantization
- 2 channels w/ time interleaving**, but only 2 opamps \rightarrow Reduced complexity
- Linearization of 5-level feedback to 1st integ \rightarrow ILA (DEM)
- 0.18 μ m CMOS tech (MiM caps)
- 66MHz clock rate (132MHz effective sampling, OSR=60)
- 85dB DR within 1.1MHz bandwidth
- 5.4mW, 1.8V
- 1.1mm²

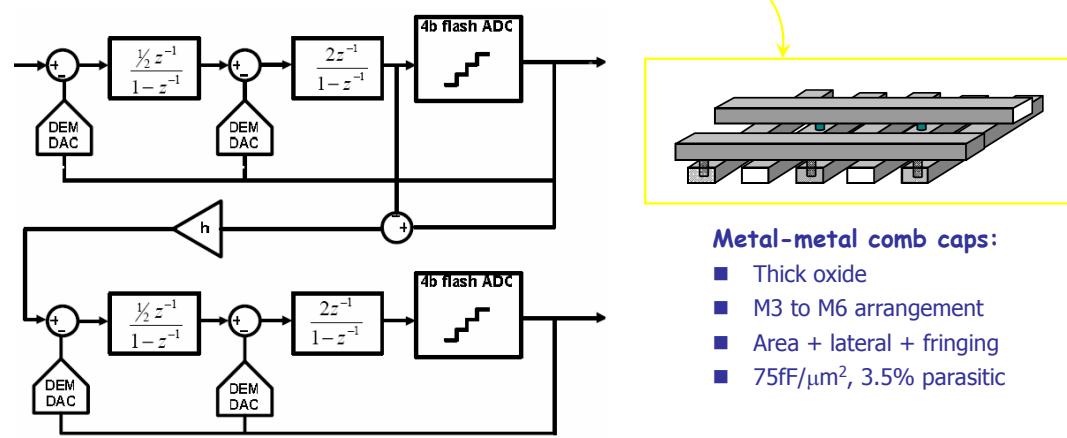


DT-LP- $\Sigma\Delta$ Ms: State of the Art / Wireless com



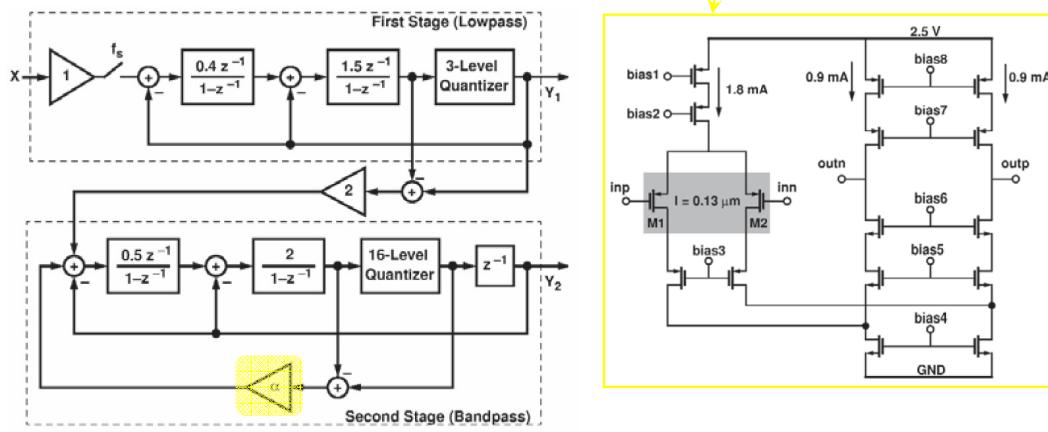
Wireless communications, WLAN [Para06]

- 2-2 cascade topology with 4-bit internal quantizers
 - Linearization of all multi-bit DACs \rightarrow rotational DWA (DEM)
- Two-stage amplifiers \rightarrow pMOS telescopic + nMOS common-source stage
- 90nm CMOS tech (1P7M) \rightarrow metal-metal caps
- 330MHz sampling rate \rightarrow OSR=8
- 67dB DR within **20MHz bandwidth**
- 78mW, 1.4V



Wireless communications, WLAN [Taba03]

- ◆ Fourth-order multi-bit cascade topology
 - 1st stage: 2nd-order LP (1.5b)
 - 2nd stage: 2nd-order BP (4b) → local resonance (α) and DAC w/o DEM
- ◆ 0.13 μ m 1.2V CMOS tech (1P6M) → 0.25 μ m 2.5V I/O MOST, MiM caps
- ◆ Folded-cascode amplifiers with 0.13 μ m input pMOS for fast settling
- ◆ 160MHz sampling rate → OSR=4!
- ◆ 53dB DR within 40MHz bandwidth
- ◆ 175mW power consumption



Band-Pass $\Sigma\Delta$ M ICs

Based on $z^1 \rightarrow -z^2$ transformation

Author	DR (bit)	fs (Hz)	fn (Hz)	Bw (Hz)	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁶
[Cor97]	9.5	1.25E+06	2.50E+05	6.25E+03	4th-ord	2um MS / 5V	---	---	---
[Long93]	15	7.20E+06	1.80E+06	3.00E+04	4th-ord	1um MS / 5V	---	---	---
[Rosa00]	11.5	6.52E+06	1.63E+06	1.00E+04	4th-ord	0.8um STD / 5V	6.00E-02	12.67	5.71
[Baza98]	6.7	4.00E+07	2.00E+07	1.25E+06	2nd-ord	0.5um MS / 5V	6.50E-02	30.31	0.09
[Park99]	12.2	2.00E+07	5.00E+06	2.00E+05	4th-ord	0.65um STD / 4V	1.80E-01	7.50	15.66
[Song95]	9	8.00E+06	2.00E+06	3.00E+04	4th-ord	2um MS / 3.3V	8.00E-04	0.78	16.48
[Andr96]	8	8.00E+06	2.00E+06	6.40E+04	6th-ord	0.5um MS (2P) / 3.3V	8.00E-03	15.38	0.42
[Haire96]	11.7	1.30E+07	3.25E+06	2.00E+05	4-2	0.8um MS (2P) / 3V	1.44E-02	1.29	64.27
[Baza99]	9.4	6.80E+07	1.70E+07	1.25E+06	4-4	0.6um MS (2P) / 3V	4.80E-02	4.03	4.18
[Sal02]	11.7	8.00E+07	2.00E+07	2.70E+05	4th-ord	0.35um / 3V	5.60E-02	0.84	99.34
[Sal02]	6.7	8.00E+07	2.00E+07	3.84E+06	4th-ord	0.35um / 3V	5.60E-02	24.57	0.11
[Sal03]	13.3	8.00E+07	2.00E+07	1.25E+06	4-4	0.35um / 3V	3.70E-02	0.18	1415.26
[Sal03]	11.7	8.00E+07	2.00E+07	1.76E+06	4-4	0.35um / 3V	3.70E-02	0.53	155.92
[Taba99]	13	8.00E+07	2.00E+07	1.25E+06	6th-ord	0.25um MS / 2.5V	9.00E-02	0.53	383.86
[Ueno02]	12.6	1.00E+07	5.66E+05	2.50E+05	2-2(3b)	0.25um MS (2P) / 2.5V	7.70E-02	17.95	8.63
[Cheu01]	6.7	4.28E+07	1.07E+07	2.00E+05	2nd-ord	0.35um STD / 1V	1.20E-02	10.69	0.24
[Cheu02]	6.8	4.28E+07	1.07E+07	2.00E+05	2nd-ord	0.35um MS (2P) / 1V	1.20E-02	9.97	0.28
[Kuo04]	10	7.13E+00	1.07E+07	2.00E+05	4th-ord	0.25um MS / 1V	8.45E-03	0.76	33.45
[Kuo04]	12.04	7.13E+00	1.07E+07	1.00E+05	4th-ord	0.25um MS / 1V	1.00E-01	1.13	563.12
[Kuo04]	12.7	7.13E+00	1.07E+07	6.00E+04	4th-ord	0.25um MS / 1V	1.00E-01	1.13	403.30
[Kuo04]	13.37	7.13E+00	1.07E+07	6.00E+04	4th-ord	0.25um MS / 1V	1.00E-01	1.13	3552.46

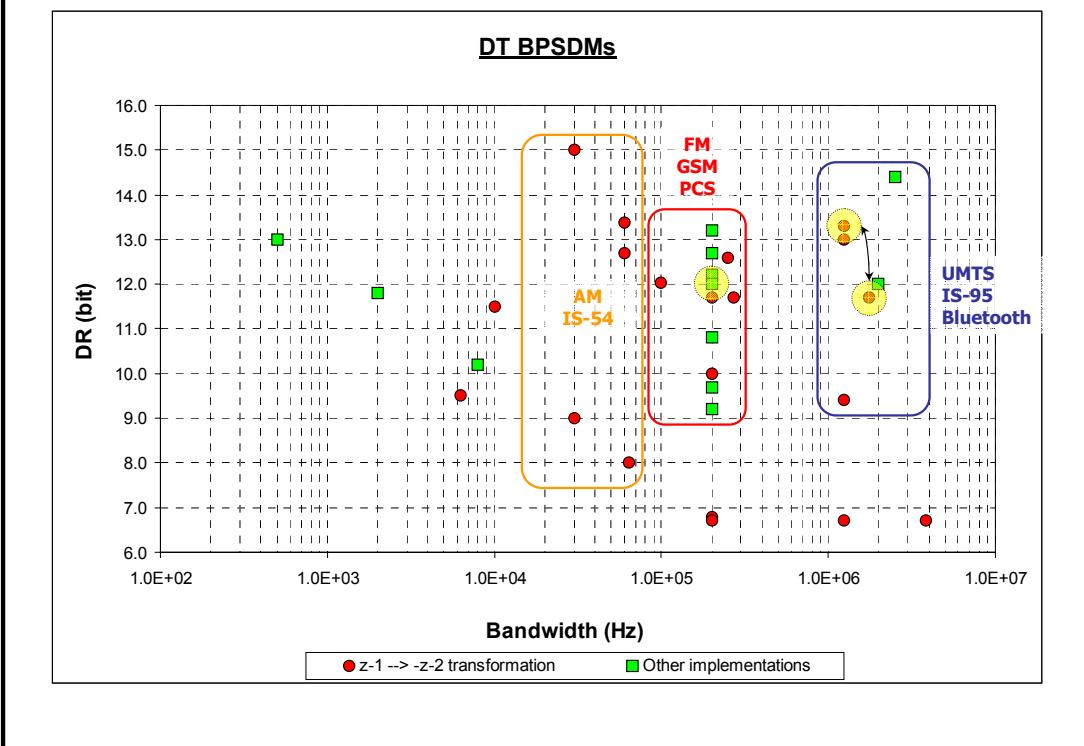
Synthesis method: $z^1 \rightarrow -z^2$ (~50%)

Other BPDSM ICs

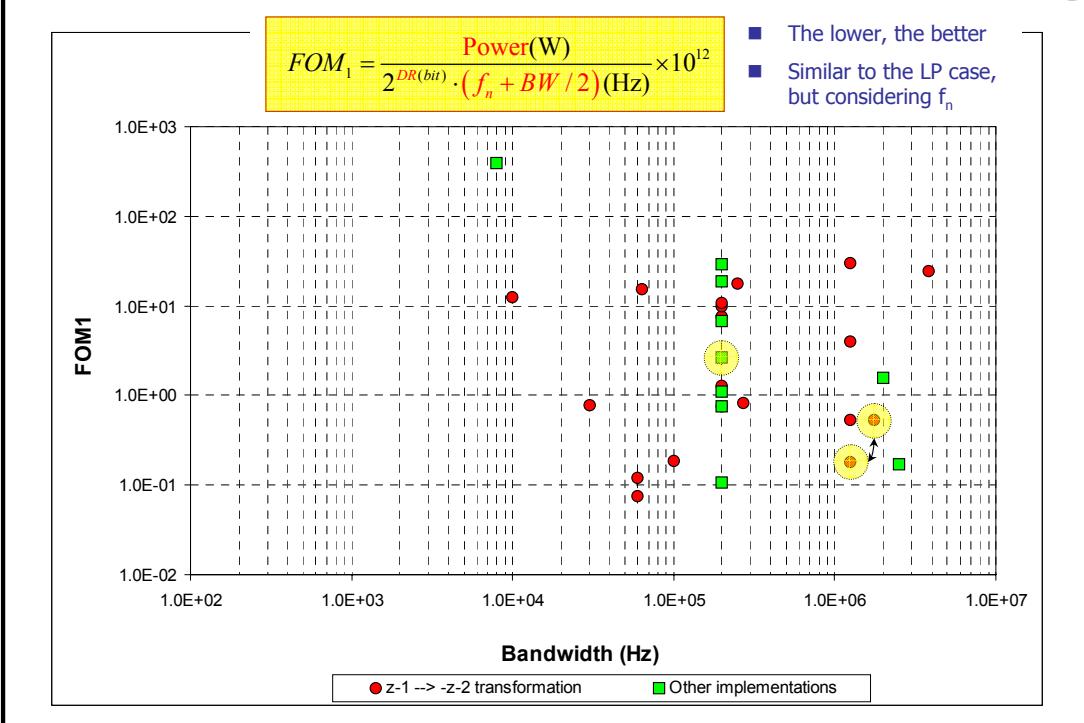
Author	DR (bit)	fs (Hz)	fn (Hz)	Bw	Architecture	Process	Power (W)	FOM1	FOM2x10 ⁶
[Chua98]	13	5.00E+05	1.25E+05	5.00E+04	4th Opt NTF	3um MS (2P) / 3V	2.70E-01	0.08	---
[Jan93]	10.2	1.83E+06	4.55E+05	8.00E+04	4th Opt NTF	3um MS (2P) / 3V	1.30E-01	18.94	2.35
[Jan97]	10.8	1.00E+07	3.75E+06	2.00E+05	4th Quadrature	0.8um STD / 5V	1.30E-01	18.94	2.35
[Liu97]	11.8	8.27E+05	4.13E+05	2.00E+03	4th Opt NTF	2um MS (2P) / 5V	---	---	---
[Cusi01]	12	3.71E+07	1.07E+07	2.00E+05	6th Opt NTF	0.35um STD / 3.3V	1.16E-01	2.62	38.99
[Ong97]	12.2	8.00E+07	2.00E+07	2.00E+05	4th-ord	0.6um STD / 3.3V	7.20E-02	0.76	154.26
[Toni99]	12.7	4.28E+07	1.07E+07	2.00E+05	6th Opt NTF	0.35um STD / 3.3V	8.00E-02	1.11	149.19
[Chen05]	9.7	1.28E+07	3.25E+06	2.00E+05	3rd Quadrature	0.35um STD / 3.3V	1.87E-02	6.71	3.09
[Andr98]	9.2	4.00E+06	1.00E+06	2.00E+05	3rd(3b) Opt NTF	0.5um MS (2P) / 3V	1.90E-02	29.37	0.50
[Taba00]	12	6.40E+07	1.60E+07	2.00E+06	6th 2-path	0.25um STD / 2.5V	1.10E-01	1.58	64.72
[Mauro05]	13.2	1.31E+07	1.00E+07	2.00E+05	2-0 Quadrature	0.25um STD / 2.1V	1.00E-02	0.11	2232.33
[Ying04]	14.4	6.00E+07	4.00E+07	2.50E+06	4th Quadrature	0.18um STD / 1.8V	1.50E-01	0.17	3208.05

Passband location: $f_n = f_s/4$ (~80%)

DT-BP- $\Sigma\Delta$ MJs: State of the Art



DT-BP- $\Sigma\Delta$ MJs: State of the Art

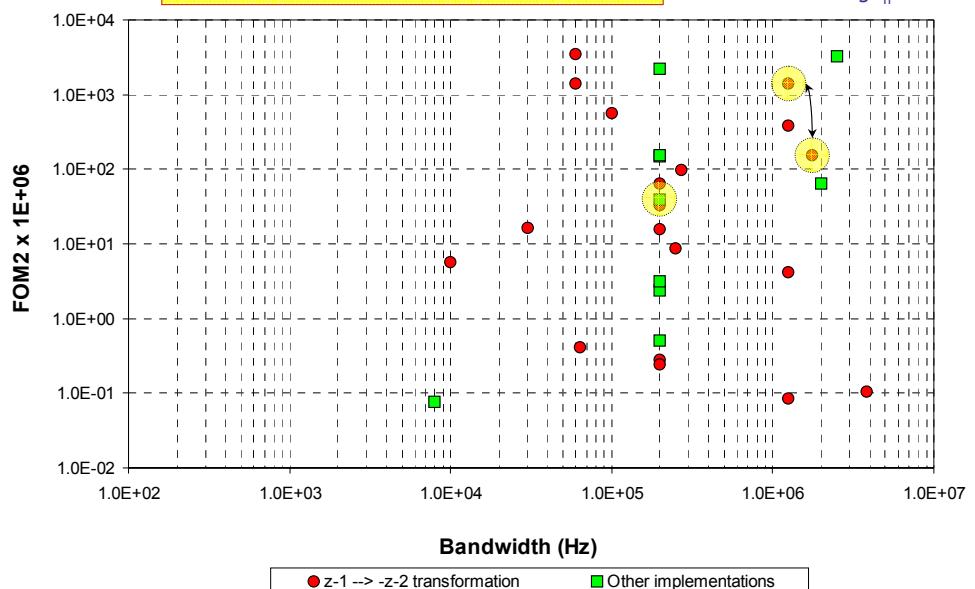


DT-BP- $\Sigma\Delta$ Ms: State of the Art



$$FOM_2 = 2kT \cdot \frac{3 \cdot 2^{2DR(\text{bit})} \cdot (f_n + BW/2) \text{ (Hz)}}{\text{Power (W)}}$$

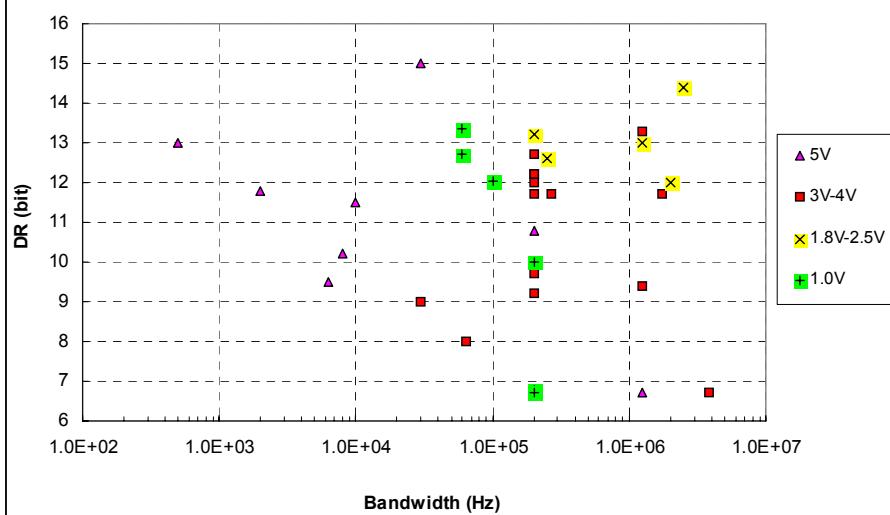
- The larger, the better
- Similar to the LP case, but considering f_n



DT-BP- $\Sigma\Delta$ Ms: State of the Art



DT BPSDMs organized per supply

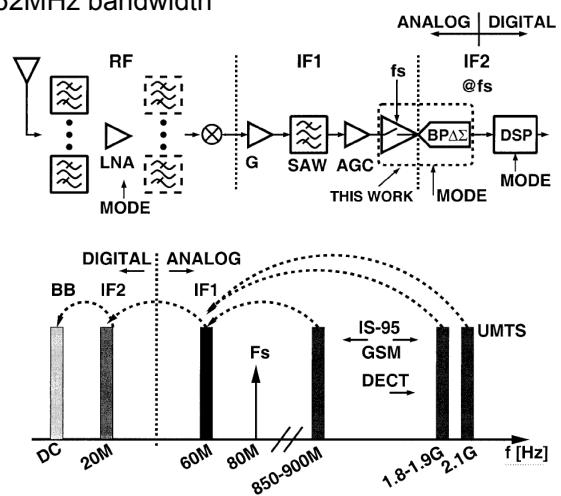
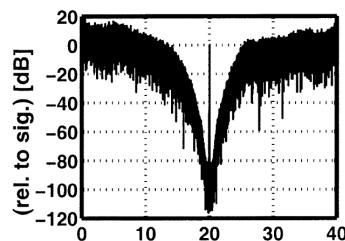


DT-BP- $\Sigma\Delta$ Ms: State of the Art / Wireless com

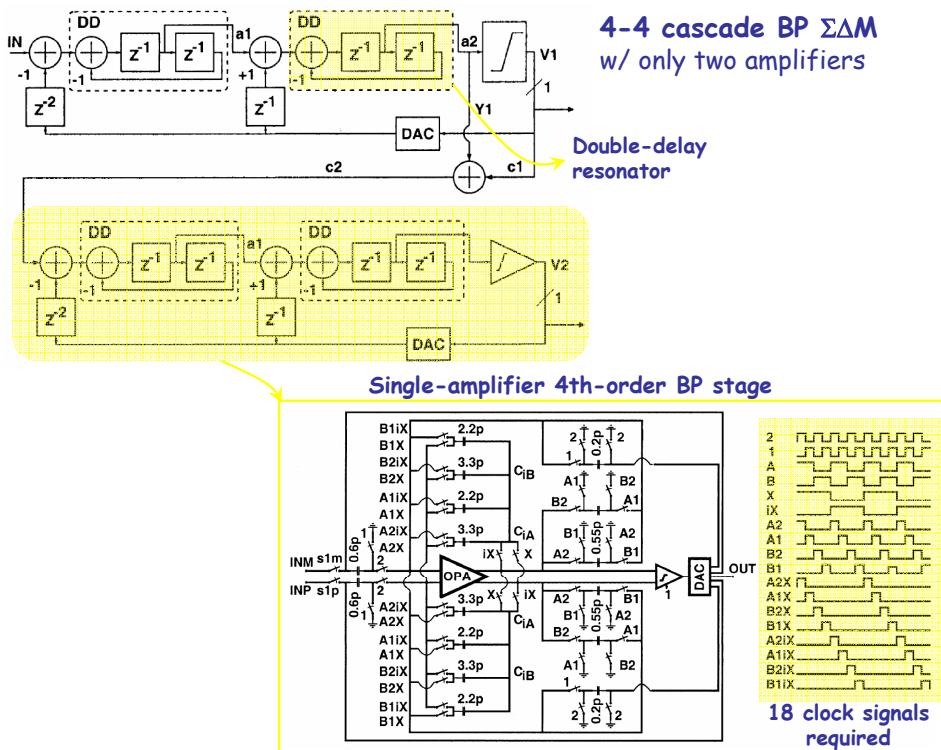


Digital IF receivers, IS-95/DECT [Salo03]

- ◆ Eighth-order bandpass cascade topology
 - 4-4 cascade BP $\Sigma\Delta$ M \rightarrow Equivalent to 2-2 LP $\Sigma\Delta$ M
 - $z^{-1} \rightarrow -z^{-2}$ transformation $\rightarrow f_n = f_s/4 = 80\text{MHz}/4 = 20\text{MHz}$
 - Double-delay (DD) resonators using only one amplifier
 - Based on single-amplifier 4th-order BP $\Sigma\Delta$ M
- ◆ Only two amplifiers required \rightarrow Folded-cascode topology
- ◆ 82/72dB DR within 1.25/1.762MHz bandwidth
- ◆ 0.35 μm CMOS tech
- ◆ 37mW, 3.0V



DT-BP- $\Sigma\Delta$ Ms: State of the Art / Wireless com

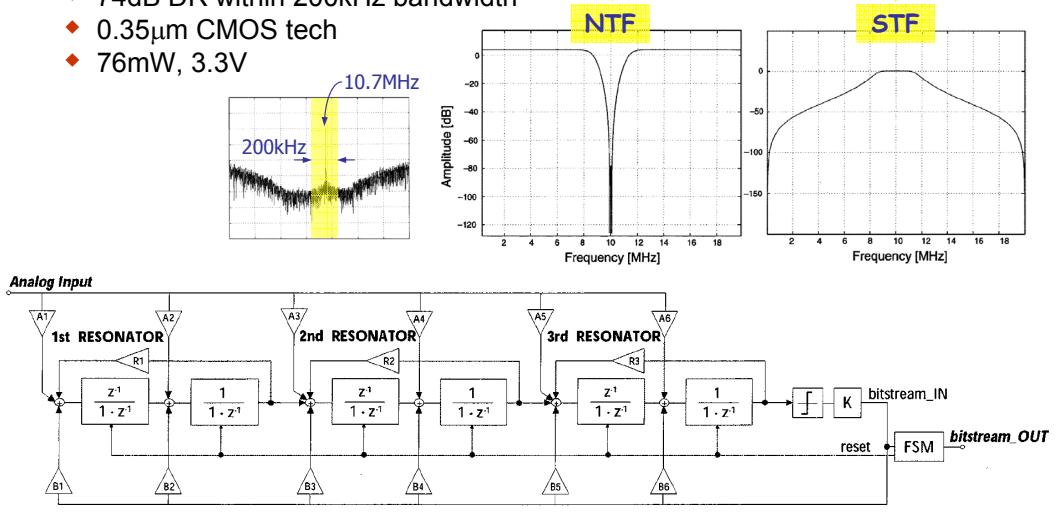


DT-BP- $\Sigma\Delta$ M: State of the Art / Wireless com



Digital IF receivers, FM [Cusi01]

- ◆ Sixth-order single-loop bandpass $\Sigma\Delta$ M
 - Distributed feedback and distributed feedforward topology
 - Optimized NTF and STF \rightarrow NTF w/ spread zeros, STF w/ interferer filtering
 - $f_n = f_s/4 = 42.8\text{MHz}/4 = 10.7\text{MHz}$
- ◆ Limited by kT/C and amplifier noise
- ◆ 74dB DR within 200kHz bandwidth
- ◆ 0.35 μm CMOS tech
- ◆ 76mW, 3.3V



CT- $\Sigma\Delta$ M: State of the Art



Low-Pass Single-bit

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)
[Badj02]	10,00	2,20E+04	64	4th-ord	0.5um CMOS 1.8V	1,70E-03
[Bree00]	13,3	2,00E+05	65	4th-ord	0.35um CMOS 2.5V	1,80E-03
[Gerf02]	11,3	5,00E+04	48	3rd-ord	0.5um CMOS 1.5V	2,50E-04
[Gerf03]	11,8	5,00E+04	48	3rd-ord	0.5um CMOS 1.5V	1,35E-04
[Lin99]	10,5	5,00E+06	16	2nd-ord	1.2um CMOS 3V	1,20E-02
[Luh00]	10	6,20E+06	64	5th-ord	0.6um CMOS 3.3V	1,60E-02
[Luh98a]	8	2,00E+06	25	2nd-ord	2um CMOS 5V	1,50E-02
[Luh98b]	9,6	2,00E+06	25	2nd-ord	2um CMOS 5V	1,66E-02
[Putt04]	12,5	2,00E+06	140	2nd-ord	0.18um CMOS / 1.8V	6,00E-03
[Veld02]	11,3	4,00E+06	38,4	4th-ord	0.18um CMOS 1.8V	6,60E-03
[Zwan96]	13	8,00E+03	64	4th-ord	0.5um CMOS 2.2V	2,00E-04
[Zwan99]	10,4	1,00E+06	10	2nd-ord	0.5um CMOS 5V	7,20E-03
[Ortm03]	10	5,00E+04	48	3rd-ord	0.5um CMOS 1.5V	7,50E-04
[Sami03]	9,4	1,00E+05	32	3rd-ord	0.5um CMOS 1.5V	7,50E-05
[Phil03]	12,3	1,00E+06	64	5th-ord	0.18um CMOS	4,40E-03
[Phil04]	14,5	2,00E+06	32	4th-ord	0.18um ST 1.8V	2,00E-03
[Blan02]	11,30	1,60E+04	62,5	4th-ord	0.35um STD/2.5V	7,50E-05
[Dagh04]	12,40	2,46E+06	813	2nd-ord	0.18um CMOS / 1.8V	1,80E-02
[Das05]	14,00	1,20E+06	213	4th-ord	90nm CMOS / 1.3V	5,40E-03
[Muñ05]	14,60	2,00E+06	32	4th-ord	0.18um CMOS / 1.8V	4,70E-03
[Naga05]	11,37	8,56E+05	150	4th-ord	0.11um CMOS / 1.2V	3,42E-03
[Naga05]	10,37	2,60E+06	50	4th-ord	0.11um CMOS / 1.2V	3,42E-03
[Pun07]	12,00	5,00E+04	64	3rd-ord	0.18um CMOS / 0.5V	3,70E-04

CT- $\Sigma\Delta$ Ms: State of the Art



■ Low-Pass Multi-bit

Author	DR (bit)	DOR (S/s)	OSR	Architecture	Process	Power (W)
[Dorr03]	10	4,00E+06	26	3rd-ord (3b) - DEM	0.13um CMOS 1.2V	3,00E-03
[Gian03]	11	3,00E+07	10	4th-ord (4b)	0.13um CMOS 1.5V	7,50E-02
[Pato04]	11	3,00E+07	10	4th-ord (4b) - DEM	0.13um CMOS 1.5V	7,00E-02
[Yan03]	14	2,00E+06	16	3rd-ord (5b)	0.5um CMOS MS /	6,20E-02
[Yan04]	14,4	2,00E+06	16	3rd-ord (5b) - Calib.	0.5um CMOS MS /	6,20E-02
[Moya03]	13	2,40E+07	10	3rd-ord (6b) - Calib.	0.5um CMOS MS/2.5V	7,50E-02
[Schi04]	14	2,40E+05	54	4th-ord (3b) - ??	0.13um CMOS /1.25V	3,00E-03
[Dorr05]	12	4,00E+06	26	3rd-ord (4b) - Tracking quant	0.13um CMOS /1.5V	3,00E-03
[Font05]	12,5	1,20E+06	42	3rd-ord (2b)	90nm CMOS / 1.5V	6,00E-03
[Morr05]	16,7	4,00E+04	128	2nd-ord(4b) - DEM	0.18um CMOS /3.3V	3,73E-02
[Nguy05]	15,9	9,60E+04	128	4th-ord (4b) - DEM	0.35um (2P) /3.3V	1,80E-02
[Cald05]	8,9	4,00E+07	5	3rd-ord (4b) - time-interleav	0.18um CMOS /1.8V	1,03E-01
[Aria06]	8,70	4,00E+07	16	2nd-order (3b) - Complex	0.25um CMOS /2.5V	3,20E-02
[Mitt06]	13	4,00E+07	16	3rd-order (4b)	0.13um CMOS / 1.2V	2,00E-02
Bree04	10,87	2,00E+07	8	2-2 (4b)	0.18um ST/1.8V	1,22E-01
Bree04	10,87	4,00E+07	8	2-2 (4b) I/Q	0.18um ST/1.8V	2,16E-01

■ Band-Pass

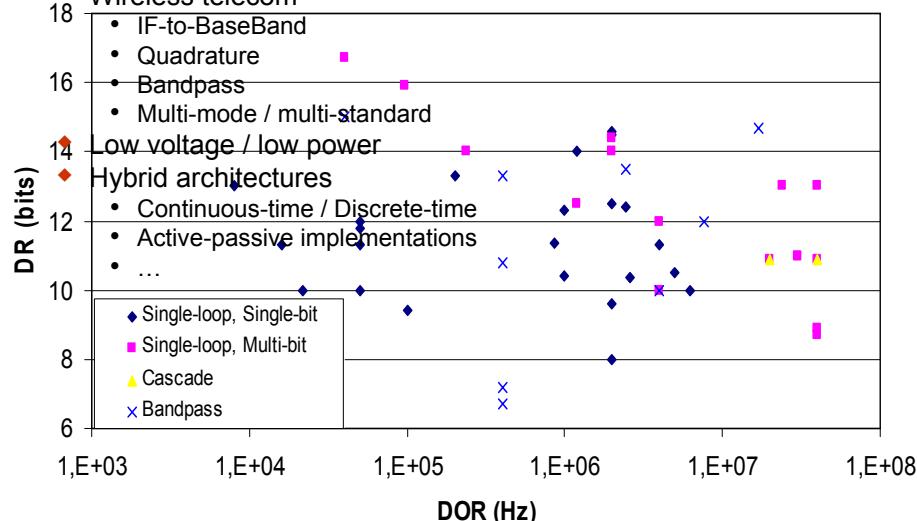
Author	DR (bit)	fs (Hz)	fn (Hz)	Bw (Hz)	DOR(Hz)	Architecture	Process	Power (W)
[Copp02]	10	1,28E+08	4,00E+06	2,00E+06	4,00E+06	2nd-ord (Complex)	0.25um CMOS 2V	1,42E-02
[Enge99]	10,8	4,00E+07	1,07E+07	2,00E+05	4,00E+05	6th-ord	0.5um CMOS 5V	6,00E-02
[Hsu00]	6,7	2,80E+08	7,00E+07	2,00E+05	4,00E+05	2nd-ord	0.5um CMOS 2.5V	3,90E-02
[Tao99]	7,2	4,00E+08	1,00E+08	2,00E+05	4,00E+05	4th-ord	0.35um CMOS 3.3V	1,65E-01
[Zwan00]	13,3	2,11E+07	1,07E+07	2,00E+05	4,00E+05	5th-ord	0.25um CMOS 2.5V	1,10E-02
[Veld03b]	15	2,60E+07	1,00E+05	2,00E+04	4,00E+04	5th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	9,10E-03
[Veld03b]	13,5	7,88E+07		1,23E+06	2,46E+06	5th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	1,31E-02
[Veld03b]	12	1,54E+08		3,84E+06	7,68E+06	5th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	1,41E-02
[Schr06]	14,7	2,64E+08	4,40E+07	8,50E+06	1,70E+07	4th-ord (Quadrat)	0.18um CMOS ST/ 2.9V	3,75E-01

CT- $\Sigma\Delta$ Ms: State of the Art



□ A Large number of different topologies and applications

- ◆ Broadband (15-20MHz) telecom
- ◆ Wireless telecom

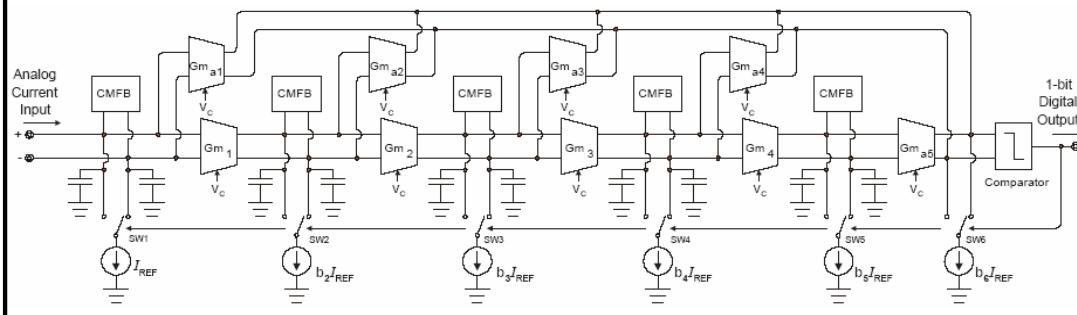
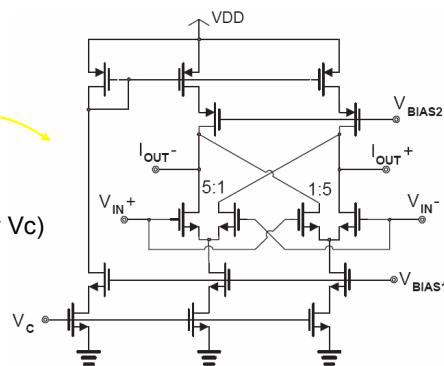


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



□ Gm-C 5th-order single-loop [Luh00]

- ◆ Fifth-order feedforward loop filter
 - Butterworth approximation
 - Gm-C implementation
 - Cross-coupled asymmetric differential pairs
 - Tunable transconductance gain (controlled by V_c)
- ◆ 0.6 μ m CMOS technology
- ◆ 62-dB DR within 3.1MHz bandwidth
- ◆ 400MHz sampling rate
- ◆ 16mW, 3.3V

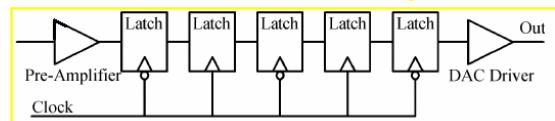
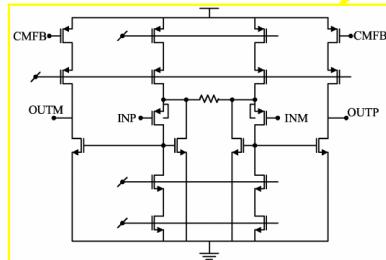
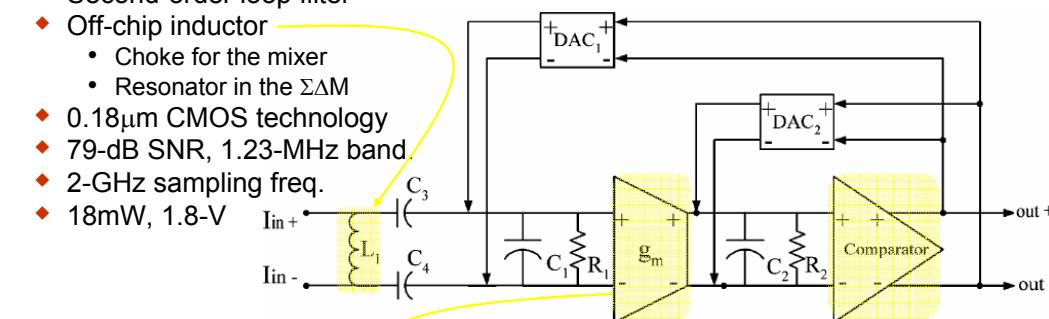


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



□ Gm-C 2nd-order single-loop for CDMA [Dagh04]

- ◆ Second-order loop filter
- ◆ Off-chip inductor
 - Choke for the mixer
 - Resonator in the $\Sigma\Delta$ M
- ◆ 0.18 μ m CMOS technology
- ◆ 79-dB SNR, 1.23-MHz band
- ◆ 2-GHz sampling freq.
- ◆ 18mW, 1.8-V



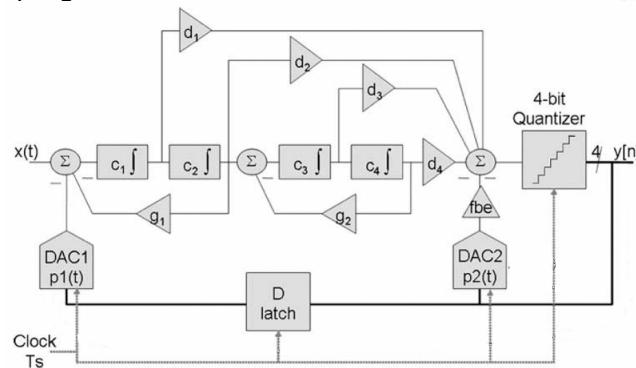
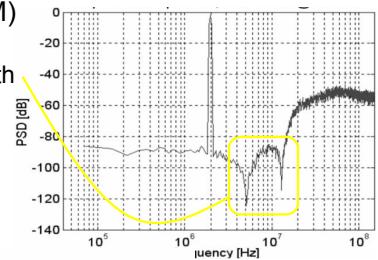
■ Additional latches to reduce metastability

CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



RC-active 4th-order (4-b) single-loop (I) [Pato04]

- 4th-order loop filter, 4-bit internal quantizer (+DEM)
- Direct synthesis method to optimize NTF
 - NTF-zero optimized to achieve the largest bandwidth
 - Robustness (stability) against process variations
- DAC2 used to compensate the excess loop delay
- 0.13 μ m CMOS technology
- 67-dB DR within 15-MHz bandwidth
- 300-MHz sampling rate
- 70mW, 1.5V

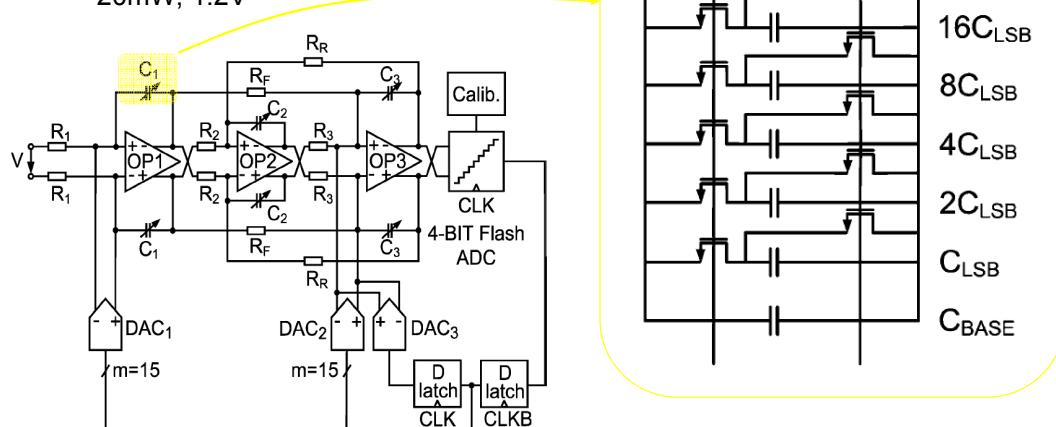


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



RC-active 3rd-order (4-b) single-loop [Mitt06]

- 3rd-order 4-bit
- Active-RC integrators
- Trimming of time-constants
- 0.13- μ m CMOS
- 12-bit ENOB within 20-MHz band
- 640-MHz sampling rate
- 20mW, 1.2V

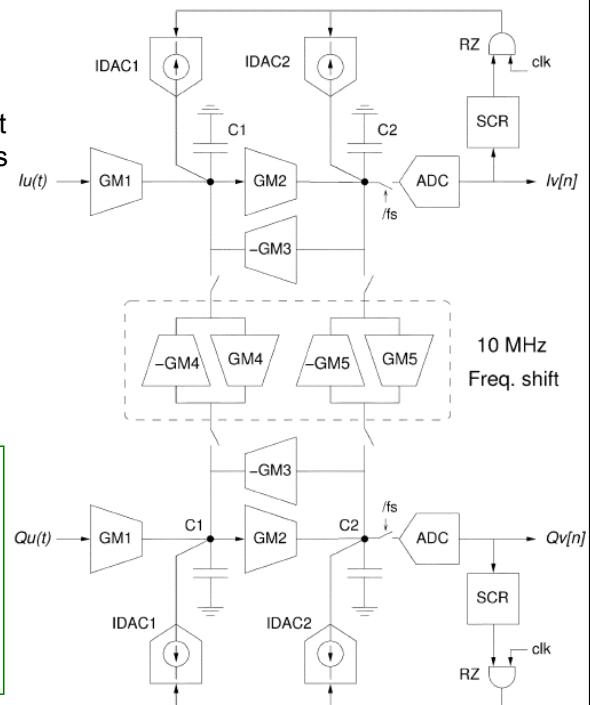
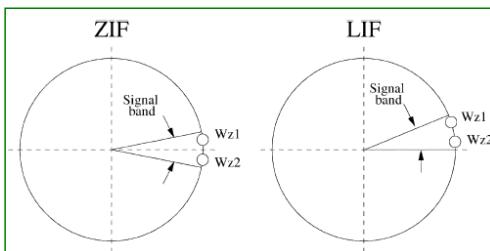


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



Complex architecture for WLAN (IEEE 802.11 a/b/g) [Aria06]

- First Complex (2x2nd-order) 3-bit
- NTF poles for ZIF and LIF modes
- Gm-C integrators
- 0.25 μ m CMOS standard technology (MOS caps)
- 8.7-bit ENOB within 20-MHz bandwidth
- 320-MHz sampling rate
- 32mW, 2.5V



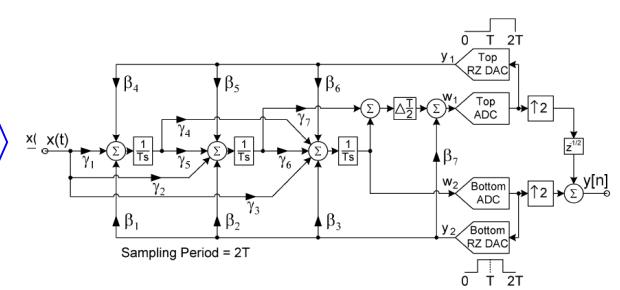
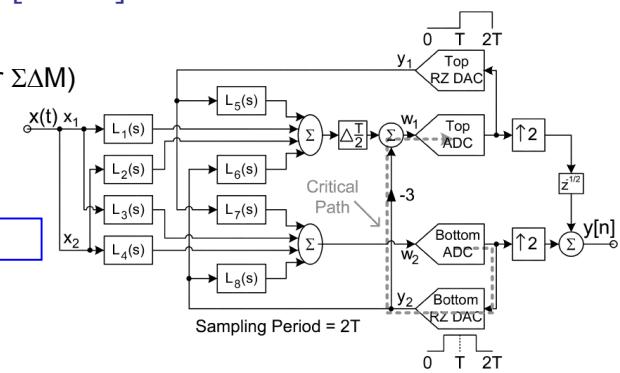
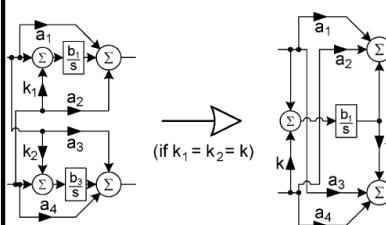
CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



Time-Interleaved architecture [Cald06]

- Time-interleaved (2x3rd-order $\Sigma\Delta$)
- 0.18- μ m CMOS
- 8.7-bit ENOB within 20-MHz
- 200-MHz sampling rate
- 103mW, 1.8V

Equivalence for integrator reduction

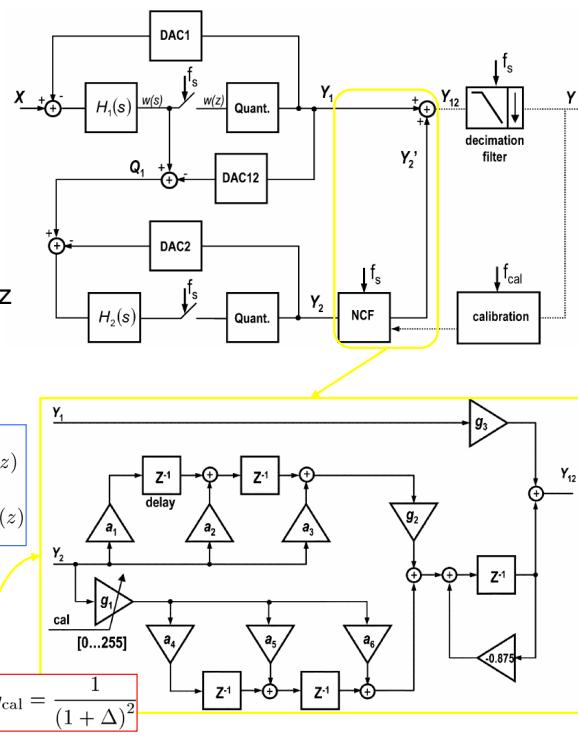


CT- $\Sigma\Delta$ Ms: State of the Art / Broadband



Cascade architecture [Bree04]

- ◆ 2-2 cascade topology
- ◆ Each stage with 4-bit quantizer
- ◆ DT-to-CT synthesis method
- ◆ 0.18 μ m CMOS technology
- ◆ 67-dB DR, 10-MHz bandwidth
- ◆ Quadrature configuration, 20-MHz
- ◆ 120mA, 1.8-V supply
- ◆ Digital calibration of NCF

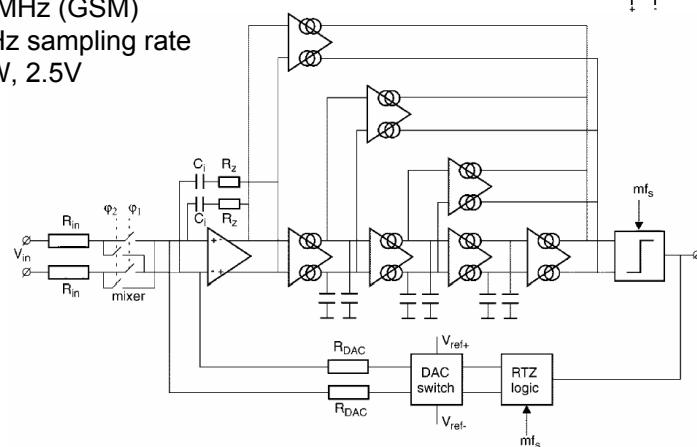


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom

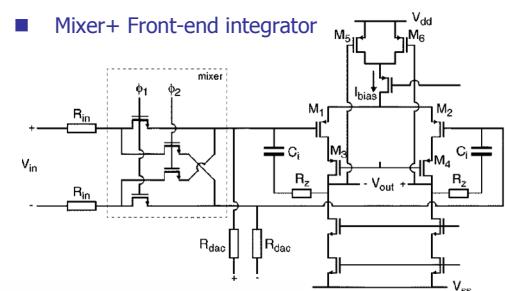


IF-to-BaseBand, GSM [Bree00]

- ◆ Fifth-order feedforward loop filter
- ◆ Quadrature configuration
- ◆ Integrated mixer+active-RC front-end integrator
- ◆ 0.35 μ m CMOS technology
- ◆ 82-dB DR within, 100-kHz band, IF=50MHz (GSM)
- ◆ 13-MHz sampling rate
- ◆ 1.8mW, 2.5V



Mixer+ Front-end integrator

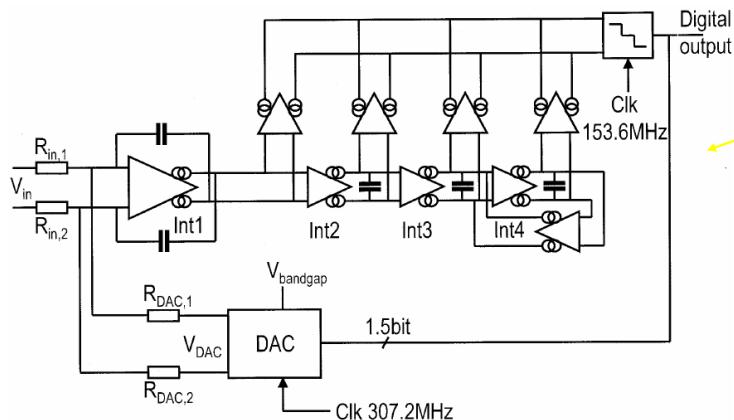
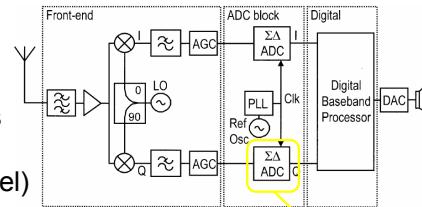


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



Quadrature architecture (I) [Veld02]

- ◆ Quadrature 4th-order, 1.5-bit topology
- ◆ Double loop to minimize internal signal swings
- ◆ 0.18 μ m CMOS technology
- ◆ 70-dB DR within 2-MHz bandwidth (per channel)
- ◆ 153.6MHz sampling rate
- ◆ 11.5mW, 1.8V

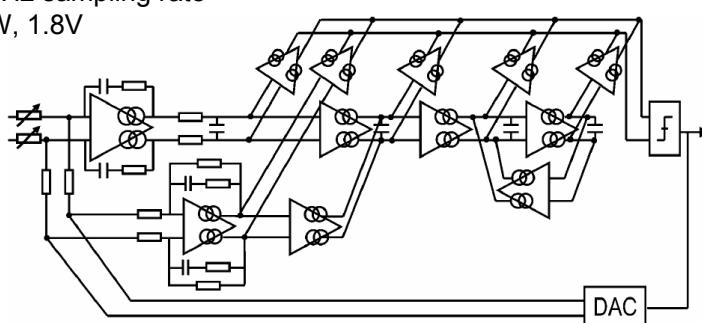
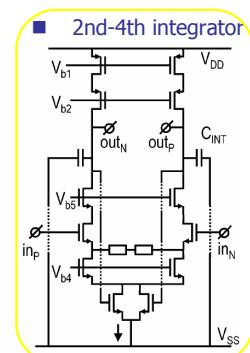
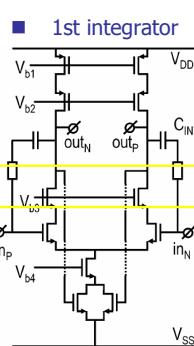


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



Programmable-gain, Merged filtering architecture [Phil04]

- ◆ Fourth-order loop filter
- ◆ Programmable gain functionality
 - Switchable input resistors (1,10,100k Ω)
- ◆ Compensating high-pass filtering
- ◆ Telescopic cascode opamps
- ◆ 0.18 μ m CMOS technology
- ◆ 89-dB DR, 1-MHz bandwidth
- ◆ 46-59 dB SNR-peak
- ◆ 64MHz sampling rate
- ◆ 2mW, 1.8V

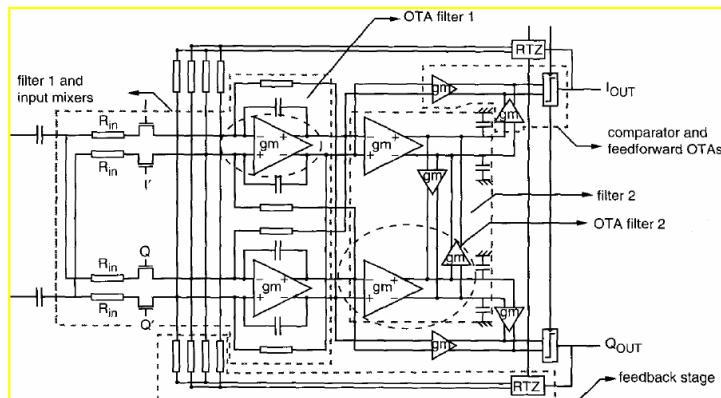
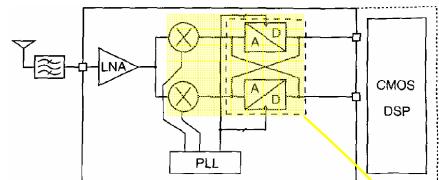


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



□ BP modulator + input mixer [Copp02]

- ◆ 1-bit, quadrature bandpass modulator
 - Second-order complex BP filter
 - Input mixing stage
- ◆ Downconversion of RF signals (0.3-1.6GHz)
- ◆ 0.25 μ m CMOS technology
- ◆ 62-dB DR, 2-MHz bandwidth, 4MHz IF
- ◆ 128-MHz sampling rate
- ◆ 14mW, 2-V

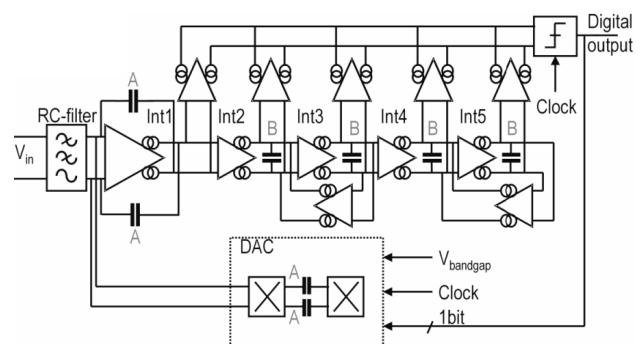
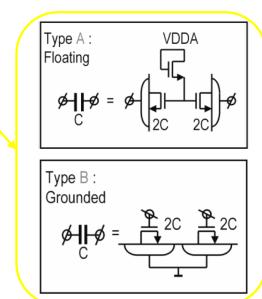
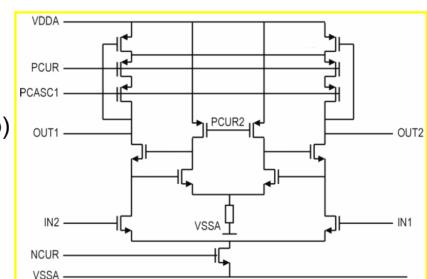


CT- $\Sigma\Delta$ Ms: State of the Art / Wireless telecom



□ MultiMode/MultiStandard applications [Veld03]

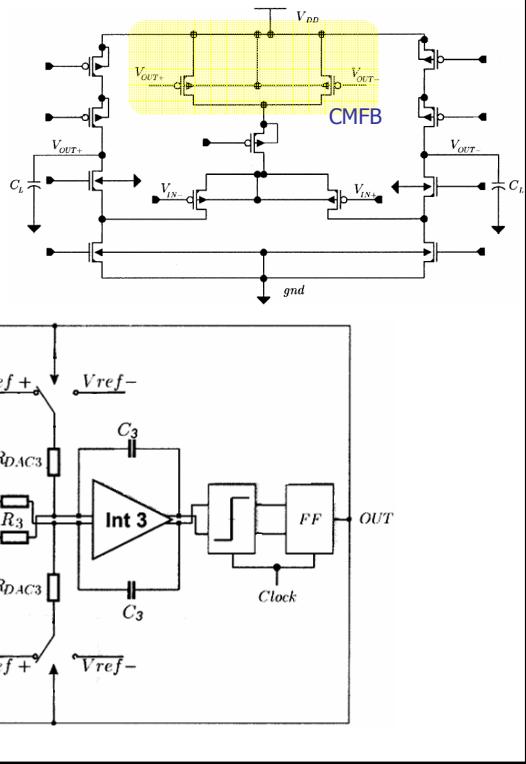
- ◆ 1-bit, complex fifth-order loop filter
 - SC DAC to reduce sensitivity to clock jitter
 - NMOS in NWELL (switchable) capacitors
 - Active RC 1st stage (regulated-cascode opamp)
 - Gm-C integrators for the remaining stages
- ◆ 0.18 μ m CMOS technology
- ◆ GSM/CDMA2000/UMTS modes
 - 92/83/72-dB DR, 200/1228/3840-kHz
 - 26/76.8/153.6-MHz sampling rate
 - 3.8/4.1/4.5mW, 1.8-V



CT- $\Sigma\Delta$ Ms: State of the Art / Low-power, low-voltage

□ Low-power Modulator [Gerb03]

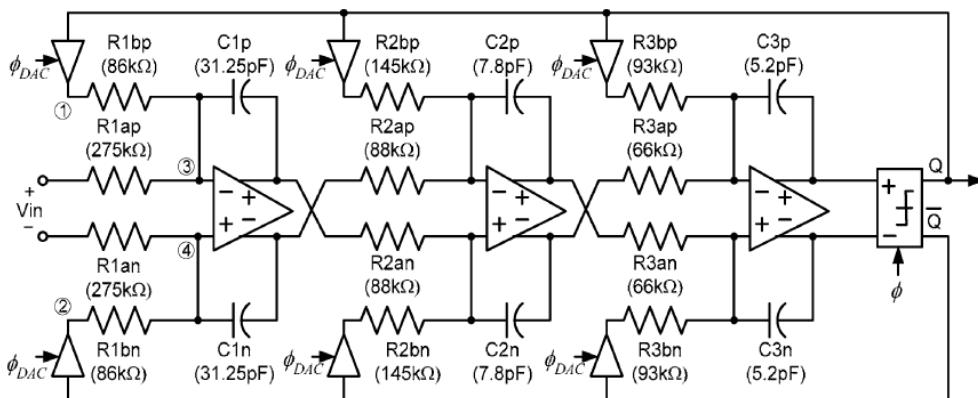
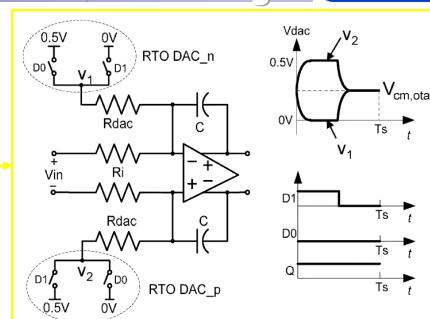
- ◆ Third-order loop filter
 - RC-active implementation
 - Folded-cascode opamps ($40\mu\text{W}$)
- ◆ 0.5 μm CMOS technology
- ◆ 80-dB DR within 25-kHz bandwidth
- ◆ 2.4MHz sampling rate
- ◆ $135\mu\text{W}$, 1.5V



CT- $\Sigma\Delta$ Ms: State of the Art / Low-power, low-voltage

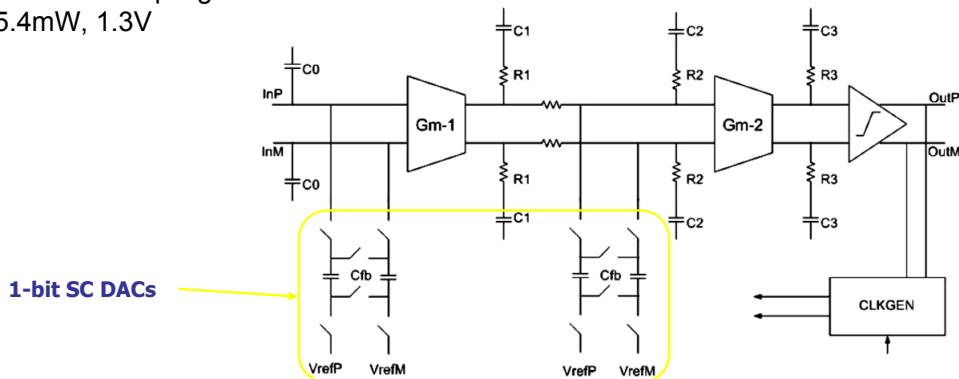
□ Low-power/Low-Voltage (0.5V) [Pun07]

- ◆ Third-order loop filter
 - RC-active integrators
 - Body-input OTAs and comparators
- ◆ Return-to-Open DAC
- ◆ 0.18 μm CMOS technology
- ◆ 74-dB DR within 25-kHz bandwidth
- ◆ $300\mu\text{W}$, 0.5V



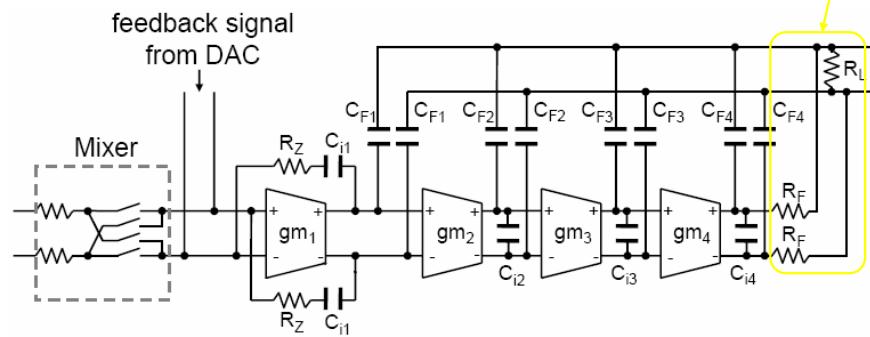
□ Active-passive implementations (I) [Das05]

- ◆ 4th-order loop filter
- ◆ Two (folded-cascode) amplifiers plus passive components
 - N-well resistors
 - PMOS capacitors
- ◆ Double loop to minimize internal signal swings
- ◆ 90nm CMOS technology
- ◆ 86-dB SNR-peak within 600-kHz bandwidth
- ◆ 256MHz sampling rate
- ◆ 5.4mW, 1.3V



□ Active-passive implementations (II) [Naga05]

- ◆ 4th-order loop filter
- ◆ Passive current-summing network in the feedforward path
 - Phase compensation
 - Reduce power consumption
- ◆ 0.11 μ m, dual- V_t CMOS technology
- ◆ Variable gain implemented by varying the DAC output power
- ◆ 57-dB DR within 1.3-MHz bandwidth
- ◆ 132-MHz sampling rate
- ◆ 3.42mW, 1.2V

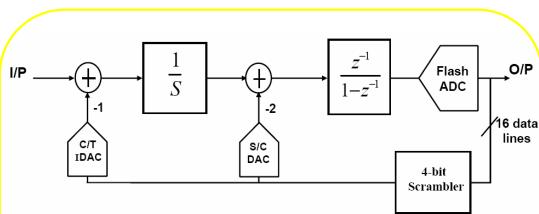


CT- $\Sigma\Delta$ Ms: State of the Art / Hybrid architectures



□ Hybrid lowpass (CT-DT) architectures [Morr05][Nguy05]

- ◆ CT front-end integrator
 - Potentially faster with less power consumption
 - Anti-aliasing filtering
 - Avoids the use of bootstrapping
- ◆ Problems
 - Sensitivity to clock jitter
 - Chopper stabilization techniques with CT filters
 - Hybrid tuning circuit required

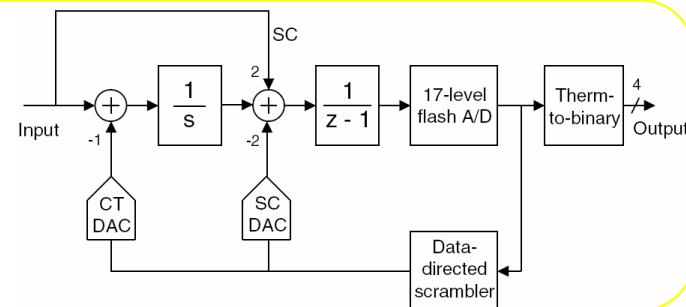


□ [Morr05]

- ◆ 0.18 μ m CMOS technology
- ◆ 102-dB DR, 20-kHz signal bandwidth
- ◆ 11.3mA, 3.3-V

□ [Nguy05]

- ◆ 0.35 μ m CMOS technology
- ◆ 106-dB DR, 192-kHz
- ◆ 36mW

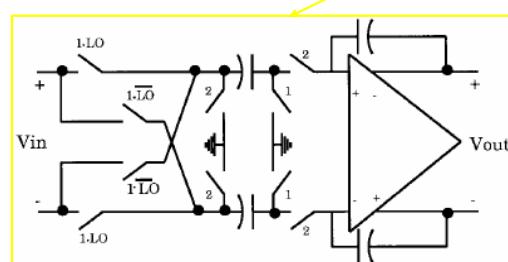
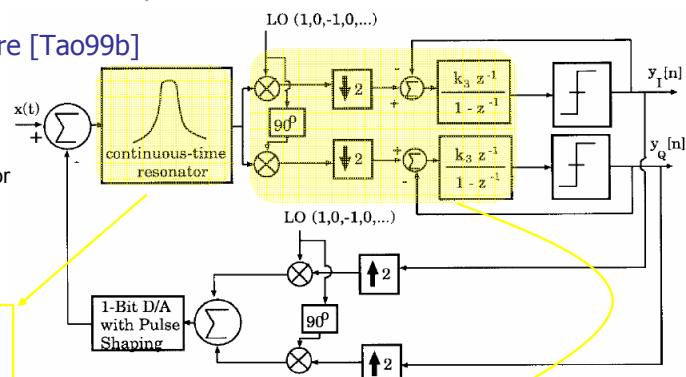
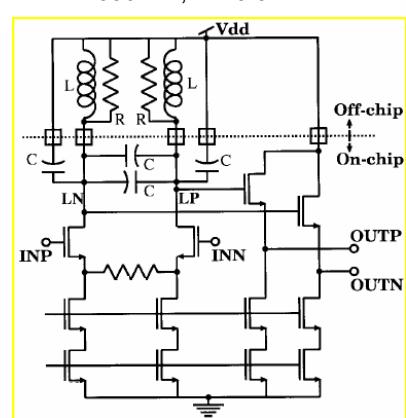


CT- $\Sigma\Delta$ Ms: State of the Art / Hybrid architectures



□ Hybrid BP (CT-DT) architecture [Tao99b]

- ◆ Fourth-order loop filter
 - IF=100MHz
 - CT front-end resonator
 - In-loop mixer+DT integrator
- ◆ 50-dB DR, 200-kHz band
- ◆ 0.35 μ m CMOS technology
- ◆ 330mW, 2.7/3.3V



DT- $\Sigma\Delta$ Ms: References



- [Chen03] F. Chen, S. Ramaswamy, and B. Bakkaloglu, “A 1.5V 1mA 80dB Passive $\Sigma\Delta$ ADC in 0.13 μ m Digital CMOS Process”. *Proc. of the IEEE International Solid-State Circuits Conference (ISSCC)*, 2003.
- [Coba99] A.L. Coban and P.E. Allen, “A 1.5V 1.0mW Audio Delta Sigma Modulator with 98dB Dynamic Range”. *Proc. of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 50-51, 1999.
- [Cusi01] P. Cusinato, D. Tonietto, F. Stefani, and A. Baschirotto, “A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass $\Sigma\Delta$ Modulator with 74-dB Dynamic Range”. *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 629-638, April 2001.
- [Good96] F. Goodenough, “Analog Techniques of all Varieties Dominate ISSCC”. *Electronic Design*, vol. 44, pp. 96-111, February 1996.
- [Kash99] D.B. Kasha, W.L. Lee, and A. Thomsen, “A 16-mW, 120-dB Linear Switched-Capacitor Delta-Sigma Modulator with Dynamic Biasing”. *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 921-926, December 1999.
- [Klem06] N. Klemmer and E. Hegazi, “A DLL-Biased, 14-Bit $\Delta\Sigma$ Analog-to-Digital Converter for GSM/GPRS/EDGE Handsets”. *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 330-338, February 2006.
- [Lee06] K.-S. Lee, S. Kwon, and F. Maloberti, “A 5.4mW 2-Channel Time-Interleaved Multi-bit $\Delta\Sigma$ Modulator with 80dB SNR and 85dB DR for ADSL”. *Proc. of the IEEE International Solid-State Circuits Conference (ISSCC)*, 2006.
- [Para06] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, “An 11-bit 330MHz 8X OSR $\Sigma-\Delta$ Modulator for Next-Generation WLAN”. *Proc. of the Symposium on VLSI Circuits*, pp. 166-167, 2006.
- [Rabi97] S. Rabii and B.A. Wooley, “A 1.8V Digital-Audio Sigma-Delta Modulator in 0.8 μ m CMOS”. *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 783-796, June 1997.
- [Salo03] T.O. Salo, S.J. Lindfors, T.M. Hollman, J.A.M. Järvinen, and K.A.I. Halonen, “80-MHz Bandpass $\Delta\Sigma$ Modulators for Multimode Digital IF Receivers”. *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 464-474, March 2003.

DT- $\Sigma\Delta$ Ms: References



- [Send97] D. Senderowicz, G. Nicollini, S. Pernici, A. Nagari, P. Confalonieri, and C. Dallavalle, “Low-Voltage Double-Sampled $\Sigma\Delta$ Converters”. *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1907-1919, December 1997.
- [Taba03] A. Tabatabaei, K. Onodera, M. Zargari, H. Samavati, and D.K. Su, “A Dual Channel $\Sigma\Delta$ ADC with 40MHz Aggregate Signal Bandwidth”. *Proc. of the IEEE International Solid-State Circuits Conference (ISSCC)*, 2003.
- [Vleu01] K. Vleugels, S. Rabii, and B. Wooley, “A 2.5-V Sigma-Delta Modulator for Broadband Communications Applications”. *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1887-1899, December 2001.

CT- $\Sigma\Delta$ Ms: References



- [Aria06] J. Arias, P. Kiss, V. Prodanov, V. Bocuzzi, M. Banu, D. Bisbal, J. San Pablo, L. Quintanilla and J. Barbosa: "A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers". *IEEE J. of Solid-State Circuits*, pp. 339-351, Feb. 2006
- [Bree00] L.J. Breems, E.J. Van der Zwan and J. Huijsing, "A 1.8-mW CMOS $\Sigma\Delta$ Modulator with Integrated Mixer for A/D Conversion of IF Signals". *IEEE Journal of Solid-State Circuits*, Vol. 35, pp. 468-475, April 2000.
- [Bree01] L. Breems and J.H. Huijsing, *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*. Kluwer Academic Publishers, 2001.
- [Bree04] L.J. Breems, R. Rutten and G. Wetzker, "A Cascaded Continuous-Time $\Sigma\Delta$ Modulator with 67-dB Dynamic Range in 10-MHz Bandwidth". *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 2152-2160, December 2004.
- [Cald06] T. C. Caldwell and D. A. Johns: "A Time-Interleaved Continuous-Time DS Modulator With 20-MHz Signal Bandwidth". *IEEE Journal of Solid-State Circuits*, Vol. 41, pp. 1578-1588, July 2006.
- [Cher00] J.A. Cherry and W.M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*. Kluwer Academic Publishers, 2000.
- [Copp02] P. Coppejans, P. Vancorenland, W. de Cock and M. Steyaert, "Continuous-Time Quadrature Bandpass $\Delta\Sigma$ Modulator With Input Mixers". *IEE Pro. Circuits and Devices Syst.*, Vol. 149, pp. 331-336, Oct/Dec 2002.
- [Dagh04] E.H. Dagher, P. A. Stubberud, W. K. Masenten, M. Conta and T. Victor Dinh, "A 2-GHz Analog-to-Digital Delta-Sigma Modulator for CDMA Receivers With 79-dB Signal-to-Noise Ratio in 1.23-MHz Bandwidth". *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 1819-1828, November 2004.
- [Das05] A. Das, R. Hezar, R. Byrd, G. Gomez and Baher Haroun, "A 4th-order 86-dB CT $\Sigma\Delta$ ADC with Two Amplifiers in 90nm CMOS". *Proc. of the 2005 IEEE Int. Solid-State Circuits Conf.*, pp. 496-497, 2005.
- [Dörr03] L. Dörrer, F. Kuttner, A. Wiesbauer, A. Di Giandomenico and T. Hartig, "A 10-Bit, 3-mW Continuous-Time Sigma-Delta ADC for UMTS in a 0.12 μ m CMOS Process". *Proc. of ESSCIRC03*, Sept. 2003.
- [Dörr05] L. Dörrer, F. Kuttner, P. Greco and S. Derksen, "A 3mW 74 SNR 2-MHz CT $\Sigma\Delta$ ADC with a Tracking-ADC-Quantizer in 0.13 μ m CMOS". *Proc. of the 2005 IEEE Int. Solid-State Circuits Conf.*, pp. 492-493, 2005.

CT- $\Sigma\Delta$ Ms: References



- [Font05] P. Fontaine, A. N. Mohieldin and A. Bellaourar, "A Low-Noise Low-Voltage CT DS Modulator with Digital Compensation of Excess Loop Delay". *Proc. of the 2005 IEEE ISSCC*, pp. 498-499, 2005.
- [Gerf03] F. Gerfers, M. Ortmanns and Y. Manoli, "A 1.5-V 12-bit Power-Efficient Continuous-Time Third-Order $\Sigma\Delta$ Modulator". *IEEE Journal of Solid-State Circuits*, Vol. 38, pp. 1343-1352, August 2003.
- [Luh00] L. Luh, J. Choma and J. Draper, "A 400-MHz 5th-Order Continuous-Time Switched-Current $\Sigma\Delta$ Modulator". *Proc. of the 2000 European Conf. on Solid-State Circuits*, pp. 72-75, September 2000.
- [Mitt06] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue and E. Romani: "A 20-mW 640-MHz CMOS Continuous-Time SD ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB". *IEEE Journal of Solid-State Circuits*, Vol. 41, pp. 2641-2649, December 2006.
- [Moya03] M. Moyal, M. Groepel, H. Werker, G. Mitteregger and J. Schambacher, "A 700/900mW/Channel CMOS Dual Analog Front-End IC for VDSL with Integrated 11.5/14.5dBm Line Drivers". *Proc. Of ISSCC03*, Feb. 2003.
- [Morr05] P. Morrow, M. Chamarro, C. Lyden, P. Ventura, A. Abo, A. Matamura, M. Keane, R. O'Brien, P. Minogue, J. Mansson, N. McGuinness, M. McGranaghan and I. Ryan, "A 0.18 μ m 102dB-SNR Mixed CT SC Audio-Band $\Delta\Sigma$ ADC". *Proc. of the 2005 IEEE Int. Solid-State Circuits Conf.*, pp. 178-179, 2005.
- [Naga05] T. Nagai, H. Satou, H. Yamazaki and Y. Watanabe, "A 1.2 3.5mW $\Delta\Sigma$ Modulator with a Passive Current Summing Network and a Variable Gain Function". *Proc. of the 2005 IEEE Int. Solid-State Circuits Conf.*, pp. 494-495, 2005.
- [Nguy05] K. Nguyen, B. Adams, K. Sweetland, H. Chen and K. McLaughlin, "A 106dB SNR Hybrid Oversampling ADC for Digital Audio". *Proc. of the 2005 IEEE Int. Solid-State Circuits Conf.*, pp. 176-177, 2005.
- [Olia03a] O. Olieai, "State-Space Analysis of Clock Jitter in Continuous-Time Oversampling Data Converters". *IEEE Transactions on Circuits and Systems I*, Vol. 50, pp. 31-37, January 2003.
- [Olia03b] O. Olieai, "Design of Continuous-Time Sigma-Delta Modulators With Arbitrary Feedback Waveform". *IEEE Transactions on Circuits and Systems II*, Vol. 50, pp. 437-444, August 2003.
- [Ortm01] M. Ortmanns, F. Gerfers, and Y. Manoli, "On the synthesis of cascaded continuous-time Sigma-Delta modulators". *Proc. of the 2001 IEEE Int. Symp. on Circuits and Systems*, Vol. 5, pp. 419-422, May 2001.

CT- $\Sigma\Delta$ Ms: References



- [Ortm04] M. Ortmanns, F. Gersers and Y. Manoli, "Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time Sigma-Delta Modulators". *IEEE Transactions on Circuits and Systems I*, Vol. 51, pp. 1088-1099, June 2004.
- [Pato04] S. Patón, A. D. Giandomenico, L. Hernández, A. Wiesbauer, T. Pötscher and M. Clara, "A 70-mW 300-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 15-MHz Bandwidth and 11 Bits of Resolution". *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 1056-1063, July 2004.
- [Phil04] K. Philips, P. A.C.M. Nuijten, R. L. J. Roovers, A. H.M. van Roermund, F. Muñoz-Chavero, M. Tejero Pallarés and A. Torralba, "A Continuous-Time $\Sigma\Delta$ ADC With Increased Immunity to Interferers". *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 1056-1063, July 2004.
- [Pun07] K. Pun, S. Chatterjee and P. R. Kinget: "A 0.5-V 74-dB SNDR 25-kHz Continuous-Time Delta-Sigma Modulator With a Return-to-Open DAC". *IEEE Journal of Solid-State Circuits*, Vol. 42, pp. 406-507, March 2007.
- [Ruiz05] J. Ruiz-Amaya, J.M. de la Rosa, F.V. Fernández, F. Medeiro, R. del Río, B. Pérez-Verdú and A. Rodríguez-Vázquez, "High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time $\Sigma\Delta$ Modulators Using SIMULINK-Based Time-Domain Behavioral Models". *IEEE Trans. on Circuits and Systems-I*, Vol. 52, pp. 1785-1810, September 2005.
- [Sami03] L. Samid and Y. Manoli, "A Micro Power Continuous-Time $\Sigma\Delta$ Modulator". *Proc. of ESSCIRC03*, Sept. 2003.
- [Schi04] M. Schimpfer, L. Dörner, E. Riccio and G. Panov, "A 3mW Continuous-Time $\Sigma\Delta$ -Modulator for EDGE/GSM With High Adjacent Channel Tolerance". *Proc. of ESSCIRC04*, Sept. 2004.
- [Tao99a] H. Tao, L. Toth and M. Khouri, "Analysis of Timing Jitter in Bandpass Sigma-Delta Modulators". *IEEE Transactions on Circuits and Systems I*, Vol. 46, pp. 991-1001, August 1999.
- [Tao99b] H. Tao and J.M. Khouri, "A 400MS/s Frequency Translating BandPass Delta-Sigma Modulator". *IEEE Journal of Solid-State Circuits*, Vol. 34, pp. 1741-1752, December 1999.
- [Tort05a] R. Tortosa, J.M. de la Rosa, A. Rodriguez-Vázquez and F.V. Fernández, "Analysis of Clock Jitter Error in Multibit Continuous-Time $\Sigma\Delta$ Modulators with NRZ Feedback Waveform". *Proc. of ISCAS*, May 2005.

CT- $\Sigma\Delta$ Ms: References



- [Tort06] R. Tortosa, J.M. de la Rosa, F.V. Fernández and A. Rodríguez-Vázquez: "A New High-Level Synthesis Methodology of Cascaded Continuous-Time Sigma-Delta modulators". *IEEE Trans. On Circuits and Systems – II: Express Briefs*, pp. 739-743, August 2006.
- [Veld02] R.H.M. van Veldhoven, B.J. Minnis, H.A. Hegi and A.H.M. Roermund, "A 3.3-mW $\Sigma\Delta$ Modulator for UMTS in 0.18- μ m CMOS With 70-dB Dynamic Range in 2-MHz Bandwidth". *IEEE Journal of Solid-State Circuits*, Vol. 37, pp. 1645-1652, December 2002.
- [Veld03] R.H.M. van Veldhoven, "A Triple-Mode Continous-Time $\Sigma\Delta$ Modulator With Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver". *IEEE Journal of Solid-State Circuits*, Vol. 37, pp. 2069-2076, December 2003.
- [Yan04] S. Yan and E. Sánchez-Sinencio, "A Continuous-Time $\Sigma\Delta$ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth". *IEEE Journal of Solid-State Circuits*, pp. 75-86, January 2004.
- [Zwan96] E.J. van der Zwan and E.C. Dijkmans, "A 0.2mW CMOS $\Sigma\Delta$ Modulator for Speech Coding with 80dB Dynamic Range". *IEEE Journal of Solid-State Circuits*, pp. 1873-1880, December 1996.
- [Zwan00] E.J. van der Zwan, K. Philips and C. A. A. Bastiaansen, "A 10.7-MHz IF-to-Baseband $\Sigma\Delta$ A/D Conversion System for AM/FM Radio Receivers". *IEEE Journal of Solid-State Circuits*, pp. 1810-1819, December 2000.