CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Systematic Design Methodology

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KTH, Stockholm, April 23-27

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   - Digital vs. Analog/Mixed-signal design
   - Simulation approaches
   - Hierarchical synthesis approach
2. Top-down design methodology
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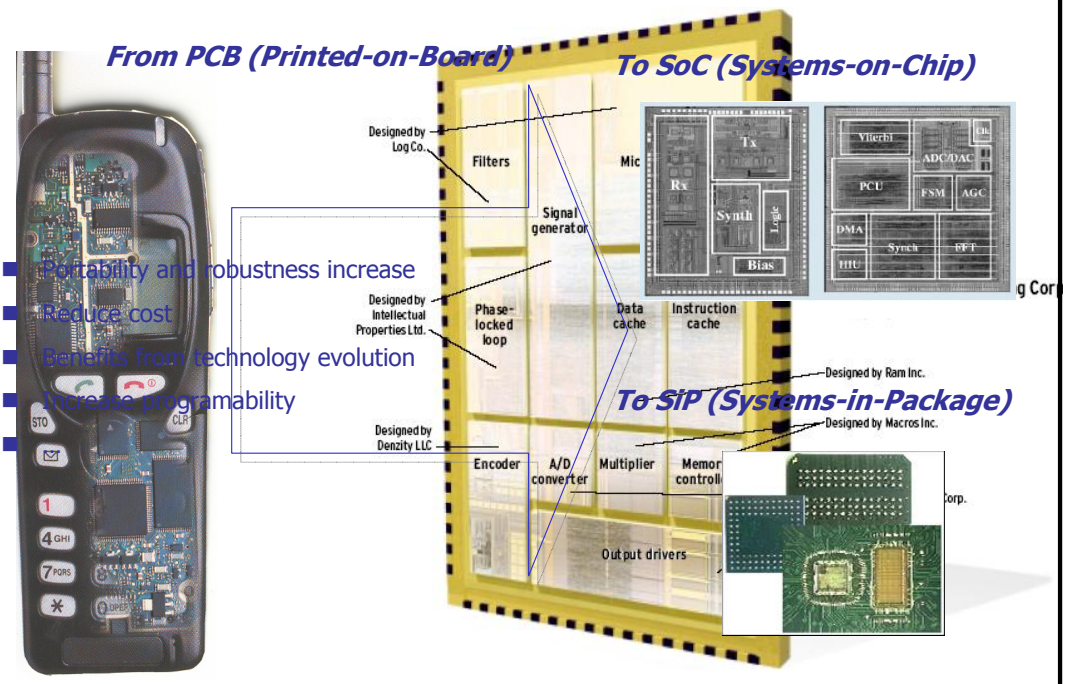
   - Optimization engine
   - Behavioral simulation
3. Introduction to SIMSIDES
   - Description of the toolbox
   - Behavioral modeling of building blocks
4. DEMO & Tutorial examples

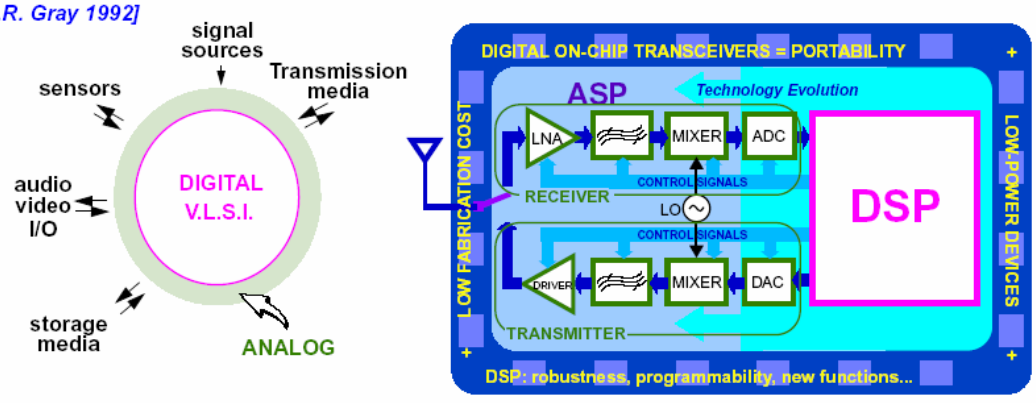
Introduction: Tendency to System Integration



- Portability and robustness increase
- Reduce cost
- Benefits from technology evolution
- Increase programability

Introduction: Digital vs. Analog&Mixed-Signal design

[P.R. Gray 1992]



Introduction: Digital vs. Analog&Mixed-Signal design

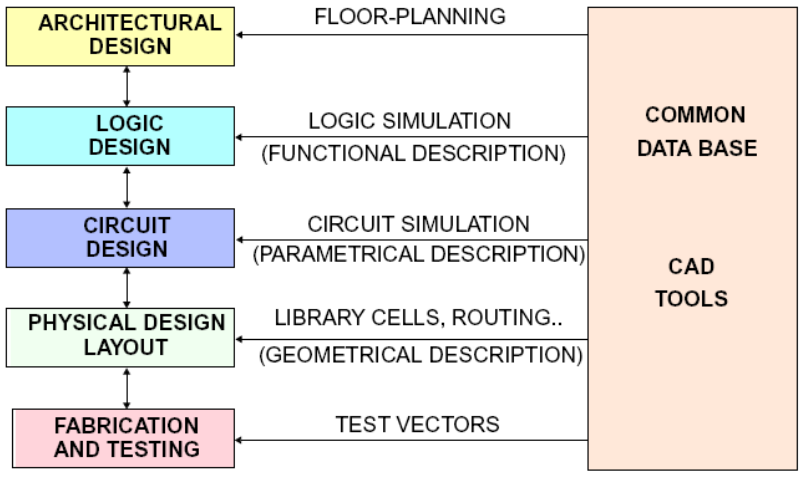
Digital Circuits

- Robustness , programmability and adaptability to different standards and protocols
- Increased performance with technology scaling
- Simplicity of the design and testing
  - Clear hierarchy leading to well-defined levels of abstraction
  - Circuit blocks are largely independent of each other
- Aumotamic top-down design from specs to silicon

A/D/A Interface = Bottle Neck of the Design Process

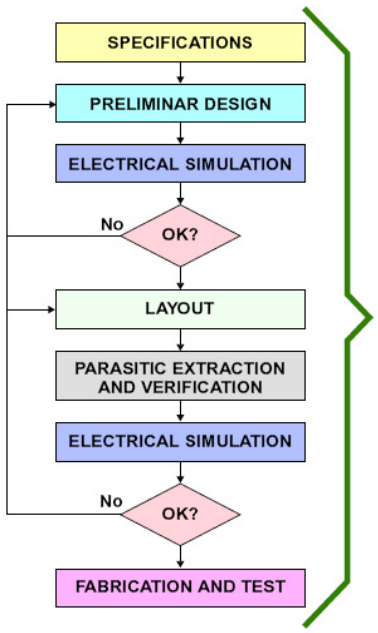
- Technology evolution demands for faster, precise and low-power A/D/A Interfaces
- Analog Circuits in Technologies dedicated to Digital Design (standard ULSI CMOS)
  - Continuously decreasing supply voltages
  - Reduced channel length and large threshold voltage in MOS transistors
  - Poor matching properties and linearity
  - Incomplete models for the analog design needs
- Proximity of noisy digital circuits
- Need of Design Automation (DA)

Introduction: Digital CAD tools



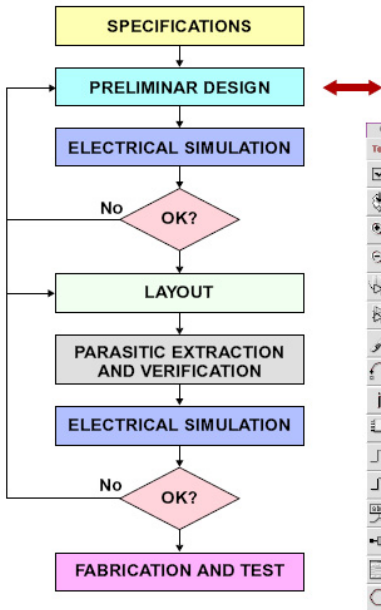
- At each design-flow level:
  - Generation of a solution
  - Simulation and verification
- Properly supported by CAD tools:
  - Simulators, verification tools, ...
  - Graphical interfaces: schematic and layout editors, ...

Introduction: Analog CAD tools

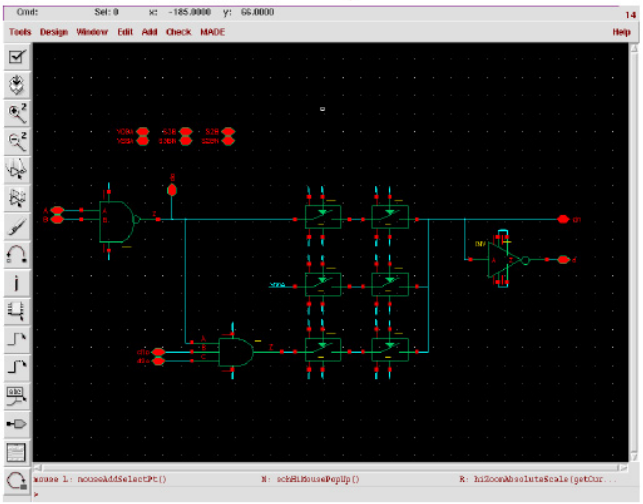


Until a few years ago: only SPICE-like simulators and post-layout verification tools

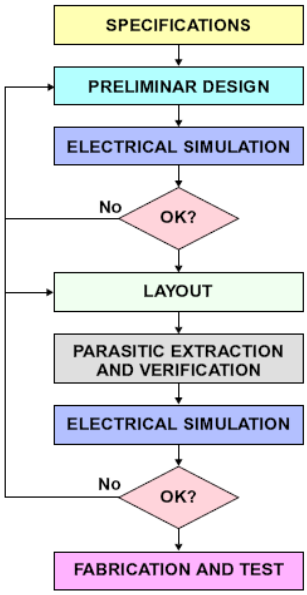
Introduction: Analog CAD tools



Schematic capture

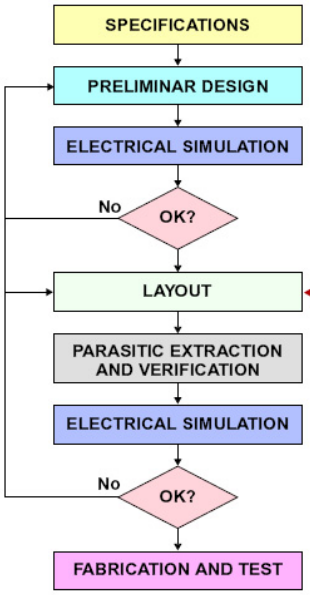


Introduction: Analog CAD tools

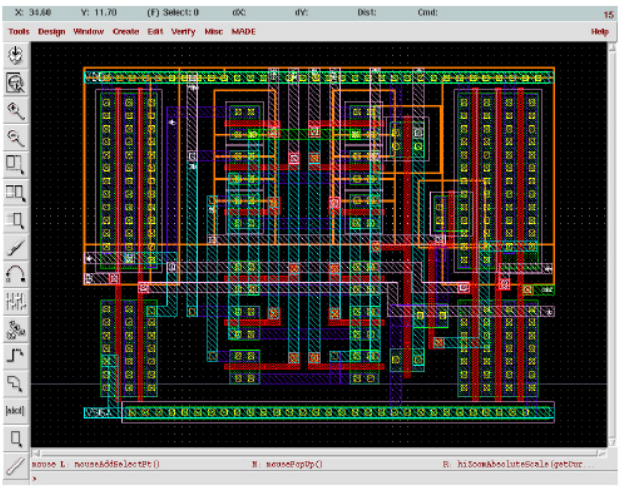


Simulators : SPICE, Spectre, ELDO, ... → Graphic editors: GSI, Awaves, ...

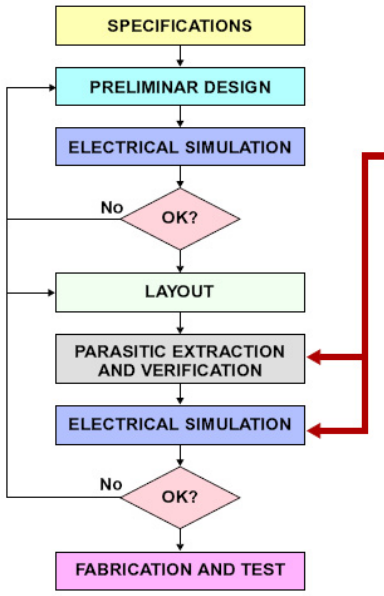
Introduction: Analog CAD tools



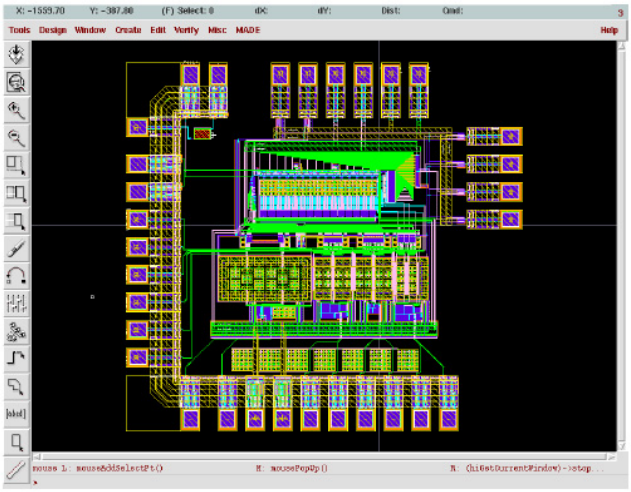
Layout editors: DFWII, Magic, ... → Checkers : DRC, ERC, LVS, ...



Introduction: Analog CAD tools



LPE, LVS and Post-Layout Simulation



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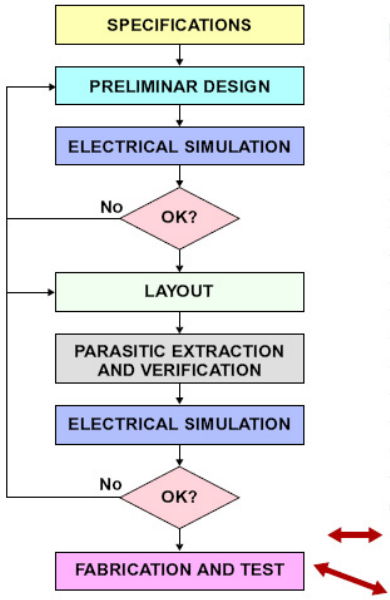
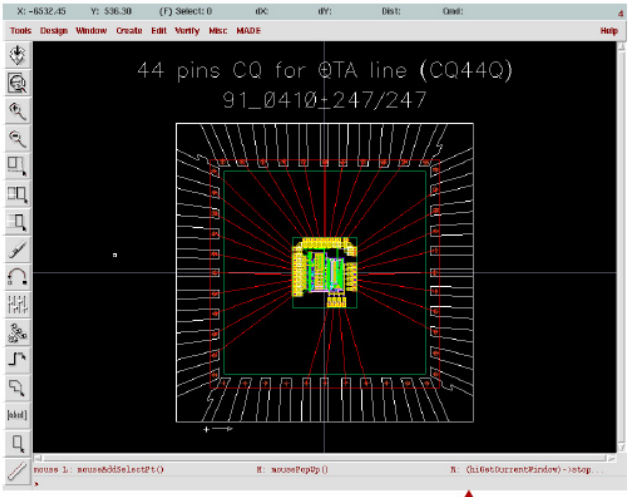
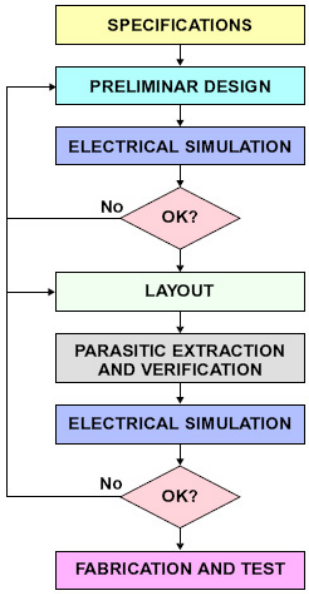




Bonding-diagram chekers: BDE

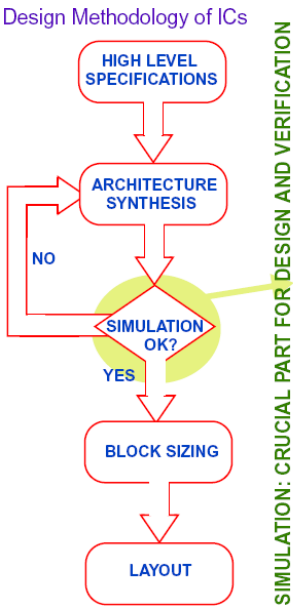
Design of PCBs

Introduction: Analog CAD tools



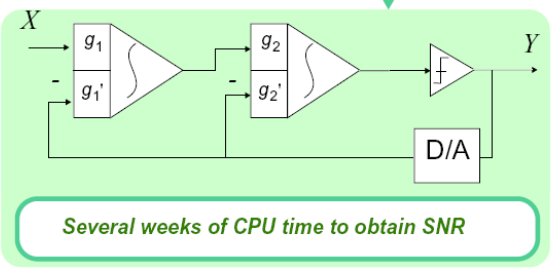
- *Clearly inefficient for the design of complex systems*
- *Excessive consumption of computational resources*

Introduction: Simulation approaches



- *Electrical simulation of relatively simple discrete-time (SC, SI) circuits is* ***COMPLETELY INEFICIENT***
  - Need of time-domain analysis
  - Several thousands of clock cycles required

Example: A 2nd-order ΣΔ ADC

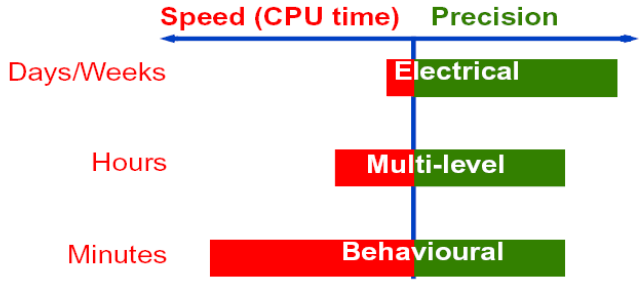


Several weeks of CPU time to obtain SNR

Need of searching other simulation approaches

Introduction: Simulation approaches

- **Electrical simulation with macromodels**: Uses numerical algorithms to solve the differential equations that result from the analysis of a circuit, thus resulting in long CPU times.
- **Multi-level simulation**: The critical parts of the system are simulated numerically while behavioural models are incorporated to emulate the rest of the system. (ELDO, SABER...)
- **Behavioural simulation (event-driven)** : The system is broken up into a set of subcircuits, often called building blocks or basic blocks. These blocks are described by explicit equations that relate the outputs in terms of the inputs and the internal state variables. Thus, the accuracy of the simulation depends on how precisely those equations describe the real behaviour of each block. The transient evolution of the voltages and currents is not important, only the final value. (TOSCA, ASIDES, MATLAB-BASED SIMULATORS...)

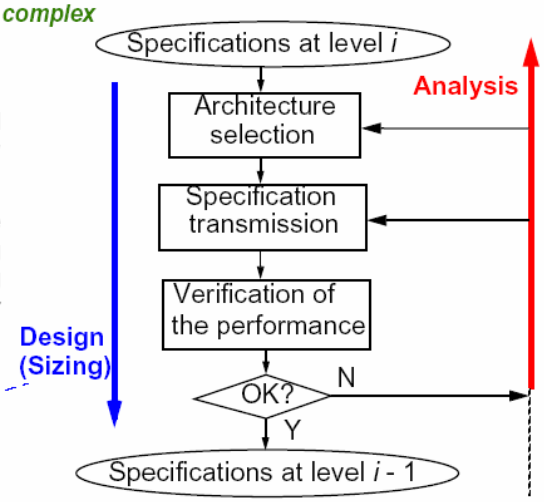


Introduction: Hierarchical synthesis approach

A very popular strategy to synthetize complex blocks is to hierarchize the design

- The complex system is partitioned in simpler blocks with relatively independent functionality.
- In each level of the hierarchy the sizing process involves selecting the architecture and transmitting the specifications to the lower level.

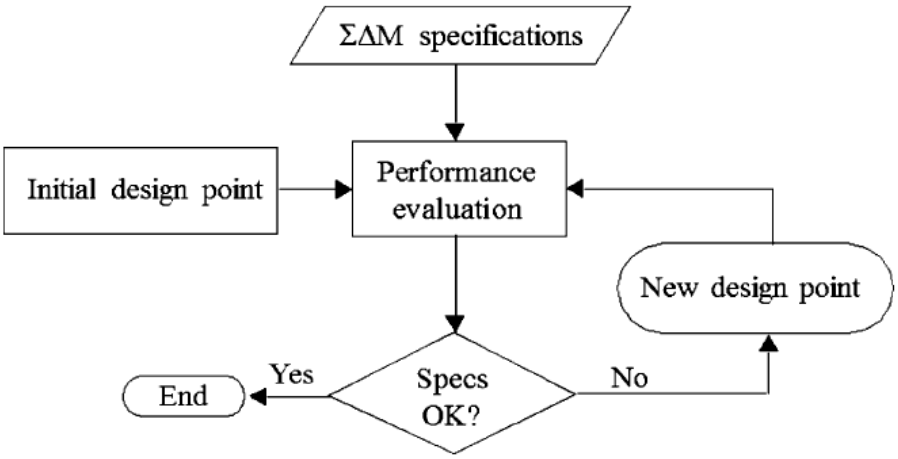
Mapping specs. on design parameters



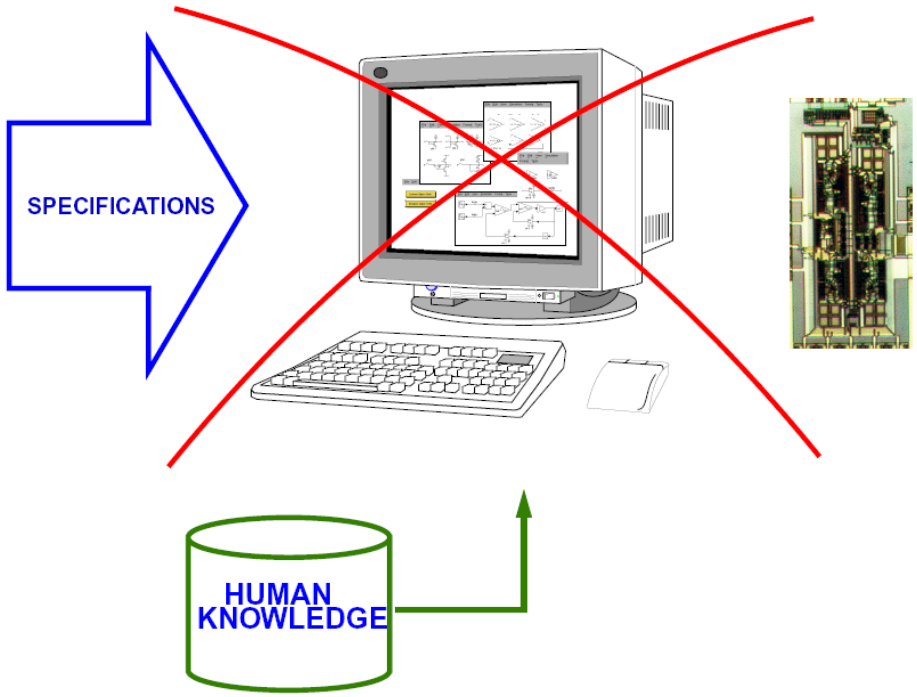
Introduction: Synthesis methods

- **Knowledge-based tools**: capture the knowledge of experienced designers
  - Short execution times
  - Not optimized: design procedures usually based on approximate equations and models
  - Closed tools
    - Limited to a reduced number of topologies
    - Addition of new ones usually restricted to the tool developers
- **Optimization-based tools**: based on an iterative optimization procedure
  - Cost function evaluation by numerical methods: ***equations*** or ***simulations***
  - Two main optimization techniques:
    - ***Deterministic***: parameter updating needs information on the cost function and on their derivatives
      - Optimization process may be trapped in a local minimum of the cost function
      - Useful for fine tuning of suboptimal designs
    - ***Statistical***: *parameters are changed randomly*
      - Avoid local minima
      - Appropriate for global optimization
      - No good initial design point is needed
      - Requires larger computational cost

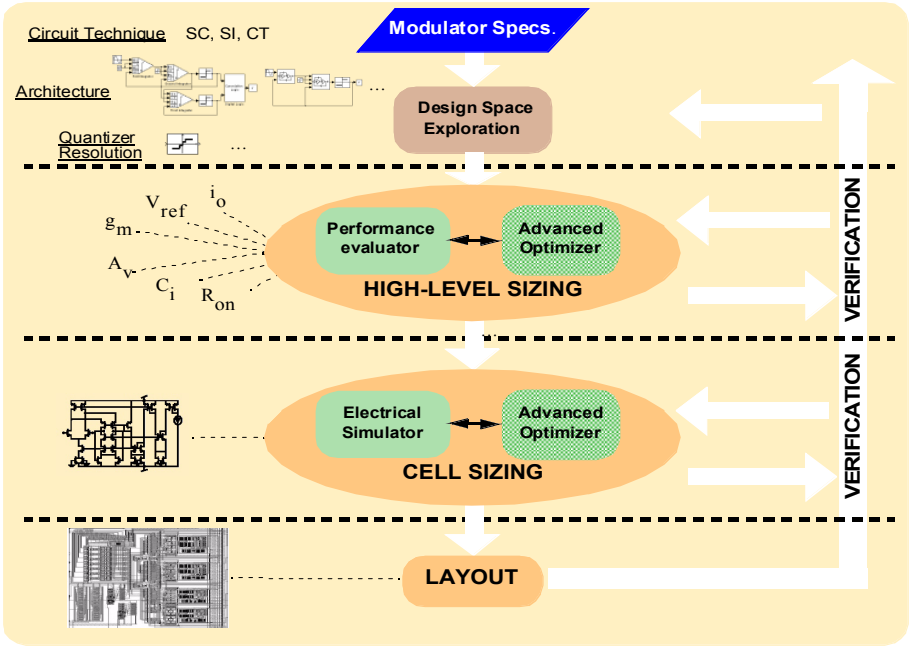
Introduction: Optimization-based synthesis approach



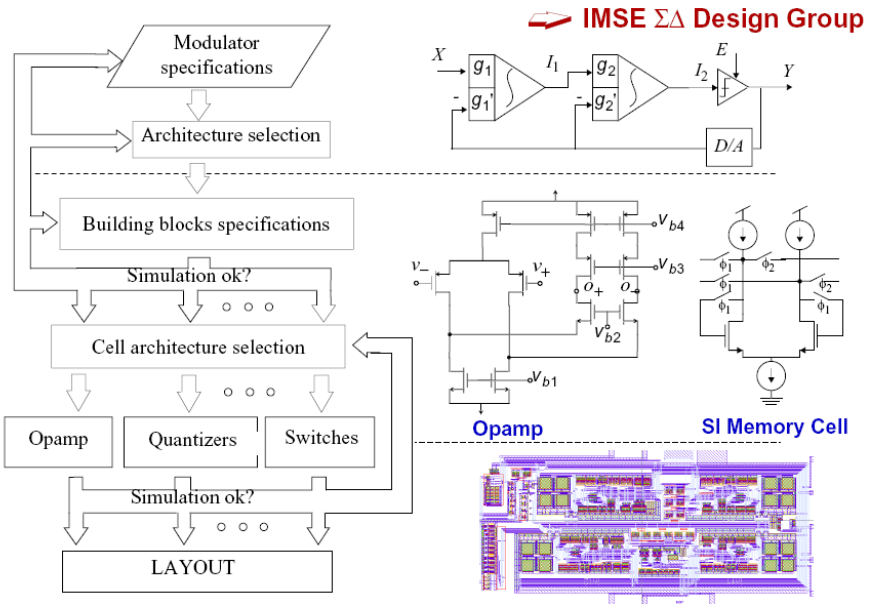
Introduction



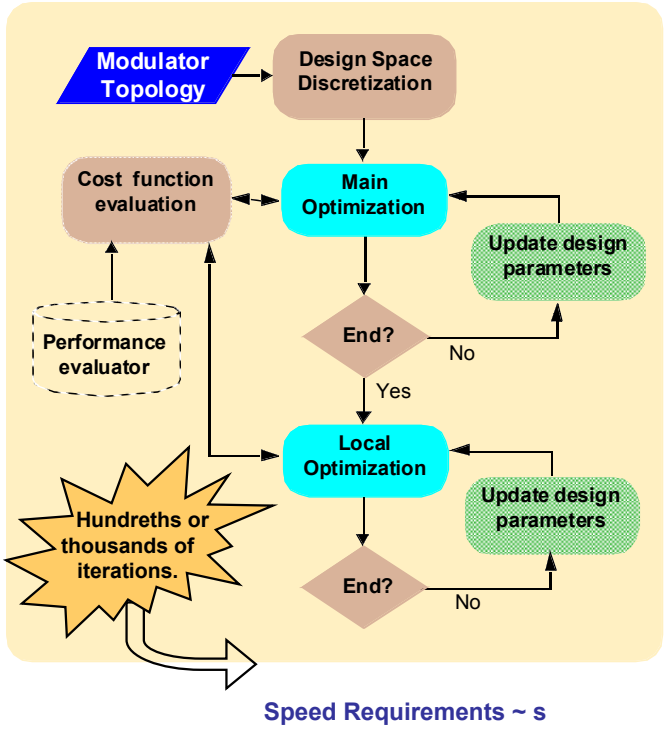
Design Methodology: Top-down & bottom-up approach



Design Methodology: Top-down & bottom-up approach



Design Methodology: Optimization



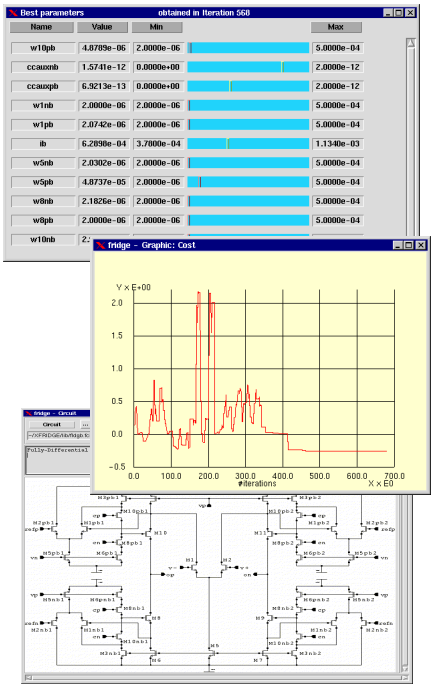
BASIC FEATURES

- ☺ Combines adaptive statistical and deterministic optimization
- ☺ Cost function formulation very versatile
- ☺ Addition of knowledge is permitted

Design Methodology: Optimization

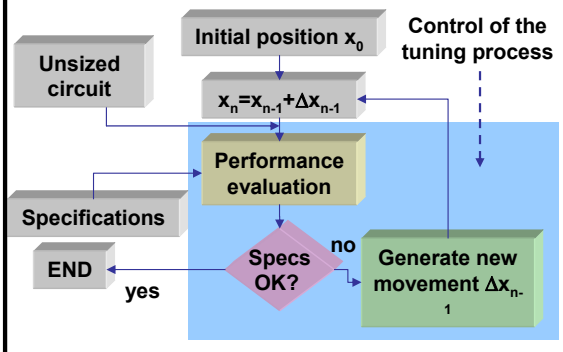
OPTIMIZATION-BASED ENGINE (FRIDGE)

- Interacts with any kind of performance evaluation approach
- Statistical + Deterministic techniques
- Designer's expertise can be added through powerful tools (embedded C++)
- Between Optimization and Knowledge-based approaches, taking the best from both worlds
- Used both for spec transmission and for cell-level sizing
- In process of being complemented with Evolutionary Algorithms
- Intese internal use

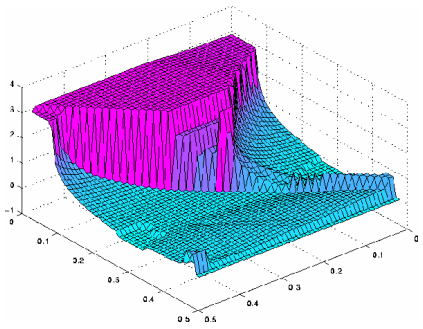


Design Methodology: Optimization

ITERATIVE CYCLE



EXAMPLE OF A COST FUNCTION



FORMULATION OF THE COST FUNCTION

Problem: minimize $y_{oi}(\mathbf{x})$,$1 \le i \le P$
subjected to $y_{rk}(\mathbf{x}) \ge Y_{rk}$ or $y_{rk}(\mathbf{x}) \le Y_{rk}$,$1 \le k \le R$

Target Specification

P design objectives

R restrictions

Cost Function

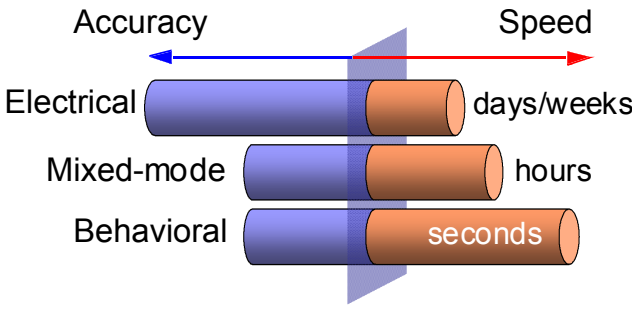
Weights used to give priority to the fulfillment of their corresponding specifications

$$\Psi(\mathbf{x}) = \begin{cases} \left(-\sum_i w_i \log\left(|y_{oi}|\right) \right) & \text{if } \mathbf{x} \in R_A \\ \max\left[-w_k \log\left(\frac{y_{rk}}{Y_{rk}} \right) \right] & \text{if } \mathbf{x} \notin R_A \end{cases}$$

Design Methodology: Simulation techniques

- **Simulation of ΣΔMs:**
  - Strongly non-linear circuits
  - Oversampling ➔ long time-domain simulation

- **Techniques**

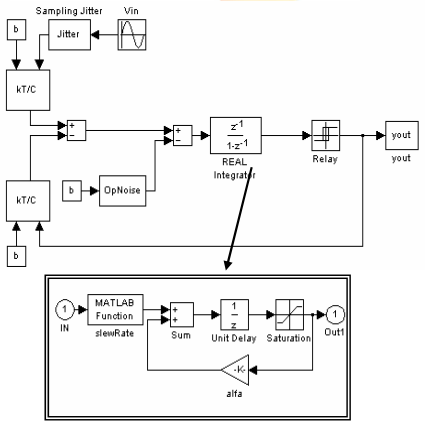


SIMSIDES: Implementation platform

- MATLAB-SIMULINK is a widely spread platform.
- Direct access to very powerful tools for signal processing and data manipulation.
- Provides a high-level language to create custom functions, structures, Graphical User Interfaces (GUIs), etc.

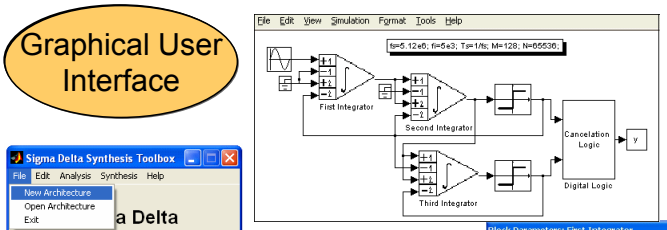
Simulink block libraries
(Malcovati et al., IEEE Trans. CAS, 2003)

- **Limited to SC circuits.**
- **Limited accuracy:**
  - **Transient response in both clock-phases not considered.**
  - **Non-linear opamp DC gain, non-linear switch-on resistance, non-linear capacitors not included.**
- **Models based on MATLAB functions ➔ excessive CPU time.**



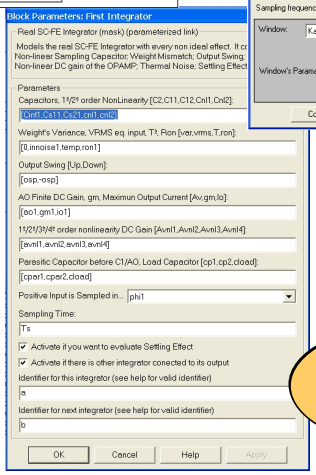
SIMSIDES: Description of the toolbox

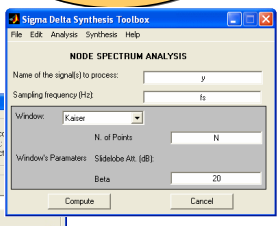
Graphical User Interface



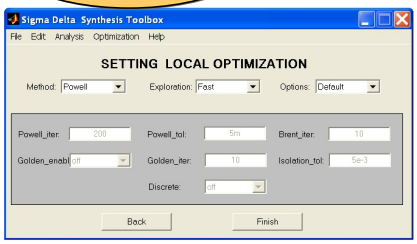
Collection of post-processing routines

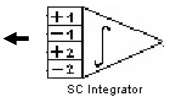
SC, SI and CT techniques





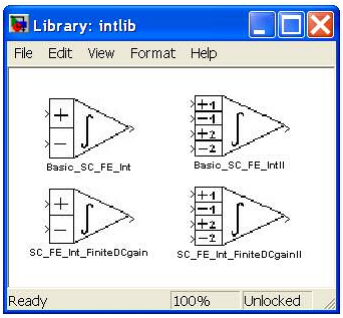
Global and efficient optimization techniques

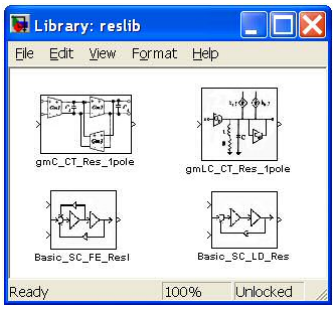


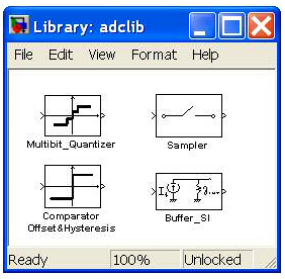


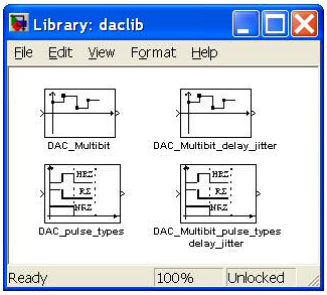
Precise behavioural models

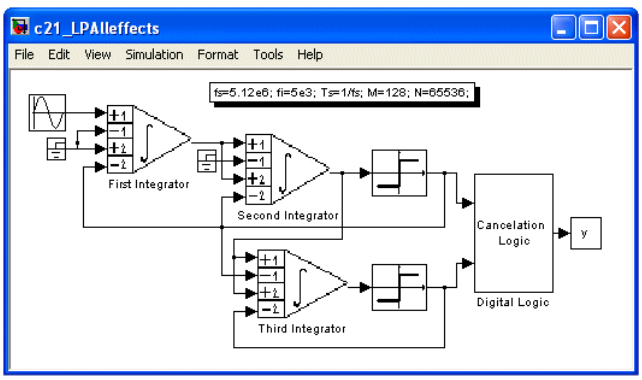
SIMSIDES: Description of the toolbox











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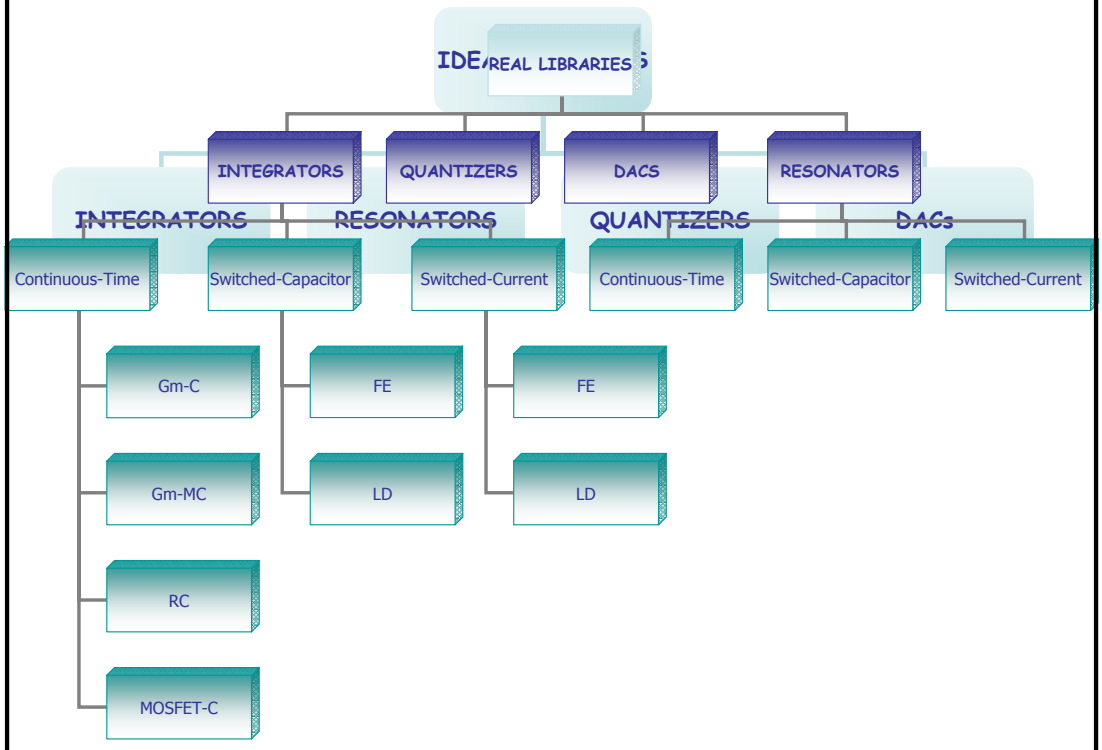
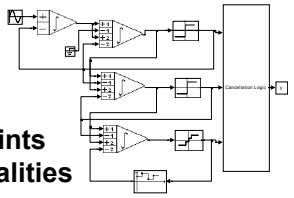


SIMSIDES: Behavioral modeling using S-functions

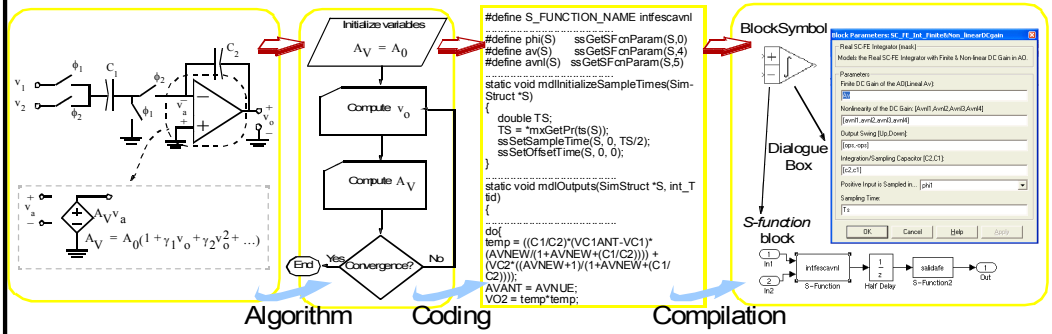
S-functions

- **Precise models:**
  - **All major non-idealities included**
  - **Time-domain models**
- **Models based on C-code ➔ fast!!**

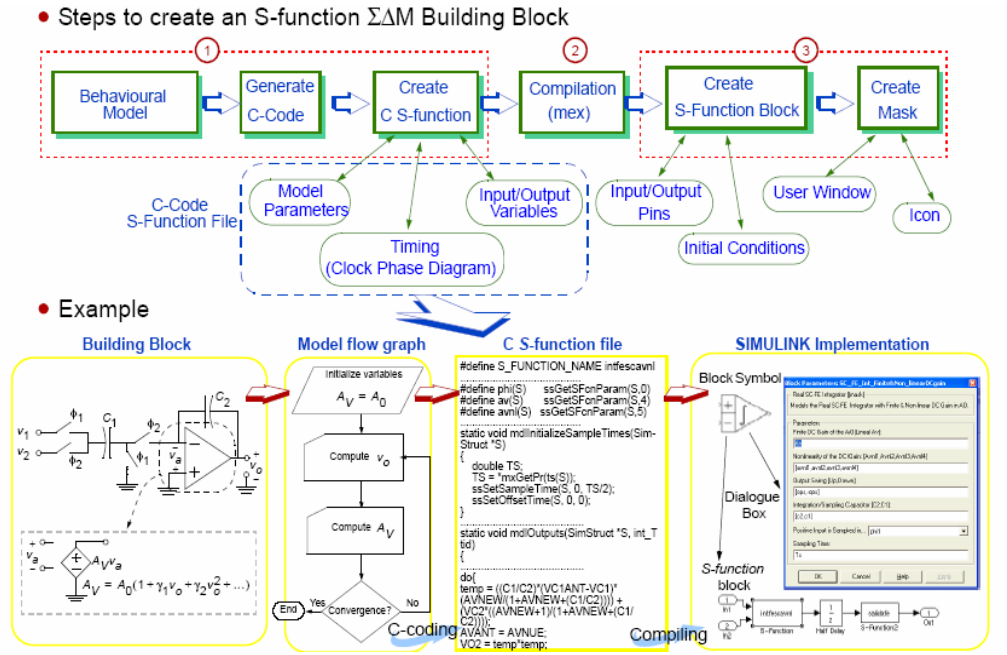


65536 points
All non-idealities

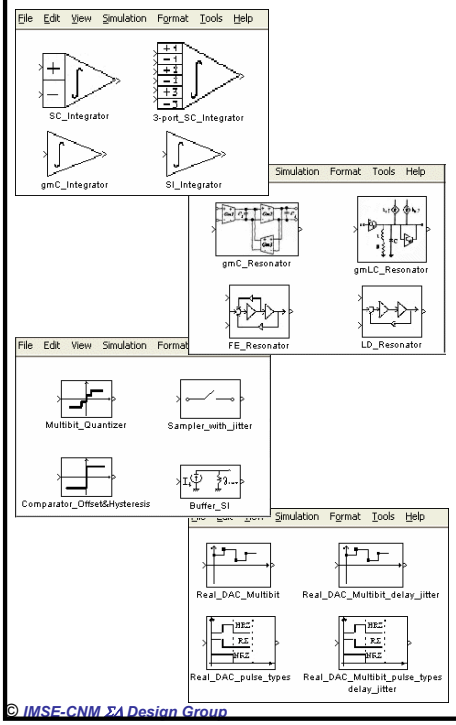
S-functions	M-functions
3 s.	141 s.



SIMSIDES: Creating S-functions

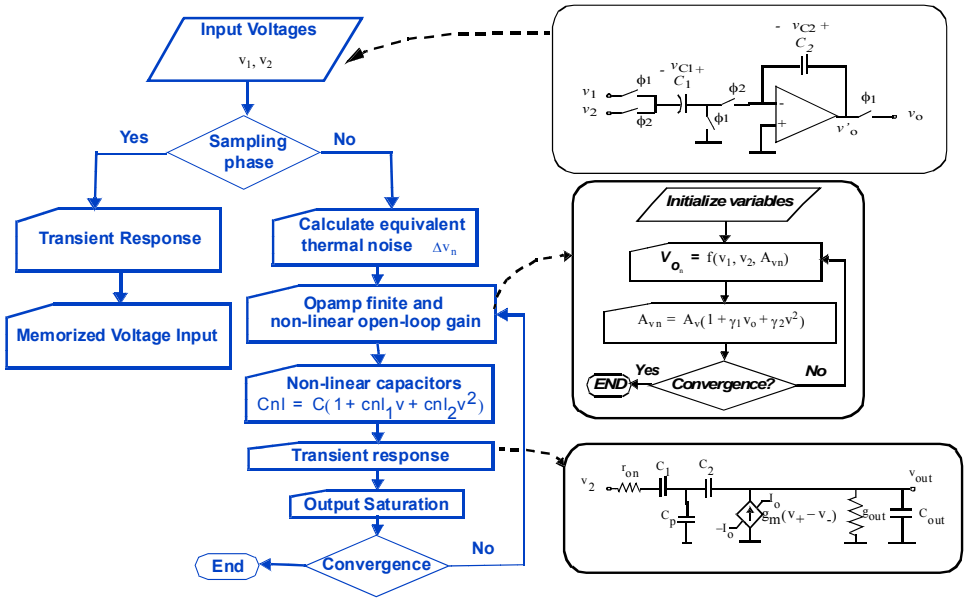


SIMSIDES: Behavioral models included in the toolbox



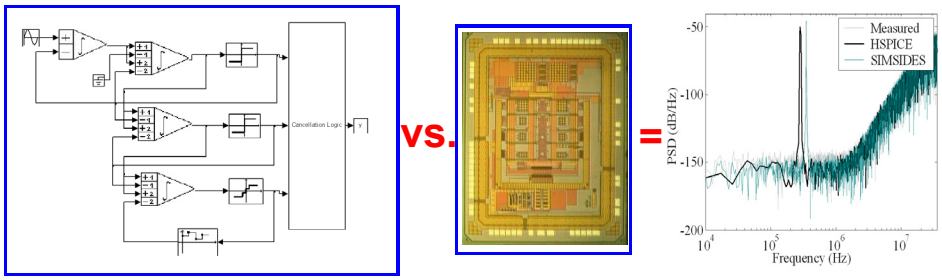
Circuit Tec.	Building Block		Non-ideality
SC	Integrators	Opamps	Finite and non-linear open-loop DC gain
			Incomplete settling error (both clock phases considered)
			Output swing limit
			Thermal noise
		Switches	Thermal noise, switch-on (non-linear) resistance
		Capacitors	Mismatch, non-linearity
	Resonators		Gain and integrator errors
SI	Integrators		Linear and non-linear gain error
			Finite output-input conductance ratio error
			Charge injection error
			Incomplete settling error
	Resonators		Gain and integrator errors
CT	Integrators		Finite and non-linear DC gain
			Non-linear transconductance
			Thermal noise
			Output swing limit
			Transient response
	Resonators		Gain and integrator errors
	Clock		Jitter
	Comparators		Hysteresis and Offset
	Quantizers DACs		Non-linearity, gain error, loop delay, offset

SIMSIDES: Behavioral modeling of SC FE Integrators

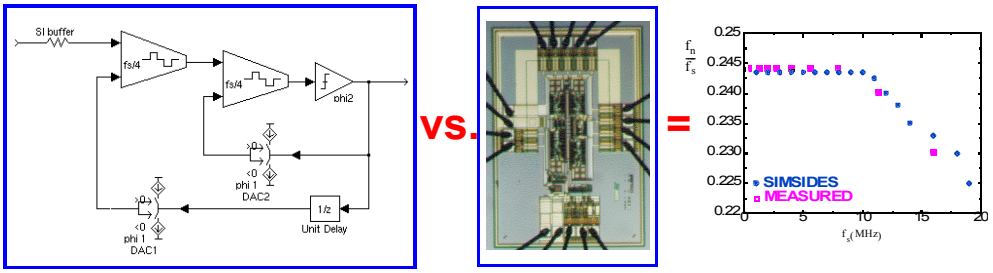


SIMSIDES: Model accuracy

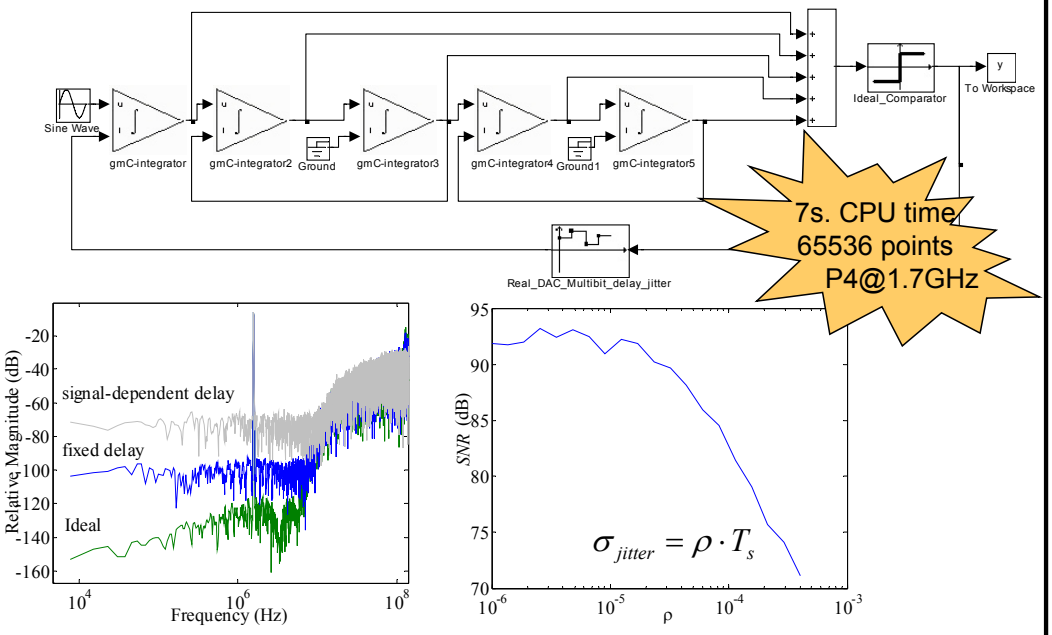
- A 0.25μm CMOS 2-1-1 cascade ΣΔ Modulator for ADSL



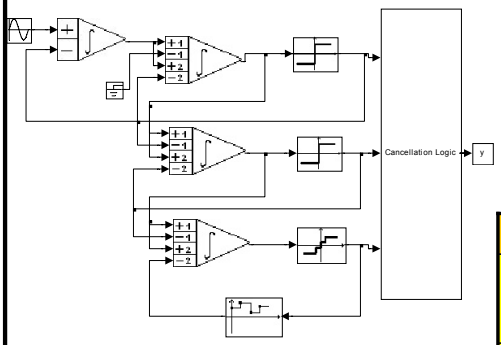
- A 0.8μm CMOS 4th-order bandpass SI ΣΔ Modulator for digital radio



SIMSIDES: Simulating a CT 5th-order LP SL ΣΔM



SIMSIDES: Sizing a SC 2-1-1 cascade ΣΔM



Specifications

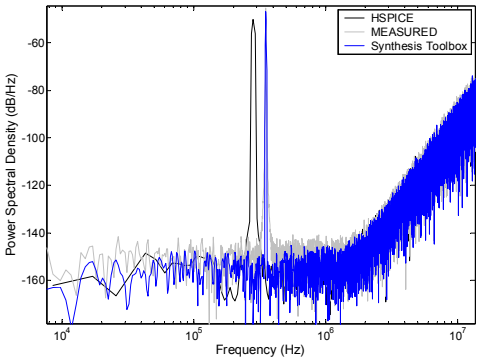
- *13bits@4.4Ms/s*
- Minimum area and power consumption

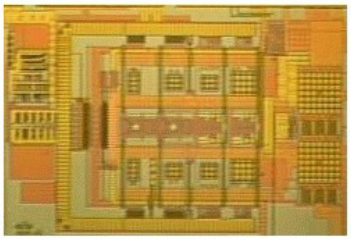
SPECIFICATIONS FOR:		I Int.	II Int.	III Int.	IV Int.
Modulator	Sampling frequency (MHz)	70.4			
	Oversampling ratio	16			
	Reference Voltage (V)	1.5			
Integrators	Feed-back capacitor (pF)	2.64	0.9	0.9	0.45
	Cap. Non-linearity (ppm/V^2)	15			
	Switch on-resistance (Ω)	≤150			
Opamps	DC-gain (dB)	≥81	≥ 65	≥ 54	≥ 54
	Input noise PSD (nV/Hz^{½})	≤1.6	≤ 1.5	≤ 2.9	≤ 2.9
	Transconductance (mA/V)	≥ 6.4	≥ 7	≥ 3.4	≥ 3.4
	Max. Output Current (mA)	≥ 1.5	≥ 2.2	≥ 1.6	≥ 1.6
Comps.	Offset (mV)	≤ 10			
	Hysteresis (mV)	≤ 20			
A/D/A converter	Resolution (bits)	3			
	DAC *INL*	≤ 0.5%*FS*			

Synthesis

All non-idealities
40.8 minutes

SIMSIDES: Sizing a SC 2-1-1 cascade ΣΔM





	Synthesis Toolbox	Measured
Clock frequency (MHz)	70.4	
Digital output rate (Ms/s)	4.4	
Oversampling ratio	16	
Reference voltage (V)	1.5	
Technology	0.25μm CMOS@2.5V	
Power consumption (mW)	-	55
Area (mm²)	-	2.78
Resolution (bits)	13.3	12.7

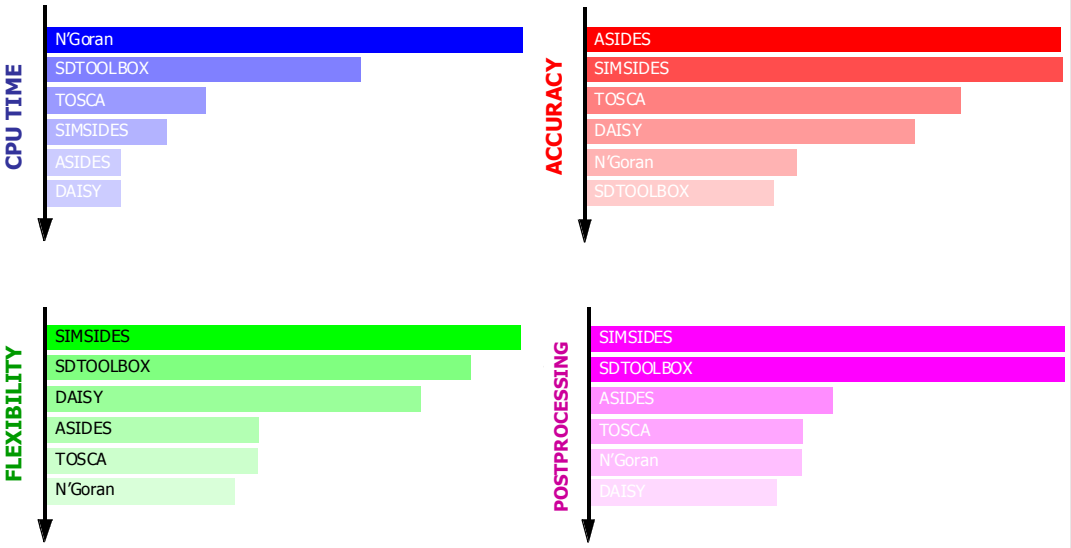
SIMSIDES: Conclusions

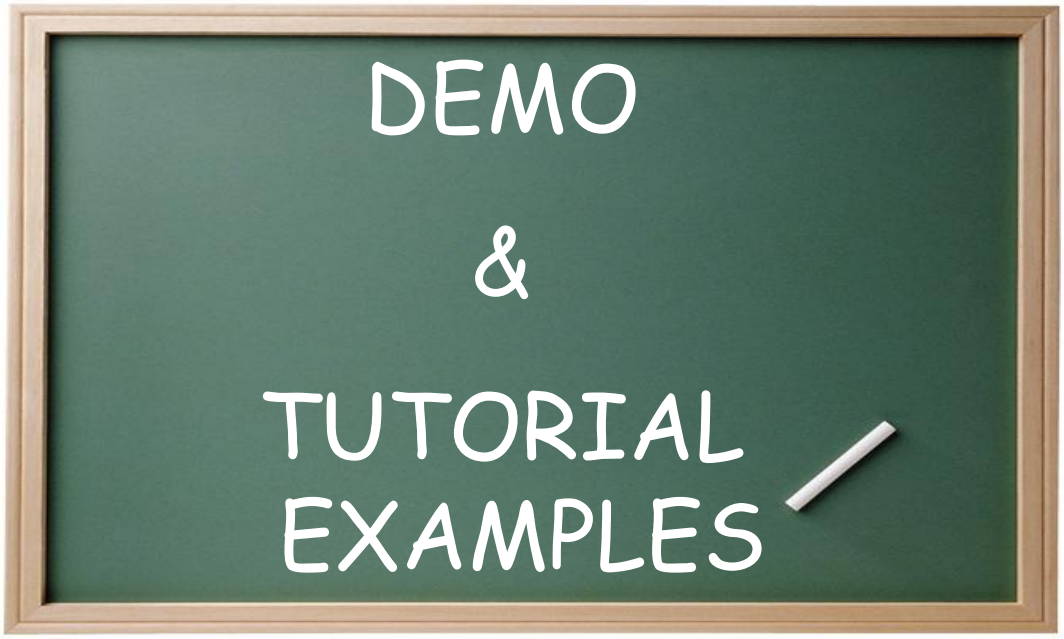
- SIMSIDES is a ΣΔM Synthesis Toolbox in the Matlab/Simulink environment.
  - It allows to efficiently map the modulator specifications into building-block specifications.
  - It deals with the synthesis of ΣΔMs using both DT and CT circuit techniques.
- The implementation platform brings numerous advantages with a relatively low penalty in computation time.

SIMULATOR	CPU-time	Flexibility	User Interface	Accuracy
ASIDES	Secs	Low	Netlist	High
DAISY	Secs	Medium	Graphical	Moderate
SDTOOLBOX (Brigati)	Secs- mins	High	Graphical	Moderate/
SIMSIDES (This work)	Secs	High	Graphical	High

Simulation Approach	CPU Time (s)
Using MATLAB-functions (Brigati, ISCAS99)	415
Using S-functions (This work)	4-5

SIMSIDES: Conclusions





References

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[Giel00] G.G. E. Gielen and R.A. Rutenbar: "Computer-Aided Design of Analog and Mixed-Signal Integrated Circuits", *Proceedings of the IEEE*, Vol. 88, pp. 1825-1852, December 2000.

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