

CMOS Sigma-Delta Converters – From Basics to State-of-the-Art

Circuits and Errors

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OUTLINE



1. Circuits and Errors in DT $\Sigma\Delta$ Modulators

- Errors degrading NTF
- Additive noise sources
- Harmonic distortion
- Case study

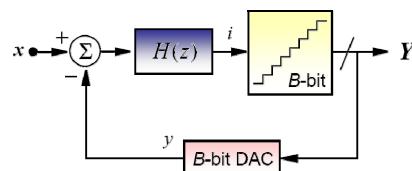
2. Circuits and Errors in CT $\Sigma\Delta$ Modulators

- CT $\Sigma\Delta$ M subcircuits
- Building-block errors
- Architectural timing errors
- Case study

3. Layout & Prototyping

- Layout floorplanning
- Chip package
- Test PCB and Set-up

DT- $\Sigma\Delta$ M: Overview of Non-idealities

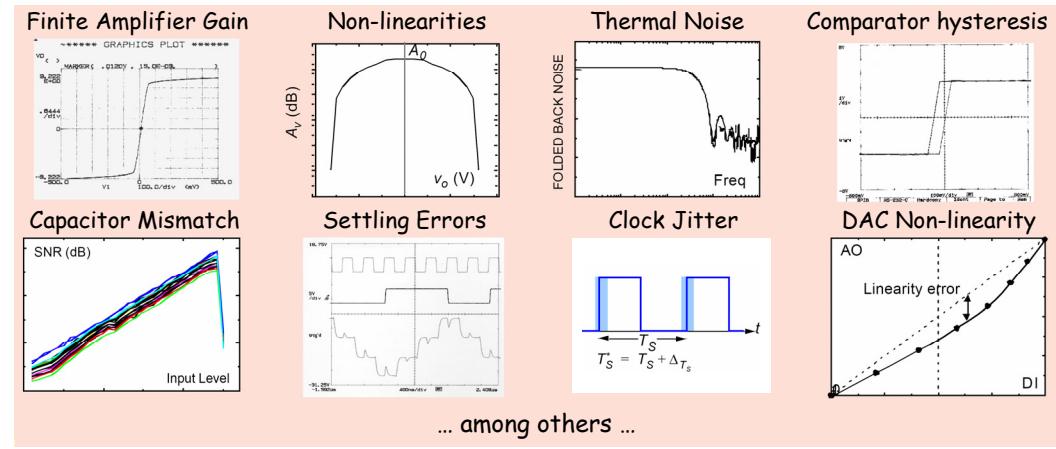


- Ideal In-Band Error Power:

$$P_Q = \frac{1}{12} \left(\frac{\Delta}{2^B - 1} \right)^2 \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

- Actual In-Band Error Power:

$$P_T = P_Q + \Delta P_Q + P_{TH} + P_J + P_{HD} + \dots$$

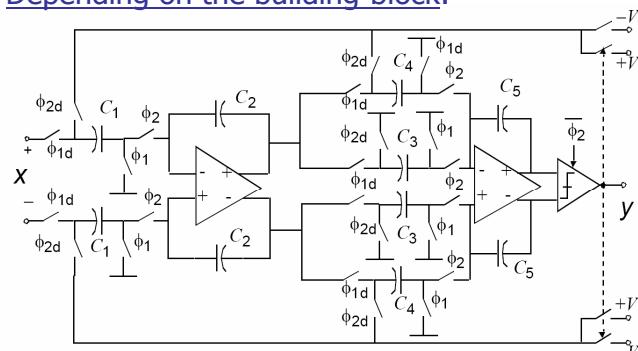


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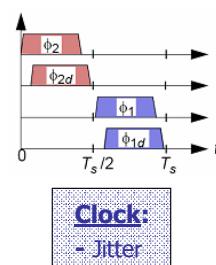
DT- $\Sigma\Delta$ M: Overview of Non-idealities



■ Depending on the building-block:



Fully-diff SC schematic
of a 2nd-order $\Sigma\Delta$ M



Clock:
- Jitter

Amplifiers:

- Output swing
- DC gain
- Dynamic limitations (GB, SR)
- Thermal and 1/f noise
- Gain non-linearity

Capacitors:

- Mismatch
- Non-linearity

Switches:

- Finite on-resistance
- Thermal noise
- Charge injection
- Clock feedthrough
- Non-linearity

Comparators:

- Hysteresis
- Offset

References:

- Thermal and 1/f noise
- Output impedance

Multi-bit ADCs & DACs:

- Gain error
- Offset error
- Non-linearity

DT- $\Sigma\Delta$ Ms: Overview of Non-idealities



- Depending on their effect:

ERRORS DEGRADING NTF

- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
 - ▼ Amplifier GB
 - ▼ Amplifier SR
 - ▼ Switch R_{on}

**Impact depends
on topology**

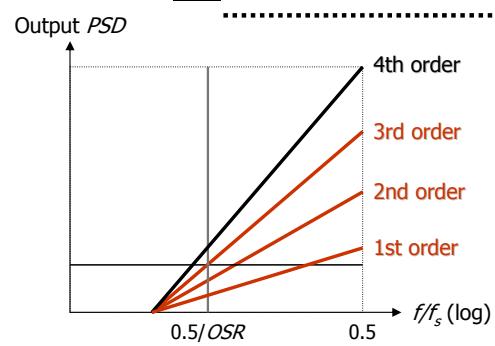
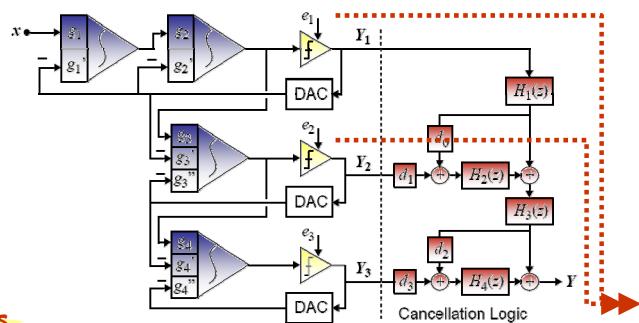
😊 SINGLE-LOOP $\Sigma\Delta$ Ms

→ Low sensitivity

😢 CASCADE $\Sigma\Delta$ Ms

→ **Noise leakages**

Imperfect cancellation of
low-order quantization errors



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DT- $\Sigma\Delta$ Ms: Overview of Non-idealities



- Depending on their effect:

ERRORS DEGRADING NTF

- AMPLIFIER DC GAIN
- CAPACITOR MISMATCH
- INTEGRATOR SETTLING
 - ▼ Amplifier GB
 - ▼ Amplifier SR
 - ▼ Switch R_{on}

**Impact depends
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😊 SINGLE-LOOP $\Sigma\Delta$ Ms

→ Low sensitivity

😢 CASCADE $\Sigma\Delta$ Ms

→ **Noise leakages**

Imperfect cancellation of
low-order quantization errors

MODELED AS ADDITIVE ERRORS

- CIRCUIT NOISE
 - ▼ Thermal noise (switches, opamps, refs)
 - ▼ 1/f noise (opamps, refs)
- CLOCK JITTER
- DISTORTION
 - ▼ Non-linear amplifier gain
 - ▼ Non-linear capacitors
 - ▼ Non-linear settling
 - ▼ Non-linear switches

Front-end
dominates

**Similar impact on
different topologies**

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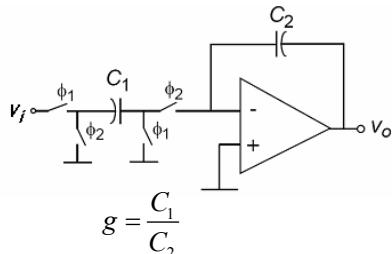
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DT- $\Sigma\Delta$ Ms: Integrator Leakage

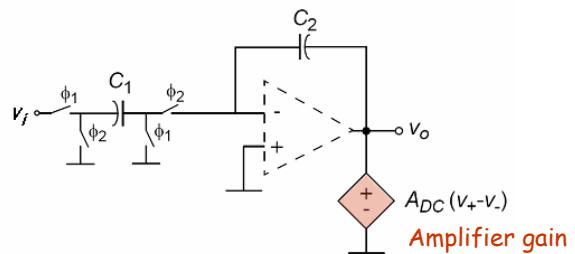


- Effect of amplifier gain on the integrator transfer function:

Ideal SC integrator



SC integrator considering amplifier finite gain



$$H(z) = g \frac{z^{-1}}{1 - z^{-1}}$$

$$H(z) \approx g \frac{z^{-1}}{1 - z^{-1} \left(1 - \frac{g}{A_{DC}} \right)} = g \frac{z^{-1}}{1 - z^{-1} (1 - g\mu)}$$

Shift of the pole from DC ($z=1$)

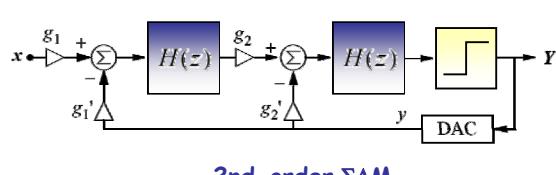
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DT- $\Sigma\Delta$ Ms: Integrator Leakage



- Effect on single-loop $\Sigma\Delta$ Ms:



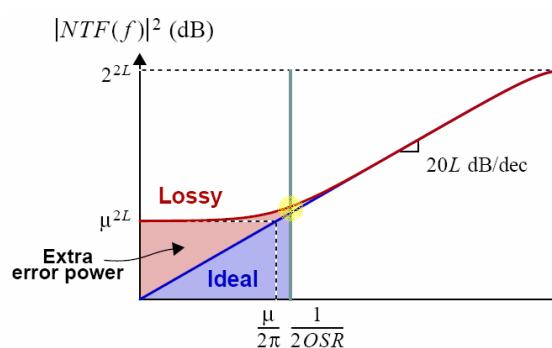
- Ideally: $H(z) = \frac{z^{-1}}{1 - z^{-1}}$

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z)$$

- In practice: $H(z) = \frac{z^{-1}}{1 - z^{-1}(1 - \mu)}$

$$\begin{aligned} NTF(z) &= [1 - z^{-1}(1 - \mu)]^2 \\ &= (1 - z^{-1})^2 + 2\mu z^{-1}(1 - z^{-1}) + \mu^2 z^{-2} \end{aligned}$$

$$P_Q(\mu) \approx \frac{\Delta^2}{12} \left(\frac{\pi^4}{5OSR^5} + \frac{2\mu^2}{3OSR^3} + \frac{\mu^4}{OSR} \right)$$



Lth-order $\Sigma\Delta$:

$$\Delta P_Q \approx \frac{\Delta^2}{12} \frac{L\mu^2 \pi^{2L-2}}{(2L-1)OSR^{(2L-1)}}$$

Quite insensitive to leakages ($\mu^2, L-1$ shaping)



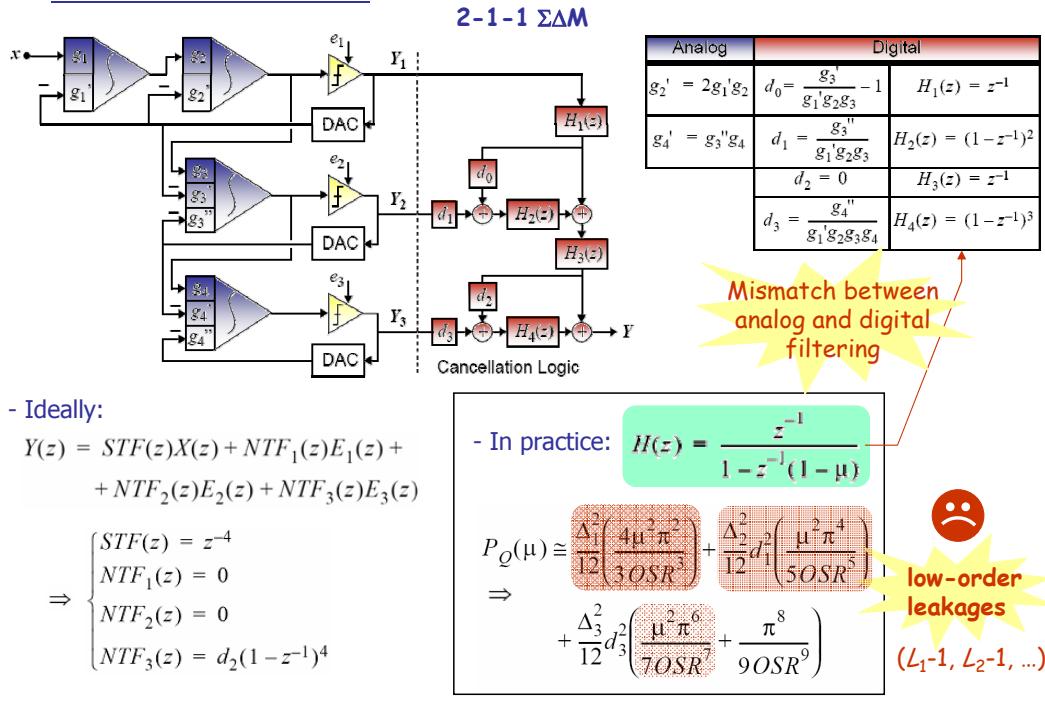
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DT- $\Sigma\Delta$ Ms: Integrator Leakage



Effect on cascade $\Sigma\Delta$ s:



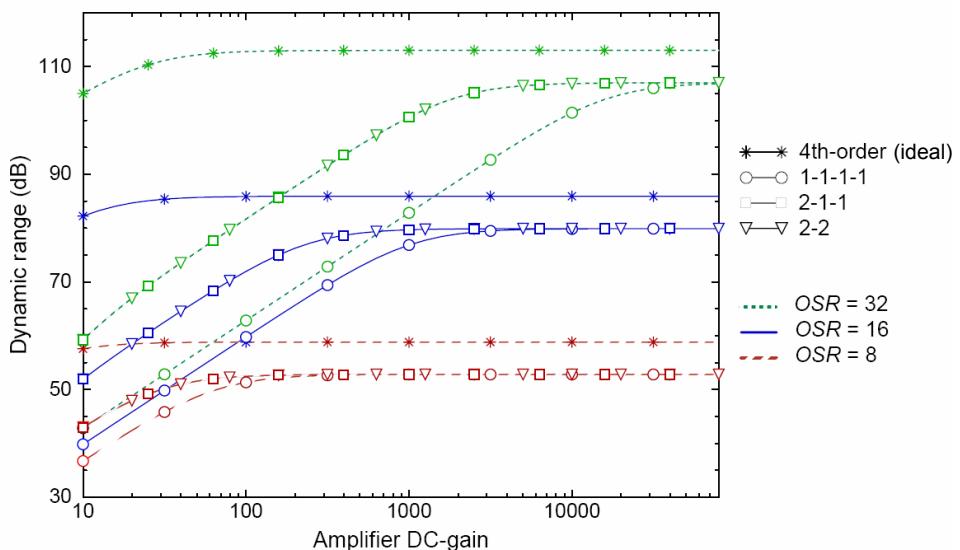
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DT- $\Sigma\Delta$ Ms: Integrator Leakage



Comparison of integrator leakage effect on 4th-order $\Sigma\Delta$ s



→ Sensitivity to integ leakages of cascades increases with OSR and L
→ 1st-stage leakages dominate (L_1-1 shaping)

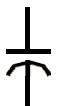
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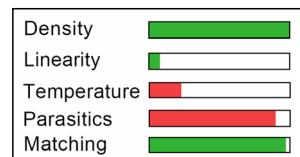
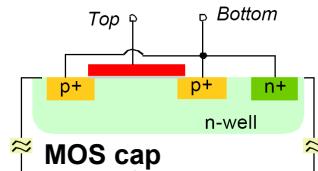
DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



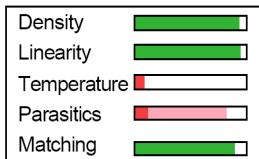
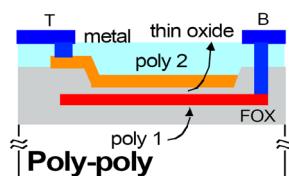
Circuit primitive:



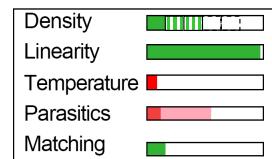
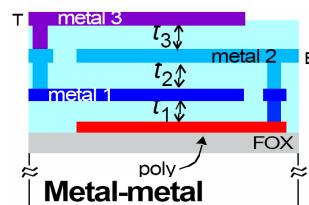
Physical implementations:



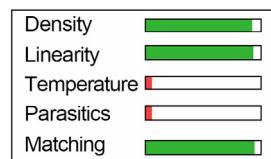
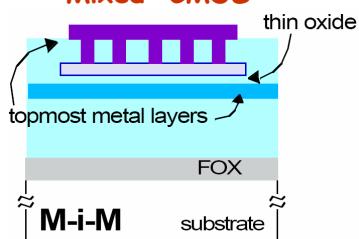
"Analog" CMOS



"Digital" CMOS



"Mixed" CMOS



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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch

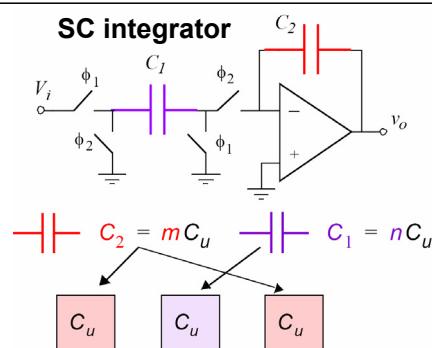
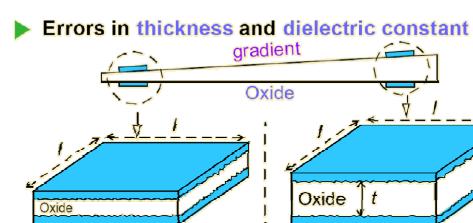
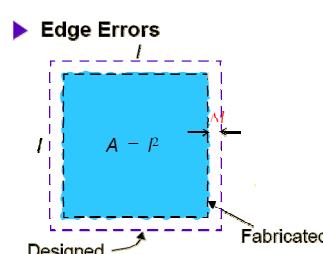


$$C = C_{oxc}^* \cdot (W \cdot L)$$

Actual \neq Ideal

Local and global errors in:

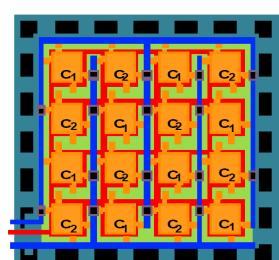
- ▶ Area
- ▶ Capacitance per Unit Area



$$g = \frac{C_1}{C_2} = \frac{nC_u}{mC_u}$$

$$\frac{\sigma_g}{g} = \sqrt{\frac{1}{n} + \frac{1}{m}} \cdot \frac{\sigma_{Cu}}{C_u}$$

$\sigma_C \sim 0.05\% - 0.1\%$
using good quality caps and adequate layout strategies



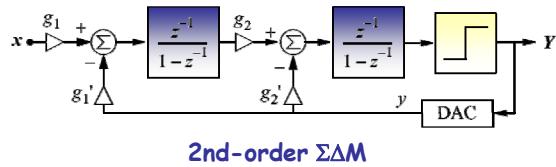
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch

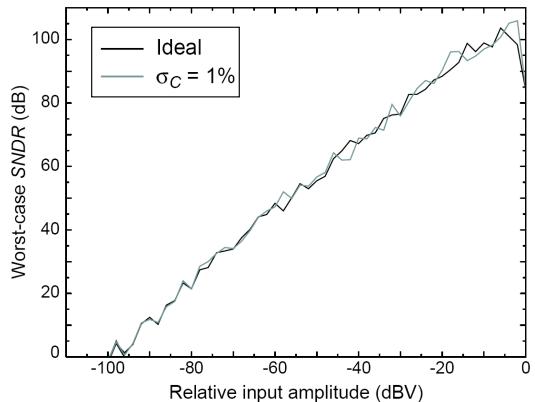
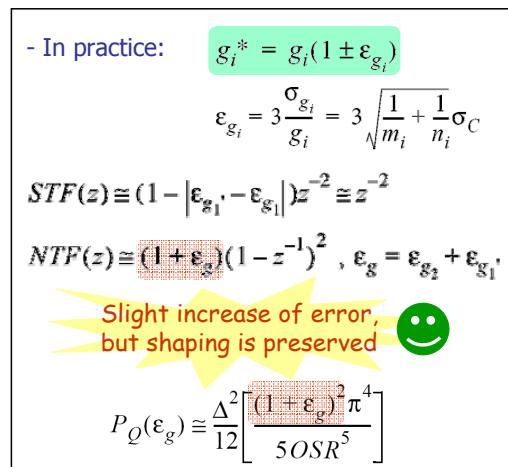


Effect on single-loop $\Sigma\Delta$ Ms:



- Ideally: $g_1 = g_1'$
 $g_2' = 2g_1'g_2$

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2E(z)$$



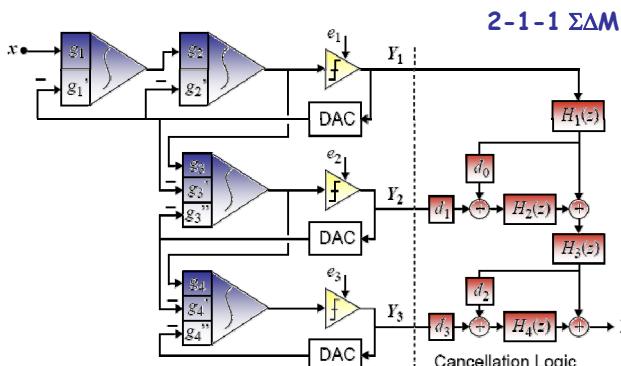
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



Effect on cascade $\Sigma\Delta$ Ms:



Analog	Digital
$g_2' = 2g_1'g_2$	$d_0 = \frac{g_3'}{g_1'g_2g_3} - 1$ $H_1(z) = z^{-1}$
$g_4'' = g_5''g_4$	$d_1 = \frac{g_5''}{g_1'g_2g_3}$ $H_2(z) = (1 - z^{-1})^2$
$d_2 = 0$	$H_3(z) = z^{-1}$
$d_3 = \frac{g_4''}{g_1'g_2g_3g_4}$	$H_4(z) = (1 - z^{-1})^3$

Mismatch between analog and digital coeffs

- Ideally:

$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) + NTF_3(z)E_3(z)$$

$$\Rightarrow \begin{cases} STF(z) = z^{-4} \\ NTF_1(z) = 0 \\ NTF_2(z) = 0 \\ NTF_3(z) = d_2(1 - z^{-1})^4 \end{cases}$$

- In practice: $g_i^* = g_i(1 \pm \varepsilon_{g_i})$

$$STF(z) \approx z^{-4}$$

$$NTF_1(z) \approx d_1 z^{-2} (1 - z^{-1})^2$$

$$NTF_2(z) \approx d_1 \varepsilon_2 z^{-1} (1 - z^{-1})^3$$

$$NTF_3(z) \approx d_2 (1 + \varepsilon_3) (1 - z^{-1})^4$$



low-order leakages
 (L_1, L_2, \dots)

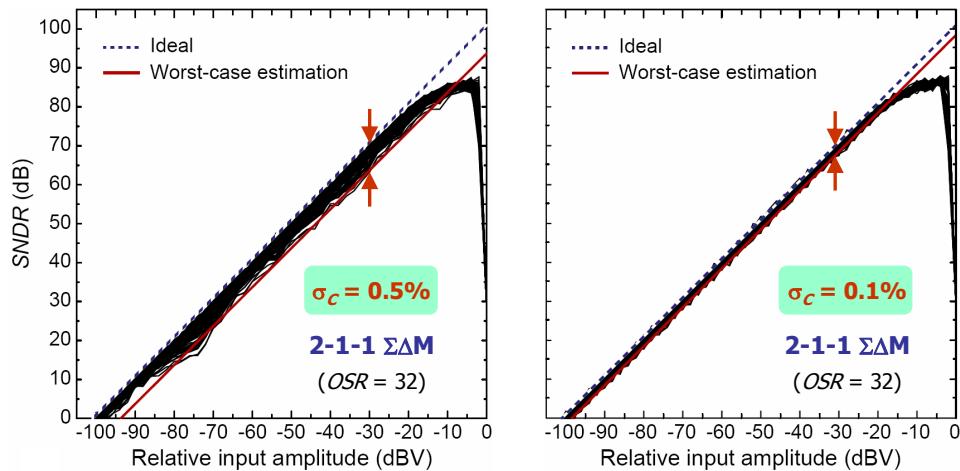
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



■ Effect on cascade $\Sigma\Delta$ Ms:



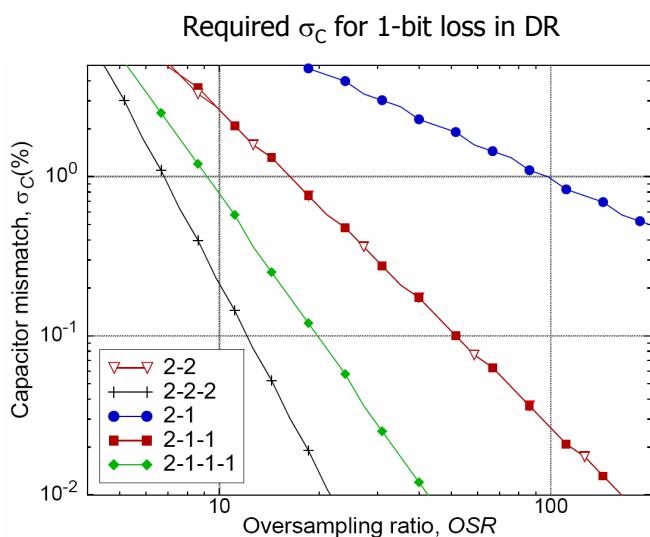
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DT- $\Sigma\Delta$ Ms: Capacitor Mismatch



■ Effect on cascade $\Sigma\Delta$ Ms:



Sensitivity to mismatch rapidly increases with:
 - Oversampling ratio (OSR)
 - Cascade order (L)

1st-stage leakages dominate (L_1 shaping)

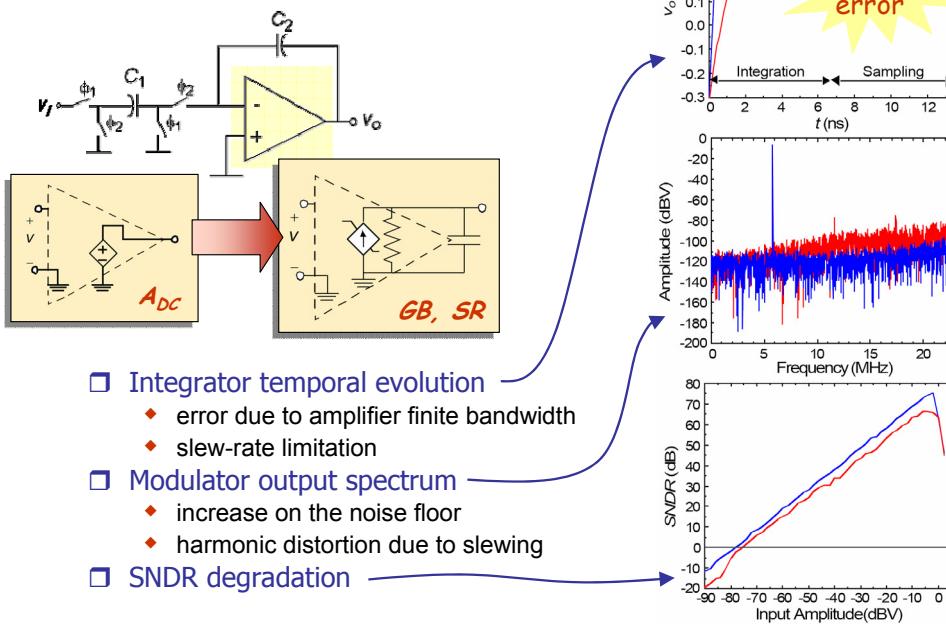
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DT- Σ Ms: Integrator Incomplete Settling



- If only amplifier gain is considered, the relation between v_o and virtual ground is assumed to be independent on time
- In practice, this relation depends is non-linear on time



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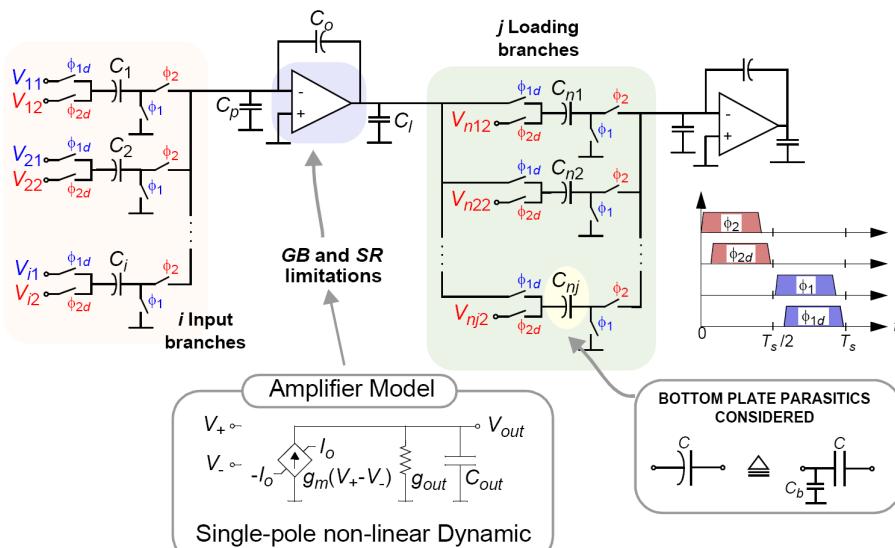
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DT- Σ Ms: Integrator Incomplete Settling



Integrator temporal evolution: [Rio00]

- Both integration and sampling dynamics considered
- 1 pole model + SR limitation in amplifiers
- All parasitic caps taken into account



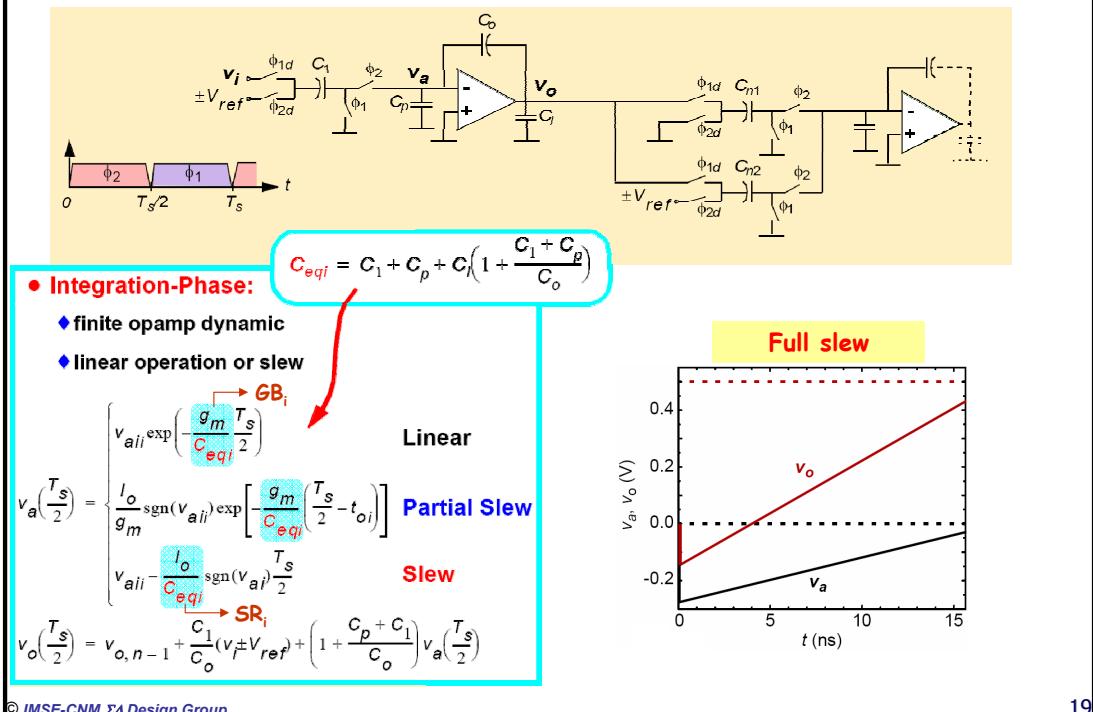
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



Integrator temporal evolution: [Rio00]



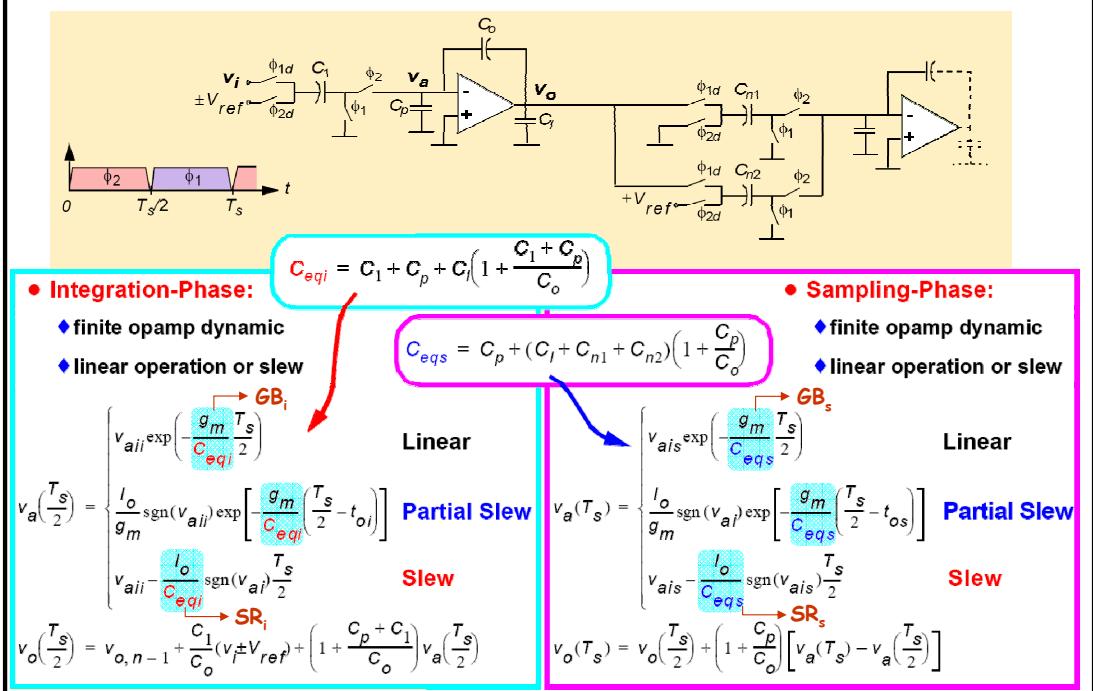
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



Integrator temporal evolution: [Rio00]



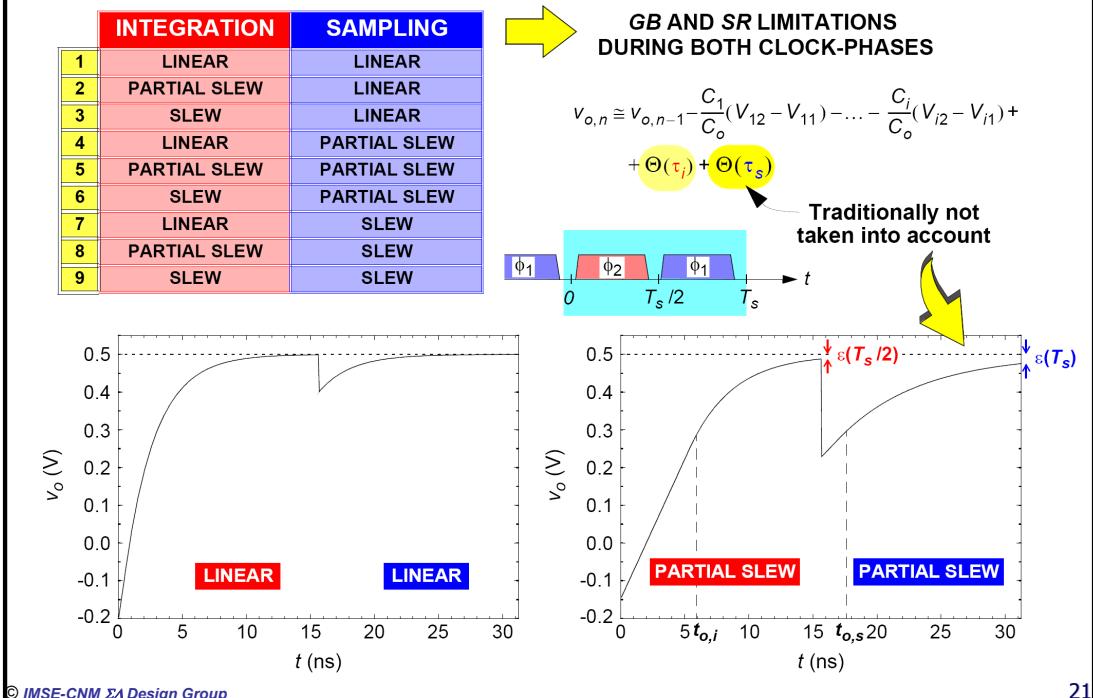
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



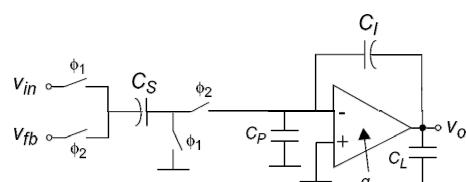
Integrator temporal evolution: [Rio00]



DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



Effect of the amplifier GB:

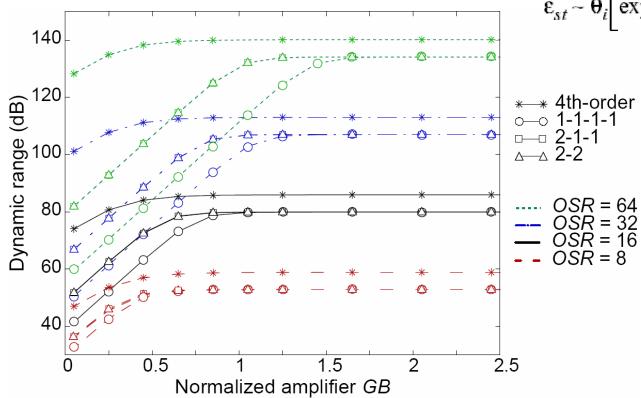


→ If only amplifier GB is considered (assuming no SR limitation)

$$GB_i = \frac{g_m}{C_{eq,i}} \quad GB_s = \frac{g_m}{C_{eq,s}}$$

$$v_o(z) = \frac{C_S}{C_I} \left(1 - \epsilon_{st} \right) \frac{z^{-1}v_{in}(z) - z^{-1/2}v_{fb}(z)}{1 - z^{-1}}$$

$$\epsilon_{st} \sim \theta_i \left[\exp \left(-GB_i \frac{T_s}{2} \right) \right] + \theta_s \left[\exp \left(-GB_s \frac{T_s}{2} \right) \right] + \theta_i \cdot \theta_s$$



- Can be viewed as a systematic error in the integrator weight
- Effect on $\Sigma\Delta$ Ms similar to a mismatch between analog and digital coeffs
- It causes low-order noise leakages in cascade $\Sigma\Delta$ Ms

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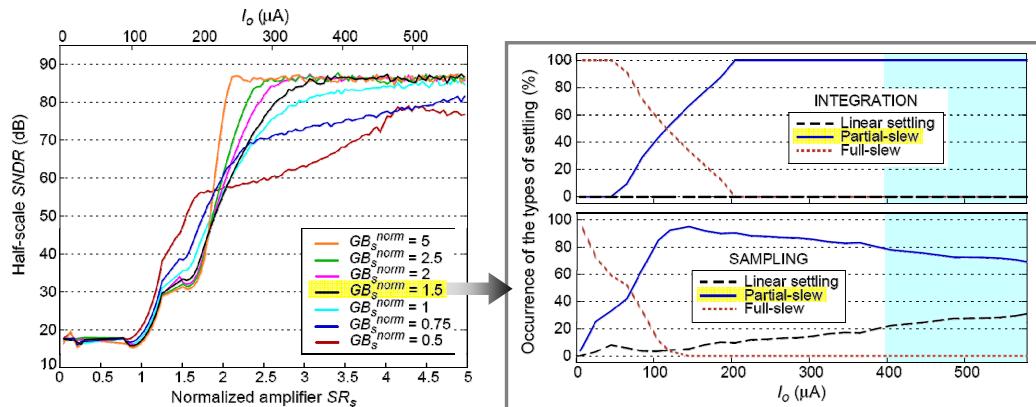
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DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



■ Additional effect of the amplifier SR (+ GB):

- "Dominant" linear dynamics are not mandatory in order to fulfill specs
- SR can trade for GB
- It can be used to optimize the power consumption of amplifiers



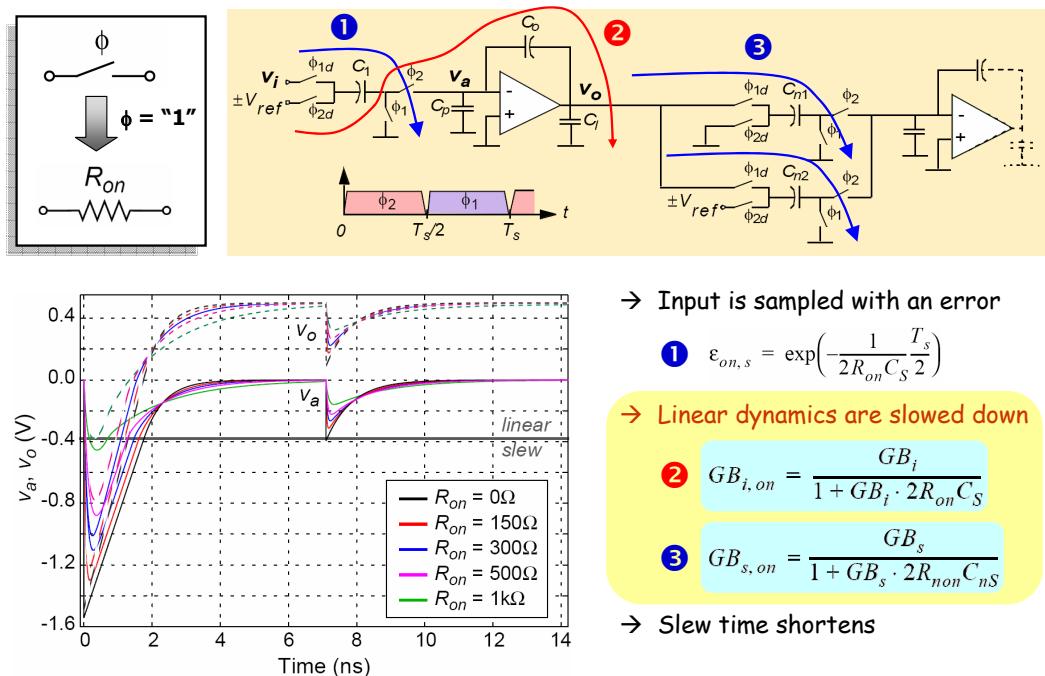
Non-linear dynamics cause distortion!

SR at the front-end integ must be carefully tackled

DT- $\Sigma\Delta$ Ms: Integrator Incomplete Settling



■ Additional effect of the switches Ron (+ GB + SR):

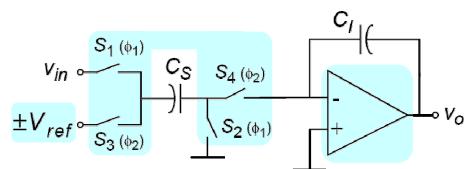
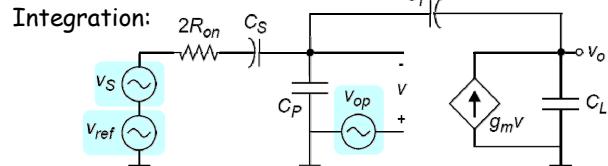
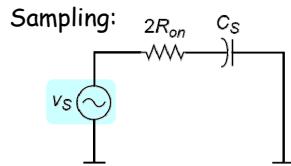


DT-ΣΔMs: Circuit Noise



Main noise sources in SC integrators:

- Switches → Thermal noise
- Amplifiers → Thermal and flicker noise
- References → Thermal and flicker noise



■ Noise contribution of the switches (input-referred):

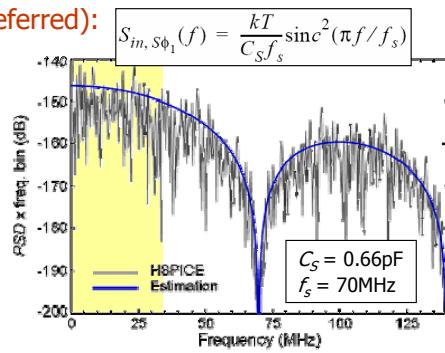
$$\text{Switches for sampling } S_S = 2kT \cdot 2R_{on}$$

$$H_{S\phi_1}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$$

$$BW_{n,S\phi_1} = \int_0^{+\infty} |H_{S\phi_1}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$$

$$S_{in,S\phi_1}(f) \cong \frac{2BW_{n,S\phi_1}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

← Aliased component [Fisc82]



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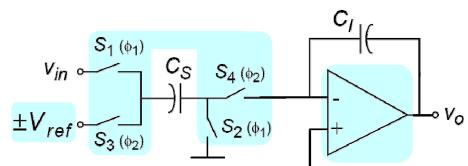
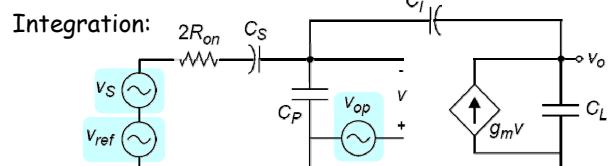
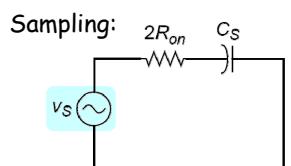
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DT-ΣΔMs: Circuit Noise



Main noise sources in SC integrators:

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■ Noise contribution of the switches (input-referred):

$$\text{Switches for sampling } S_S = 2kT \cdot 2R_{on}$$

$$\text{Switches for integration } S_S = 2kT \cdot 2R_{on}$$

$$H_{S\phi_1}(s) = \frac{1}{1 + s \cdot 2R_{on}C_S}$$

$$H_{S\phi_2}(s) = \frac{1 + s/z_1}{(1 + s/p_1)(1 + s/p_2)} \quad z_1 = \frac{g_m}{C} \quad p_1 \equiv \frac{g_m}{C_{eq,i}} \quad p_2 \equiv \frac{C_{eq,i}}{C} \cdot \frac{1}{2R_{on}C_S}$$

$$BW_{n,S\phi_1} = \int_0^{+\infty} |H_{S\phi_1}(f)|^2 df = \frac{1}{4 \cdot 2R_{on}C_S}$$

$$BW_{n,S\phi_2} = \int_0^{+\infty} |H_{S\phi_2}(f)|^2 df \cong \frac{p_2}{4} \approx \frac{1}{4 \cdot 2R_{on}C_S}$$

$$S_{in,S\phi_1}(f) \cong \frac{2BW_{n,S\phi_1}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

$$S_{in,S\phi_2}(f) \cong \frac{2BW_{n,S\phi_2}}{f_s} \cdot S_S \cong \frac{kT}{C_S f_s}$$

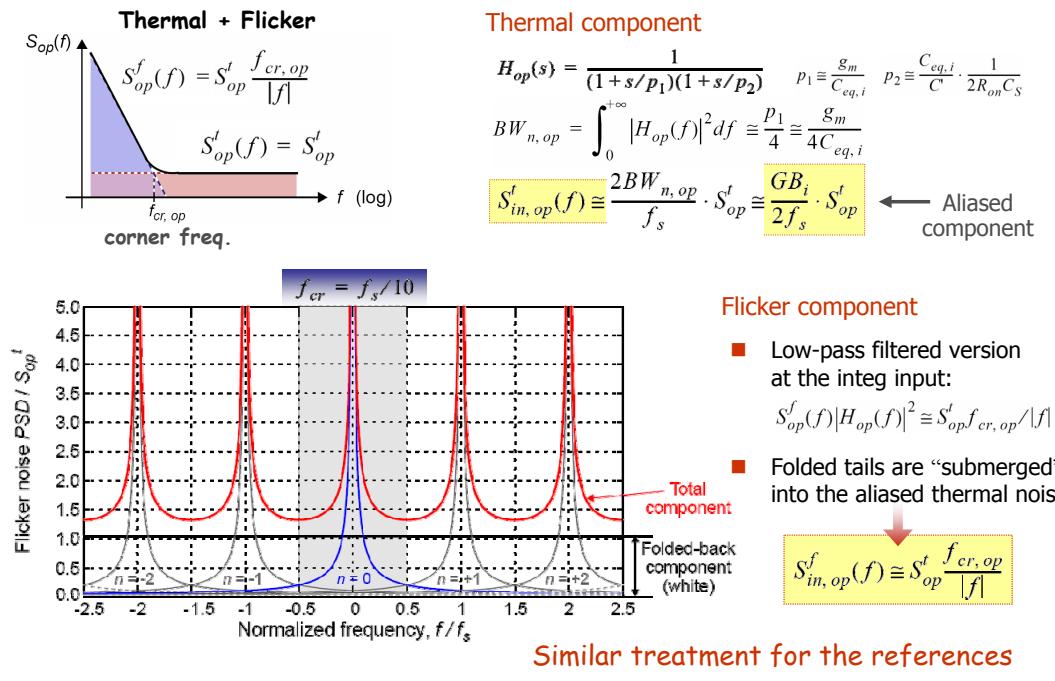
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DT- $\Sigma\Delta$ Ms: Circuit Noise



- Noise contribution of the amplifier (input-referred):



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DT- $\Sigma\Delta$ Ms: Circuit Noise



Total noise PSD for the front-end integ:

$$S_{eq, in}(f) \approx \underbrace{\frac{2kT}{C_S f_s}}_{\text{switches}} + \underbrace{S'_op \left(\frac{GB_i}{2f_s} + \frac{f_{cr, op}}{|f|} \right)}_{\text{amplifier}} + \underbrace{S'^t_{ref} \left(\frac{GB_{ref}}{2f_s} + \frac{f_{cr, ref}}{|f|} \right)}_{\text{references}}$$

Switches:

- kT/C is the ultimate limitation on the converter resolution
- It can only be decreased by increasing C_S and/or f_s (it does not depend on R_{on} !)
- $\times 2$ in fully-diff implementations (3-dB increase, but signal power is 6dB larger!)

Amplifiers & References:

- GBs should be as low as settling errors allow (reduces folding!)
- 1/f contributions decrease with the corner frequency
- Adequate techniques can be applied in low-freq apps: CDS, chopper, ... [Enz96]

$$P_{CN, in} \approx \left[\frac{2kT}{C_S} + S'_op \frac{GB_i}{2} + S'^t_{ref} \frac{GB_{ref}}{2} \right] \frac{1}{OSR} + 2 \ln \left(\frac{f_b}{f_o} \right) (S'_op f_{cr, op} + S'^t_{ref} f_{cr, ref})$$

In-band error power due to circuit noise in the $\Sigma\Delta$ M

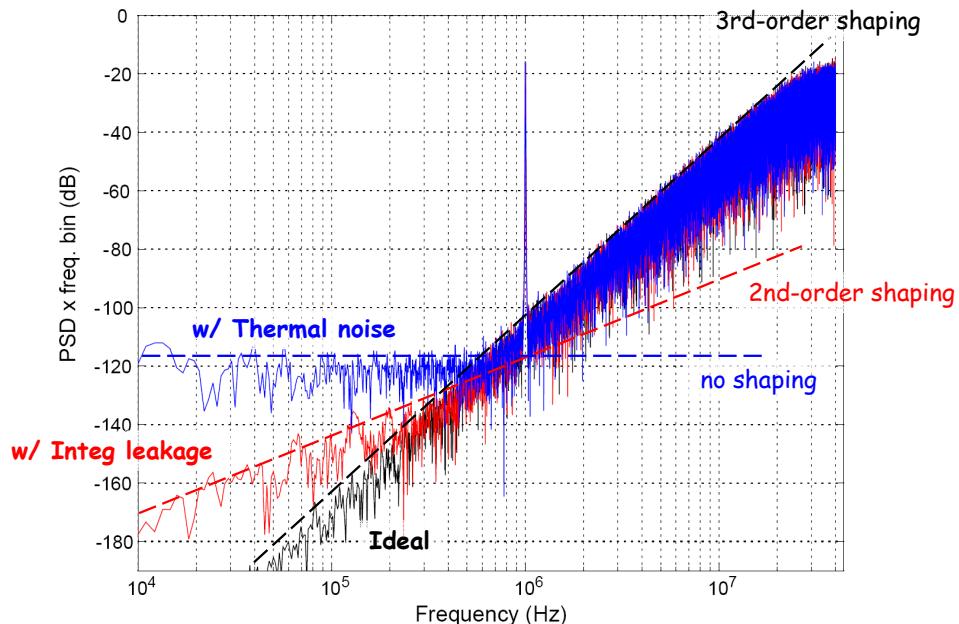
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DT- $\Sigma\Delta$ Ms: Circuit Noise



Effect of noise leakages and thermal noise on a 2-1 cascade



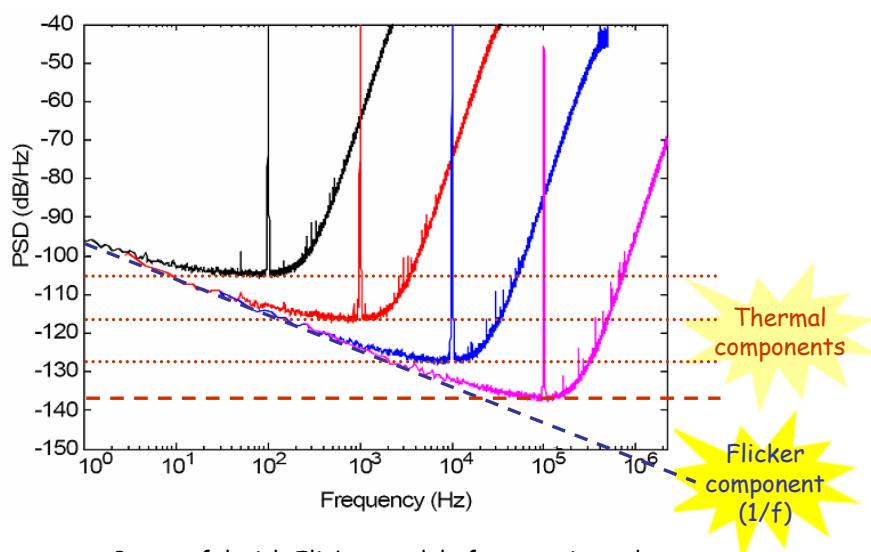
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DT- $\Sigma\Delta$ Ms: Circuit Noise



Effect of 1/f and thermal noise on the spectra of a 4th-order $\Sigma\Delta$ M
(silicon results for several fs)



Be careful with Flicker models for transistors!
Front-end amplifier needed redesign!

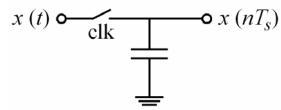
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DT-ΣΔMs: Clock Jitter



- Sampling time uncertainty [Boser88]:



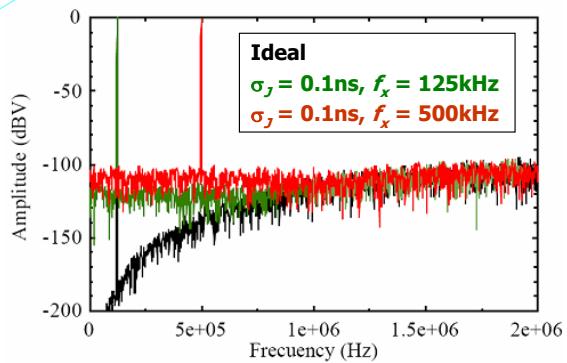
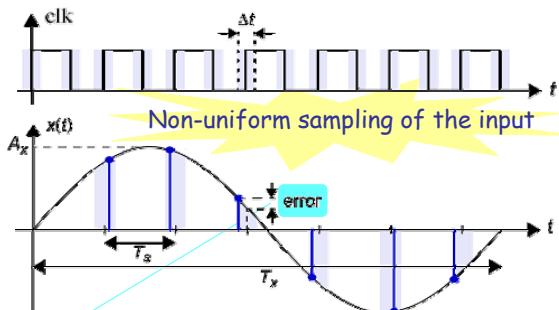
→ If jitter is modeled as random:

$$\text{Jitter distribution: } \sigma_J \quad \text{Sampling period: } \Delta t$$

$$S_J = \frac{A_x^2(2\pi f_x \sigma_J)^2}{2 f_s}$$

$$P_J = \frac{A_x^2(2\pi f_x \sigma_J)^2}{2 OSR}$$

Error is larger, the larger input freq (wideband apps!)



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DT-ΣΔMs: Non-linearity of Capacitors



- In an ideal capacitor: $dq = Cdv$
- In practice: $dq = C(v)dv$, with C being voltage-dependent

$$C(v) = C(1 + a_1 v + a_2 v^2 + \dots)$$

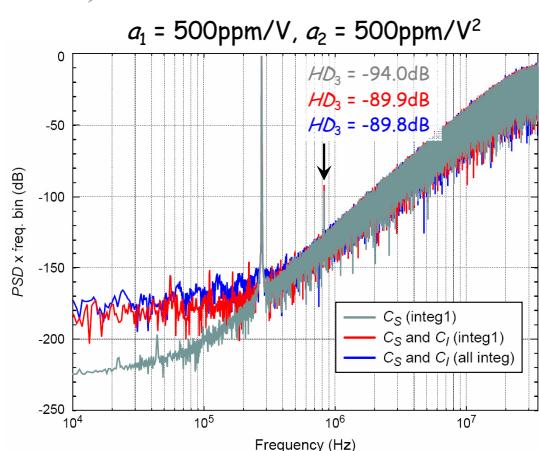
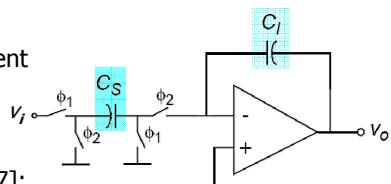
→ Considering the effect of the sampling cap only [Bran97]:

$$v_{o,n} \approx v_{o,n-1} + g_1 v_{in,n-1} \left(1 + \frac{a_1}{2} v_{in,n-1} + \frac{a_2}{3} v_{in,n-1}^2 \right)$$

$$A_2 \approx \frac{1}{2} \left(\frac{a_1}{2} A_x^2 \right) \Rightarrow HD_2 \approx 20 \log_{10} \left(\frac{a_1}{4} A_x \right)$$

$$A_3 \approx \frac{1}{4} \left(\frac{a_2}{3} A_x^3 \right) \Rightarrow HD_3 \approx 20 \log_{10} \left(\frac{a_2}{12} A_x^2 \right)$$

- Even-order distortion cancels w/ fully-diff
- Non-linearity of sampling cap dominates
- Valid for weak non-linearities (MOS caps are very non-linear!)



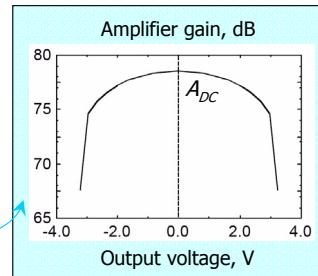
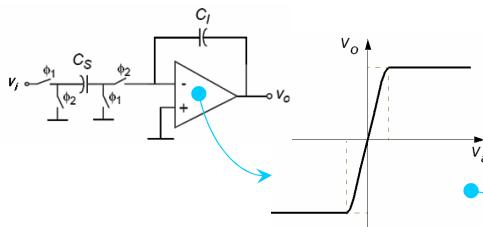
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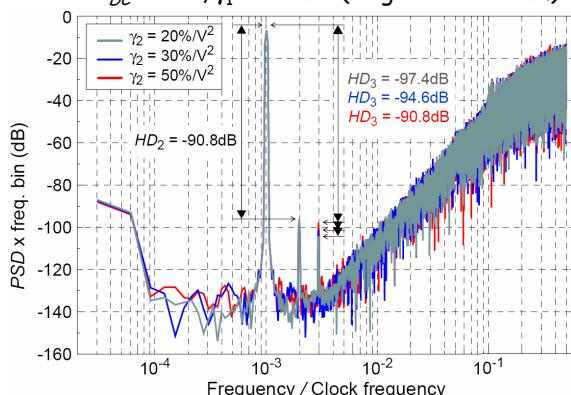
DT- $\Sigma\Delta$ M: Non-linear Amplifier Gain



→ Actual amplifier gain depends on output voltage:



$$A_{DC} = 500, \gamma_1 = 10\%/\text{V} \text{ (single-ended } \Sigma\Delta\text{M)}$$



$$A_{DC}(v_o) = A_{DC}(1 + \gamma_1 v_o + \gamma_2 v_o^2 + \dots)$$

$$HD_2 \cong 20 \log_{10} \left(\frac{\gamma_1 (1+g)}{2} g A_x \right)$$

$$HD_3 \cong 20 \log_{10} \left(\frac{\gamma_2 (1+g)}{4} g^2 A_x^2 \right) \quad [\text{Yin94}]$$

- Increasing A_{DC} helps a lot!
- A_{DC} at the front-end larger than noise leakages require

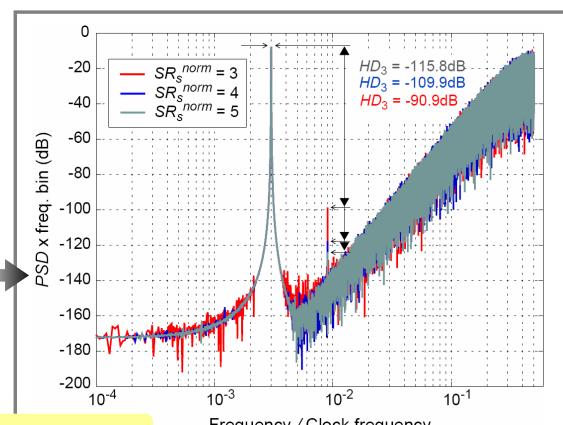
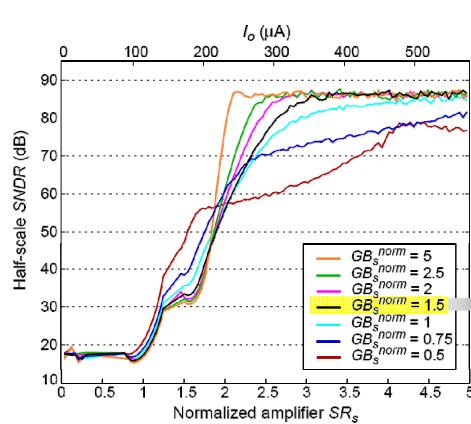
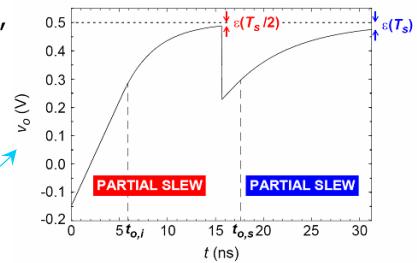
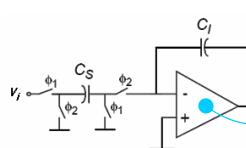
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DT- $\Sigma\Delta$ M: Non-linear Settling



→ SR can trade for GB in the integrator settling, but non-linear dynamics cause distortion:



SR at the front-end larger than settling requires

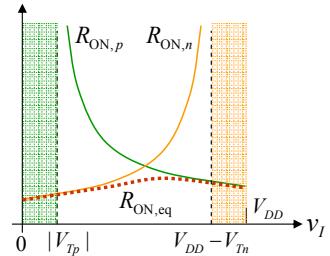
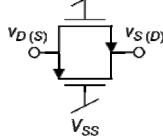
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DT- $\Sigma\Delta$ Ms: Non-linear Switch Resistance



→ Switches exhibit a finite R_{ON} which is also non-linear:

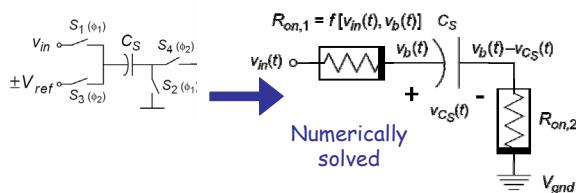


$$R_{ON,n} = \frac{1}{k'_n \left(\frac{W}{L}\right)_n (V_{DD} - v_I - V_{Th})}$$

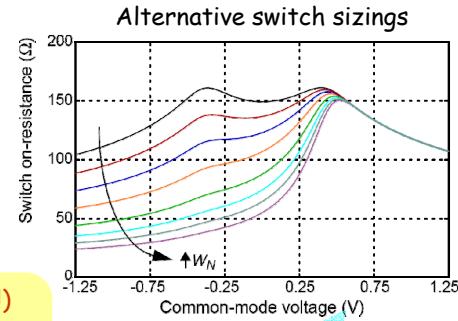
$$R_{ON,p} = \frac{1}{k'_p \left(\frac{W}{L}\right)_p (v_I - |V_{Tp}|)}$$

$$R_{ON,eq} = R_{ON,n} // R_{ON,p}$$

■ Non-linear sampling [Geer02]:



- Distortion is dynamic (increases with input freq!)
- Front-end switch dominates
- R_{ON} at the front-end smaller than settling requires
- Very important in low-voltage!



Most suited sizing depends on parasitics, Vref/Vsupply, ...

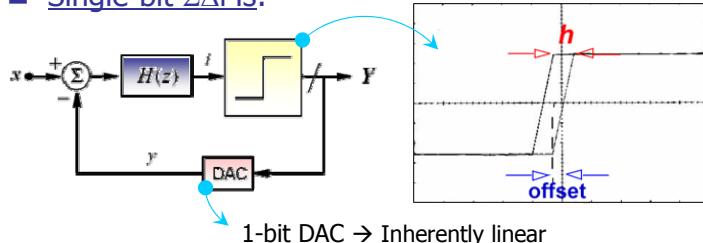
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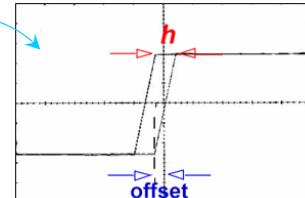
DT- $\Sigma\Delta$ Ms: Comparators and Multi-bit Quantizers



■ Single-bit $\Sigma\Delta$ Ms:



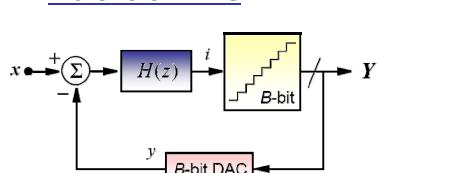
Comparator:



- **Offset** → Attenuated by the integrator DC gain
- **Hysteresis** → Shaped similarly to quantization error [Boser88]

$$P_h = 4h^2 \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

■ Multi-bit $\Sigma\Delta$ Ms:



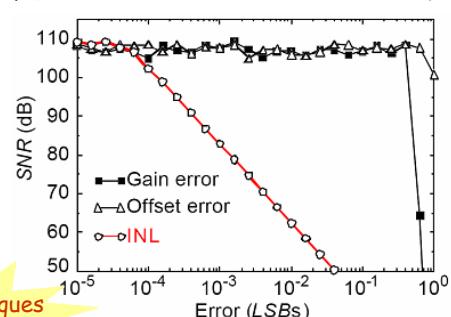
Multi-bit ADC → Errors attenuated/shaped

Multi-bit DAC → Non-linearity directly added to the input!

$$[\text{Mede99}]: \sigma_D^2 = \frac{1}{2} \left(\frac{\Delta}{2^B - 1} \right)^2 \text{INL}_{\text{LSB}}^2$$

DEM techniques
Dual quantization

Effect of DAC errors on a 2nd-order 3-bit $\Sigma\Delta$ M



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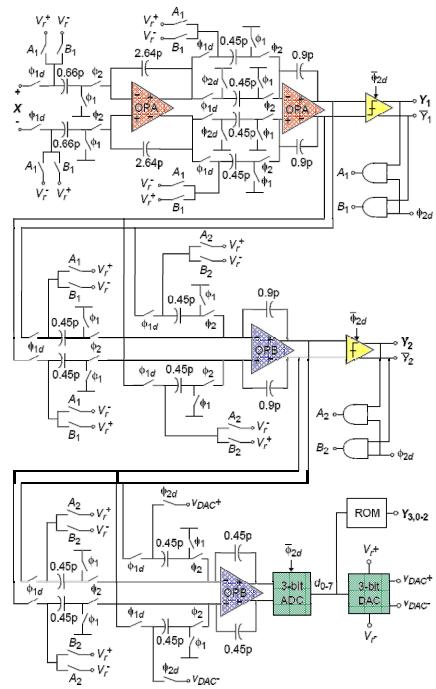
DT- $\Sigma\Delta$ Ms: Case Study



- A case study: A 2.5-V Cascade $\Sigma\Delta$ M in CMOS 0.25um for ADSL/ADSL+

2-1-1 w/ dual quantization

- Two different amplifiers: 2-stage OA in the 1st stage, and 1-stage OA in 2nd and 3rd stages.
- Standard CMOS switches (no clock-boosting).
- Only 2-branch integrators and 2x16 unit capacitors (MiM).
- Comparators: regenerative latch + preamplification stage.
- 3-bit quantizer in the last stage:
 - Resistive-ladder DAC (no calibration).
 - Flash ADC: Static differential input stage + latched comparators.
- Power-down control.



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DT- $\Sigma\Delta$ Ms: Case Study



Blocks Specs

EQUATION DATABASE

	Typical	Worst Case
Quantization noise	-88.1dB	-86.2dB
Id corner analysis:	-90.3dB	
DC gain	16dB	
Cap. mismatch leakage	-95.4dB	-89.4dB
($\sigma_C = 0.05\%$) variation in the 2.5-V supply		
DAC error	-96.4dB	
Thermal noise	-84.8dB	-82.2dB
kT/C noise	-88.1dB	-86.0dB
Amplifier noise	-87.5dB	-84.5dB
Clock jitter	-90.1dB	
In-band error power	-82.3dB	-80.3dB
Dynamic range	82.8dB (13.5bit)	80.8dB (13.1bit)

MODULATOR	Topology	2-1-1(3b)
	Oversampling ratio	16
	Reference voltage	1.5V
	Clock frequency	70.4MHz
	Clock jitter	15ps (0.1%)
FRONT-END INTEGRATOR	Sampling capacitor	0.66pF
	Cap. sigma (MiM, 1pF)	0.05%
	Cap. tolerance	$\pm 20\%$
	Bottom parasitic cap.	1%
	Switch on-resistance	150 Ω
AMPLIFIER	DC gain	3000 (70dB)
	GB (1.5pF)	265MHz
	Slew rate (1.5pF)	800V/ μ s
	Output swing	$\pm 1.8V$
	Input equivalent noise	6nV/sqrt(Hz)
COMPARATORS	Hysteresis	20mV
	Offset	$\pm 10mV$
	Resolution time	3ns
3-bit QUANTIZER	DAC I/NL	0.5%FS

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DT- $\Sigma\Delta$ Ms: Case Study

$$P_{CN} = P_{kT/C} + P_{op} = \frac{4kT}{C_S} \cdot \frac{1}{OSR} + \frac{2\pi \cdot GB_{eff} S_{op}^t}{2OSR}$$

$$GB_{eff} \cong \frac{GB}{1 + GB/f_{on}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_{on}C_S}$$

	Typical	Worst Case
Quantization noise	-88.1dB	-86.2dB
Ideal	-90.3dB	
DC gain leakage	-99.8dB	
Cap. mismatch leakage ($\sigma_C = 0.05\% \mid 0.1\%$)	-95.4dB	-89.4dB
DAC error	-96.4dB	
Thermal noise	-84.8dB	-82.2dB
kT/C noise	-88.1dB	-86.0dB
Amplifier noise	-87.5dB	-84.5dB
Clock jitter	-90.1dB	
In-band error power	-82.3dB	-80.3dB
Dynamic range	82.8dB (13.5bit)	80.8dB (13.1bit)

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	Cap. sigma (MiM, 1pF)	0.05%
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	Bottom parasitic cap.	1%
	Switch on-resistance	150 Ω
AMPLIFIER	DC gain	3000 (70dB)
	GB(1.5pF)	265MHz
	Slew rate (1.5pF)	800V/ μ s
	Output swing	$\pm 1.8V$
	Input equivalent noise	6nV/sqrt(Hz)
COMPARATORS	Hysteresis	20mV
	Offset	$\pm 10mV$
	Resolution time	3ns
3-bit QUANTIZER	DAC I/NL	0.5%FS

DT- $\Sigma\Delta$ Ms: Case Study

Integrator Dynamics

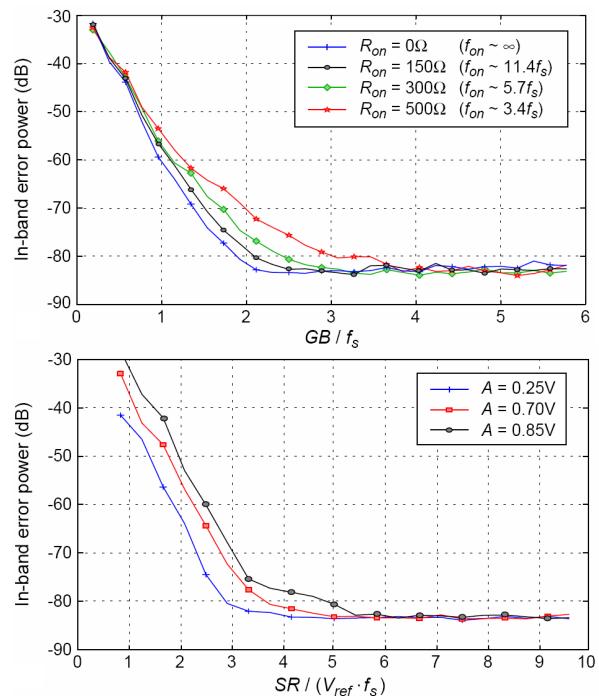
- $GB > 2.5f_s$ is ideally enough to limit settling errors (this architecture w/ $OSR = 16$).
- Switch on-resistance slows down the effective amplifier response:

$$GB_{eff} \cong \frac{GB}{1 + GB/f_{on}} = \frac{GB}{1 + GB \cdot 2\pi \cdot 2R_{on}C_S}$$

$R_{on} \sim 150\Omega$ requires just $GB > 3.2f_s$

Standard switches $GB = 265MHz$
(no clock-boosting) (assuming that 85% of the clock cycle is useful)

- Slew rate must be large enough to let the linear dynamic to correctly settle.
 $SR/(V_{ref} \cdot f_s) = 6.5 \rightarrow SR = 800V/\mu s$
- Partially slew-rate limited operation of the front-end integrator introduces distortion.



DT- Σ M: Case Study

Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)		265MHz	210MHz	
Slew rate (1.5pF)		800V/ μ s	350V/ μ s	
Output swing		\pm 1.80V	\pm 1.60V	
Input equivalent noise	6nV/sqrt(Hz)		50nV/sqrt(Hz)	

OPA

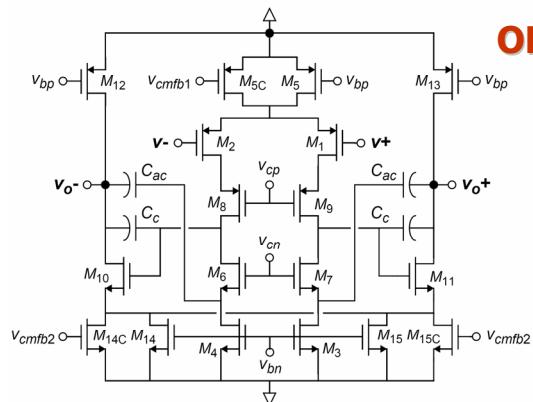
OPB

- SC CMFB nets
- pMOS input scheme
Cancelled body effect
(substrate noise coupling)
- Smaller 1/f noise

DT- Σ M: Case Study

Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)		265MHz	210MHz	
Slew rate (1.5pF)		800V/ μ s	350V/ μ s	
Output swing		\pm 1.80V	\pm 1.60V	
Input equivalent noise	6nV/sqrt(Hz)		50nV/sqrt(Hz)	



OPA 2-stage amplifier Telescopic 1st stage
2-path compensation

	Typical	Worst Case
DC gain	78.6dB	73.5dB
GB (1.5pF)	446.8MHz	331.5MHz
PM (1.5pF)	64.0°	57.9°
SR (1.5pF)	1059V/ μ s	883V/ μ s
Output swing	\pm 2.09V	\pm 1.86V
Input eq. noise	5.1nV/sqrt(Hz)	5.5nV/sqrt(Hz)
Input capacitance	126fF	129fF
Power consumption	17.2mW	19.4mW

DT- $\Sigma\Delta$ Ms: Case Study



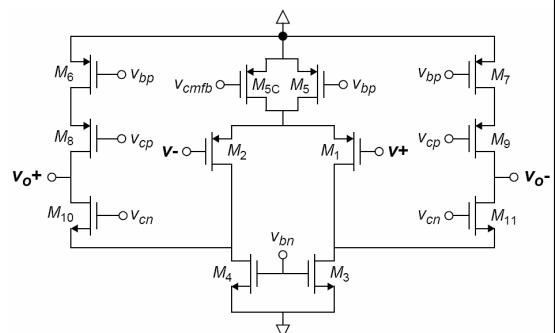
Amplifiers

	INTEG. 1	INTEG. 2	INTEG. 3	INTEG. 4
Unit capacitor	0.66pF	0.45pF	0.45pF	
DC gain	3000 (70dB)		600 (56dB)	
GB (1.5pF)		265MHz	210MHz	
Slew rate (1.5pF)		800V/ μ s	350V/ μ s	
Output swing		$\pm 1.80V$	$\pm 1.60V$	
Input equivalent noise		6nV/sqrt(Hz)	50nV/sqrt(Hz)	

- SC CMFB nets
- pMOS input scheme
- Cancelled body effect
(substrate noise coupling)
- Smaller 1/f noise

OPB folded-cascode amplifier

	Typical	Worst Case
DC gain	58.0dB	56.8dB
GB (1.5pF)	393.5MHz	331.7MHz
PM (1.5pF)	70.3°	67.7°
SR (1.5pF)	377V/ μ s	373V/ μ s
Output swing	$\pm 1.97V$	$\pm 1.72V$
Input eq. noise	4.1nV/sqrt(Hz)	5.1nV/sqrt(Hz)
Input capacitance	300fF	343fF
Power consumption	6.6mW	6.9mW



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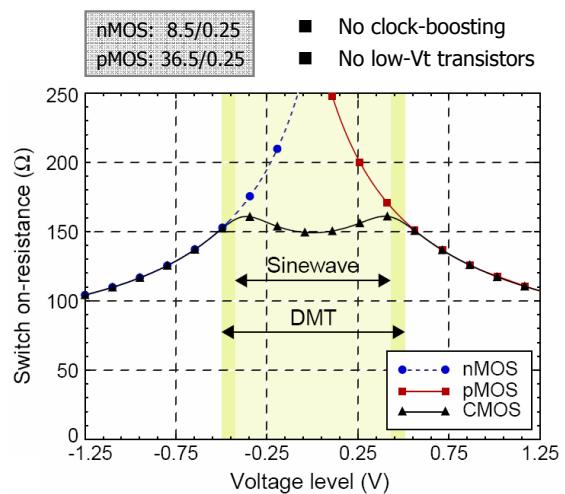
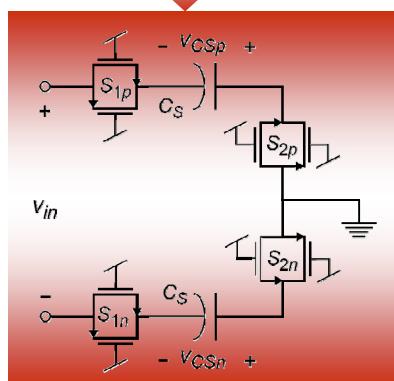
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Switch on-resistance

- Slow-down of the integrators dynamics
- Incomplete sampling (RC time constant)
- Dynamic distortion (front-end integrator)

Standard CMOS switches



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DT- $\Sigma\Delta$ Ms: Case Study

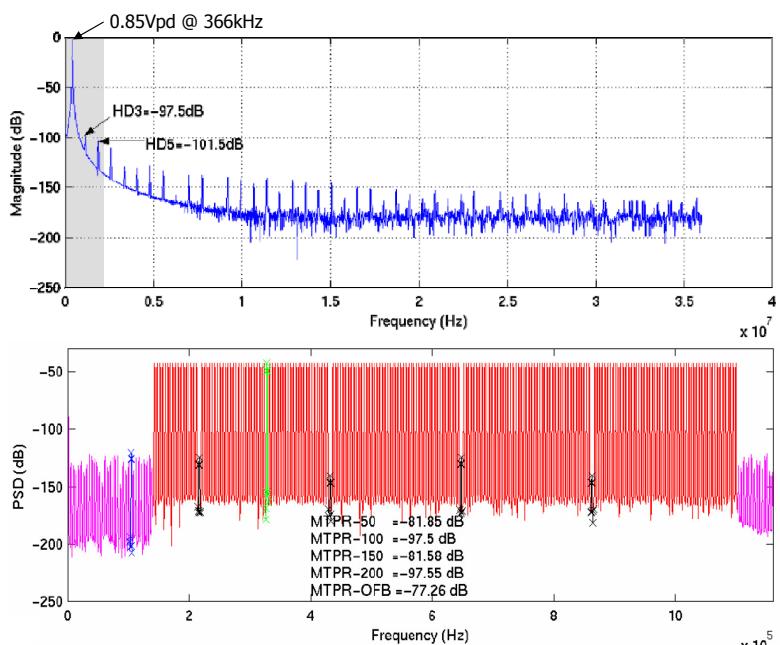
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CENTRO INVESTIGACIONES DE MICROELECTRÓNICA

Switch on-resistance

Dynamic distortion
evaluated through
electrical simulation

■ Sinewave input

THD < -96dB



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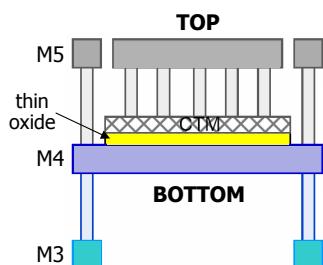
DT- $\Sigma\Delta$ Ms: Case Study

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MiM capacitors

CMOS tech with
mixed-signal facilities

Thin oxide between
metal 4 and metal 5



Cap. matching	0.05% (1pF)
Bottom plate parasitic	1%
Cap. spread	$\pm 20\%$

→ Very good matching (0.1% assumed for 6- σ design)

→ Helps to limit the capacitive load to integrators

→ Integrators weights:

- Front-end integ, 0.66pF: $27\mu\text{m} \times 27\mu\text{m}$
- Remaining integs, 0.45pF: $22\mu\text{m} \times 22\mu\text{m}$

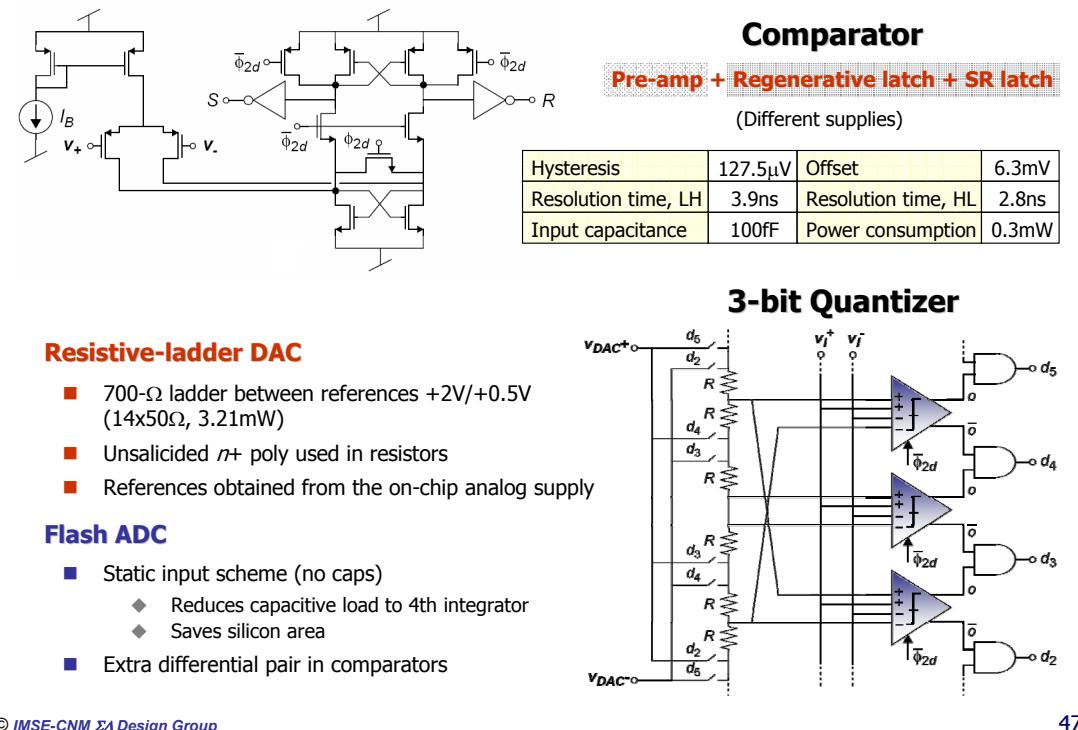
→ Also MiM caps in OPA, in the SC CMFB nets, and in the anti-aliasing filter

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DT- $\Sigma\Delta$ Ms: Case Study

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CENTRO INVESTIGACIONES Y ESTUDIOS AVANZADOS



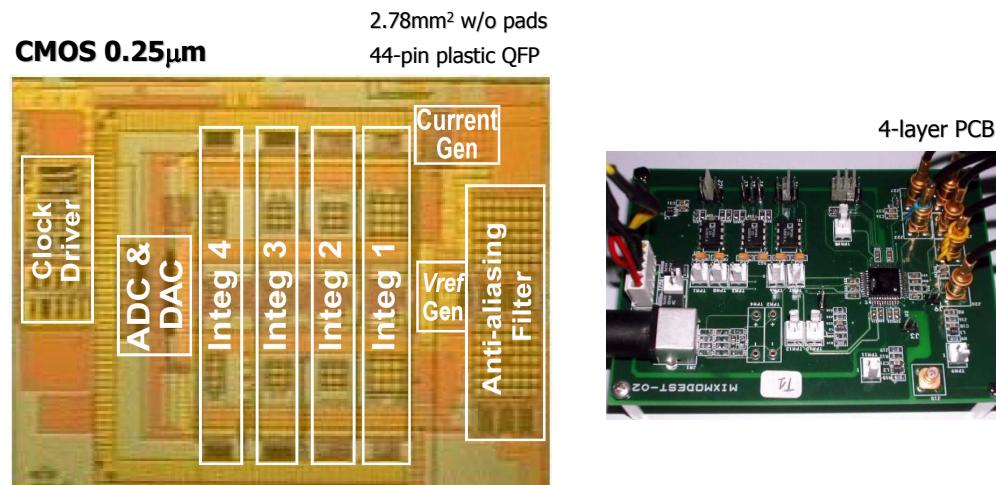
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DT- $\Sigma\Delta$ Ms: Case Study

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CENTRO INVESTIGACIONES Y ESTUDIOS AVANZADOS

Layout & Prototyping



- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

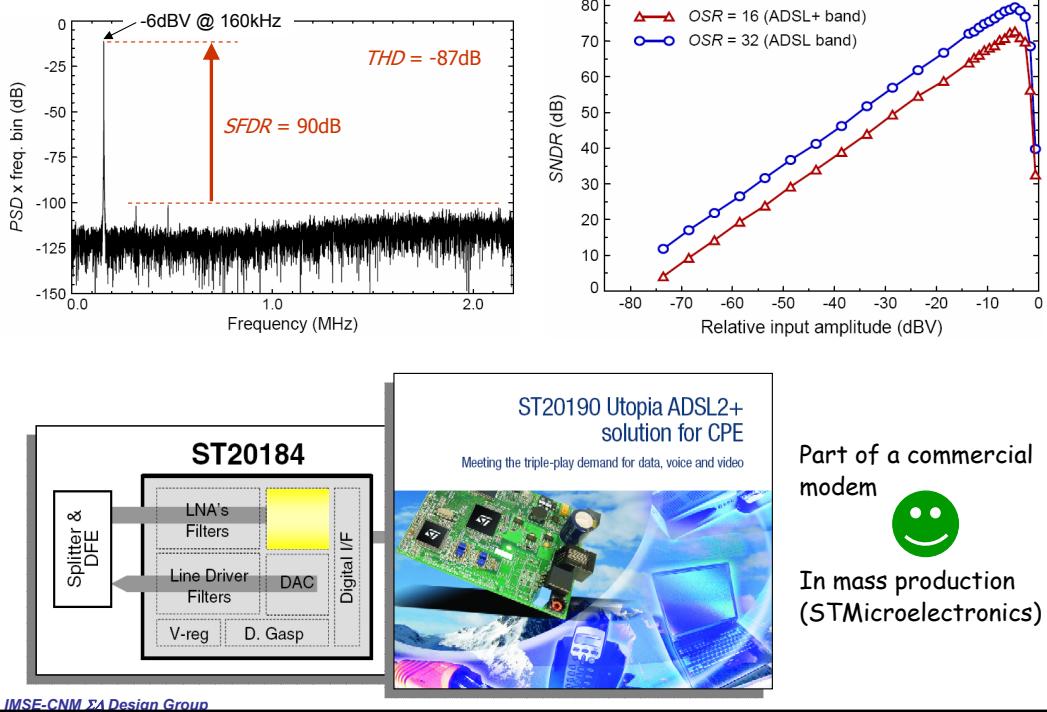
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DT- $\Sigma\Delta$ M: Case Study

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CENTRE INVESTIGACIÓ EN MICROELECTRÒNICA

Experimental results



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CT- $\Sigma\Delta$ M : Overview of CT- $\Sigma\Delta$ M Non-idealities

CNM

CT- $\Sigma\Delta$ M Non-Idealities

Building-block Errors

- Opamp finite (non-linear) DC gain
- Integrator transient response
- Element tolerances
- Time-constant error
- Non-linearity (Front-end V-I and DAC)
- Noise

Architectural Timing Errors

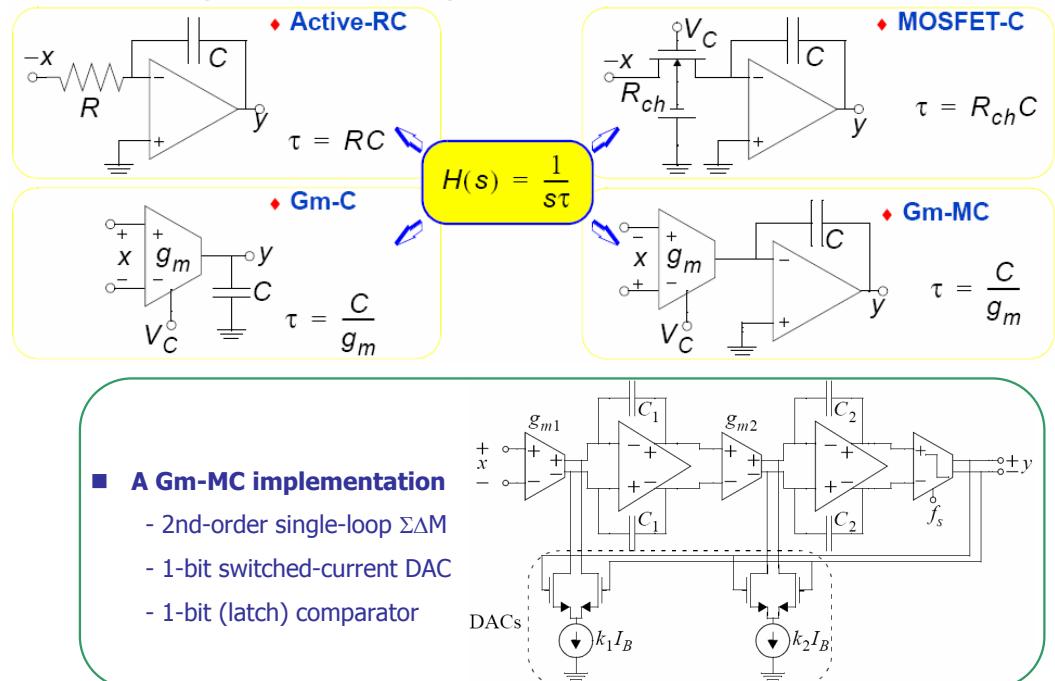
- Quantizer metastability
- Excess loop delay
- Clock jitter

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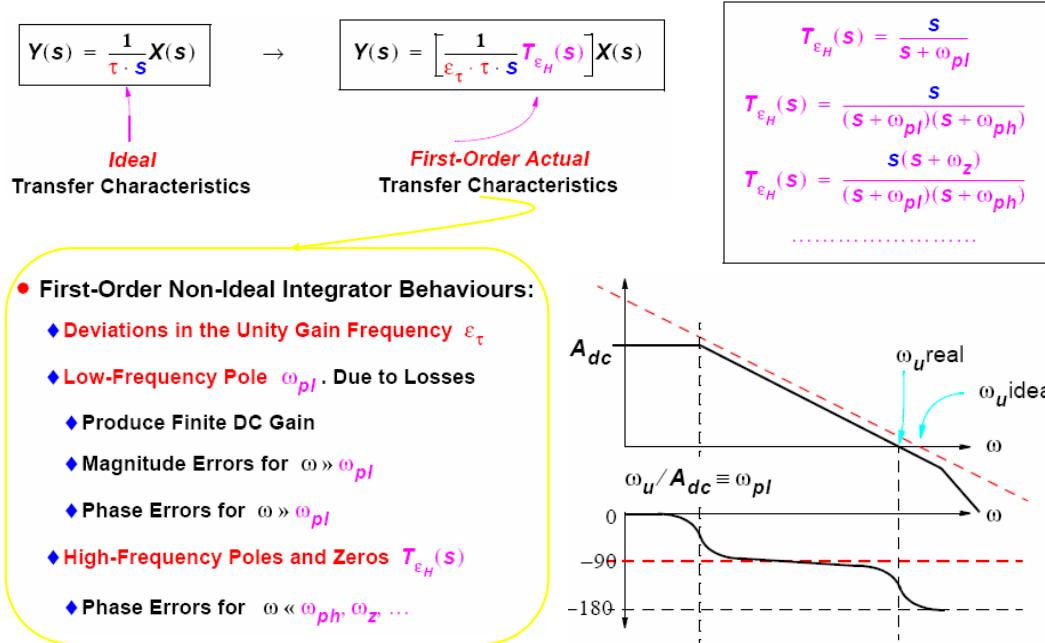
CT- $\Sigma\Delta$ Ms: Basic building blocks

□ Basic building blocks – CT Integrators



CT- $\Sigma\Delta$ Ms: Non-ideal Integrator Transfer Function

□ Integrator Transfer Function (ITF) degraded by circuit non-idealities



CT- $\Sigma\Delta$ M: Effect of finite DC gain error



Opamp finite DC gain (I)

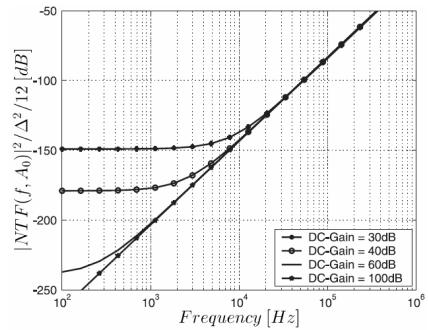
RC	MOSFET-C	Gm-C	Gm-MC
$\omega_{pl} < \frac{G}{C \cdot A_0} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{G_{ch}}{C \cdot A_0} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{\omega_u G_{go}}{\varepsilon_T G_m} = \frac{\omega_u}{A_0}$	$\omega_{pl} < \frac{G_{go}}{C \cdot A_0} = \frac{\omega_u G_{go}}{A_0 G_m} = \frac{\omega_u}{A_0}$

RC integrators [Gerd03]

$$\text{ITF}(s) = \frac{\alpha/\tau}{s + \gamma} \quad \alpha = \frac{A_0}{1 + A_0} \quad \gamma = \frac{1/\tau}{1 + A_0}$$

- Same IBN degradation as in SC $\Sigma\Delta$ Ms ($\tau = 1/f_s$)

$$P_{A_0} = \frac{\Delta^2}{12k_1^2 k_q^2} \left[\frac{1}{A_0^{2L} M} + \sum_{m=1}^L \frac{\pi^{2L} L(L-1)\dots(L-m+1)}{(2m+1)M^{2L+1} A_0^{2(L-m)} m!} \right]$$



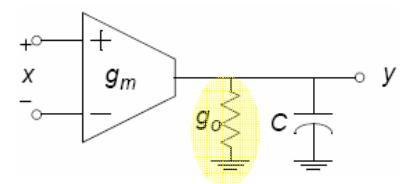
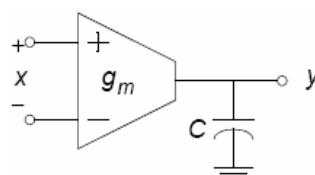
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CT- $\Sigma\Delta$ M: Effect of finite DC gain error



Opamp finite DC gain (II) – Gm-C integrators

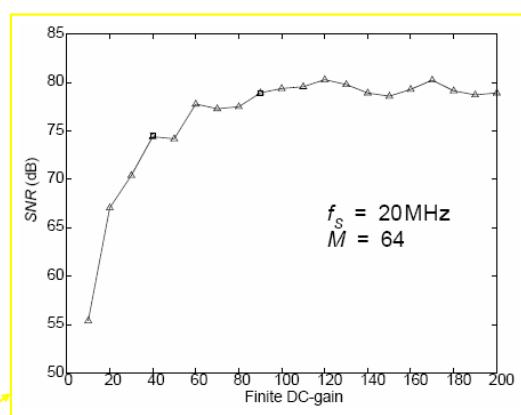


Power Spectral Density of an L th-order $\Sigma\Delta$ M

$$S_Q(f) = \left[\sum_{i=0}^{L-1} \binom{L}{i} \left(\frac{j\omega}{\omega_{pl}} \right)^i \right]^2 \cdot \frac{\Delta^2}{12 \cdot A_{dc}^{2L} \cdot f_s}$$

Relative increase of P_Q in a 2nd-order $\Sigma\Delta$ M

$$\frac{P_Q}{P_Q|_{A_{dc} \rightarrow \infty}} \approx \frac{5}{\pi^2} \left(\frac{M}{A_{dc}} \right)^4 + \frac{10}{3\pi^2} \left(\frac{M}{A_{dc}} \right)^2 + 1$$



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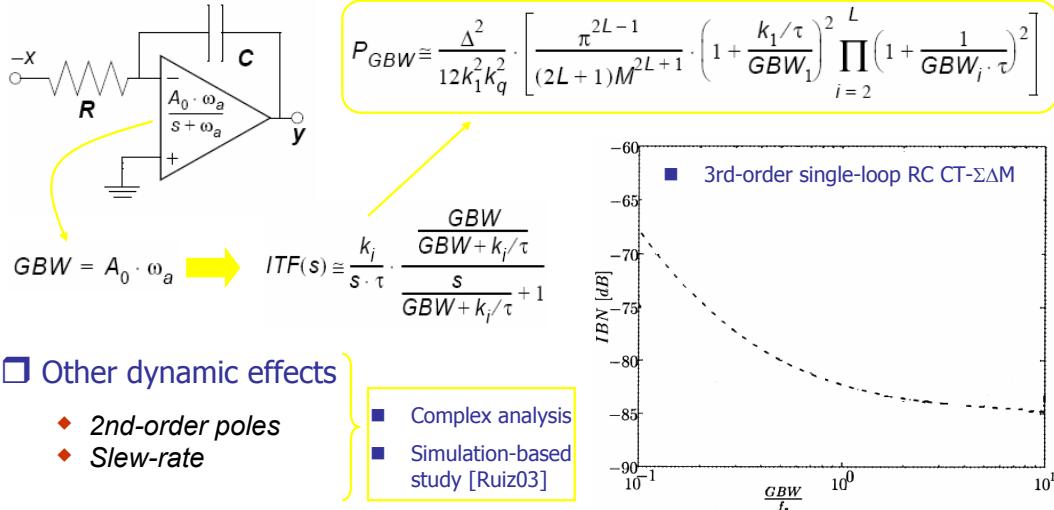
CT- $\Sigma\Delta$ Ms: Integrator transient response



☐ Integrator transient response (I)

- ♦ Less critical than in DT $\Sigma\Delta$ Ms
- ♦ Need to be taken into account, specially in broadband applications

☐ Influence of GBW [Geff03]



☐ Other dynamic effects

- ♦ 2nd-order poles
- ♦ Slew-rate

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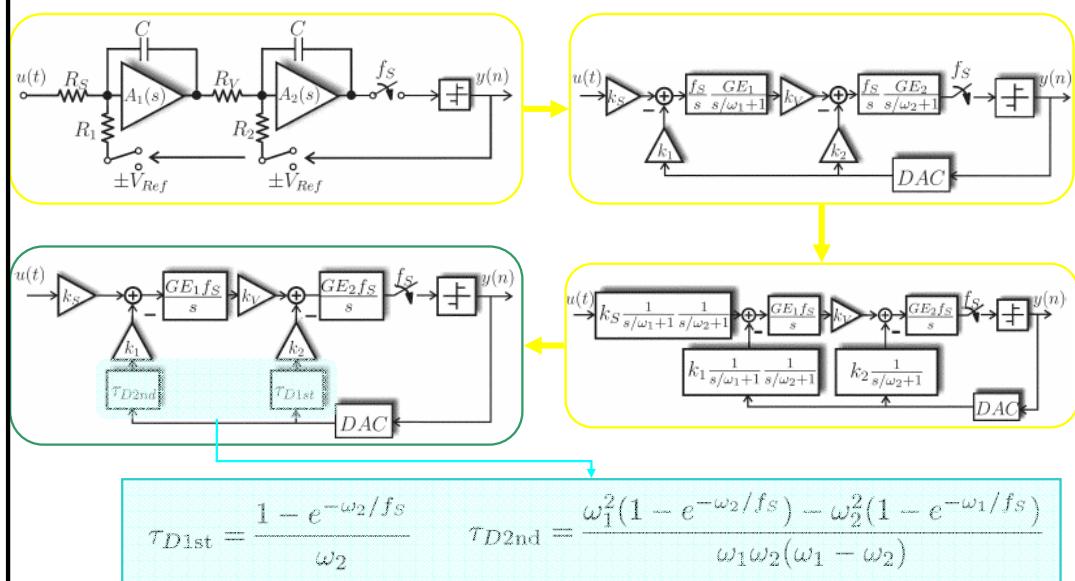
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CT- $\Sigma\Delta$ Ms: Integrator transient response



☐ Model of GBW for RC-active based CT- $\Sigma\Delta$ Ms [Ortm04]

- ♦ Modeled as a gain error (GE) and extra loop delay
- ♦ Each delay is different for each feedback path



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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Element tolerances

- ◆ Scaling coefficients accuracy limited by random errors in resistors/capacitors

$$\frac{\Delta \tau}{\tau} = \frac{\Delta C}{C} - \frac{\Delta g_m}{g_m} \quad \Rightarrow \quad \sigma_\tau = \sqrt{\sigma_C^2 + \sigma_{g_m}^2}$$

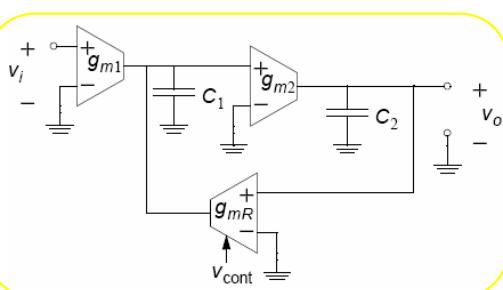
- ◆ Especially critical in:

- High-order single-loop architectures (instability)
- Cascade architectures (analog/digital coefficient ratios)

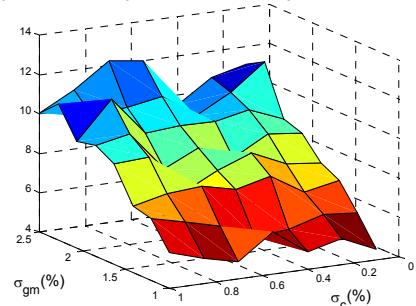
- ◆ Two types of random errors:

- Absolute tolerances: variations from chip to chip (10-20%)
- Relative mismatches: variations from device to device on one chip (0.5-1%)

■ Electrical control of frequency tuning



■ System-level optimization and synthesis method



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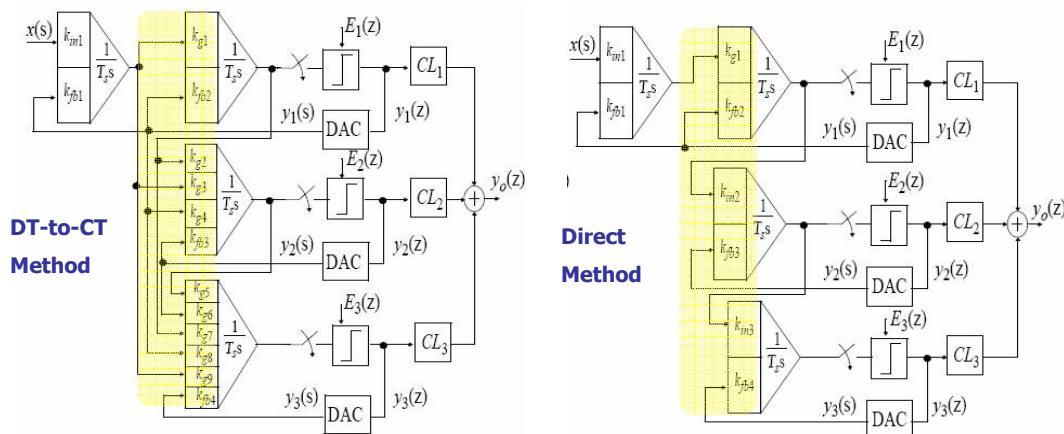
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Direct synthesis method of CT cascade architectures [Tort06]:

- ◆ Optimum placement of poles/zeroes of the NTF
- ◆ Synthesis of both analog and digital part of the cascade CT $\Sigma\Delta$ Modulator
- ◆ Reduced number number of analog components
- ◆ Reduced sensitivity to element tolerances



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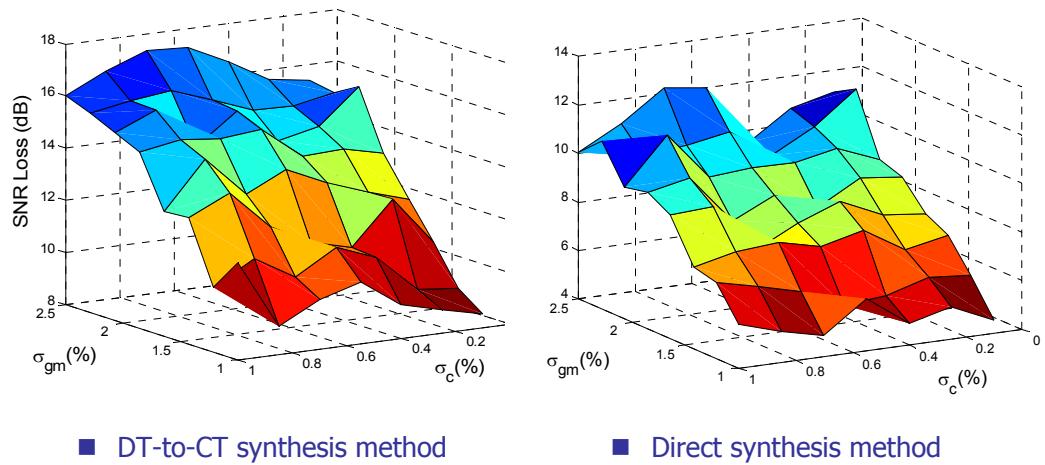
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Direct synthesis of cascade architectures (I) [Tort06]

- ◆ Sensitivity to mismatch (gm, C)
- ◆ A 2-1-1 example



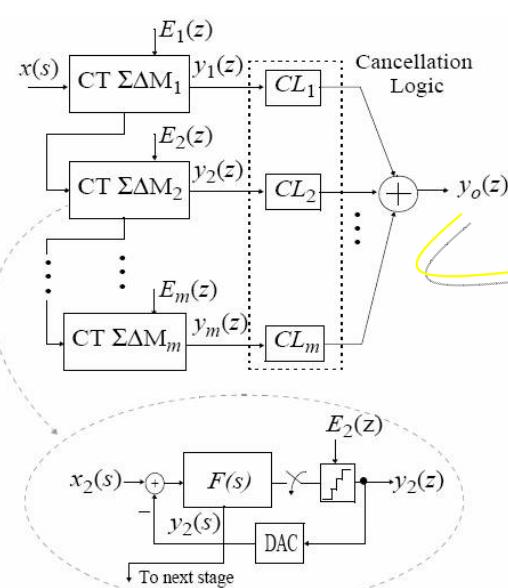
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



□ Direct synthesis of cascade architectures (II) [Tort06]



$$y_o(z) = \sum_{k=1}^m y_k(z) CL_k(z)$$

$$E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)$$

$$y_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{kk}}$$

$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}}$$

$$\left[Z_{km} \equiv Z \left(L^{-1}(H_D F_{km}) \Big|_{n T_s} \right) \right]$$

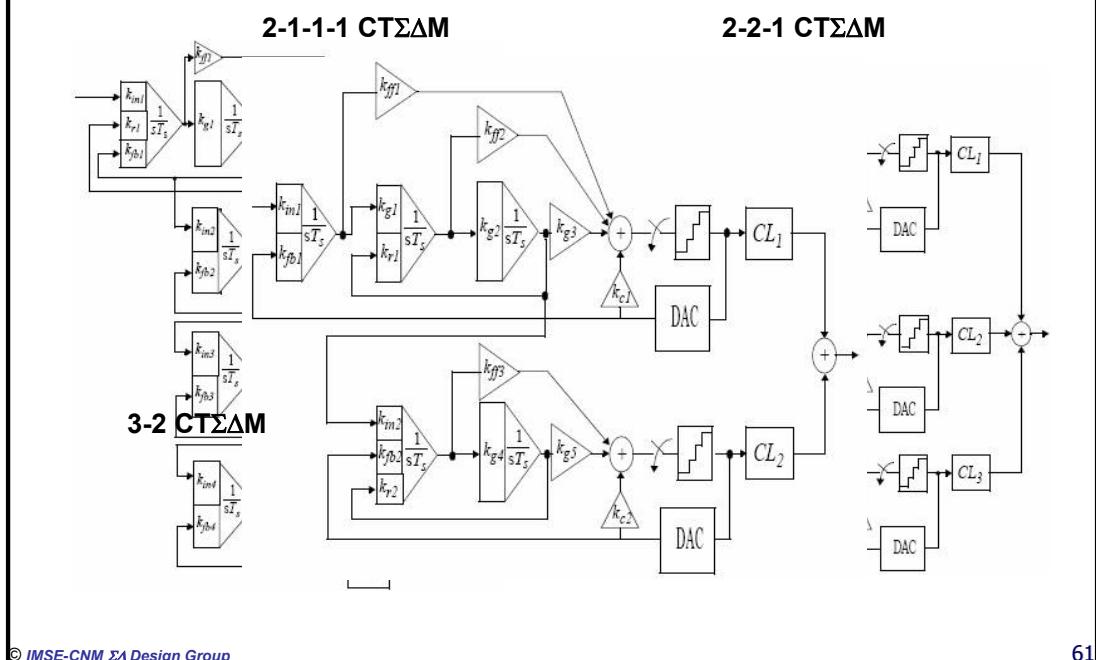
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CT- $\Sigma\Delta$ Ms: Circuit element tolerances



- Synthesized cascaded CT $\Sigma\Delta$ Ms to cope with 12-bit@20-MHz



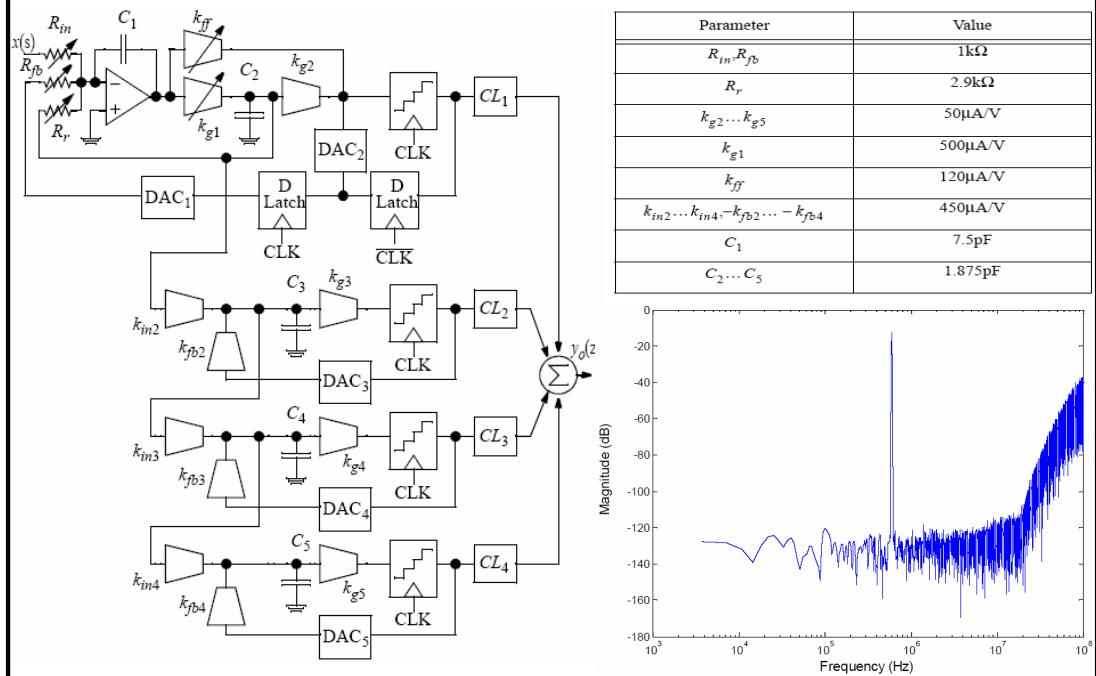
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CT- $\Sigma\Delta$ Ms: Synthesis Methods



- A case study: A 12-bit@20MHz, 4-b, 2-1-1 CT $\Sigma\Delta$ M (RC/Gm Integrators)



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CT- $\Sigma\Delta$ Ms: Integrator time-constant error

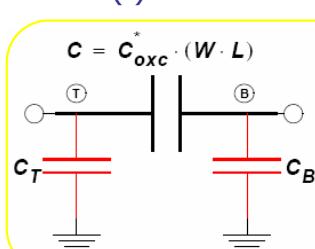


☐ Integrator time-constant error (I)

$$ITF(s) = \frac{A_0}{1 + sC(1 + \varepsilon_\tau)/g_o}$$

$$\varepsilon_\tau = C_p/C$$

$$C = C_{oxc}^* \cdot (W \cdot L)$$



- ♦ Capacitor plate parasitic capacitances
- ♦ Parasitic capacitances of the interconnection lines
- ♦ Parasitic input capacitances of the circuits connected to the node
- ♦ Parasitic output capacitances of the circuits connected to the node

RC ε_τ	MOSFET-C ε_τ	Gm-C ε_τ	Gm-MC ε_τ
$1 + \frac{G}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$	$1 + \frac{G_{ch}}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$	$1 + \frac{C_T}{C}$	$1 + \frac{G_{go}}{C \cdot A_0 \cdot \omega_a} + \frac{C + C_T}{C \cdot A_0}$

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CT- $\Sigma\Delta$ Ms: Integrator time-constant error

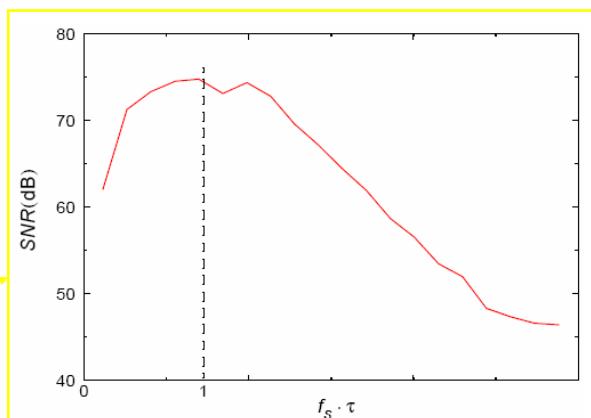


☐ Integrator time-constant error (II)

$$\Delta P_{Q_{A_0 \cdot \varepsilon_\tau}} \Big|_{\text{dB}} \cong \begin{cases} \frac{3M^2}{\pi^2} \cdot \frac{1}{A_o^2} + (1 + \varepsilon_\tau)^2 & \text{(1st-order modulator)} \\ (1 + \varepsilon_\tau)^4 + \frac{10}{3\pi^2} \cdot \frac{(1 + \varepsilon_\tau)^2}{A_o^2} M^2 + \frac{5}{\pi^4 A_o^4} M^4 & \text{(2nd-order modulator)} \end{cases}$$

Optimum SNR for:

$$\tau = 1/f_s$$



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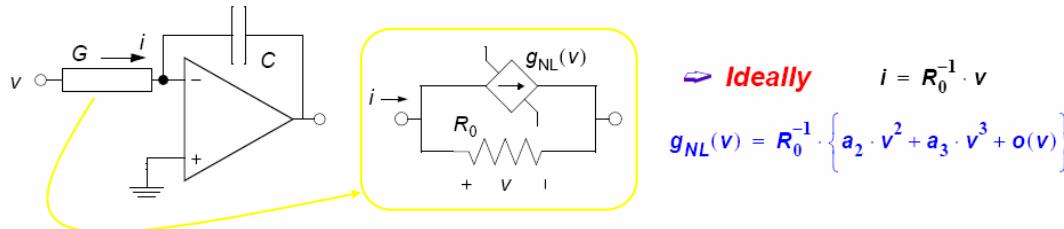
CT- $\Sigma\Delta$ Ms: Non-linear errors



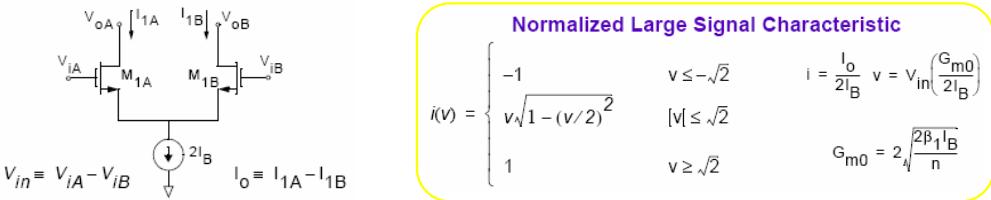
□ Non-linearity (I): Causes

- ◆ Intrinsic non-linearity of the resistor material
- ◆ Modulation of thickness of the conductive layer with resistor voltage

□ V-I transformation in RC integrators



□ V-I transformation in Gm-C integrators



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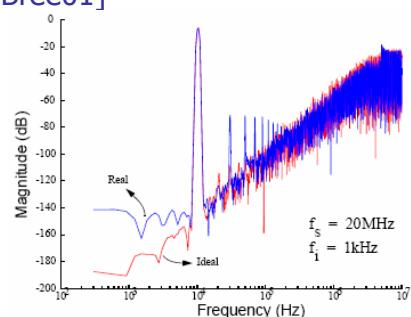
CT- $\Sigma\Delta$ Ms: Non-linear errors



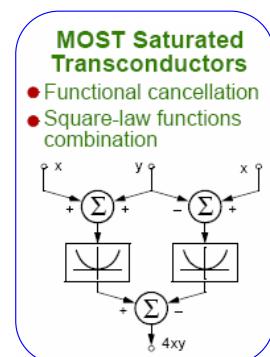
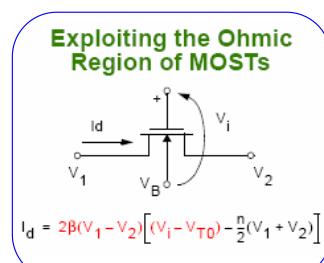
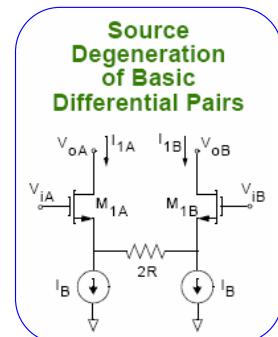
□ Non-linearity (II): Effect on Gm-C CT- $\Sigma\Delta$ Ms [Bree01]

$$\left. \begin{aligned} i(v) &= \beta v \sqrt{2I_B/\beta - v} \approx \sum_{k=1}^{\infty} g_{m_k} v^k \\ i(v) &\equiv g_{m_1} v + g_{m_3} v^3 \end{aligned} \right\}$$

$$THD \equiv HD_3 \equiv \frac{g_{m_3}}{g_{m_1}} V_i^2$$



□ Linearization strategies



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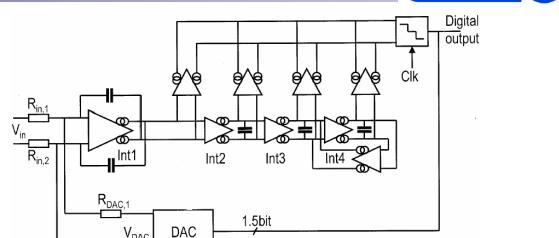
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CT- $\Sigma\Delta$ Ms: Non-linear errors



Non-linearity (III) – Commonplace architecture

- RC-active front-end integrator
- Gm-C subsequent integrators



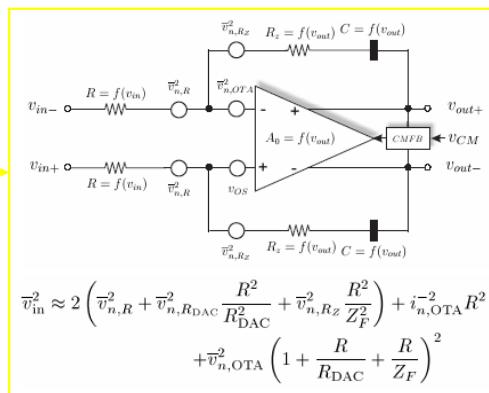
Other sources of non-linearity

- Multi-bit DACs
- Linearity must be the same or lower than the required resolution
- Corrected by same techniques as those employed in SC $\Sigma\Delta$ Ms
 - DEM
 - Calibration

Circuit noise

- Dominated by noise sources from the front-end integrator and DAC
- Flicker noise reduced by proper sizing and/or chopper techniques
- Unsampled noise – effect of sampling reduced by the loop gain

$$P_{Th} \approx \frac{KT}{4C} \frac{\pi^{2L}}{(2L+1)M}$$



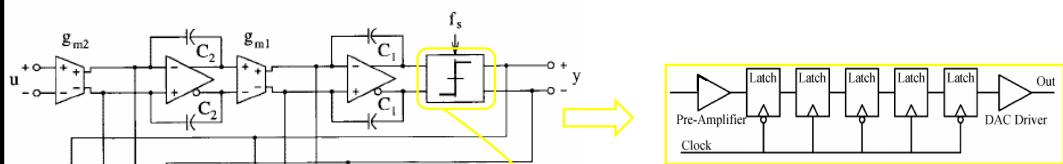
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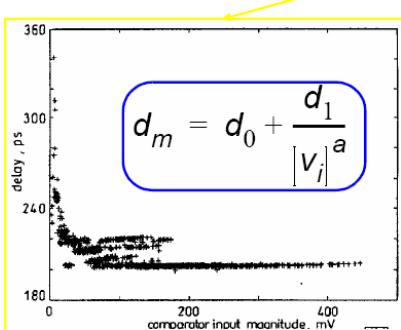
CT- $\Sigma\Delta$ Ms: Comparator metastability



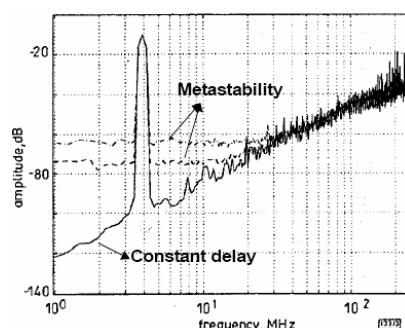
Comparator metastability



- Can be cancelled by using additional latches [Dagh04]



- Modeled as a jitter noise [Cher00]



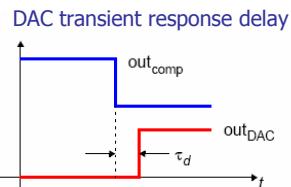
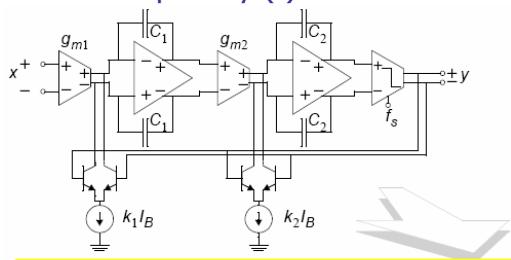
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CT- $\Sigma\Delta$ Ms: Excess loop delay



☐ Excess loop delay (I)

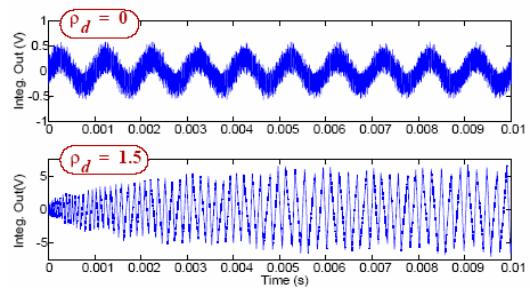


$$Y(f) = \frac{g_q g_1 g_2}{(st)^2 + g_q g_1' g_2' e^{-\tau_d s} + g_q g_2' e^{-(st)} e^{-\tau_d s}} X(f) + \frac{(st)^2}{(st)^2 + g_q g_1' g_2' e^{-\tau_d st} + g_q g_2' \cdot (st) e^{-\tau_d s}} E(f)$$

- ◆ Adds additional poles to STF/NTF
- ◆ Causes instability
- ◆ Stability condition:

• 2nd-order $\rho_d \leq \frac{g'_2}{2g'_1 g_2}$

• *L*th-order $\rho_d \propto \frac{1}{|H(f)|_{\text{outband}}}$



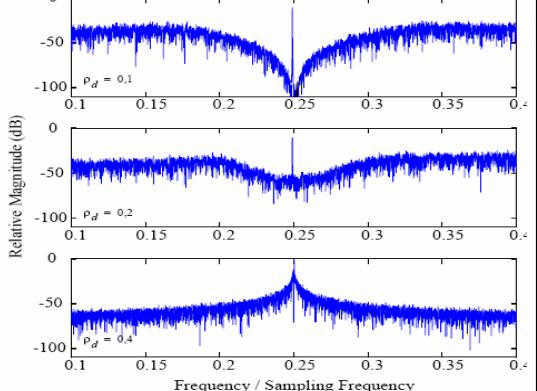
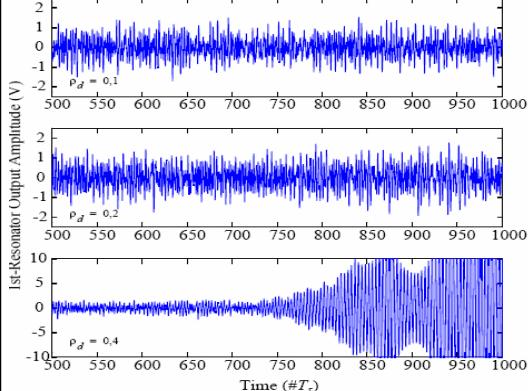
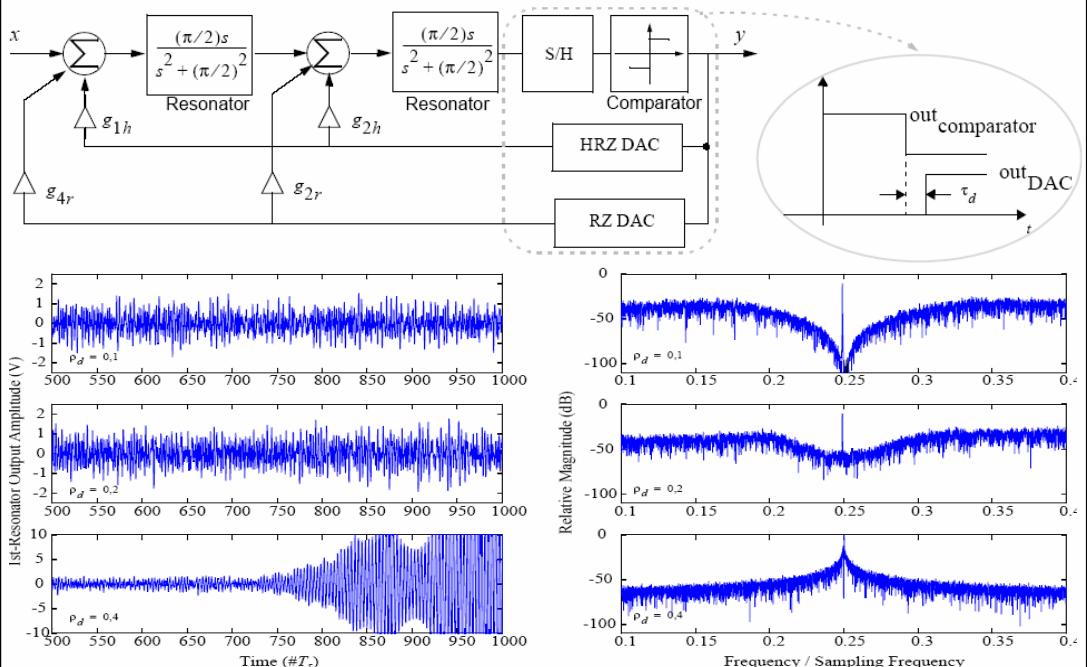
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CT- $\Sigma\Delta$ Ms: Excess loop delay



☐ Excess loop delay (II) – an example of instability



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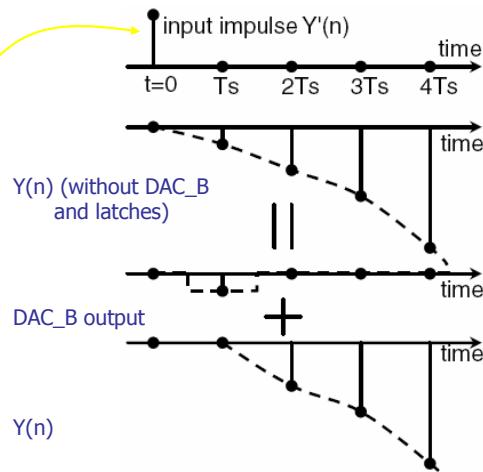
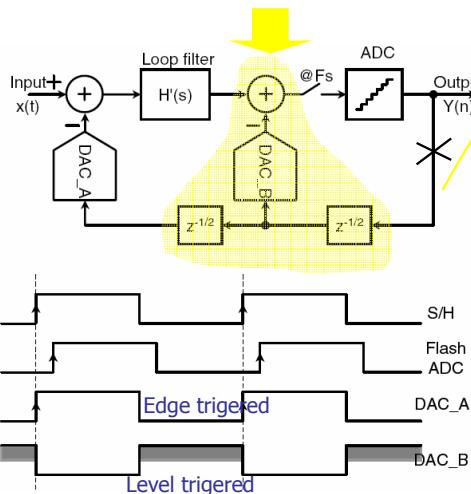
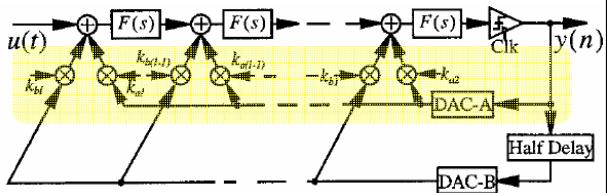
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CT- $\Sigma\Delta$ Ms: Excess loop delay



Excess loop delay (III) – cancellation techniques

- Extra feedback paths (DACs) with tunable gains [Cher00]
- Additional DAC and two latches [Yan04]



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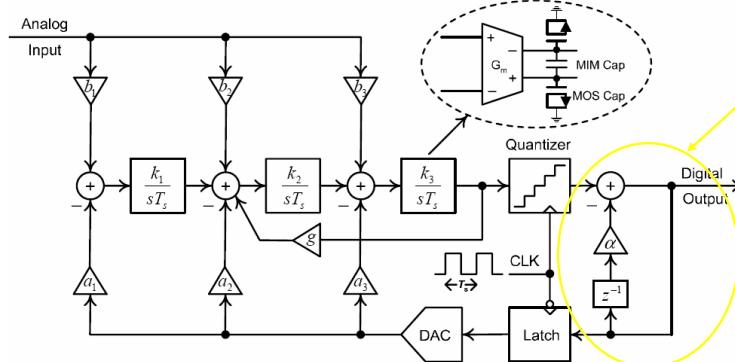
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CT- $\Sigma\Delta$ Ms: Excess loop delay



Excess loop delay (IV) - Digital compensation [Font05]

- Implemented in a 3rd-order single loop architecture with 5-level quantizer
- 90nm CMOS
- 74-dB SNDR-peak, 600kHz bandwidth
- 6.0mW, 1.5V
- Excess loop delay compensated in the digital domain
- Half-a-clock-cycle delay
 - Relax comparators speed
 - Provide maximum isolation between quantizer and DAC switch events



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CT- $\Sigma\Delta$ Ms: Clock jitter error



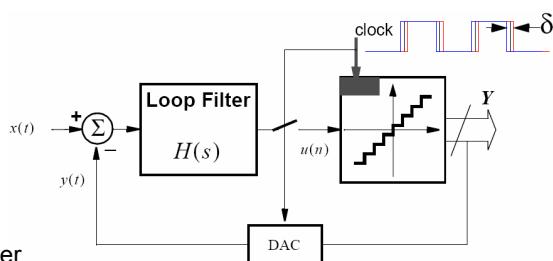
☐ Clock jitter (I)

◆ S/H

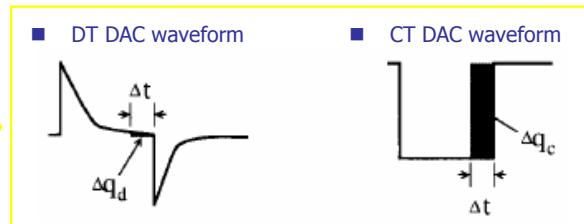
- Shaped by the modulator NTF
- Can be neglected

◆ DAC

- Directly adds with the input
- Increases the in-band noise power



CT $\Sigma\Delta$ Ms are more sensitive to clock jitter than DT $\Sigma\Delta$ Ms



☐ White noise model approximation (NRZ DAC) [Cher00][Zwan96]

◆ Standard deviation of jitter error: $\sigma_j^2 \approx \sigma_j^2 I_{\text{DAC}}^2$

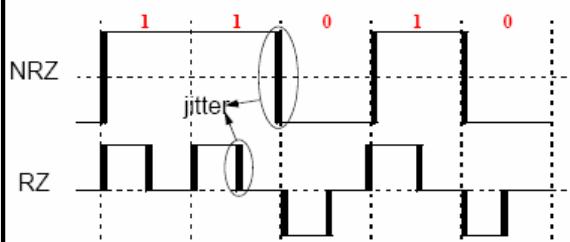
◆ SNR degradation: $SNR_J = 10 \log \left(\frac{1}{16MB_w^2 \sigma_j^2} \right)$

$$\frac{\sigma_{j_{\text{CT}}}}{\sigma_{j_{\text{DT}}}} = \left(\frac{\pi}{2M} \right)^2$$

CT- $\Sigma\Delta$ Ms: Clock jitter error



☐ Clock Jitter (II) – White noise model approximation (NRZ/RZ DAC) [Tao99a]

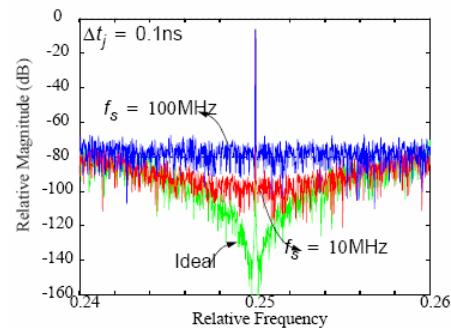


■ Lowpass CT- $\Sigma\Delta$ Ms

$$P_{\text{jitter}}|_{\text{RZ}} \approx \left(\frac{T_s}{T_0} \right)^2 P_{\text{jitter}}|_{\text{NRZ}}$$

■ Bandpass CT- $\Sigma\Delta$ Ms

$$SNR_J \approx \begin{cases} 10 \log \left[\frac{\text{sinc}(\pi f_n T_s)}{64 \sigma_j^2 B_w^2 M} \right] & \text{NRZ} \\ 10 \log \left[\frac{\text{sinc}(\pi f_n T_s)}{64 \left(\frac{T_s}{T_0} \right)^2 \sigma_j^2 B_w^2 M} \right] & \text{RZ} \end{cases}$$



CT- $\Sigma\Delta$ Ms: Clock jitter error



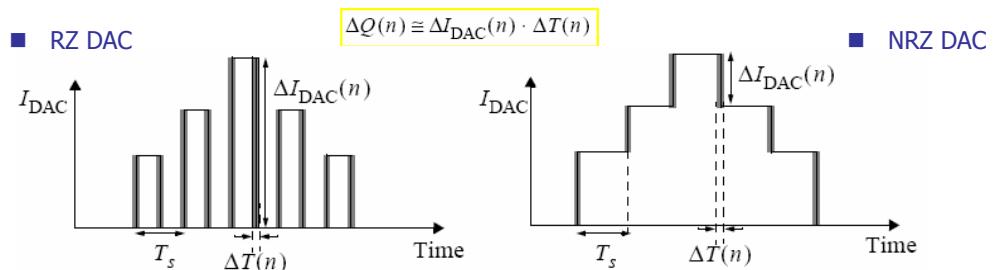
□ Clock Jitter (III) – lingering effect [Olia03a]

- ◆ Jitter-induced noise includes both **white** and **shaped** components
- ◆ State-space analysis of CT- $\Sigma\Delta$ Ms with RZ DAC shows that:

$$S_\varepsilon(z) = (\sigma_s^2 T) \sum_{m_2=1}^N \sum_{j_2=1}^{m_2-1} \sum_{m_1=1}^N \sum_{j_1=1}^{m_1-1} a_{m_1} a_{m_2} z^{j_1-j_2} \times \mathbf{C} \mathbf{A}^{m_1-j_1-1} \mathbf{\Lambda} \mathbf{A}_T^{m_2-j_2-1} \mathbf{C}_T$$

□ Multi-bit NRZ DACs

- ◆ Commonly used in CT- $\Sigma\Delta$ Ms for broadband telecom applications
- ◆ Less sensitive to clock jitter



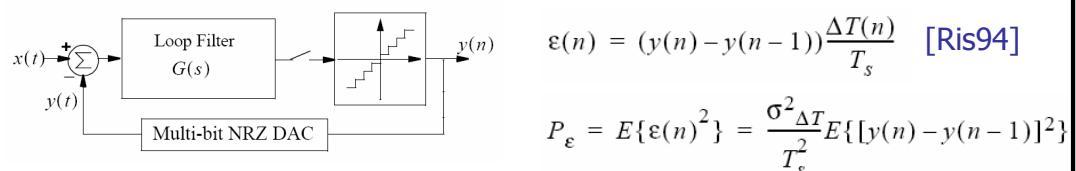
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CT- $\Sigma\Delta$ Ms: Clock jitter error



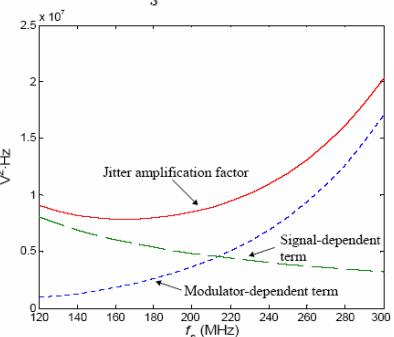
□ Clock Jitter (IV) – Multi-bit NRZ DACs [Tort05]



- Using state-space formulation of NTF:

$$P_\varepsilon = \frac{\sigma_{\Delta T}^2}{T_s^2} \cdot \left(\frac{T_s^2 A^2 \omega_{in}^2}{2} + \frac{X_{FS}^2}{6(2^B - 1)^2} \cdot \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right)$$

$$\psi(\bar{g}, \bar{p}, \bar{\lambda}, L) = 1 - \bar{g}^T \bar{p} + \sum_{k=1}^L \sum_{j=1}^L g_k p_k g_j p_j \frac{\lambda_k^{-1} - \lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}}$$



$$SNR_{\text{jitter}} \equiv \frac{A^2}{2 \cdot P_{\varepsilon_{\text{band}}}} = \frac{A^2}{2 \cdot B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2 \omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3(2^B - 1)^2} \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \right]}$$

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CT- $\Sigma\Delta$ Ms: Clock jitter error



- ☐ Clock Jitter (V): Comparison of [Tort05] with previous approaches

Assuming that SNR_{jitter} is dominated by the signal-dependent term:

$$SNR_{MAX} = 10\log\left(\frac{M}{4\pi^2\sigma_{\Delta T}^2 B_w^2}\right) \quad [\text{Boser, JSSC, 1988}]$$

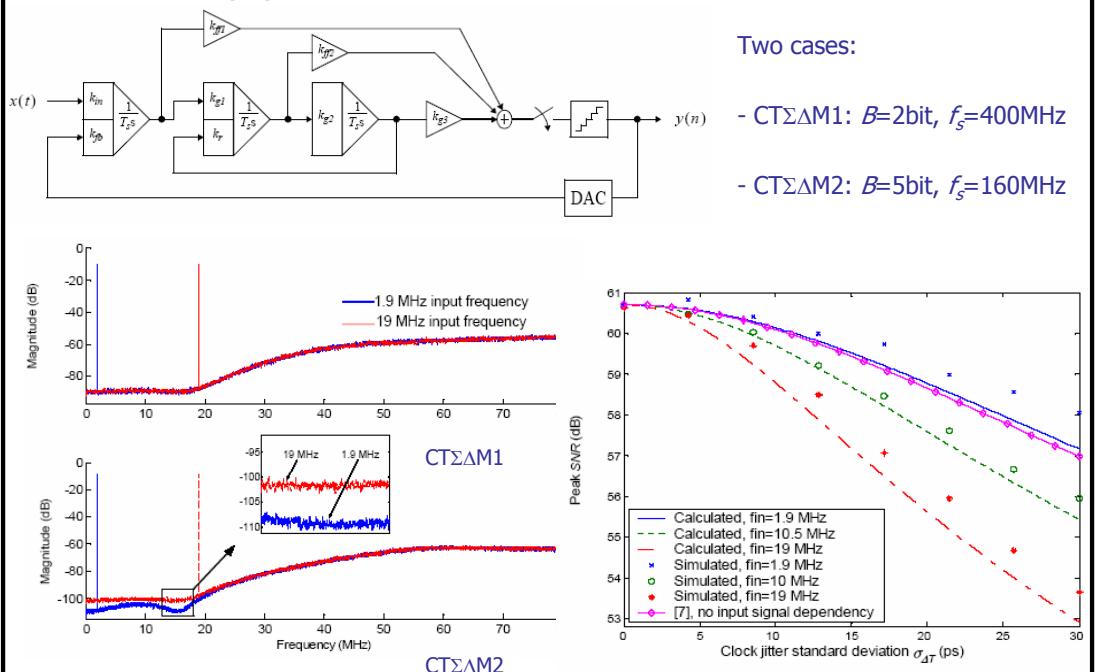
If the modulator-dependent term dominates (single-bit quantization):

$$SNR_{jitter} = 10\log\left(\frac{1}{16M\sigma_{\Delta T}^2 B_w^2}\right) \quad [\text{Van der Zwan, JSSC, 1996}]$$

CT- $\Sigma\Delta$ Ms: Clock jitter error



- ☐ Clock Jitter (VI) – Multi-bit NRZ DACs [Tort05]

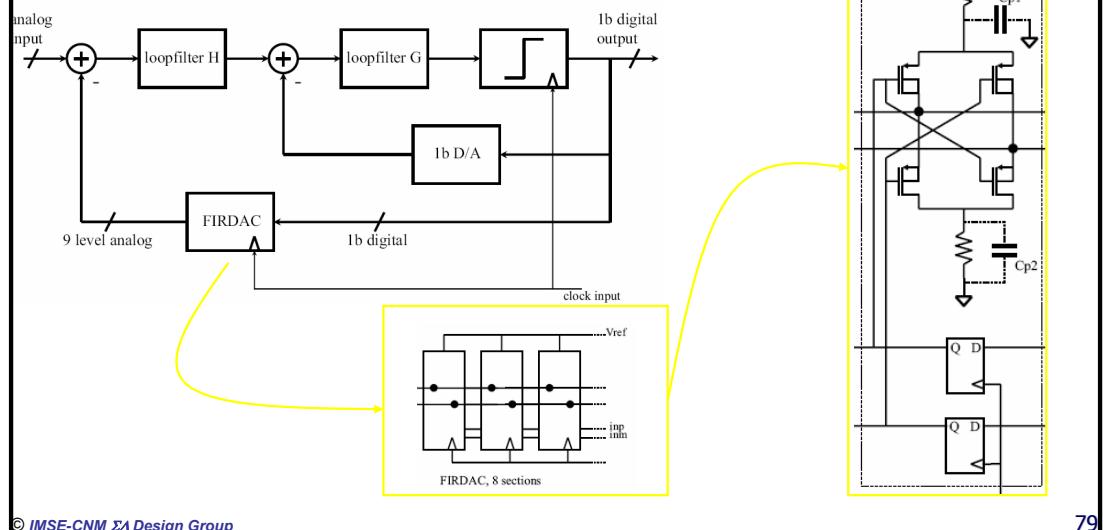


CT- $\Sigma\Delta$ Ms: Clock jitter error



□ Clock Jitter (VII) – Compensation techniques

- ◆ Multi-bit quantization (non-linear DAC)
- ◆ Switched-capacitor DAC [Veld03]
 - Voltage-mode operation (proper for active RC integrators)
 - Slower than switched-current (current steering) DAC
- ◆ FIRDAC to generate a multilevel signal [Putt04]



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CT- $\Sigma\Delta$ Ms: Case Study

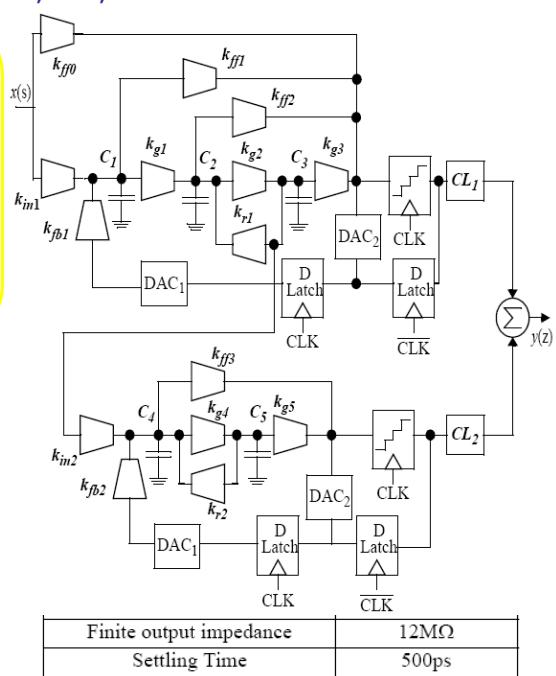


□ A case study: A Gm-C 12-bit@20MHz, 4-b, 3-2 CT $\Sigma\Delta$ M

- ◆ 130nm mixed-signal CMOS, 1P8M
- ◆ Cascade 3-2 multi-bit (4b) CT $\Sigma\Delta$
- ◆ Gm-C loop-filter implementation
- ◆ Current-steering feedback DACs + DEM
- ◆ 12-bit effective resolution
- ◆ 40MS/s output rate (20MHz bandwidth)
- ◆ 240MHz clock frequency
- ◆ 1.2V \pm 10% analog/digital power supply
- ◆ On-chip tuning of analog components
- ◆ Estimated power consumption is 45mW

Loop-filter coefficients

$C_u = 3.65 \text{ pF}$	$k_u = 190 \mu\text{A/V}$
$C_1 = C_2 = C_3 = C_u$	$C_4 = C_5 = 2C_u$
$k_{in1} = 852 \mu\text{A/V}$	$k_{fb1} = 730 \mu\text{A/V}$
$k_{ff0} = 2k_u$	$k_{ff1} = 4k_u$
$k_{ff2} = 2k_u$	$k_{ff3} = 5k_u$
$k_{g1} = k_{g5} = 3k_u$	$k_{g2} = 5k_u$
$k_{g3} = k_u$	$k_{g4} = 7k_u$
$k_{in2} = 5k_u$	$k_{fb2} = 6k_u$
$k_{r1} = k_{r2} = k_u$	



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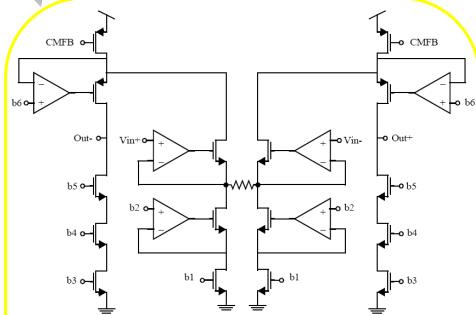
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CT- $\Sigma\Delta$ Ms: Case Study



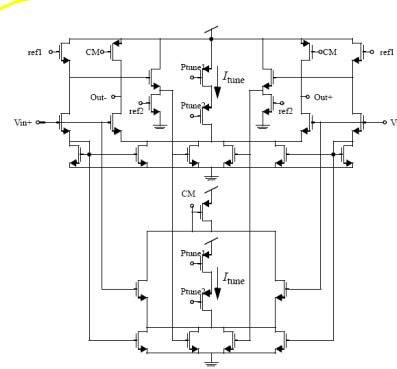
□ Transconductors

- ◆ Resistive source degenerated front-end transconductor
- ◆ Loop-filter transconductors based on quadratic term cancellation



Transistor-level performance

DC Gain	78.3 dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
HD3	-89dB
Power consumption	8.8mW



DC Gain	52dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
HD3	-60dB
Power consumption	622μW

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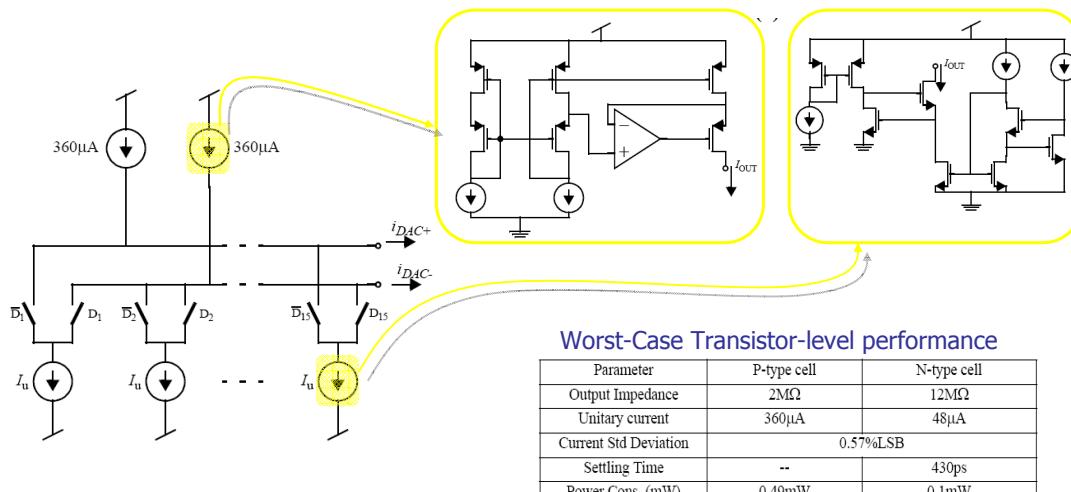
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CT- $\Sigma\Delta$ Ms: Case Study



□ Current-steering DACs

- ◆ 2 360- μ A P-type gain-boosted current sources
- ◆ 15 N-type regulated-cascode current cells



Worst-Case Transistor-level performance

Parameter	P-type cell	N-type cell
Output Impedance	2MΩ	12MΩ
Unitary current	360μA	48μA
Current Std Deviation	0.57%LSB	--
Settling Time	--	430ps
Power Cons. (mW)	0.49mW	0.1mW

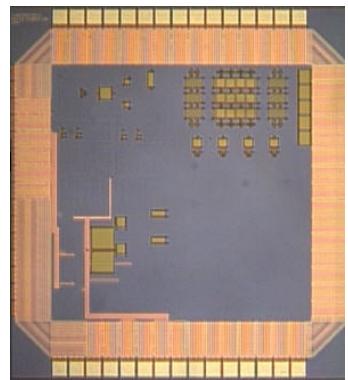
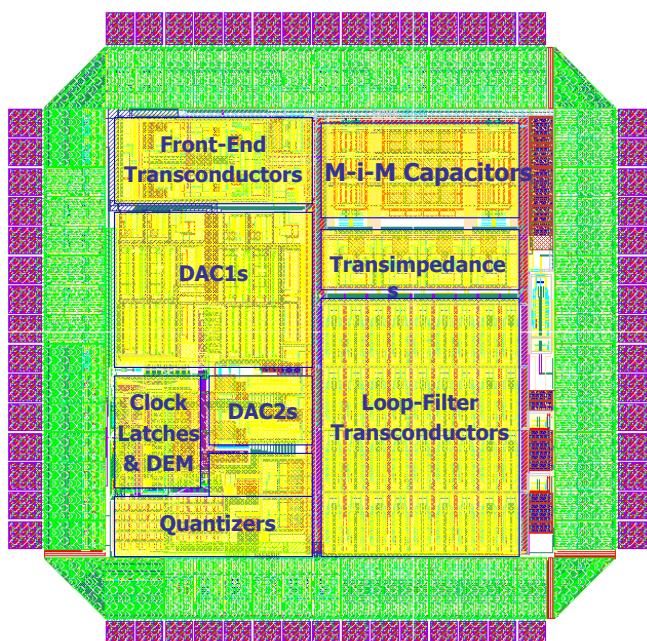
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CT- $\Sigma\Delta$ Ms: Case Study



Chip implementation



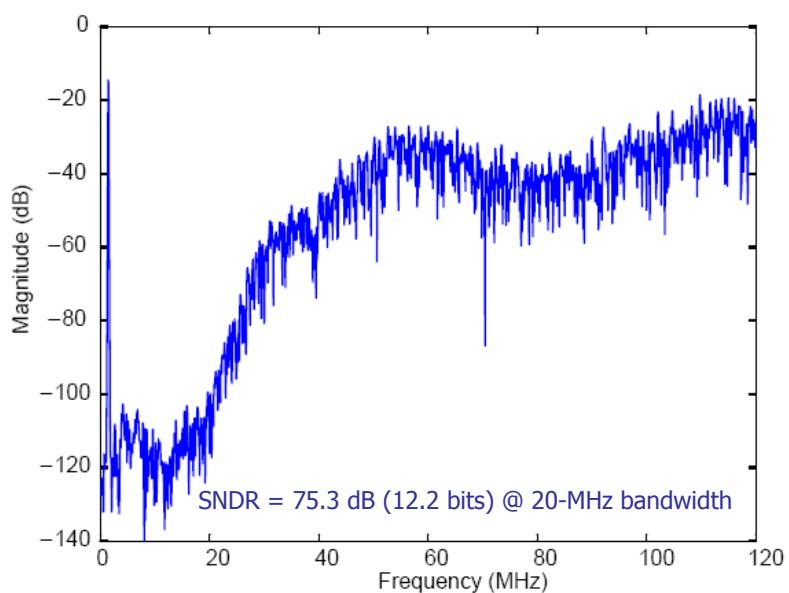
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CT- $\Sigma\Delta$ Ms: Case Study



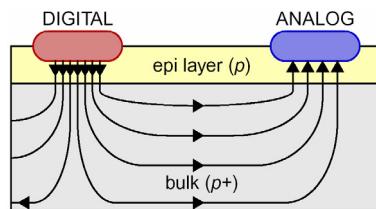
Transistor-level simulation results



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Low-resistive bulk

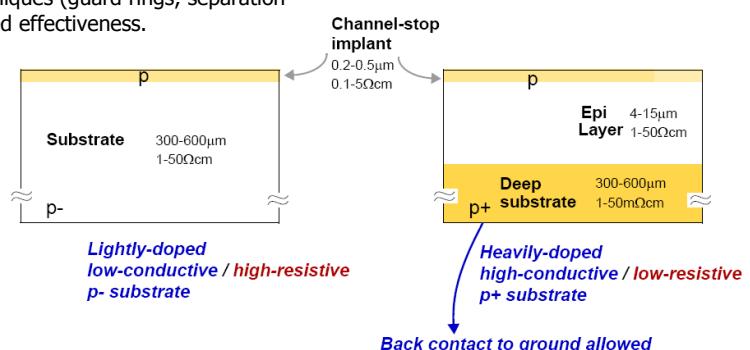


Most Standard CMOS technologies

Epitaxial process with heavily-doped bulk

Impact of the on-chip switching activity

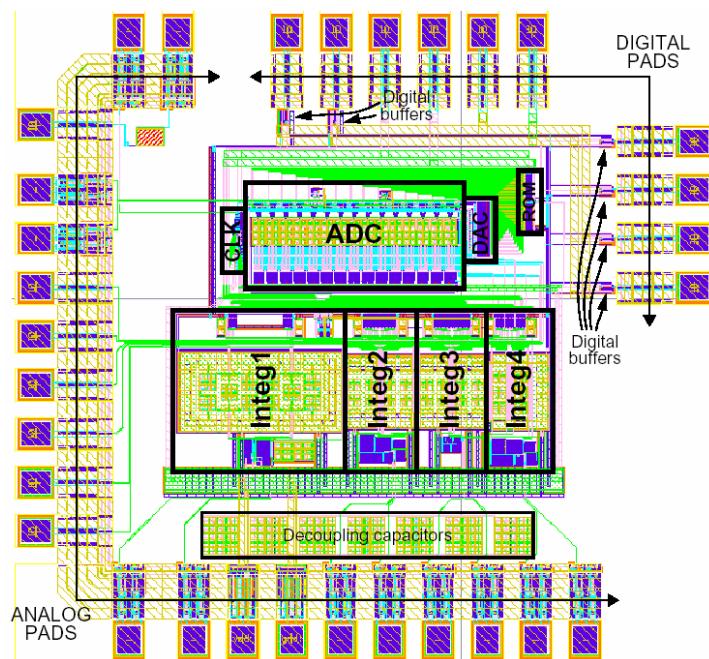
- The deep-substrate is a low-impedance path for injected disturbances.
- Traditional layout techniques (guard rings, separation of blocks) have a limited effectiveness.



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Typical $\Sigma\Delta M$ layout example

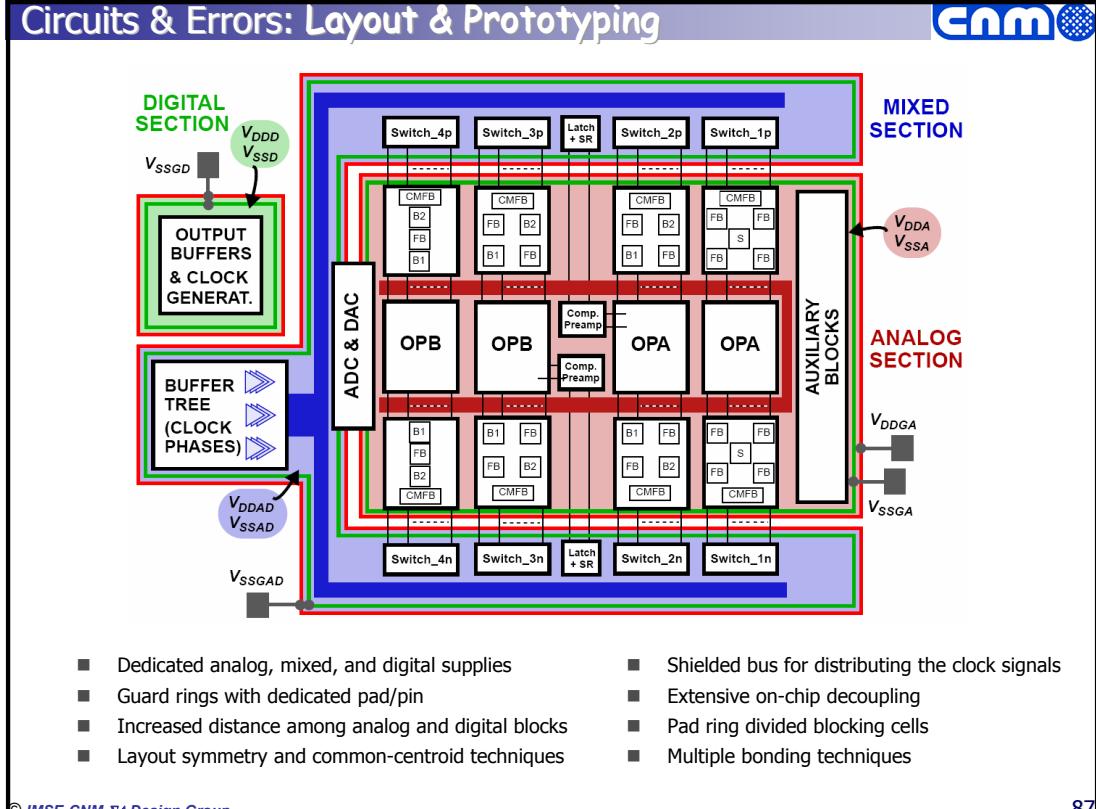


- Dedicated analog and digital supplies:
 - Analog core
 - Digital core
 - Digital output buffers
- Open pad ring
- Common-centroid layout techniques
- Guard rings
- Increased distance among analog and digital blocks

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Circuits & Errors: Layout & Prototyping



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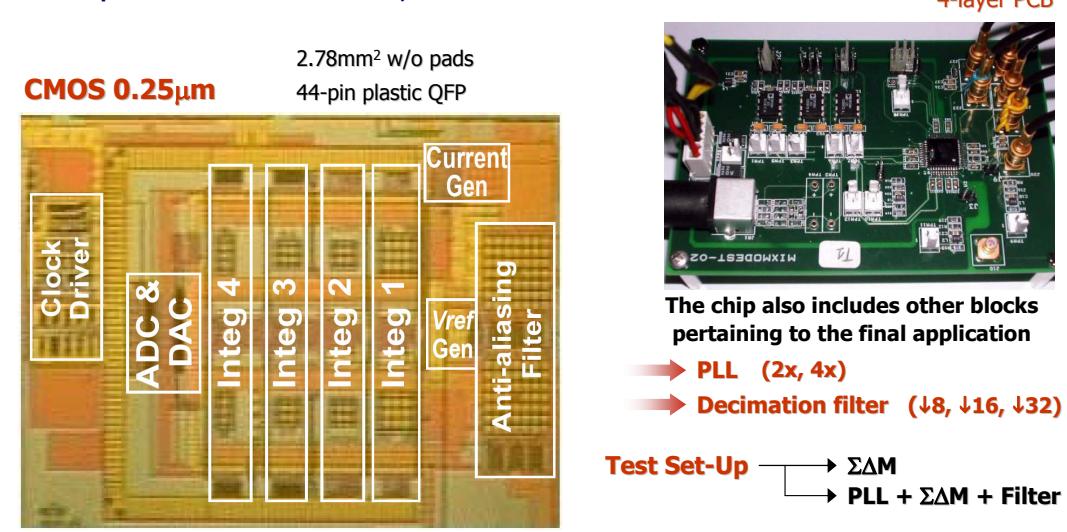
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Circuits & Errors: Layout & Prototyping



Example: A $\Sigma\Delta M$ in $0.25\mu m$ for ADSL/ADSL+

4-layer PCB

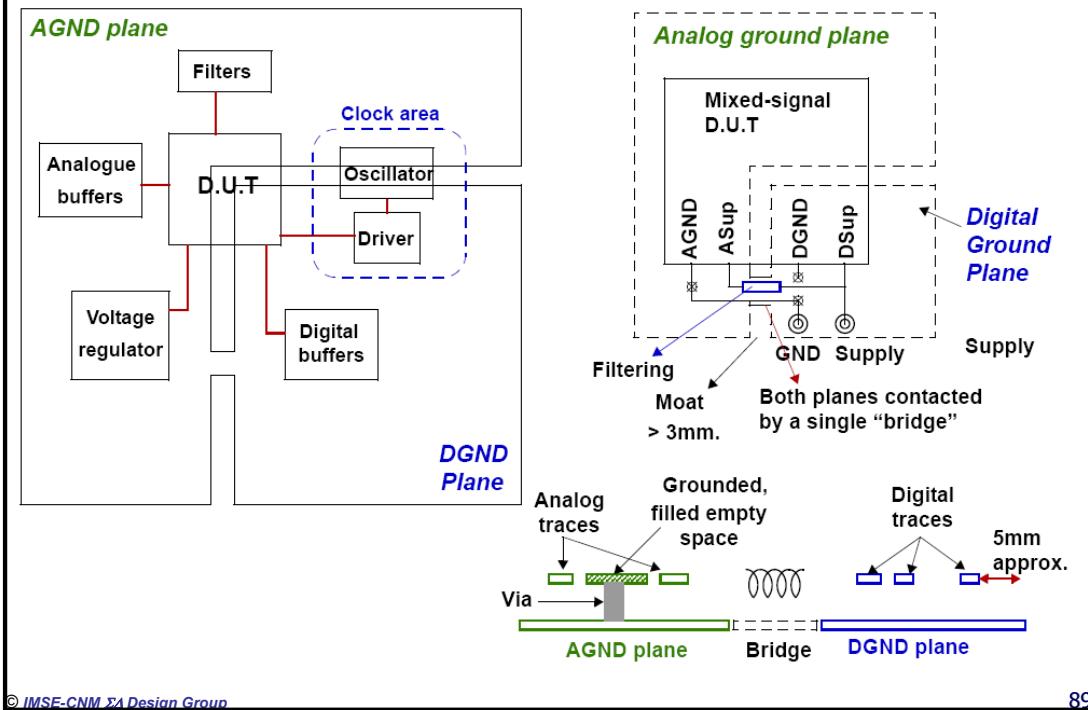


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- Dedicated analog, mixed, and digital supplies
- Guard rings with dedicated pad/pin
- Increased distance among analog and digital blocks
- Layout symmetry and common-centroid techniques
- Shielded bus for distributing the clock signals
- Extensive on-chip decoupling
- Pad ring divided blocking cells
- Multiple bonding techniques

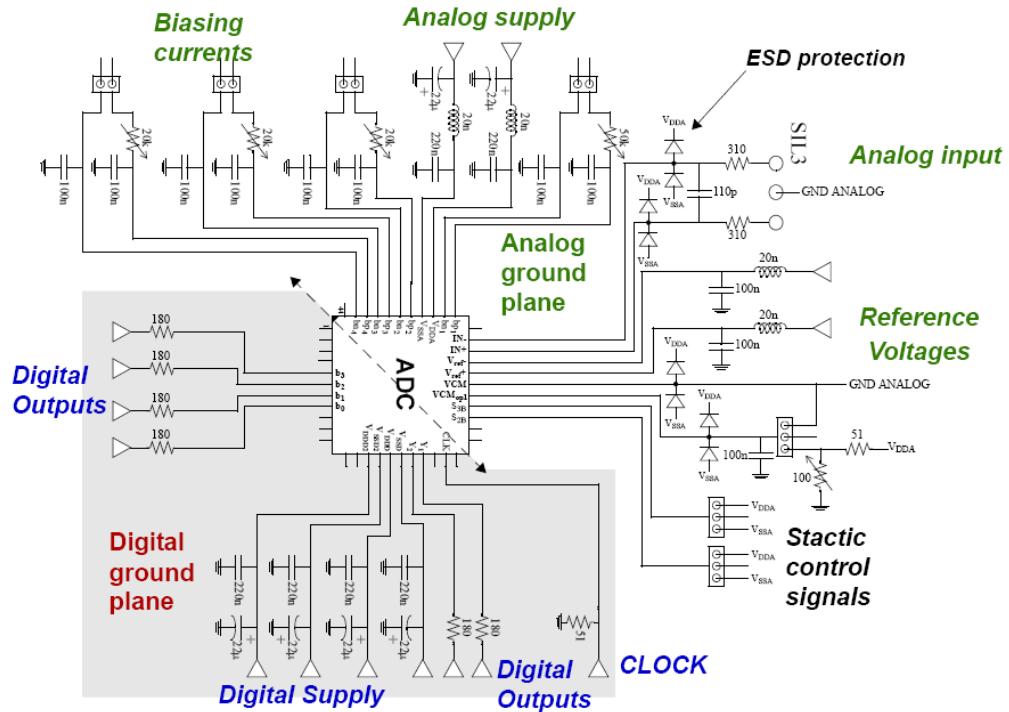
Circuits & Errors: Test PCB



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Circuits & Errors: Test PCB



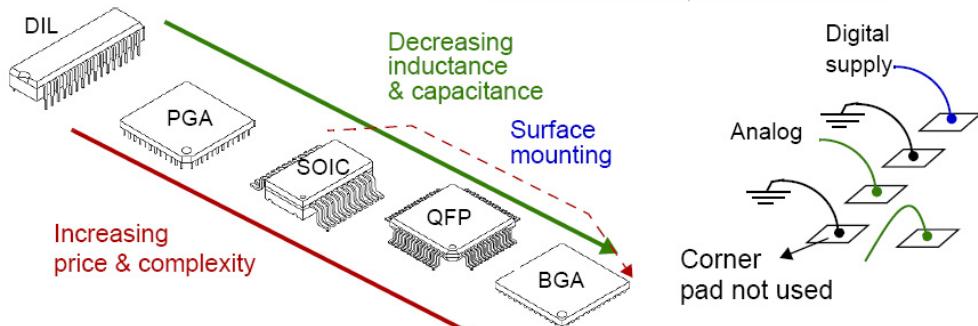
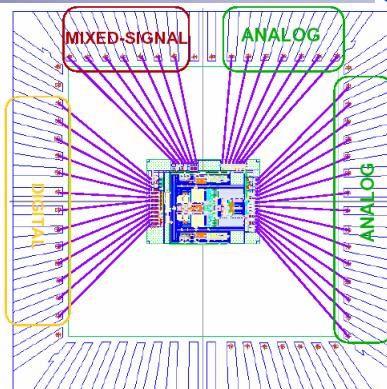
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Circuits & Errors: Chip Package



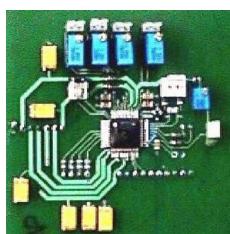
- Double-bonding and multiple pins for supplies
- Different pin assignment for analog, mixed and digital



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Circuits & Errors: Test Set-up

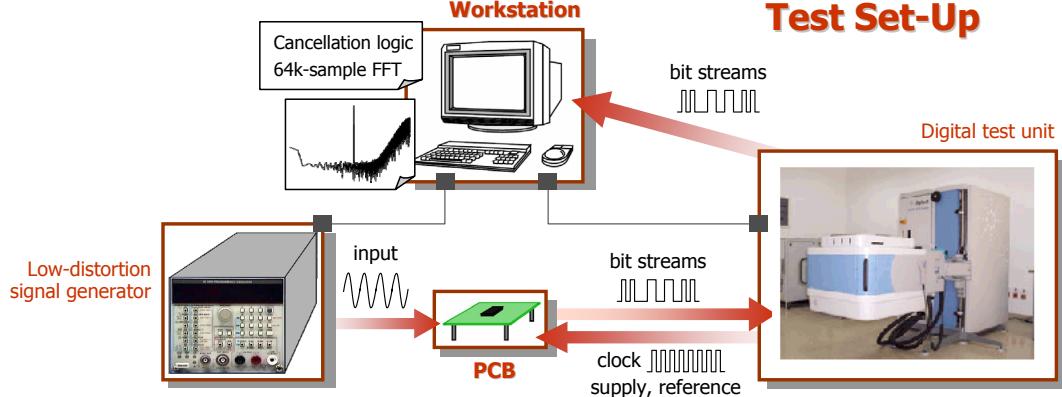


Two-layer PCB

- Soldered samples (in order to avoid socket parasitics)
- Anti-aliasing filter (passive, 1st order)
- Independent control of amplifier bias currents
- Decoupling
- Impedance termination

Novel tech (characterization not yet confirmed by silicon results)

Test Set-Up



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DT- $\Sigma\Delta$ Ms: References



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