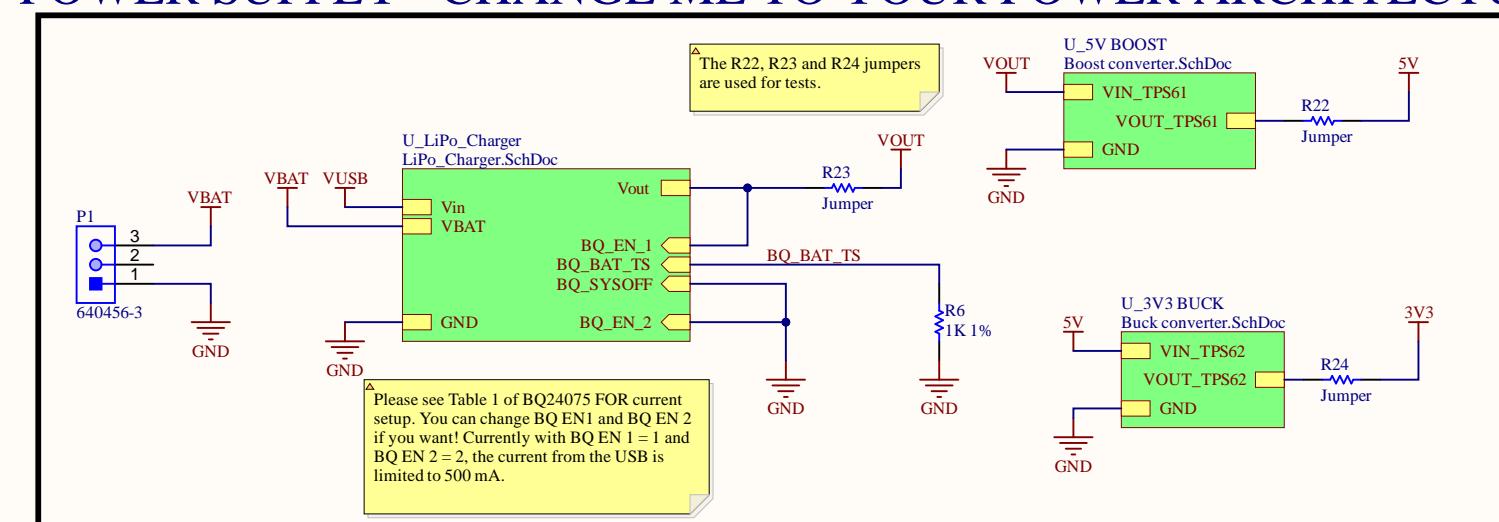


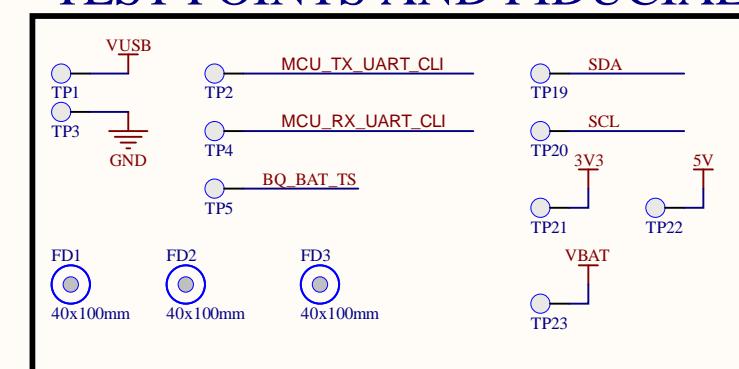
POWER SUPPLY - CHANGE ME TO YOUR POWER ARCHITECTURE



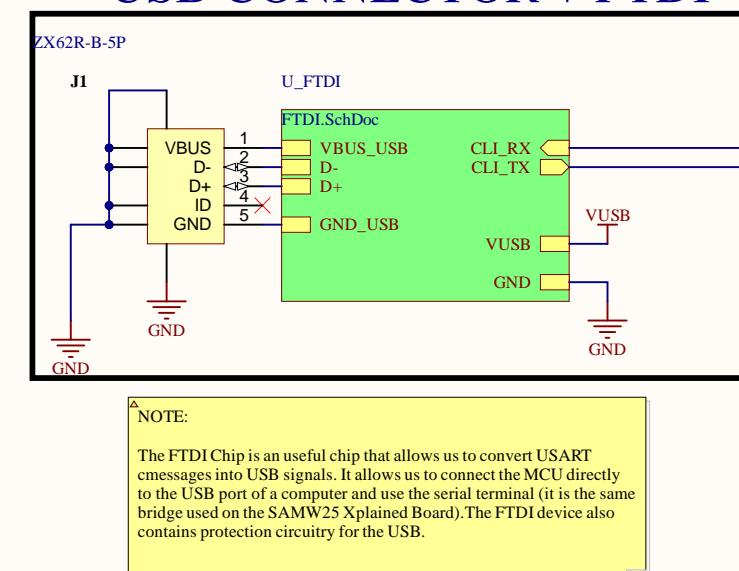
NOTES

Section to add version notes or any other general information

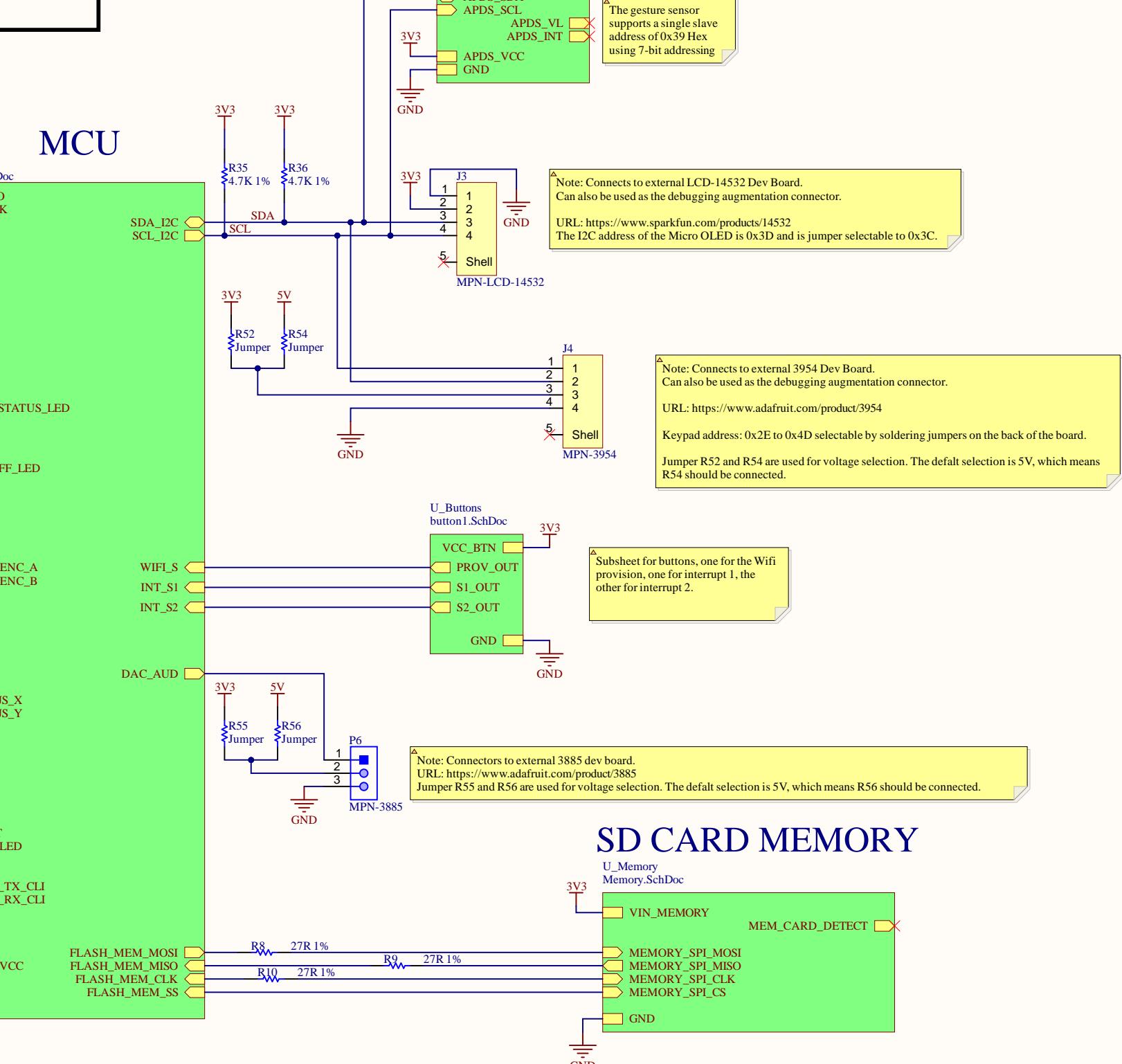
TEST POINTS AND FIDUCIALS



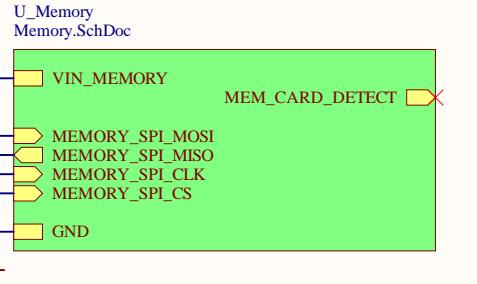
USB CONNECTOR + FTDI



MCU



SD CARD MEMORY



APPROVALS		DATE	PROJECT			
ENG:	RTZ, HYW	02/15/22	SimonSayGator	Practical Engineering 42 South 33rd St Engineering, PA UNIVERSITY OF PENNSYLVANIA 19104		
DSN:	RTZ, HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION: DESIGN ITEM: 1.0		
CHK:	RTZ, HYW	02/15/22	TITLE:			
REFERENCE DOCUMENTS		MAIN				
BOM:	*	ASSY DWG: TBD				
FAB DWG: TBD		SIZE	CAGE CODE	DWG NO.		
PCB DWG: TBD		C	TBD	TBD		
SCALE		NA	FILE NAME	MAIN.SchDoc		
SHEET 1 OF 11				REV *		

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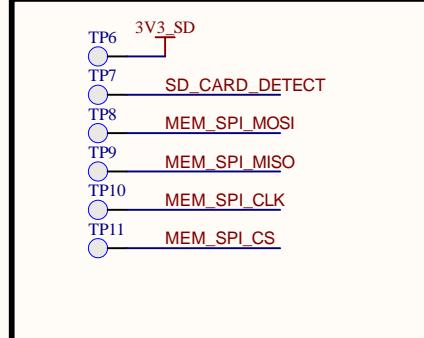
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TESTPOINTS



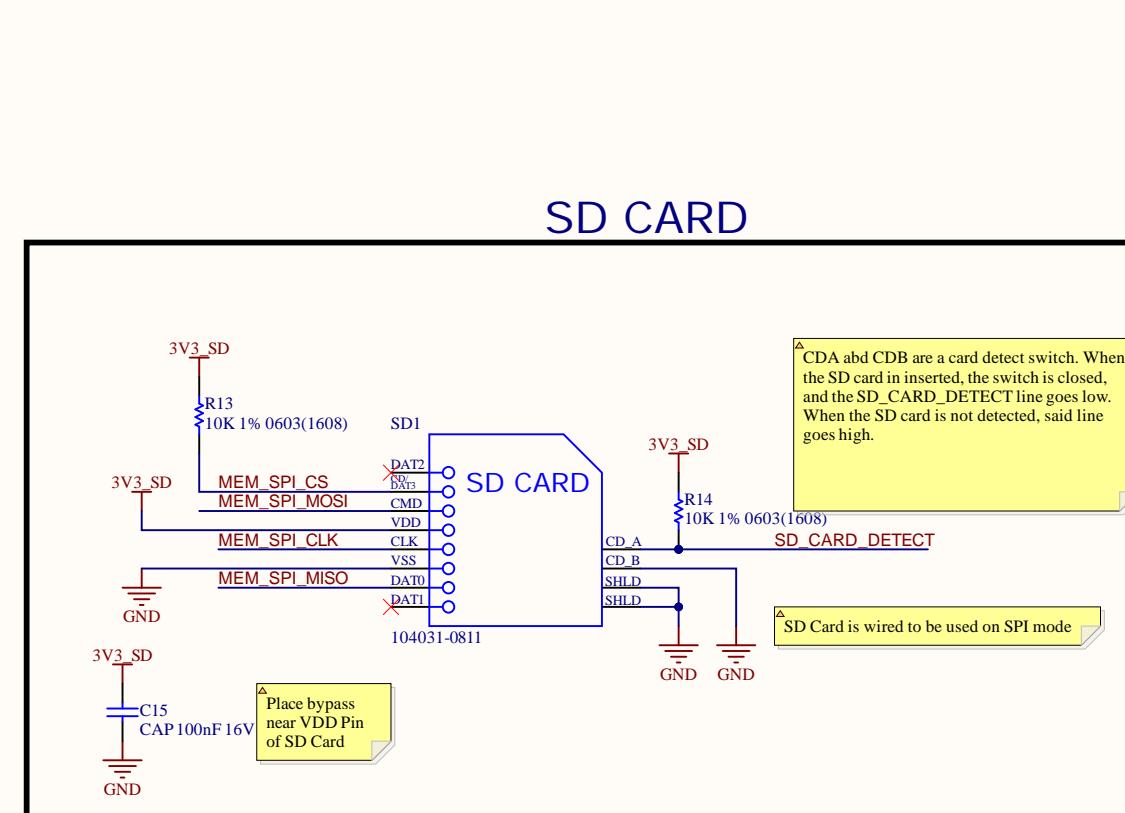
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TESTPOINTS



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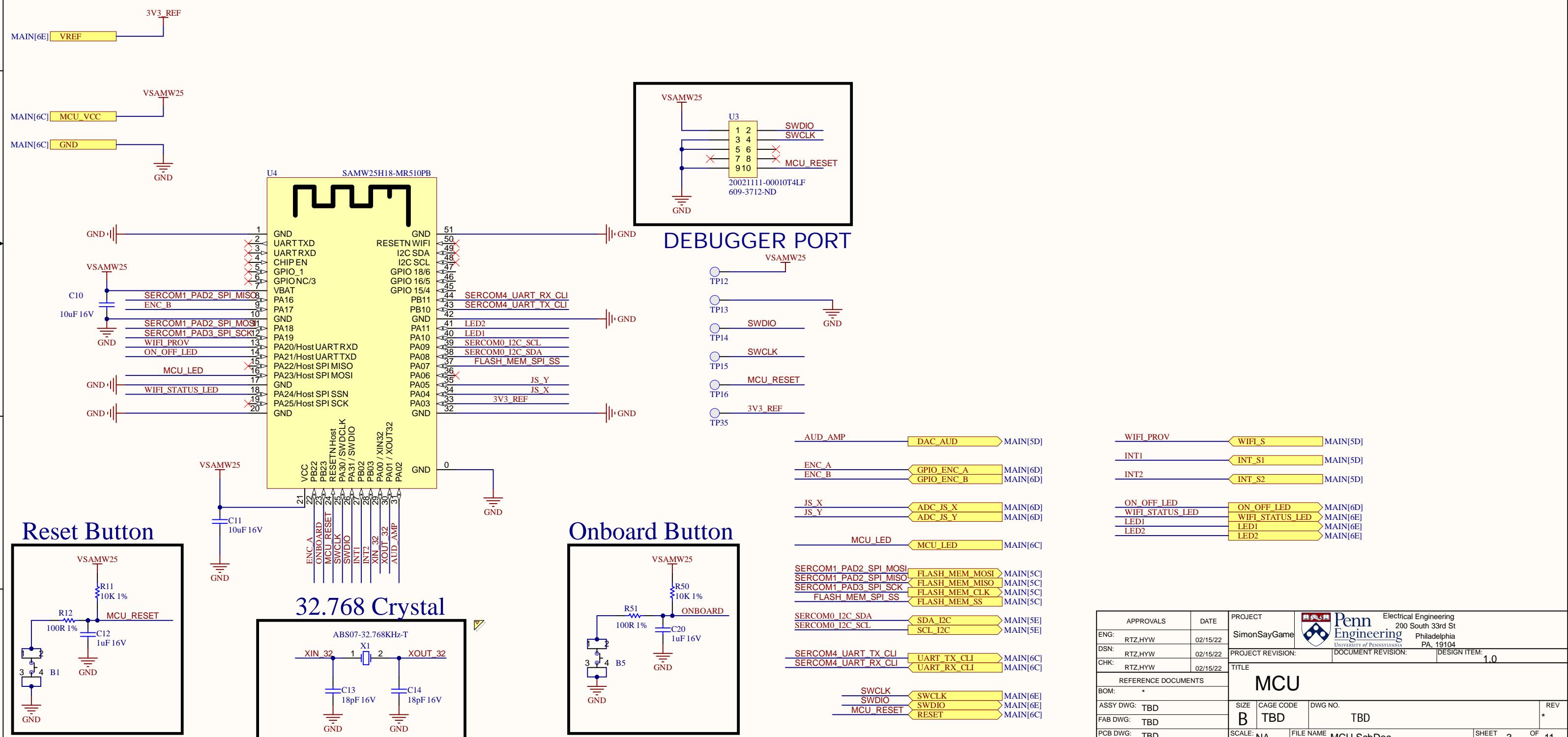
TESTPOINTS

F

APPROVALS	DATE	PROJECT	Penn Engineering		
ENG: RTZ_HYW	02/15/22	SimonSayGame	200 South 33rd St	Philadelphia	
DSN: RTZ_HYW	02/15/22	UNIVERSITY OF PENNSYLVANIA	PA, 19104		
CHK: RTZ_HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	1.0
MEMORY					
REFERENCE DOCUMENTS	BOM: *	SIZE	CAGE CODE	DWG NO.	REV.
ASSY DWG: TBD	FAB DWG: TBD	B	TBD	TBD	*
FAB DWG: TBD	PCB DWG: TBD	SCALE: NA	FILE NAME	Memory.SchDoc	SHEET 2 OF 11

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REVISION	DESCRIPTION	DATE	APPROVED



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2	1		
REVISION	DESCRIPTION	DATE	APPROVED

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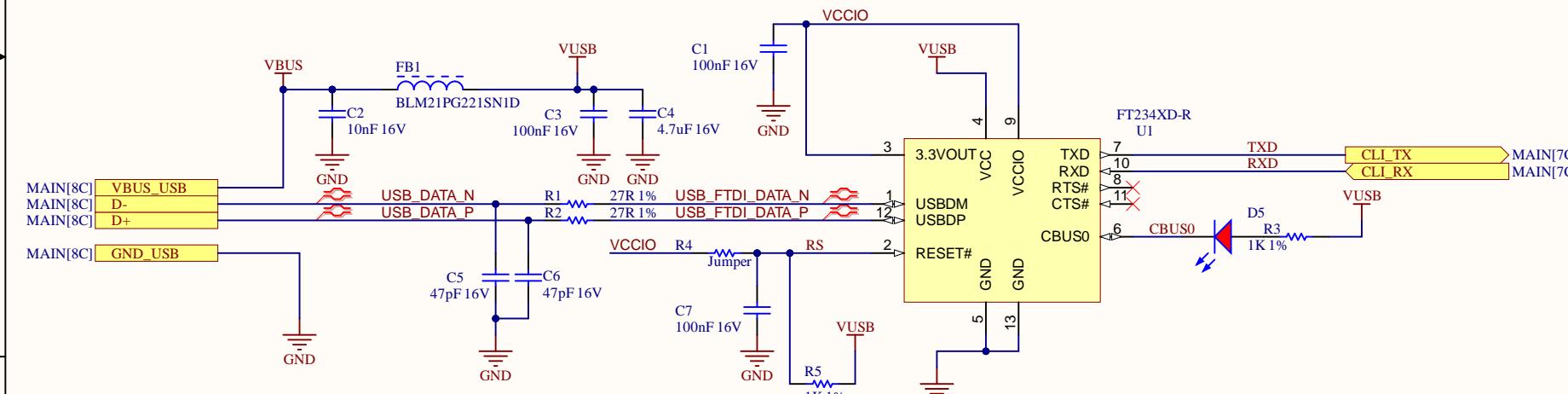
10

10

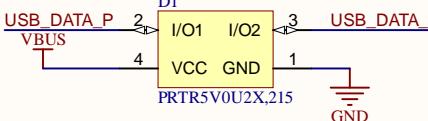
10

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FTDI CHIP



USB ESD PROTECTIO



APPROVALS	DATE	PROJECT		Penn Engineering <small>UNIVERSITY OF PENNSYLVANIA</small>	Electrical Engineering 200 South 33rd St Philadelphia PA, 19104
ENG: RTZ, HYW	02/15/22	SimonSayGame			
DSN: RTZ, HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM: *	
CHK: RTZ, HYW	02/15/22	TITLE			
REFERENCE DOCUMENTS					
BOM: *					
ASSY DWG: TBD		SIZE	CAGE CODE	DWG NO.	REV
FAB DWG: TBD		B	TBD	TBD	*
PCB DWG: TBD		SCALE: *	FILE NAME	FTDI SchDoc	SHEET 4 OF 11

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REVISION	DESCRIPTION	DATE	APPROVED

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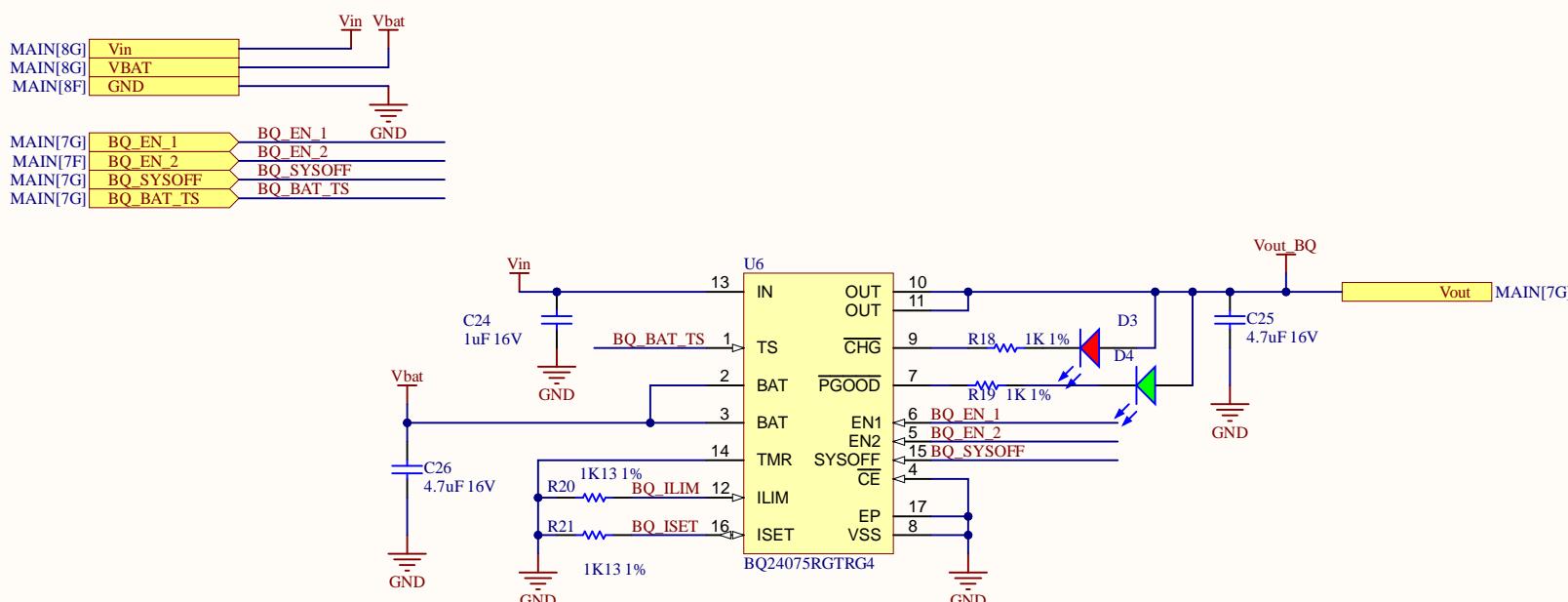
C

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APPROVALS	DATE	PROJECT	Electrical Engineering		
ENG: RTZ_HYW	02/15/22	SimonSayGame	Penn	Engineering	200 South 33rd St
DSN: RTZ_HYW	02/15/22		UNIVERSITY OF PENNSYLVANIA		Philadelphia PA, 19104
CHK: RTZ_HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	1.0
TITLE					
LIPO_CHARGER					
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG NO.	REV
BOM: *		ASSY DWG: TBD	TBD	TBD	*
ASSY DWG: TBD		FAB DWG: TBD			
FAB DWG: TBD		PCB DWG: TBD			
PCB DWG: TBD		SCALE: na	FILE NAME: LiPo_Charger.SchDoc	SHEET 5 OF 11	

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REVISION	DESCRIPTION	DATE	APPROVED
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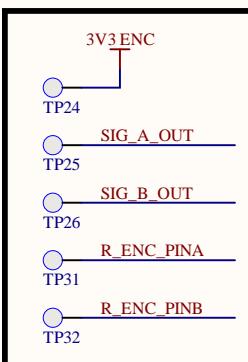
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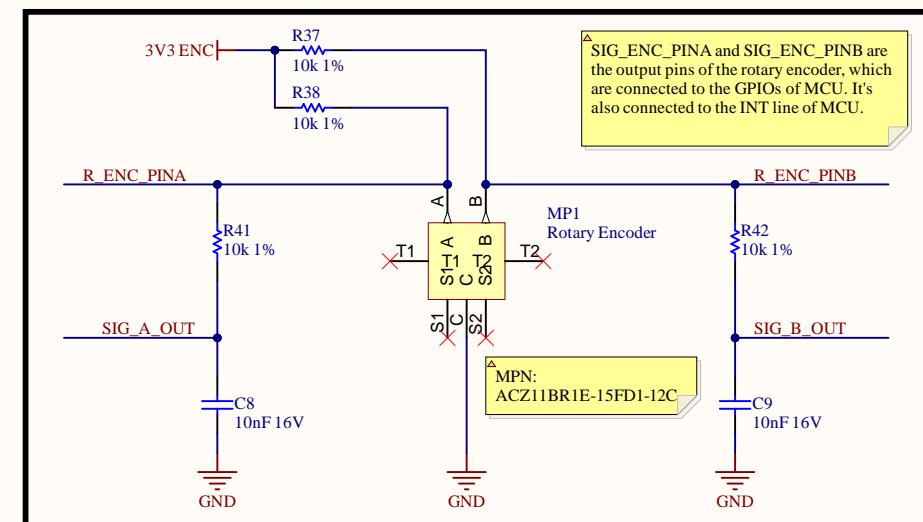
MAIN[6D] ENC_PINA SIG_A_OUT
MAIN[6D] ENC_PINB SIG_B_OUT

3V3 ENC
MAIN[6D] ENC_VIN
MAIN[6D] GND GND

Testpoints



Rotary Encoder



APPROVALS	DATE	PROJECT	Penn Engineering
ENG: RTZ_HYW	02/15/22	SimonSayGame	200 South 33rd St
DSN: RTZ_HYW	02/15/22		Philadelphia PA, 19104
CHK: RTZ_HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION: DESIGN ITEM: 1.0
ROTARY ENCODER			
REFERENCE DOCUMENTS	BOM: *	SIZE	CAGE CODE DWG NO.
ASSY DWG: TBD	FAB DWG: TBD	B	TBD
PCB DWG: TBD	SCALE: NA	FILE NAME	Rotary Encoder.SchDoc SHEET 6 OF 11

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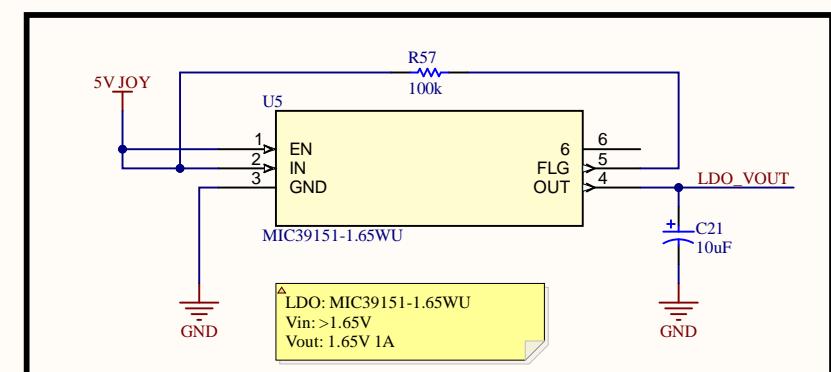
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MAIN[6D] JS_X ANG_X_AXIS

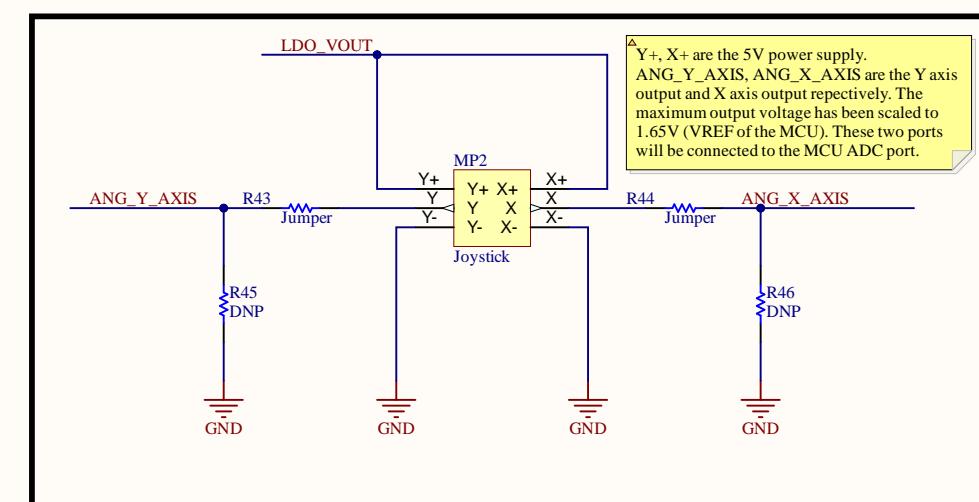
MAIN[6D] JS_Y ANG_Y_AXIS

MAIN[6C] JS_5V

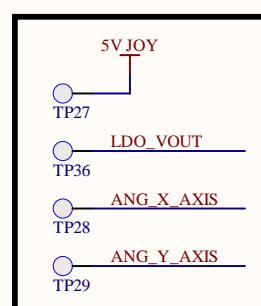
MAIN[6C] GND

5V_JOY

Joy Stick



Testpoints



APPROVALS	DATE	PROJECT	Penn Engineering
ENG: RTZ_HYW	02/15/22	SimonSayGame	200 South 33rd St
DSN: RTZ_HYW	02/15/22		Philadelphia
CHK: RTZ_HYW	02/15/22		PA, 19104
JOYSTICK			
REFERENCE DOCUMENTS		SIZE	CAGE CODE
BOM: *		DWG NO.	
ASSY DWG: TBD		B	TBD
FAB DWG: TBD			TBD
PCB DWG: TBD		SCALE: NA	FILE NAME: Joystick.SchDoc
		SHEET 7	OF 11

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F

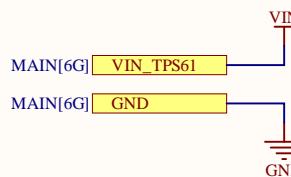
F

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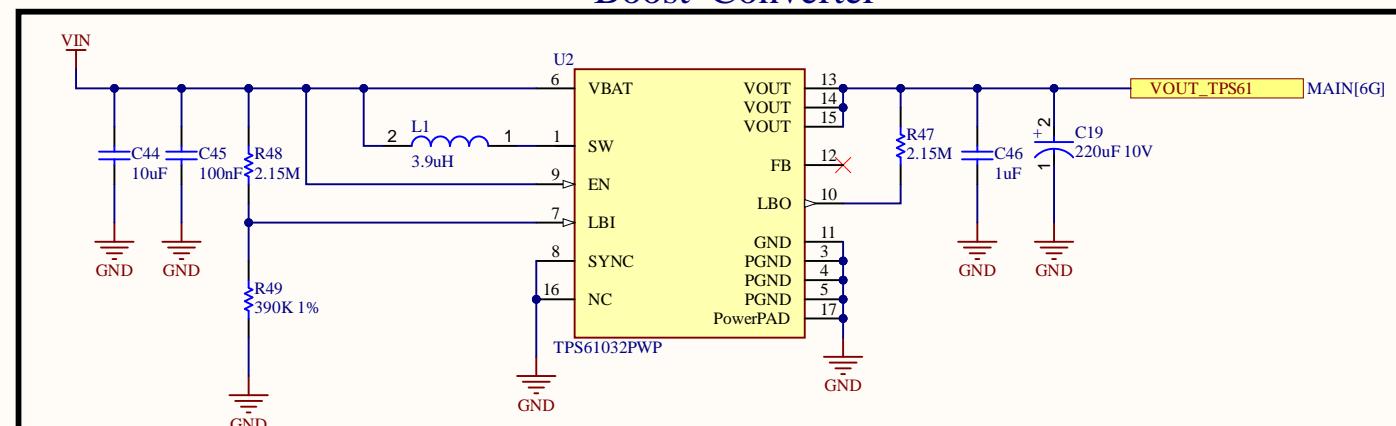
E

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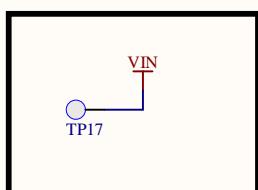


Boost Converter



TPS61032PWP
VIN: 3.3V to 4.2V
OUT: 5V up to 1A

Testpoints



APPROVALS	DATE	PROJECT	BOOST CONVERTER		
ENG: RTZ_HYW	02/15/22	SimonSayGame	Penn Engineering	Electrical Engineering	200 South 33rd St
DSN: RTZ_HYW	02/15/22		UNIVERSITY OF PENNSYLVANIA	Philadelphia	PA, 19104
CHK: RTZ_HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	1.0
REFERENCE DOCUMENTS					
BOM: *		ASSY DWG: TBD	SIZE	CAGE CODE	DWG NO.
		FAB DWG: TBD	B	TBD	TBD
		PCB DWG: TBD	SCALE: NA	FILE NAME	Boost converter.SchDoc

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TBD	DWG. NO.	* REV.	9	SHT.
REVISION	DESCRIPTION	DATE	APPROVED	

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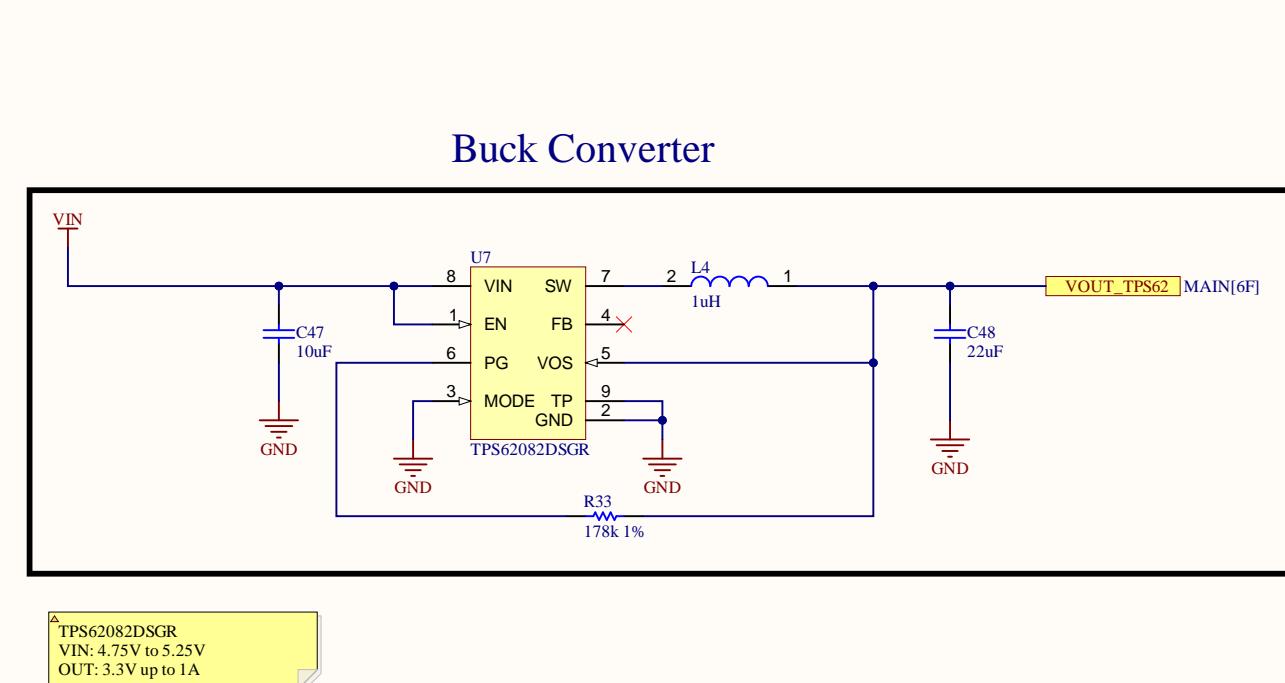
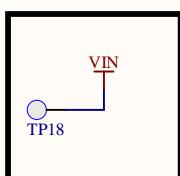
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Testpoint



APPROVALS	DATE	PROJECT	Electrical Engineering		
ENG: RTZ_HYW	02/15/22	SimonSayGame	Penn	Engineering	200 South 33rd St
DSN: RTZ_HYW	02/15/22		UNIVERSITY OF PENNSYLVANIA	Philadelphia	PA, 19104
CHK: RTZ_HYW	02/15/22	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	1.0
TITLE					
BUCK CONVERTER					
REFERENCE DOCUMENTS		SIZE	CAGE CODE	DWG NO.	REV
BOM: *		TBD		TBD	*
ASSY DWG: TBD					
FAB DWG: TBD					
PCB DWG: TBD					
SCALE: NA	FILE NAME	Buck converter.SchDoc	SHEET	9	OF 11

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TBD	DWG. NO.	* REV.	10 SHT.	
REVISION	DESCRIPTION	DATE	APPROVED	

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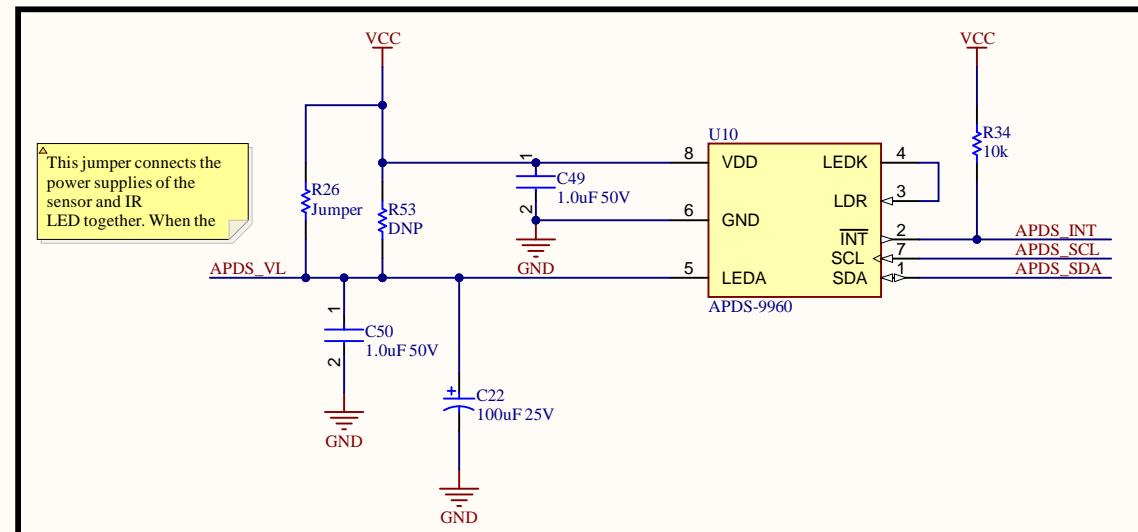
B

B

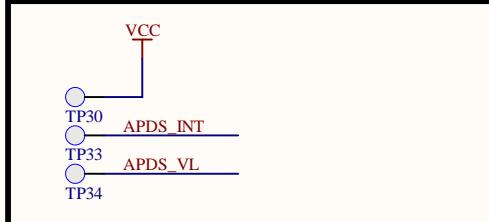
A

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Gesture Sensor



Testpoint



APPROVALS	DATE	PROJECT	GESTURE SENSOR		
ENG: RTZ_HYW	02/15/22	SimonSayGame	Penn Engineering	Electrical Engineering	200 South 33rd St
DSN: RTZ_HYW	02/15/22		University of Pennsylvania	Philadelphia	PA, 19104
CHK: RTZ_HYW	02/15/22		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM: 1.0
REFERENCE DOCUMENTS					
BOM: *					
ASSY DWG: TBD			SIZE	CAGE CODE	DWG NO.
FAB DWG: TBD			B	TBD	TBD
PCB DWG: TBD			REV	*	
SCALE: NA	FILE NAME	Gesture_Sensor.SchDoc	SHEET	10	OF 11

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REVISION	DESCRIPTION	DATE	APPROVED

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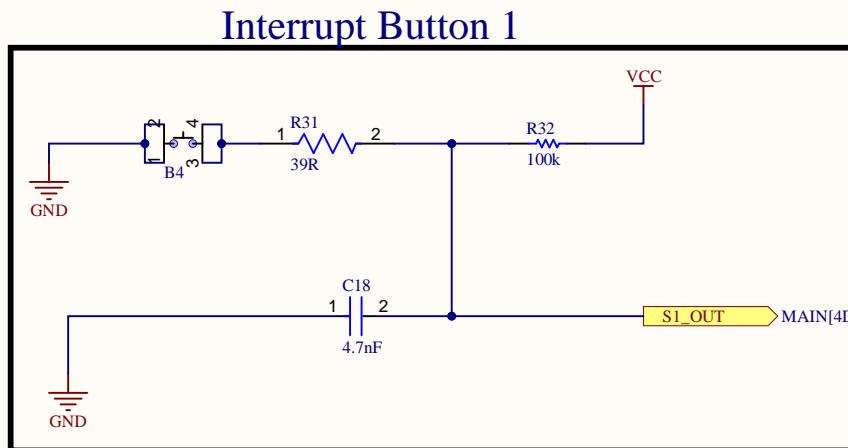
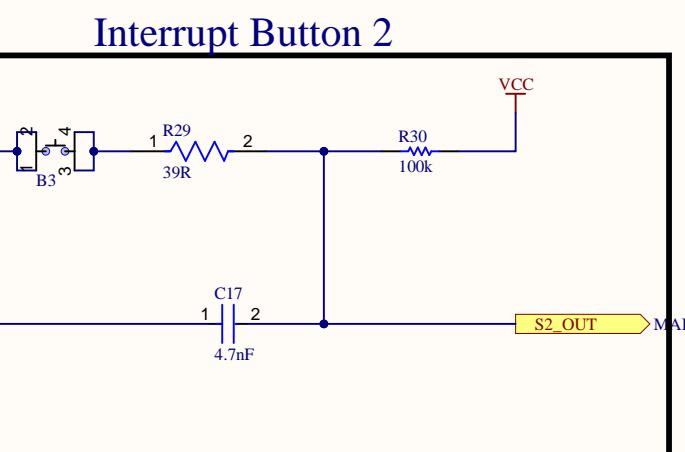
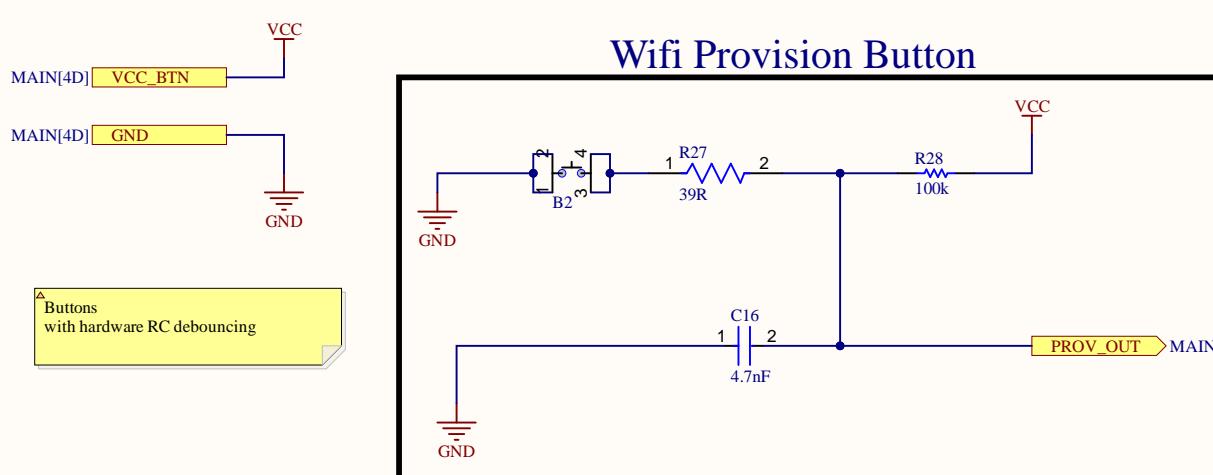
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APPROVALS	DATE	PROJECT	Electrical Engineering		
ENG: RTZ_HYW	02/15/22	SimonSayGame	Penn	Engineering	200 South 33rd St
DSN: RTZ_HYW	02/15/22		University of Pennsylvania		Philadelphia PA, 19104
CHK: RTZ_HYW	02/15/22				DESIGN ITEM: 1.0
TITLE					
BUTTONS					
REFERENCE DOCUMENTS	*	SIZE	CAGE CODE	DWG NO.	REV
BOM:	*	TBD	TBD	TBD	*
ASSY DWG:	TBD	FAB DWG:	TBD	PCB DWG:	TBD
FILE NAME	button1.SchDoc	SCALE:	NA	SHEET	11 OF 11

Manufacturing Notes

Four (4) Layers

Dimensions: 60mm x 60mm

Thickness: 0.062"

Material: FR4

All layers are unmirrored - should be able to "see straight through"

Scoring: none

Finished Thickness : 0.062 inches

Surface Finish : ENEPIG

Gold Fingers : No

Outer Layer Finish Copper : 1 Oz

Inner Copper : 0.5 oz Inners

Number of Holes Per Board:

Minimum Hole Size : 0.008 Inches or more

Minimum Trace (Outer layer) : 0.006 Inches

Minimum Space (Outer layer) : 0.006 Inches

Minimum Trace (Inner layer) : 0.006 Inches

Minimum Space (Inner layer) : 0.006 Inches

Solder Mask : Yes, Solder Mask Sides : Top and Bottom

Solder Mask Color : Green

Solder Mask Type : LPI

Solder Mask Finish : Standard (Semi-Gloss)

Silk Screen : Yes

Silk Screen Sides : Both

Silk Screen Color : White

Internal Slots : None

Counter Sink : No

Counter Bore : No

Edge Plating : No

Route and Retain : Yes

Scoring : Yes

Controlled Impedance : None

Controlled Dielectric : No

Thru-Hole Via in Pad : No

Thickness Tolerance : Plus or Minus 10%

Logo Allowed : In copper or silk screen

UL Marking Required : Yes

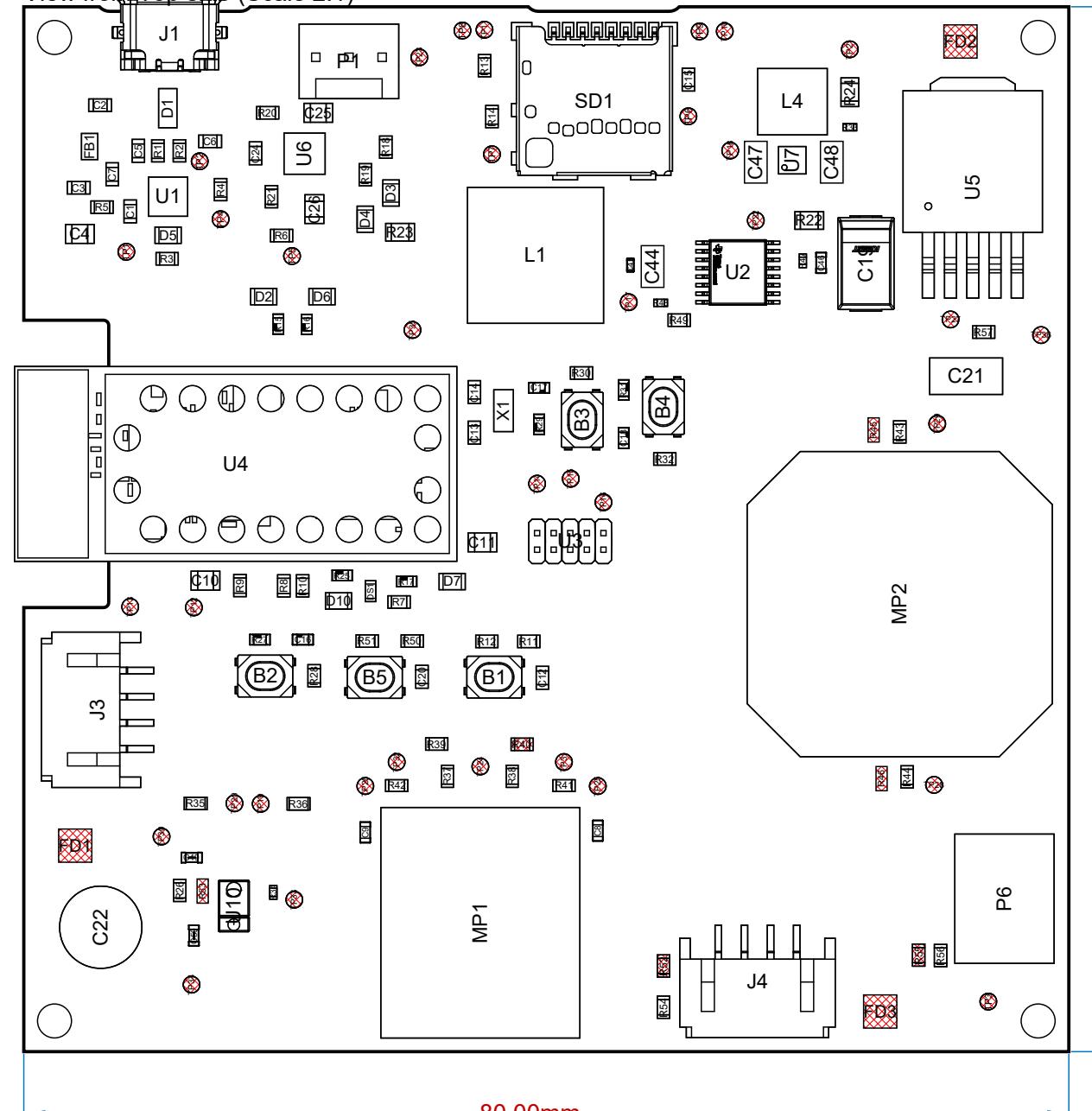
Rohs Marking : Yes

ITAR? : No

Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Surface Material	Top Overlay			Legend	GTO
	Copper	Top Solder	0.03mm(1mil)	Solder Resist	Solder Mask	GTS
		Top Layer	0.04mm(2mil)		Signal	GTL
	Prepreg		<i>0.33mm(13mil)</i>	PP-006	Dielectric	
	CF-004	GroundPlane	0.02mm(1mil)		Signal	G1
			<i>0.71mm(28mil)</i>	Core-009	Dielectric	
	Core	PowerPlane	0.02mm(1mil)		Signal	G2
	CF-004		<i>0.33mm(13mil)</i>	PP-006	Dielectric	
	Prepreg	Bottom Layer	0.04mm(2mil)		Signal	GBL
	Copper		<i>0.33mm(13mil)</i>	PP-006	Solder Mask	GBS
	Surface Material	Bottom Solder	0.03mm(1mil)	Solder Resist	Legend	GBO
		Bottom Overlay				
	Total thickness: 1.53mm(60mil)					

View from Top side (Scale 2:1)



80.00mm

.lt

PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: =PCB_ENGINEER

DESIGNER: =PCB_DESIGNER

CHECKER: =PCB_CHECKER

REFERENCE DOCUMENTS

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
TM

Electrical Engineering
200 South 33rd St
Philadelphia
PA, 19104

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

=PCB_TITLE_1
=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO

REV: 1 OF 10

SCALE: FILE NAME: StarterBoardFabrication.PCDBdwf

HEET: 1 OF 10

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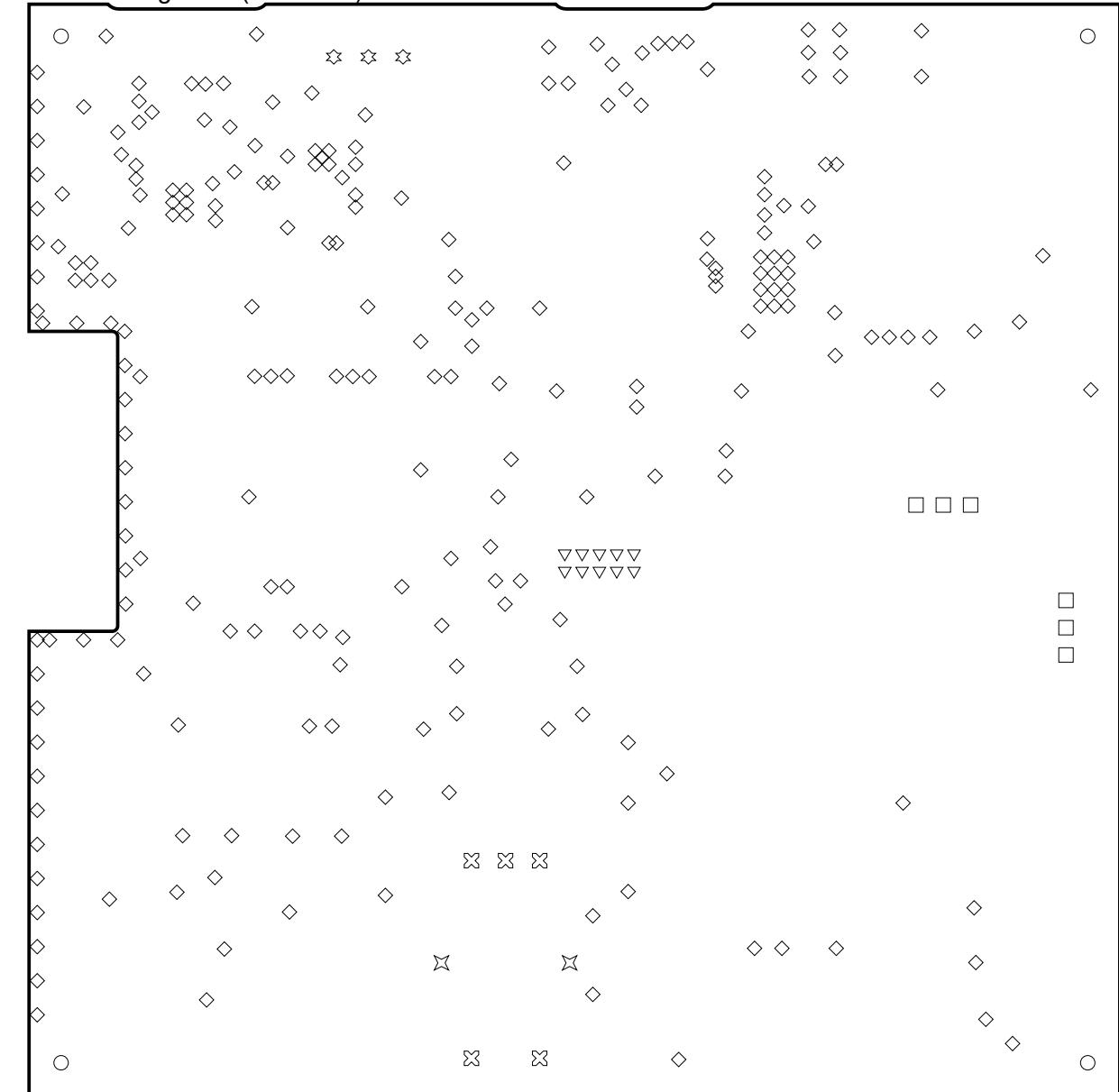
REV STATUS OF SHEETS		REV									
SHEET											

REVISIONS		DESCRIPTION	DATE	APPROVED

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
◇	239	0.20mm	Plated	
▽	10	0.65mm	Plated	
□	6	0.90mm	Plated	
☒	5	1.20mm	Plated	
⊛	3	1.27mm	Plated	
☒	2	1.80mm	Plated	
○	4	2.70mm	Plated	
269 Total				

Drill Drawing View (Scale 2:1)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: =PCB_ENGINEER =PCB_ENGINEER

DESIGNER: =PCB_DESIGNER =PCB_DESIGNER

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
TM

 Electrical Engineering
 200 South 33rd St
 Philadelphia
 PA, 19104

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: =PCB_TITLE_1

=PCB_TITLE_2

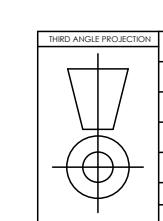
SIZE: CAGE CODE: DWG NO:

B =CAGE_CO

REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf

SHEET: 2 OF 10



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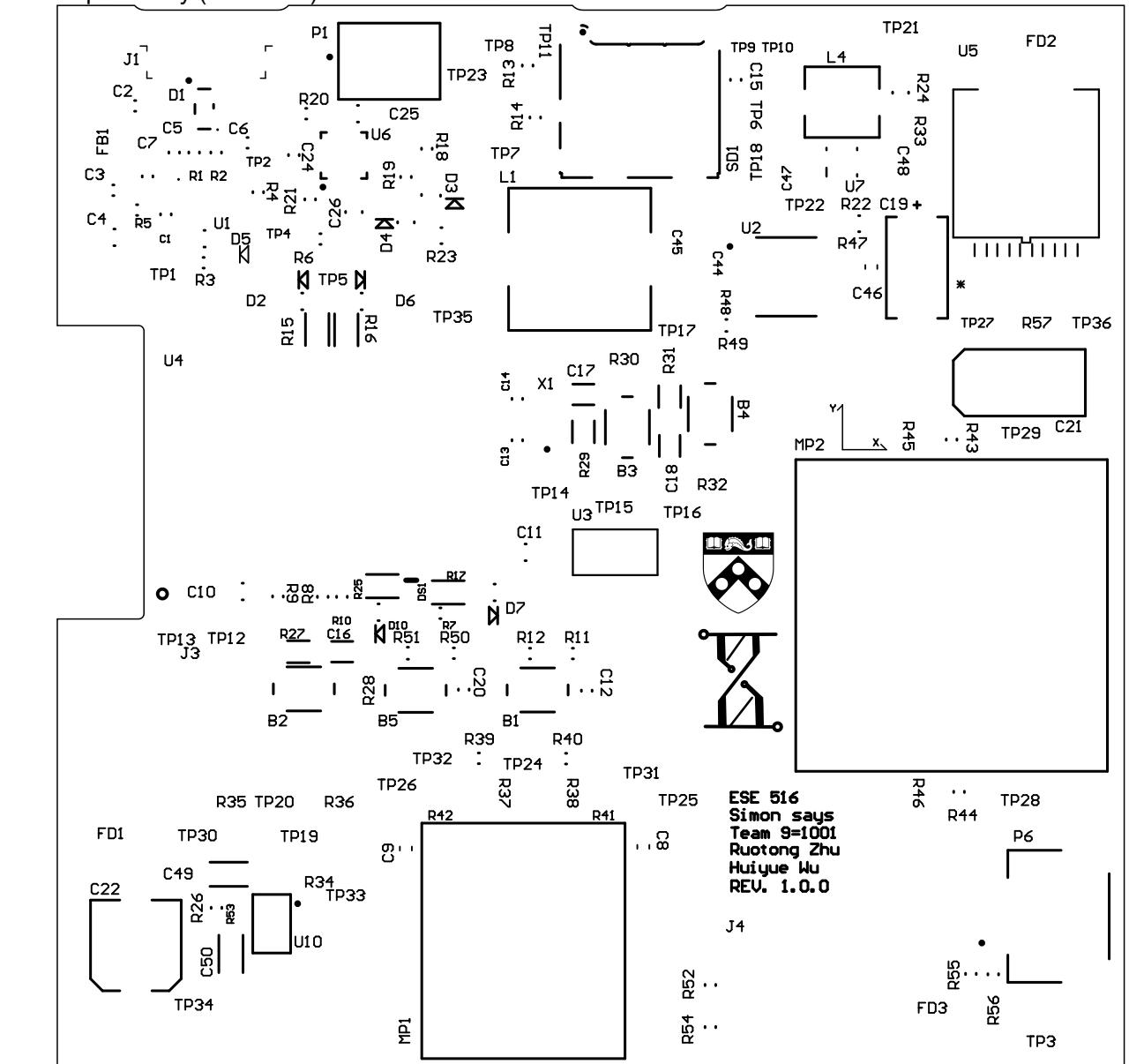
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REV STATUS OF SHEETS		REV						
SHEET								

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Overlay (Scale 2:1)



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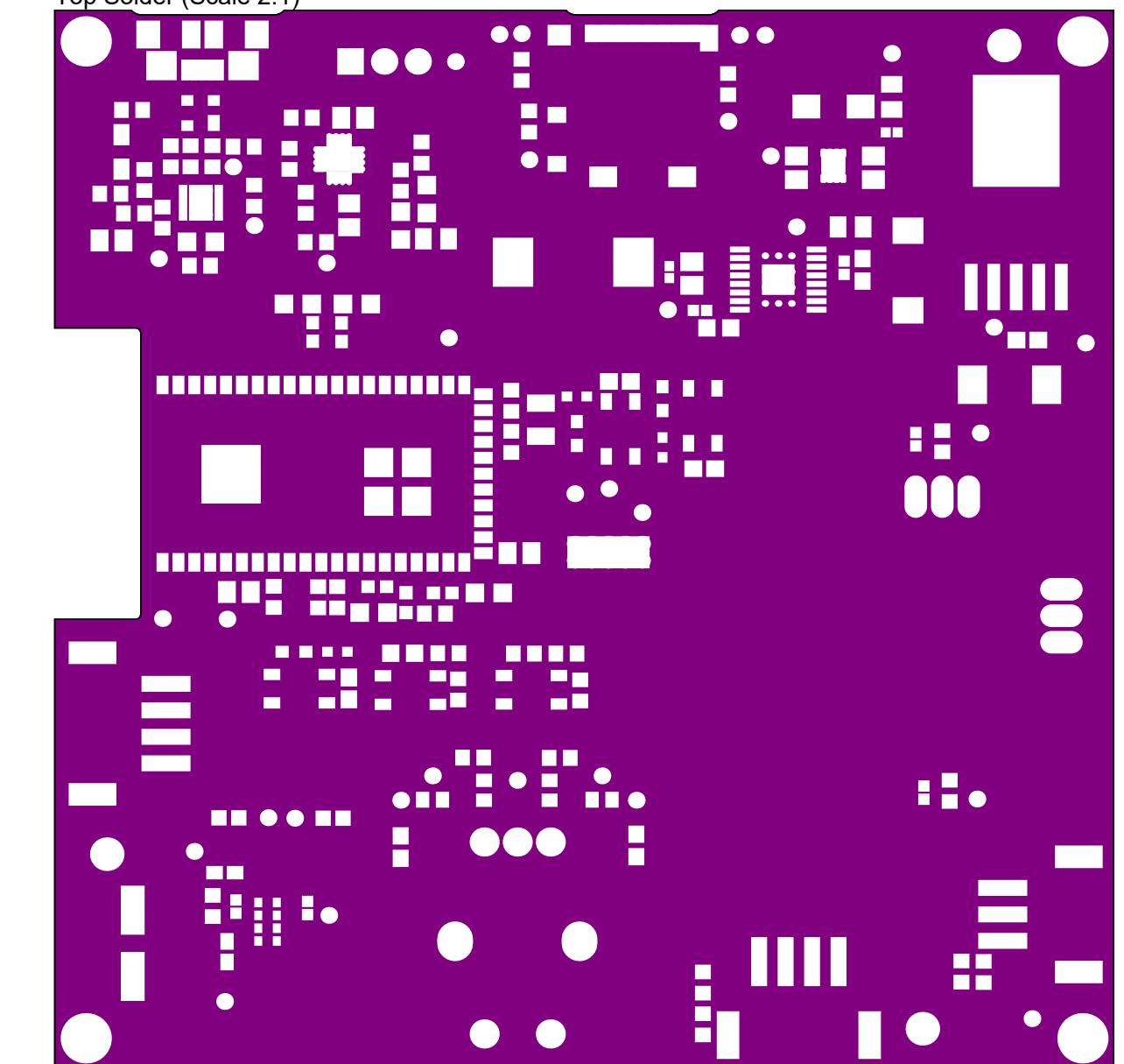
F

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REV STATUS OF SHEETS		REV					DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET								

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Solder (Scale 2:1)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium Electrical Engineering 200 South 33rd St Philadelphia PA, 19104
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEER		
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNER		
CHECKER: =PCB_CHECKER	=PCB_CHECKER		
Reference Documents			DESIGN ITEM: .Item
BOM DOC: =DOC_NO_BOM			DESIGN ITEM REVISION: .ItemRevision
ASSY DOC: =DOC_NO_FAB_DWG			TITLE: =PCB_TITLE_1
SCH DOC: =DOC_NO_SCH_DWG			=PCB_TITLE_2
PCB DOC: =PCB_DWG_NO			SIZE: CAGE CODE: DWG NO:
APPLICATION			B =CAGE_CO REV:
			SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 4 OF 10

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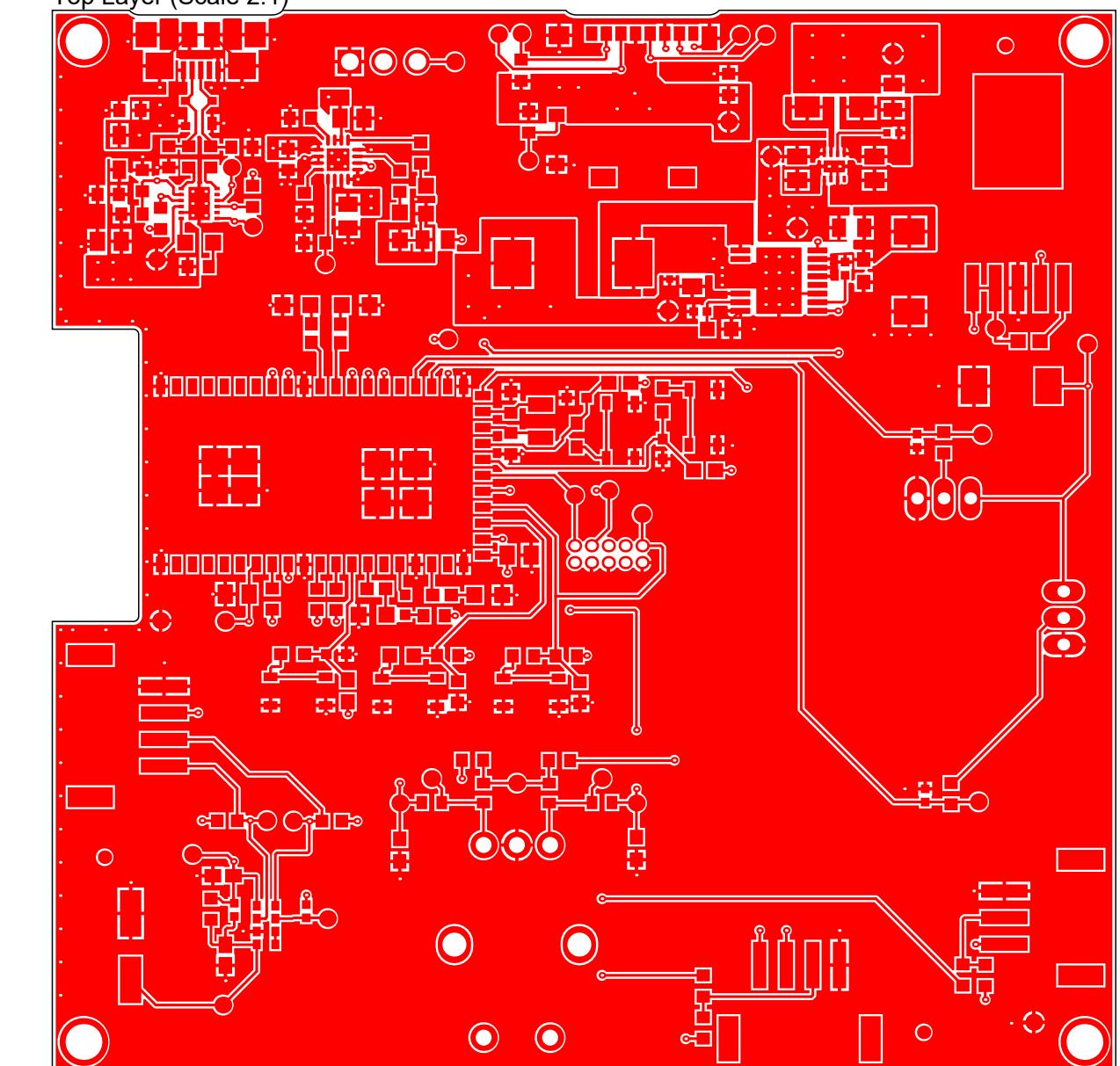
E

F

REV STATUS OF SHEETS		REV					DWG NO.: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET								

REVISIONS	
DESCRIPTION	DATE

Top Layer (Scale 2:1)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE
ENGINEER: =PCB_ENGINEER =PCB_ENGINEER

DESIGNER: =PCB_DESIGNER =PCB_DESIGNER

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

TITLE: =PCB_TITLE_1

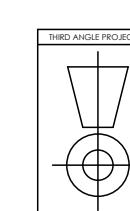
=PCB_TITLE_2

SIZE: CAGE CODE: DWG NO:

B =CAGE_CO REV:

SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 5 OF 10

Alti**um**™ Electrical Engineering
200 South 33rd St
Philadelphia
PA, 19104



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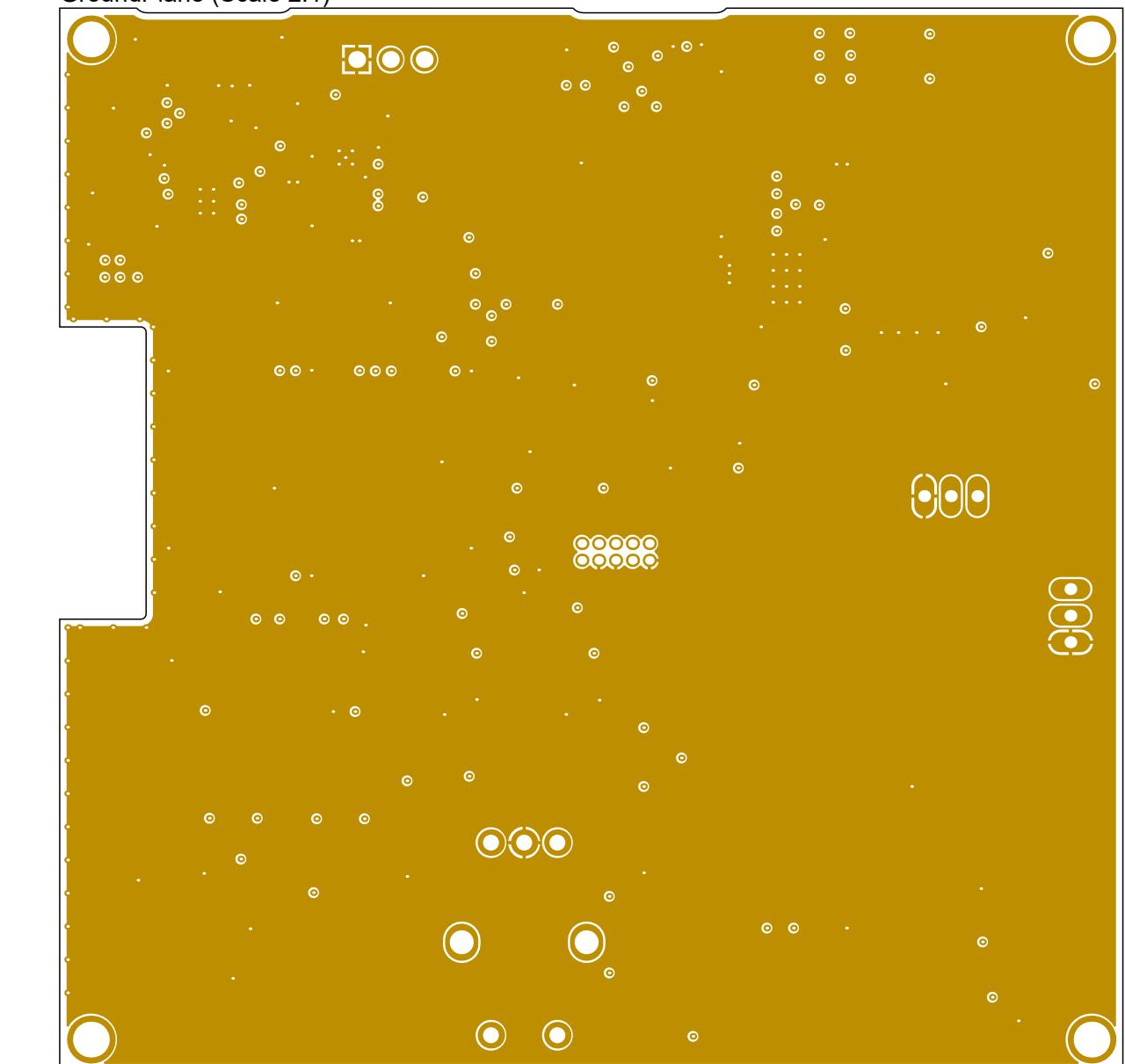
F

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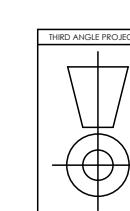
DWG NO:		=DOC_NO_ASSY_DWG		REV:	.lfe	
REV STATUS OF SHEETS		SHEET				
					ZONE	REV

REVISIONS		
DESCRIPTION	DATE	APPROVED

GroundPlane (Scale 2:1)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium TM	Electrical Engineering		
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEER			200 South 33rd St		
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNER			Philadelphia		
CHECKER: =PCB_CHECKER	=PCB_CHECKER			PA, 19104		
DESIGN ITEM: .Item		DESIGN ITEM REVISION: .ItemRevision				
TITLE: =PCB_TITLE_1		=PCB_TITLE_2				
BOM DOC: =DOC_NO_BOM						
ASSY DOC: =DOC_NO_FAB_DWG						
SCH DOC: =DOC_NO_SCH_DWG						
PCB DOC: =PCB_DWG_NO						
SCALE: 6 OF 10	FILE NAME: StarterBoardFabrication.PCBDwf	SHEET: 6 OF 10				



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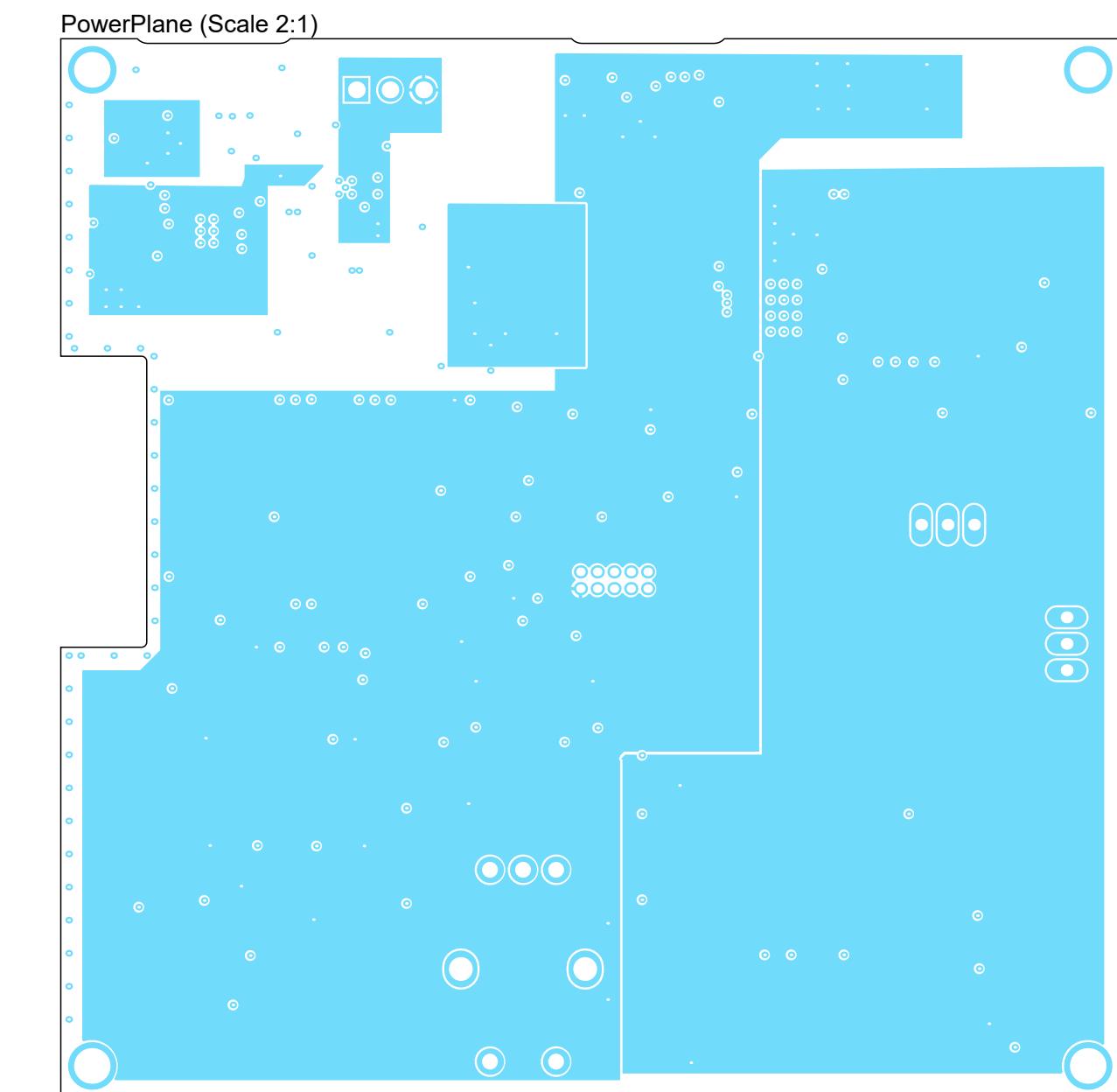
D

E

F

DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

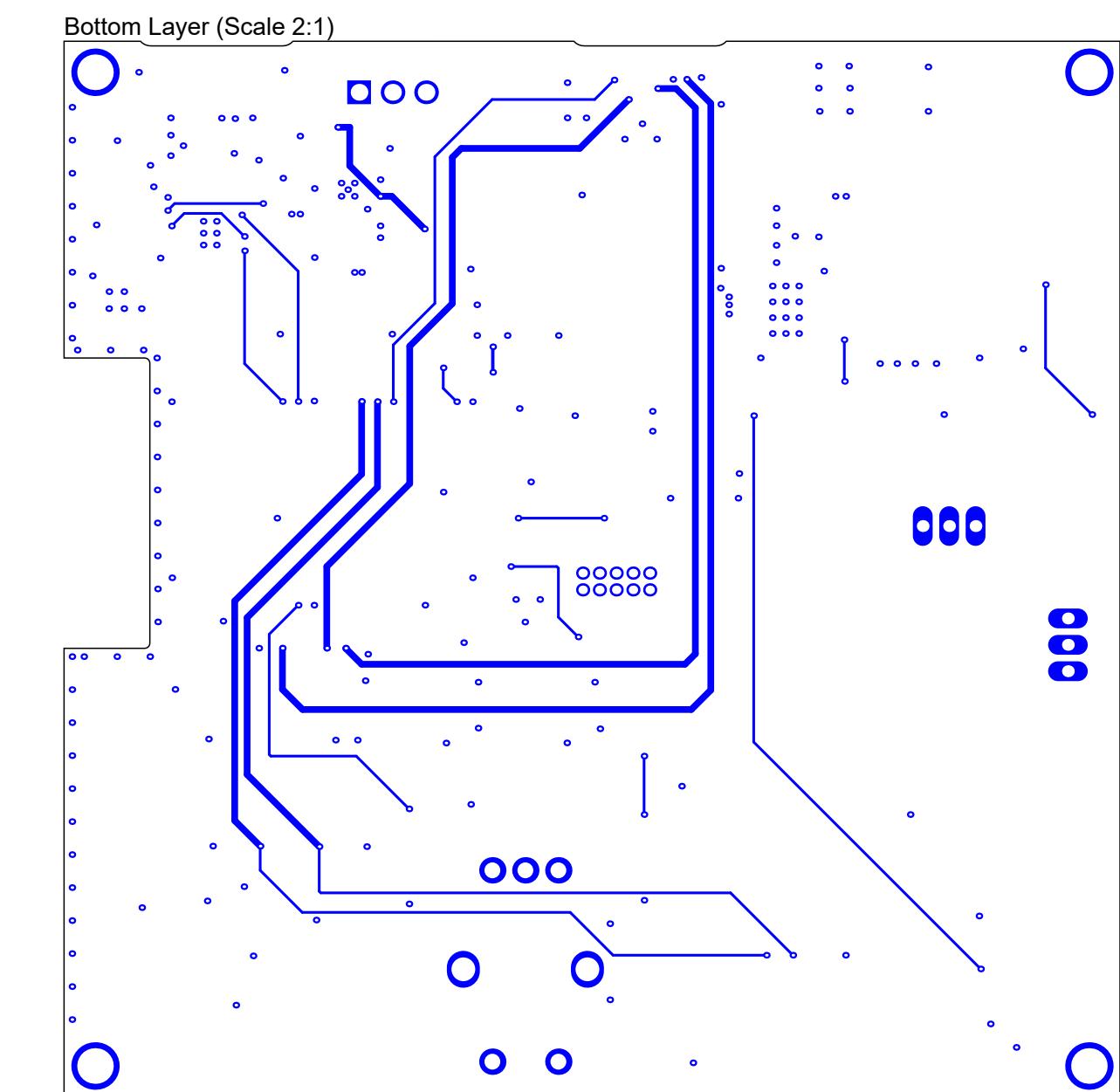
REVISIONS		
DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium Electrical Engineering 200 South 33rd St Philadelphia PA, 19104
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEER		
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNER		
CHECKER: =PCB_CHECKER	=PCB_CHECKER		
Reference Documents			DESIGN ITEM: .Item
BOM DOC: =DOC_NO_BOM			DESIGN ITEM REVISION: .ItemRevision
ASSY DOC: =DOC_NO_FAB_DWG			TITLE: =PCB_TITLE_1
SCH DOC: =DOC_NO_SCH_DWG			=PCB_TITLE_2
PCB DOC: =PCB_DWG_NO			SIZE: CAGE CODE: DWG NO: B =CAGE_CO
APPLICATION			REV: .lfe
NEXT ASSY	USED ON		SCALE: FILE NAME: StarterBoardFabrication.PCBDwf
			SHOOT: 7 OF 10

DWG NO:		REV:	=DOC_NO_ASSY_DWG		.lfe
REV STATUS OF SHEETS	SHEET				

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium Electrical Engineering 200 South 33rd St Philadelphia PA, 19104
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEER		
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNER		
CHECKER: =PCB_CHECKER	=PCB_CHECKER		
REFERENCE DOCUMENTS			DESIGN ITEM: .Item
BOM DOC: =DOC_NO_BOM			DESIGN ITEM REVISION: .ItemRevision
ASSY DOC: =DOC_NO_FAB_DWG			TITLE: =PCB_TITLE_1
SCH DOC: =DOC_NO_SCH_DWG			=PCB_TITLE_2
PCB DOC: =PCB_DWG_NO			SIZE: CAGE CODE: DWG NO: B =CAGE_CO
APPLICATION			REV: 8 OF 10
NEXT ASSY	USED ON		SCALE: FILE NAME: StarterBoardFabrication.PCBDwf
THIRD ANGLE PROJECTION			

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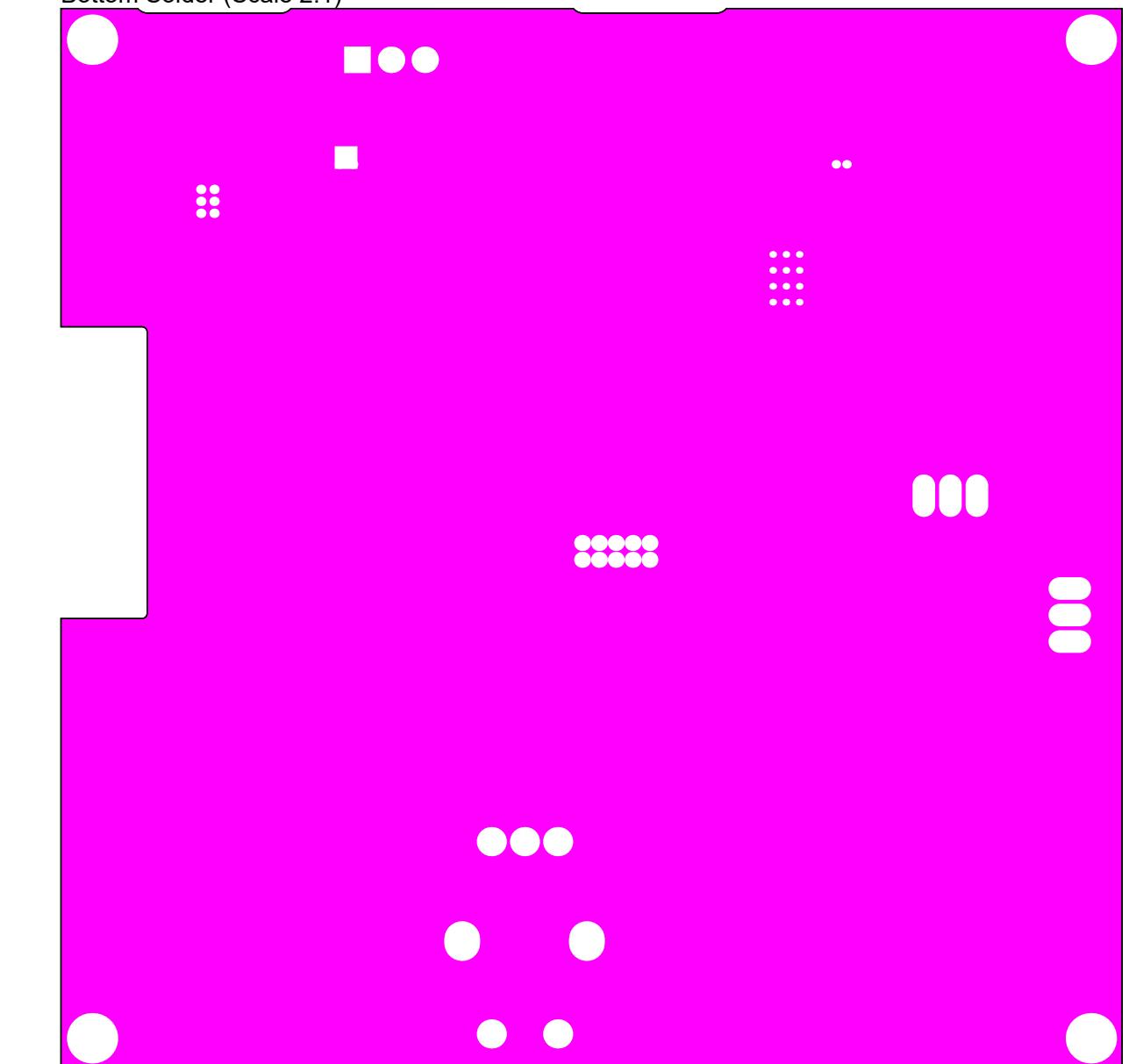
F

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DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Solder (Scale 2:1)



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium Electrical Engineering 200 South 33rd St Philadelphia PA, 19104
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEER		
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNER		
CHECKER: =PCB_CHECKER	=PCB_CHECKER		
Reference Documents		TITLE: .Item	DESIGN ITEM REVISION: .ItemRevision
BOM DOC: =DOC_NO_BOM			
ASSY DOC: =DOC_NO_FAB_DWG			
SCH DOC: =DOC_NO_SCH_DWG			
PCB DOC: =PCB_DWG_NO			
APPLICATION			
SIZE: B	CAGE CODE: =CAGE_CO	DWG NO: .lfe	REV: .lfe
FILE NAME: StarterBoardFabrication.PCBDwf			
SCALE: 9 OF 10			

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B

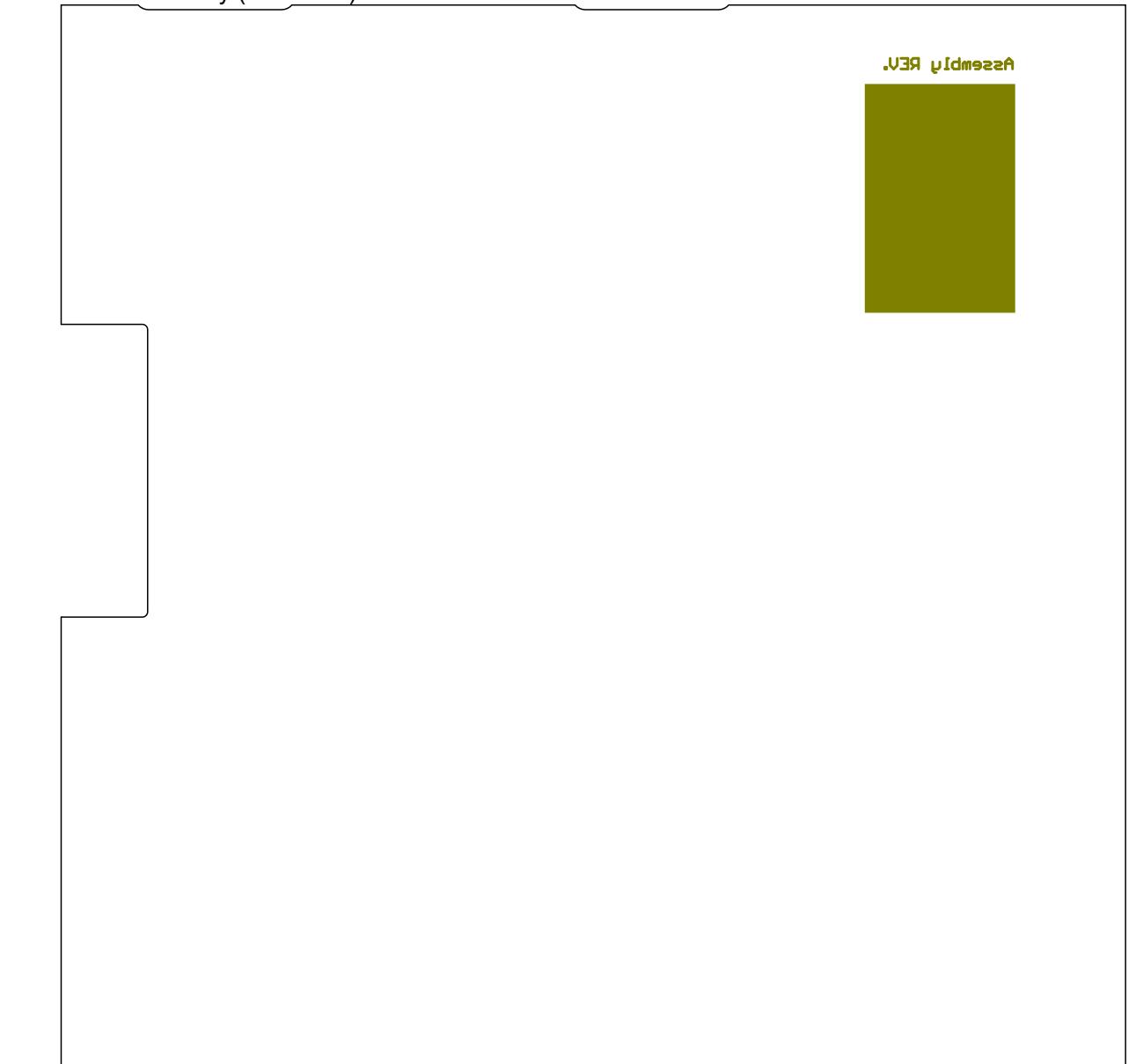
C

D

E

F

REV STATUS OF SHEETS	REV									ZONE	REV	REVISIONS	DESCRIPTION	DATE	APPROVED
SHEET															

1
Bottom Overlay (Scale 2:1)

Assembly Rev.

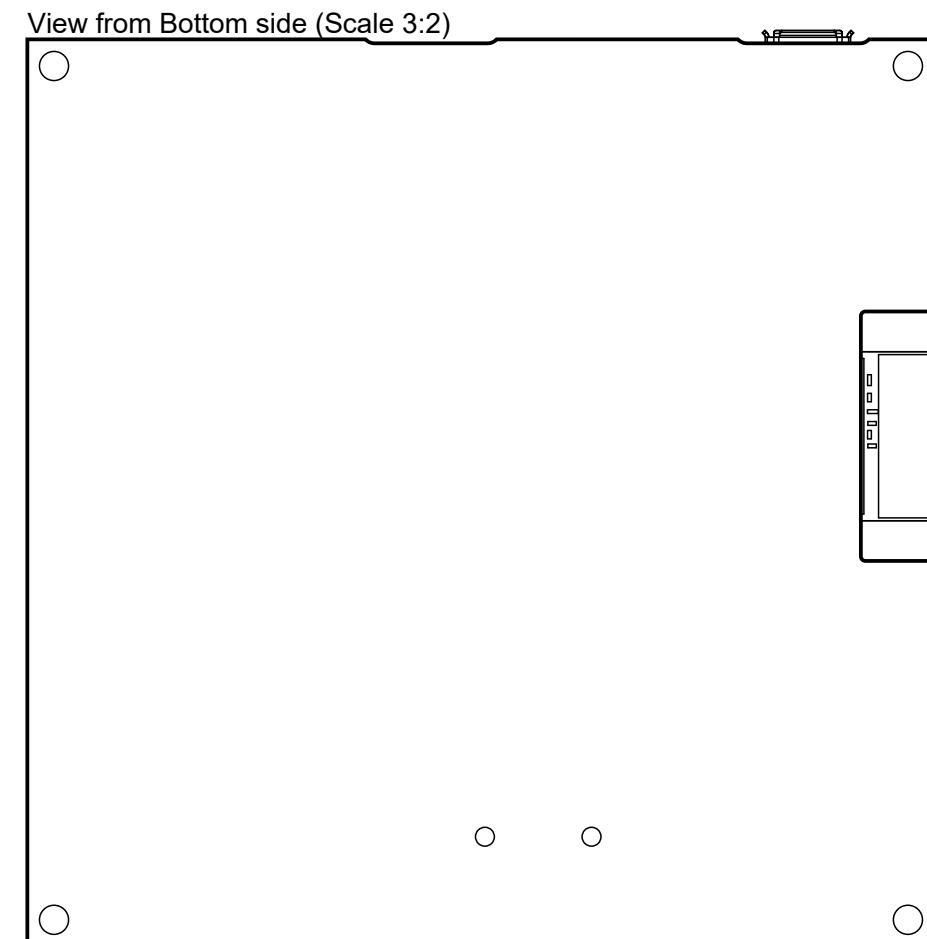
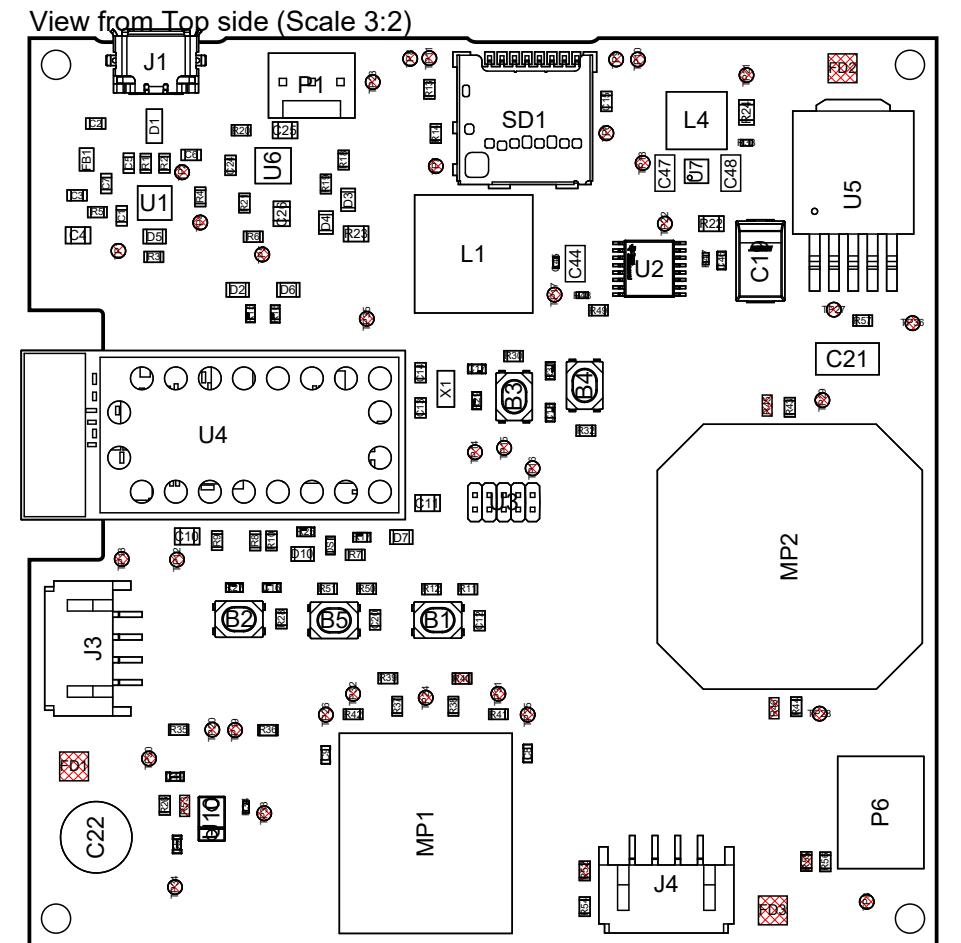
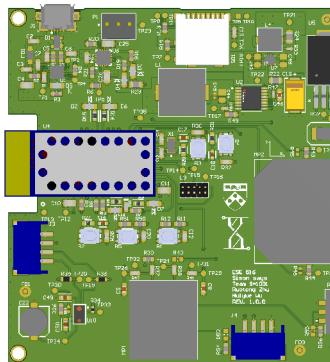


Assembly Instruction

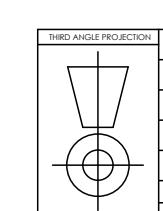
NOTES:

1. THIS ITEM IS ELECTROSTATIC SENSITIVE AND SHALL BE HANDLED ACCORDINGLY
2. WORKMANSHIP WILL CONFORM TO IPC-610 CLASS 2, IPC-7711 WILL APPLY TO ALL REQUIRED REWORK OR MODIFICATION
3. ASSEMBLY IS TO BE IDENTIFIED BY A LABEL INDICATING- SERIAL NUMBER PART NUMBER and REVISION VENDOR DATE CODE
4. THE SUPPLIED INSERTION DATA FOR THIS PCBA IS PROVIDED TO ASSIST PROGRAMMING, COMPONENT OFFSET AND ROTATION ARE RELATIVE TO THE ENGINEERING DESIGN ENVIRONMENT AND MAY NOT MATCH REEL PACKAGING OR FEED ORIENTATION, COMPONENTS, ESPECIALLY POLARIZED PARTS, MUST BE VERIFIED AGAINST THE ACTUAL PCBA DRAWING TO INSURE PROPER INSTALLATION

Realistic View



View from Right side (Scale 3:2)



PART NO: =PCB_PART_NUMBER

APPROVALS DATE

ENGINEER: =PCB_ENGINEER =PCB_ENGINEER

DESIGNER: =PCB_DESIGNER =PCB_DESIGNER

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
™

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item
DESIGN ITEM REVISION: .ItemRevision
TITLE:
=PCB_TITLE_1
=PCB_TITLE_2

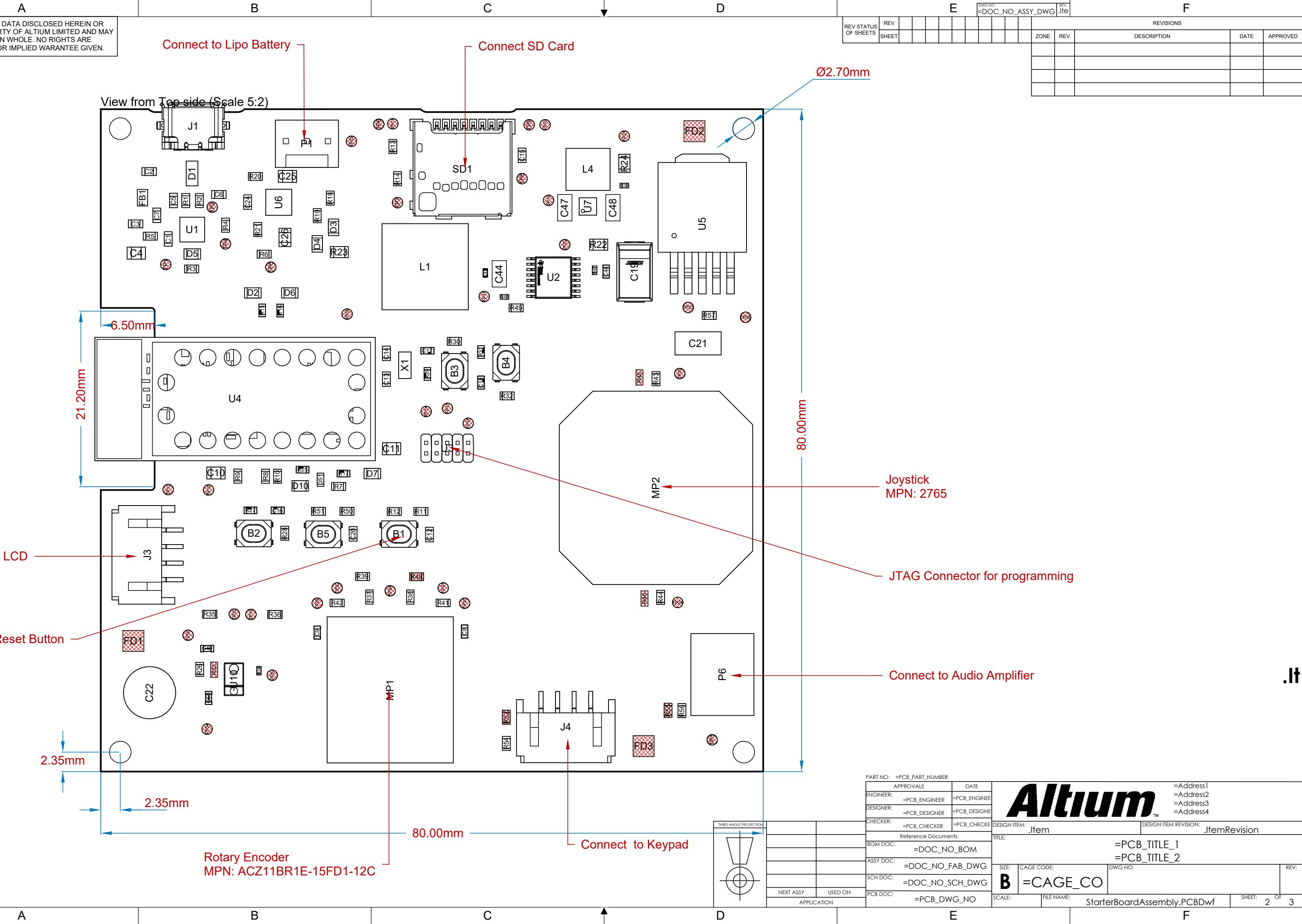
SIZE: CAGE CODE: DWG NO:
B =CAGE_CO

DWG NO:
DOC_NO_ASSY_DWG

REV:
1.0

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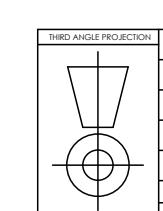


Bill Of Materials

Line #	Designator	Name	Quantity
	C46	1uF	1
	L4	1uH	1
	R47, R48	2.15M	2
	L1	3.9uH	1
	C8, C9	10nF 16V	2
	C21	10uF	1
	C44, C47	10uF	2
	C48	22uF	1
	C45	100nF	1
	C22	100uF 25V	1
	R33	178k 1%	1
	R49	390K 1%	1
	C16, C17, C18	06035C472KAT2A	3
	R37, R38, R41, R42	AF0603FR-0710KL	4
	U10	APDS-9960	1
	R27, R29, R31	CPF0603B39RE1	3
		Custom item 1	0
		Custom item 2	0
		Custom item 3	0
	R34	ERJ2RKF1002X	1
	R35, R36	ERJ-3EKF4701V	2
	MP2	Joystick	1
	U5	MIC39151-1.65WU	1
	J4	MPN-3954	1
	J3	MPN-LCD-14532	1
	R15, R16, R17, R25	RMCF0603FG1K00	4
	MP1	Rotary Encoder	1
	P6	S3B-PH-SM4-TB(LF)(SN)	1
	C19	T495D227K010ATE100	1
	R28, R30, R32, R57	TNPW0603100KBEEA	4
	U2	TPS61032PWPR	1
	U7	TPS62082DSGR	1
	C49, C50	UMK107BJ105KA-T	2
2	R20, R21	1K13 1% 0603(1608)	2
3	R3, R5, R6, R7, R18, R19	1K 1% 0603(1608)	6
4	C12, C20, C24	CAP 1uF 16V 0603(1608)	3
5	C4, C25, C26	CAP 4.7uF 16V 0805(2012)	3
6	R11, R13, R14, R50	10K 1% 0603(1608)	4
7	C2	CAP 10nF 16V 0603(1608)	1
8	C10, C11	CAP 10uF 16V 0805(2012)	2
9	C13, C14	CAP 18pF 16V 0603(1608)	2
11	R1, R2, R8, R9, R10	27R 1% 0603(1608)	5
14	C5, C6	CAP 47pF 16V 0603(1608)	2
16	C1, C3, C7, C15	CAP 100nF 16V 0603(1608)	4
17	R12, R51	100R 1% 0603(1608)	2
19	SD1	104031-0811	1
20	P1	640456-3	1
21	U3	20021111-00010T4LF	1
22	X1	ABS07-32.768KHz-T	1
24	FB1	BLM21PG221SN1D	1
25	U6	BQ24075RGTRG4	1
27	U1	FT234XD-R	1
28	R4, R26, R39, R43, R44, R54, R56	Jumper 0603(1608)	7
29	R22, R23, R24	Jumper 0805(2012)	3
30	D2, D3, D5, D6	LTST-C170CKT	4
31	D4, D7, D10	LTST-C170GKT	3
32	DS1	LTST-C191KGKT	1
34	D1	PRTR5V0U2X,215	1
35	B1, B2, B3, B4, B5	PTS810 SJK 250 SMTR LFS	5
36	U4	SAMW25H18-MR510PB	1
39	J1	ZX62R-B-5P	1

REV STATUS OF SHEETS	REV								
DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe								

REVISIONS	
ZONE	REV



PART NO: =PCB_PART_NUMBER	APPROVALS	DATE	Altium =Address1 =Address2 =Address3 =Address4
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEE		
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNE		
CHECKER: =PCB_CHECKER	=PCB_CHECKE		
DESIGN ITEM: .Item			
DESIGN ITEM REVISION: .ItemRevision			
Reference Documents			
BOM DOC:	=DOC_NO_BOM		
ASSY DOC:	=DOC_NO_FAB_DWG		
SCH DOC:	=DOC_NO_SCH_DWG		
NEXT ASSY	USED ON	PCB DOC:	
		=PCB_DWG_NO	
APPLICATION			
SIZE: B	CAGE CODE: =CAGE_CO	DWG NO: .lfe	
SCALE: 3 OF 3	FILE NAME: StarterBoardAssembly.PCBDwf	REV: .lfe	