Final Project Proposal–

Improve FIR & SDRAM

Group 12

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Outline

- ★ Step 1: Improve FIR workload
- ★ Step 2: Improve SDRAM

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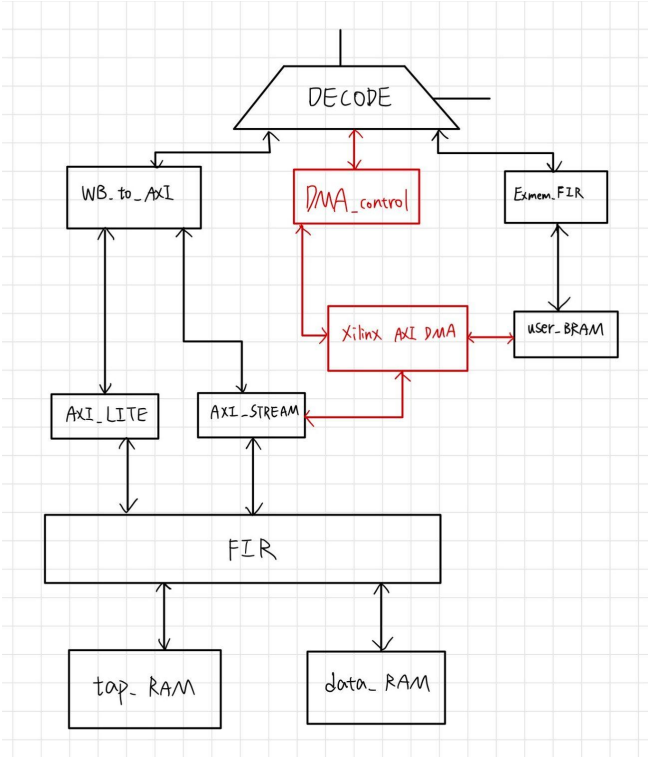
- ★ **Step 1: Improve FIR workload**
  - Add DMA engine
  - Improve speed by hardware-software co-design
- ★ Step 2: Improve SDRAM

Improve FIR – Add DMA engine

- To reduce the cycle number of CPU accessing data
- Add the DMA controller
- Directly access stream data from user bram



Improve FIR – Improve speed by hardware-software co-design

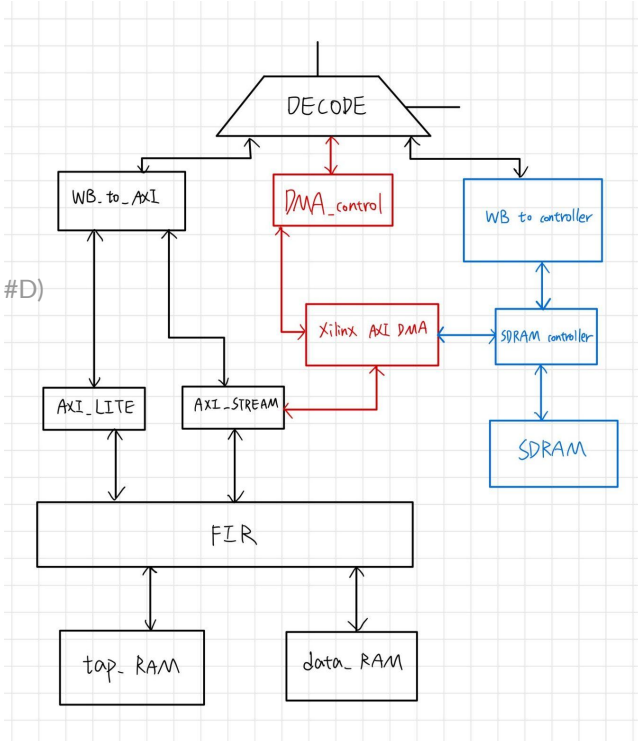
- firmware is the bottleneck:
  1. Reduce non-necessary firmware code (like some parts for checking)
  2. Make good use of cache in CPU
- Add FIFO in FIR engine

Outline

- ★ Step 1: Improve FIR workload
  - Add DMA engine
  - Improve speed by hardware-software co-design
- ★ **Step 2: Improve SDRAM**

Improve SDRAM

- Add SDRAM burst cycle
- Add prefetch (completed in Lab #D)
- Adjust linear address map (bank interleave) (completed in Lab #D)
- Add DMA & bus arbiter



Work partition

蕭方凱: decode and add configuration map

尤弘瑋: design the code between DMA and AXI_stream

葉承泓: design the code between DMA and user bram

Teamworks: integration, synthesis, implementation, report

Schedule plan & deliverables

schedule plan–

12/12~12/26: finish the design and debugging

12/26~1/10 : finish the synthesis and find any way to improve

deliverables–

Have better performance than lab4-2 and compare the result