

Wenhao Zhan

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EDUCATION

Princeton University

Aug 2021-present

Ph.D. Student, Advisor: Jason D. Lee, Yuxin Chen

- **Academic:** Overall GPA 4.00/4.00.

Tsinghua University

Bachelor of Electronic Engineering

Aug 2017-Jul 2021

- **Academic:** Major GPA 3.97/4.00, Overall GPA 3.92/4.00, rank 1/242.

RESEARCH INTERESTS

Mathematical Theory of High-Dimensional Statistics and Optimization

PUBLICATIONS&PREPRINTS

- W. Zhan, M. Uehara, W. Sun, J. D. Lee, "PAC Reinforcement Learning for Predictive State Representations", 2023. The 11th International Conference on Learning Representations
- W. Zhan, J. D. Lee, Z. Yang, "Decentralized Optimistic Hyperpolicy Mirror Descent: Provably No-Regret Learning in Markov Games", 2023. The 11th International Conference on Learning Representations.
- W. Zhan*, S. Cen*, B. Huang, Y. Chen, J. D. Lee, Y. Chi, "Policy Mirror Descent for Regularized Reinforcement Learning: A Generalized Framework with Linear Convergence", 2021. Accepted to SIAM Journal on Optimization. (*=equal contributions)
- W. Zhan, B. Huang, A. Huang, N. Jiang, J. D. Lee, "Offline Reinforcement Learning with Realizability and Single-policy Concentrability", 2022. The 35th Annual Conference on Learning Theory.
- C. Z. Lee, L. P. Barnes, W. Zhan, A. Özgür, "Over-the-Air Statistical Estimation of Sparse Models", 2021. The 2021 IEEE Global Communications Conference.
- W. Zhan, H. Tang, J. Wang, "Delay Optimal Cross-Layer Scheduling Over Markov Channels with Power Constraint", 2020. The IEEE International Symposium on Broadband Multimedia Systems and Broadcasting 2020.

TEACHING EXPERIENCE

- **Special Topics in Information Sciences and Systems: Theory of Deep Weakly Supervised Learning**
TA, Fall 2022, Princeton

HONORS&AWARDS

- Honorable mention for the 2023 Jane Street Graduate Research Fellowship
- 2017-2020 Tsinghua Academic Excellence Award
- 2018-2020 Tsinghua Scientific Research Excellence Award
- 2018-2020 National Encouragement Scholarship

TECHNICAL SKILLS

- Programming languages: C/C++, Python, Matlab, Verilog