Primitive microprocessor

for the lab project

Features

- sixteen 16-bit registers (general purpose)
- no RAM
- 16-bit instructions
  - ALU: ADD, SUB, AND, OR
  - LDA, LDB – direct register loading (by byte)
  - NOP

General instruction structure

Operation	Function	Immediate
<15>	<14:12>	<11:0>

Data processing – ALU operations

Operation	Function	WA	RB	RA
0	<14:12>	<11:8>	<7:4>	<3:0>

Data processing – register write

Operation	Function	WA	Data
0	<14:12>	<11:8>	<7:0>

Branch instruction

Operation	Function	Not used	Relative branch target
1	<14:12>	<11:8>	<7:0>

Data processing – ALU operations

Mnemonic	Operation	Function	WA	RB	RA	Description
ADD	**0**	**000**	<11:8>	<7:4>	<3:0>	R[WA] = R[RB] + R[RA]
SUB	**0**	**001**	<11:8>	<7:0>	<3:0>	R[WA] = R[RB] - R[RA]
AND	**0**	**010**	<11:8>	<7:0>	<3:0>	R[WA] = R[RB] & R[RA]
OR	**0**	**011**	<11:8>	<7:0>	<3:0>	R[WA] = R[RB] | R[RA]
NOP	**0**	**111**	X	X	X	No operation

WA – address of the register to store the result.
RB, RA – addresses of the registers
R[X] – contents of the register with address **X**

Data processing – register write

Mnemonic	Operation	Function	WA	Data	Description
LDA	**0**	**100**	<11:8>	<7:0>	R[WA][7:0] = Data - load 8 LSB bits of the register **WA** with **Data)**
LDB	**0**	**101**	<11:8>	<7:0>	R[WA][15:8] = Data - load 8 MSB bits of the register **WA** with **Data**

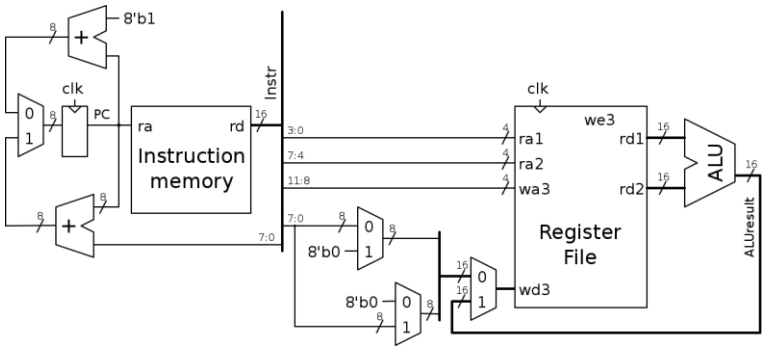
WA – address of the register to store the result.
Data – bits to be written into the register
R[WA] – register with address **WA**

Branch instructions

Mnemonic	Operation	Function	NU	Target	Description
B1	**1**	**010**	<11:8>	<7:0>	Branch if input 1 is true
BR	**1**	**100**	<11:8>	<7:0>	Always branch
BN0	**1**	**101**	<11:8>	<7:0>	Branch if input 0 is false

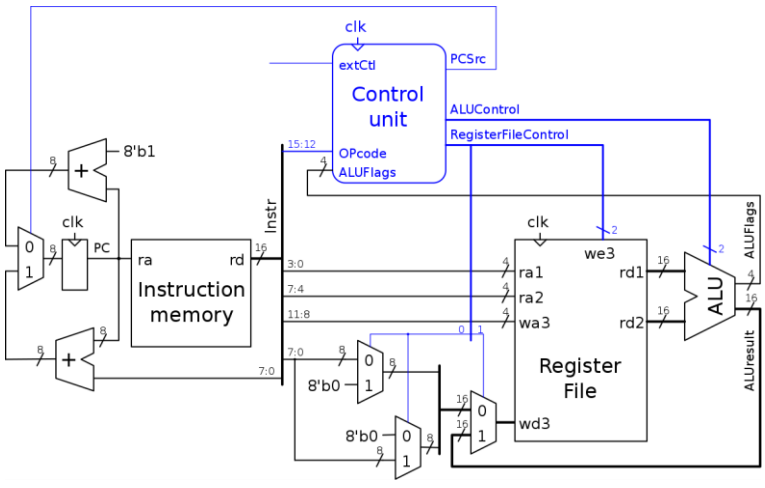
Target – address of the next instruction (relative to PC)

Other instructions can be defined by user.



Datapath

Control



Datapath

Control unit