

# 4-bit CLA Adder

## VLSI Course Project

1<sup>st</sup> Vignesh Vembar

ECE, IIIT Hyderabad

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vigneshvembar.m@students.iiit.ac.in

**Abstract**—This document is a report on the Design and Simulation of a 4-bit Carry Look Ahead Adder.

*C. Full Circuit*

### I. INTRODUCTION

### IV. NGSPICE SIMULATION

The Carry Look Ahead Adder is a digital circuit that is used to add two 4 bit binary numbers. It is faster than the Ripple Carry Adder as it generates the carry signals for all the bits at the same time.

#### A. Inverter

### II. PROPOSED DESIGN

#### A. CLA Adder

#### B. D Flip Flop

### III. VERILOG SIMULATION

#### A. CLA Adder



Fig. 1: GTKWave Plot of CLA Adder Verilog Simulation

#### B. D Flip Flop

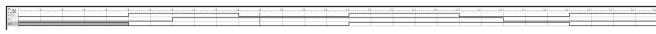


Fig. 2: GTKWave Plot of D Flip Flop Verilog Simulation

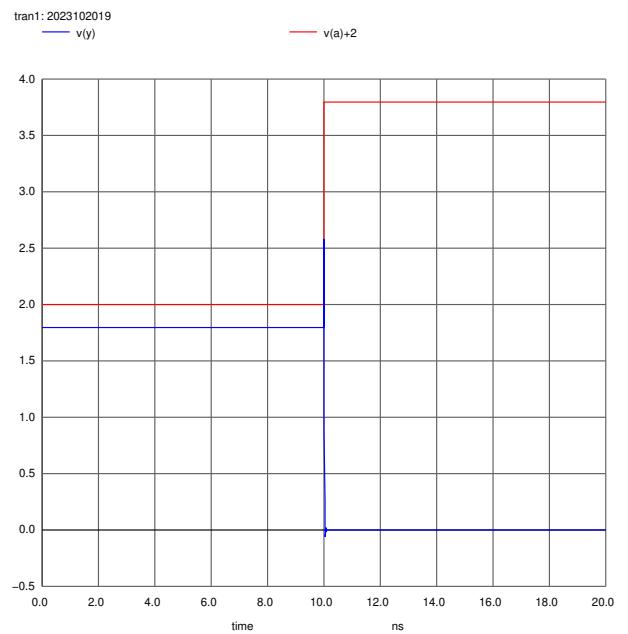


Fig. 3: NGSPICE Plot of Inverter

## B. NAND Gate

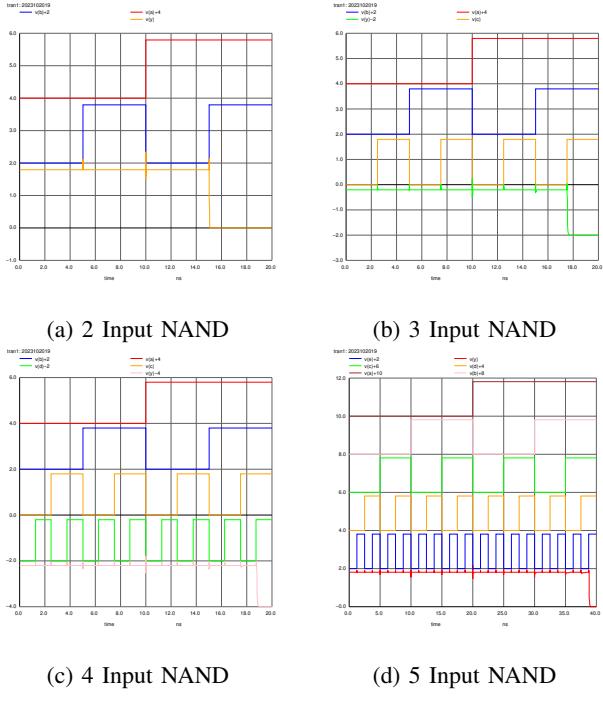


Fig. 4: NGSPICE Plot of NAND Gates

## C. NOR Gate

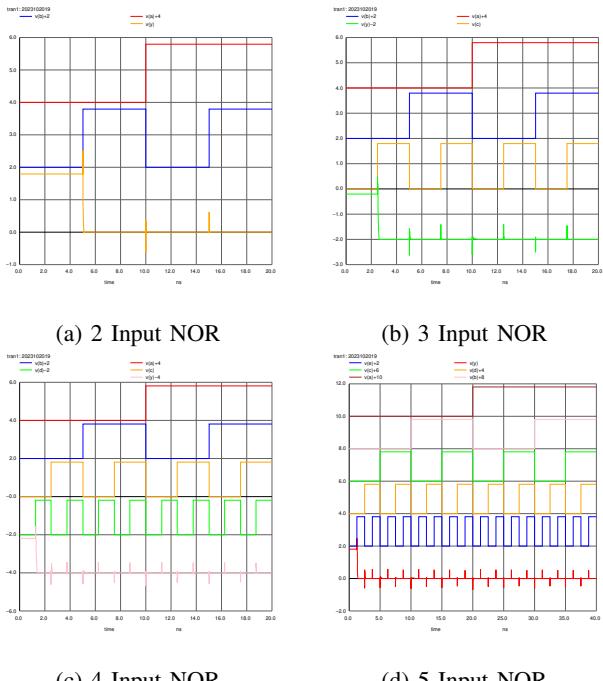


Fig. 5: NGSPICE Plot of NOR Gates

## D. XOR Gate

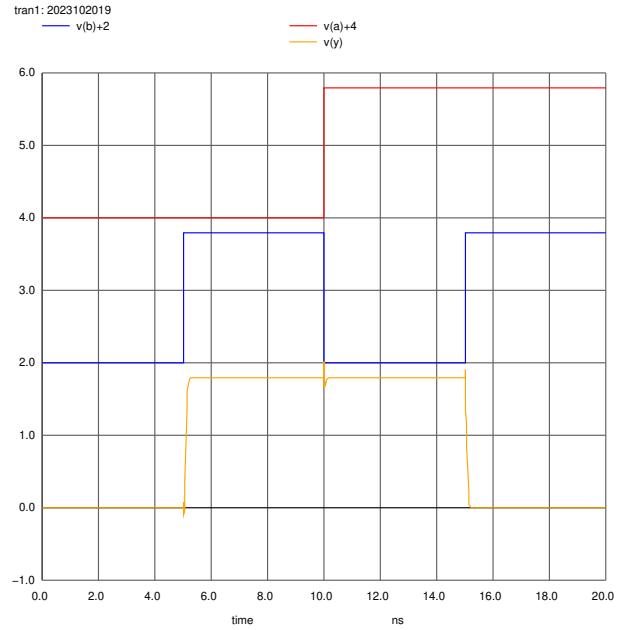


Fig. 6: NGSPICE Plot of CMOS XOR Gate

### 1) CMOS Implementation:

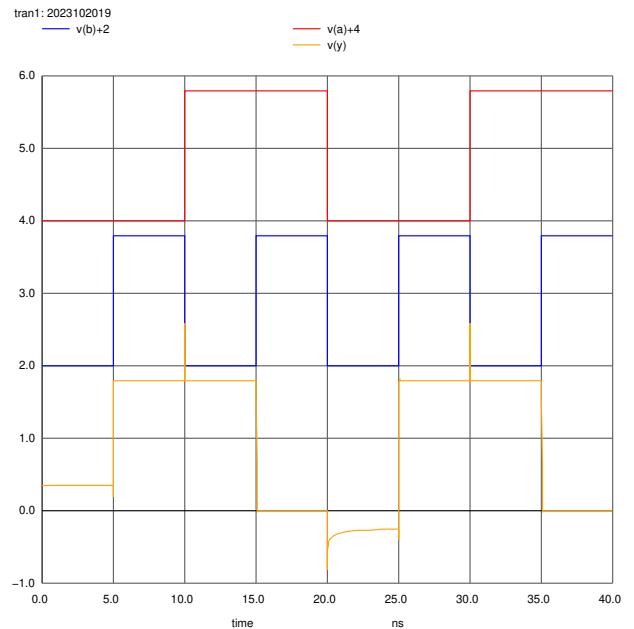


Fig. 7: NGSPICE Plot of CPTL XOR Gate

### 2) Complimentary Pass Transistor Implementation:

### E. Propagate/Generate Generator

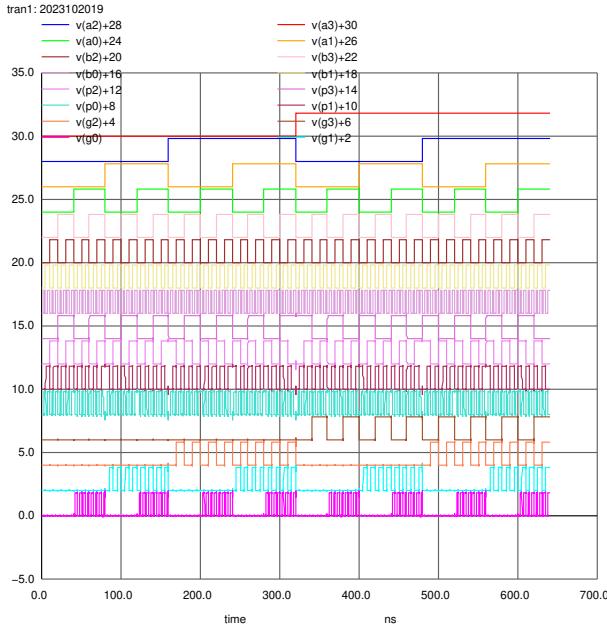


Fig. 8: NGSPICE Plot of CMOS Propagate/Generate Generator

#### 1) CMOS Implementation:

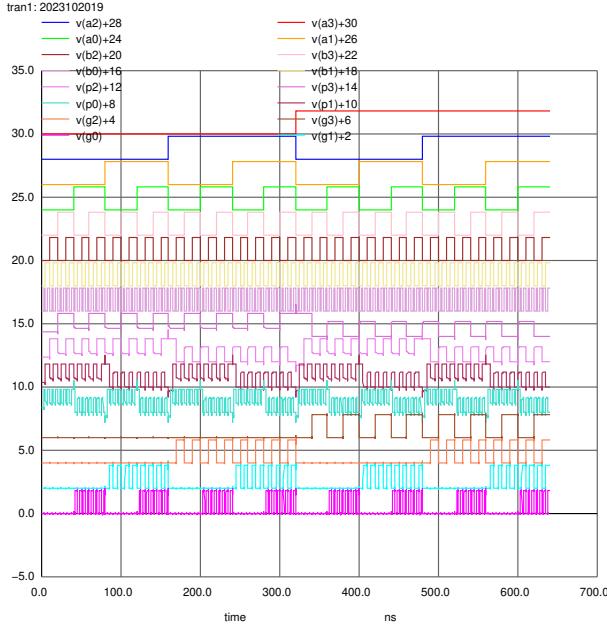


Fig. 9: NGSPICE Plot of CPTL Propagate/Generate Generator

#### 2) Complimentary Pass Transistor Implementation:

### F. Carry Look Ahead Generator

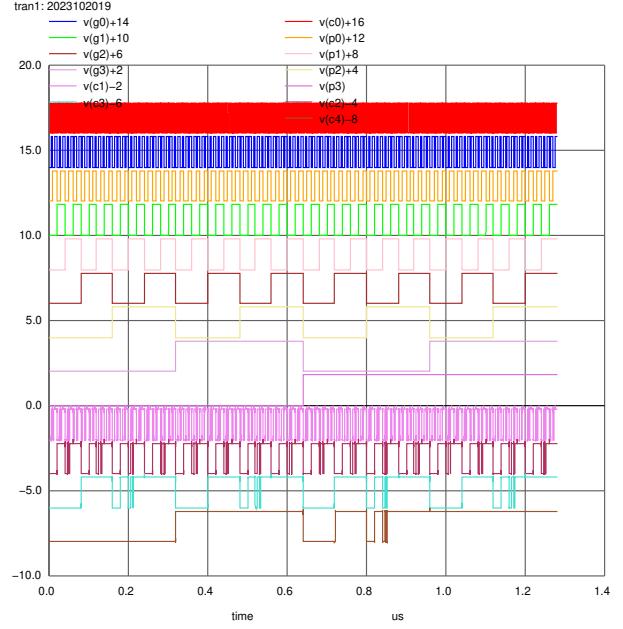


Fig. 10: NGSPICE Plot of CMOS Carry Look Ahead Generator

### G. Sum Generator

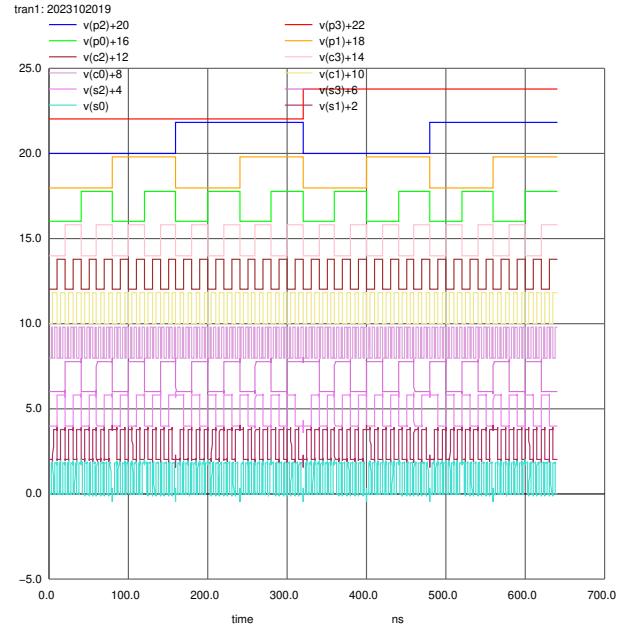


Fig. 11: NGSPICE Plot of CMOS Sum Generator

#### 1) CMOS Implementation:

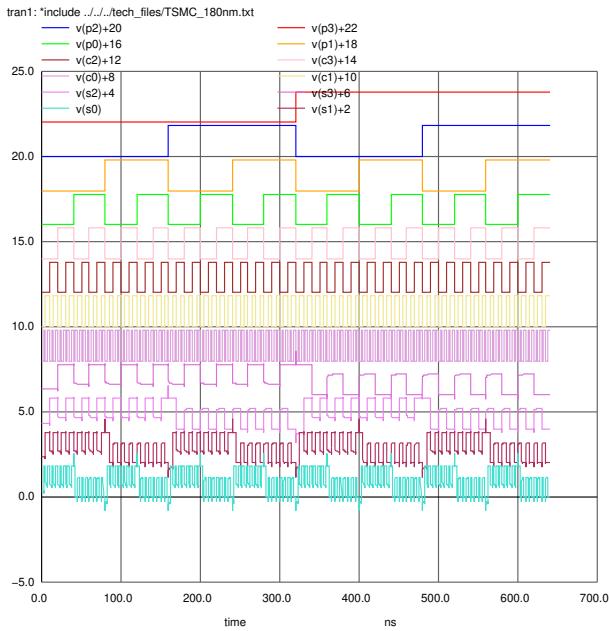


Fig. 12: NGSPICE Plot of CPTL Sum Generator

## 2) Complementary Pass Transistor Implementation:

### *H. D Flop Flop*

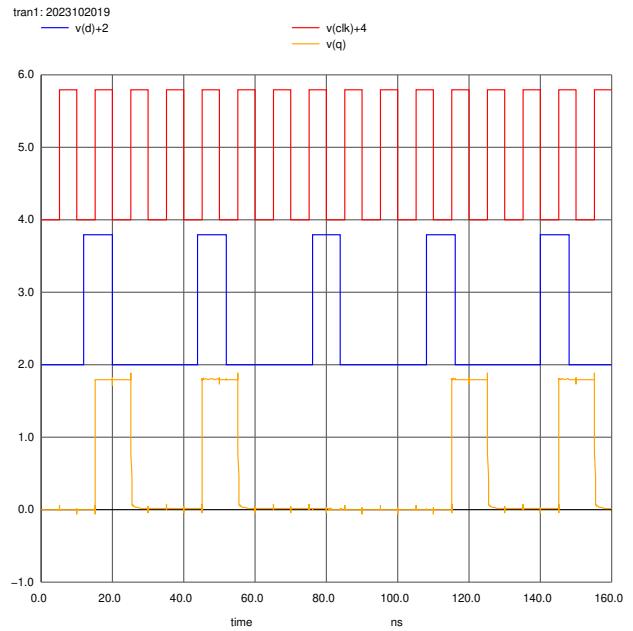


Fig. 14: NGSPICE Plot of Optimized D Flip Flop

### *2) Optimized Implementation:*

### *I. Full Circuit*

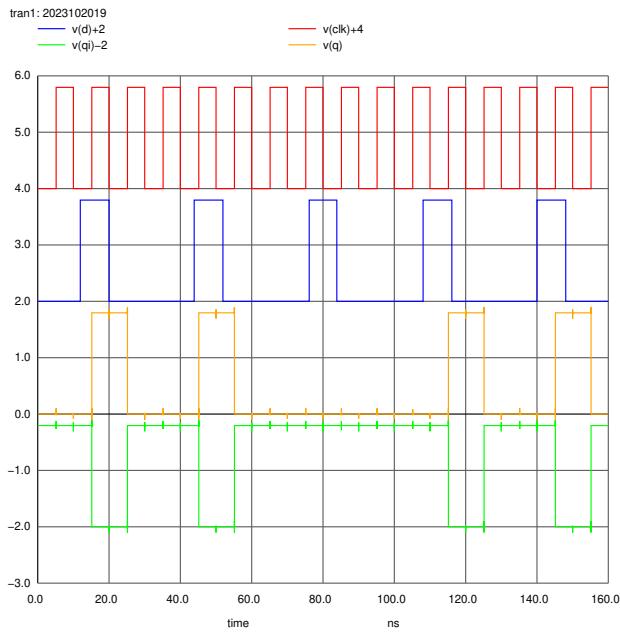


Fig. 13: NGSPICE Plot of CMOS D Flip Flop

### *1) CMOS Implementation:*

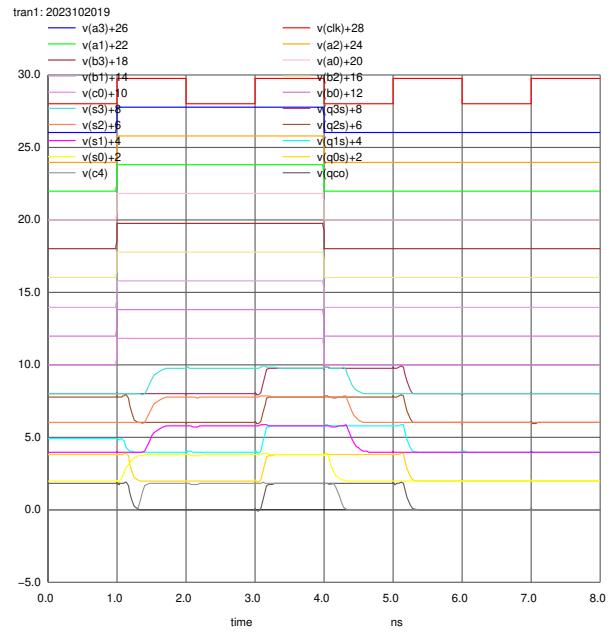


Fig. 15: NGSPICE Plot of CMOS Circuit

### *1) CMOS Implementation:*

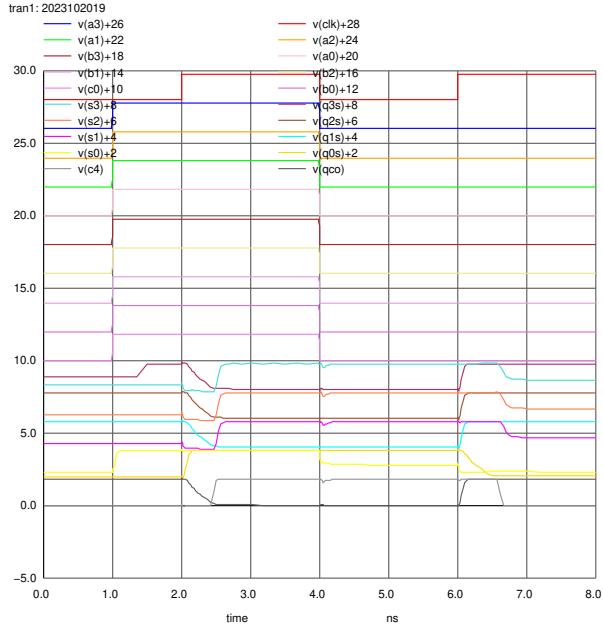


Fig. 16: NGSPICE Plot of Optimized Circuit

## 2) Optimized Implementation:

### V. MAGIC LAYOUT

#### A. Inverter

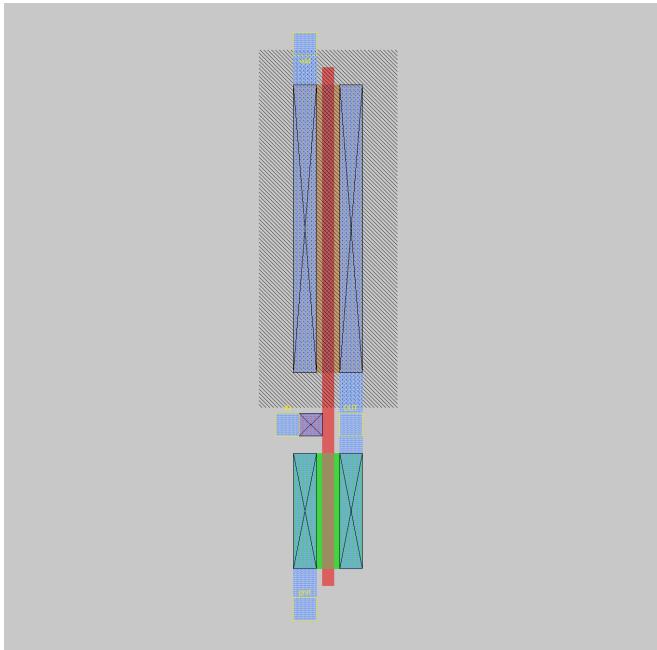


Fig. 17: MAGIC Layout of CMOS Inverter

#### B. NAND Gate

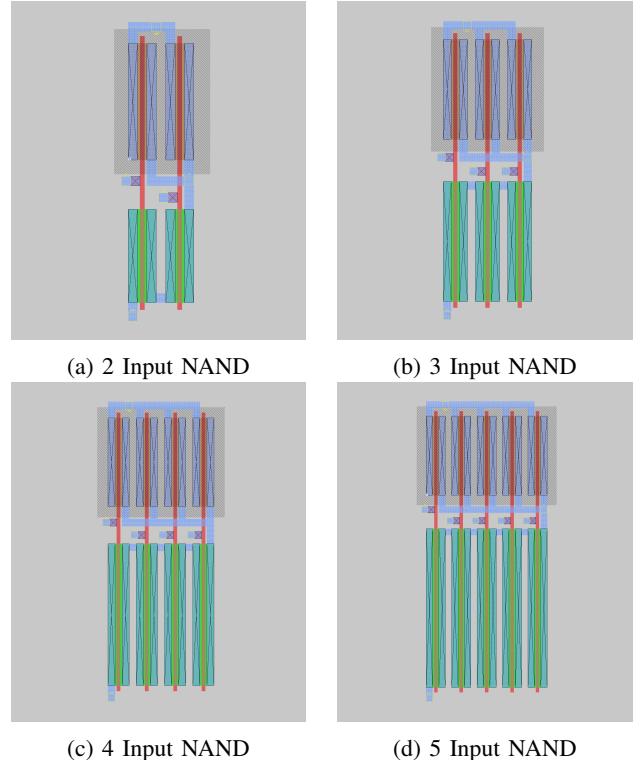


Fig. 18: MAGIC Layout of NAND Gates

#### C. NOR Gate

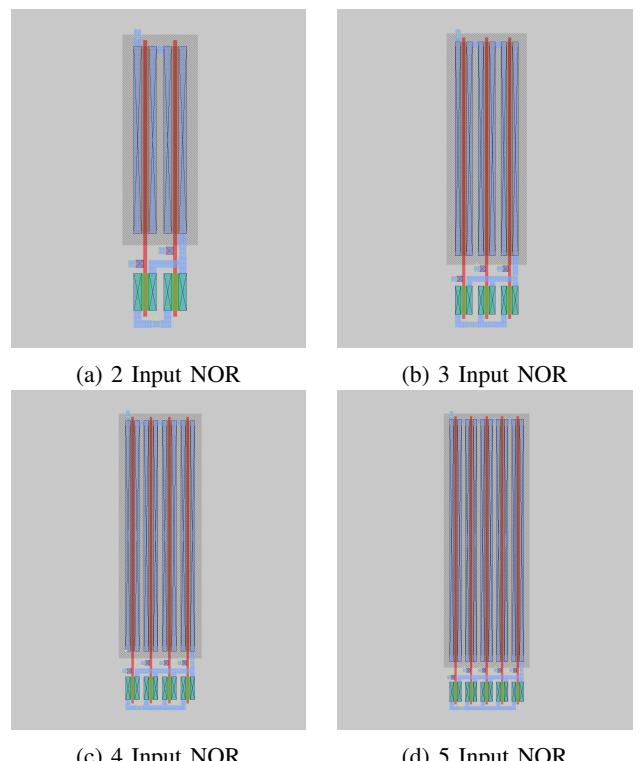


Fig. 19: MAGIC Layout of NOR Gates

D. XOR Gate

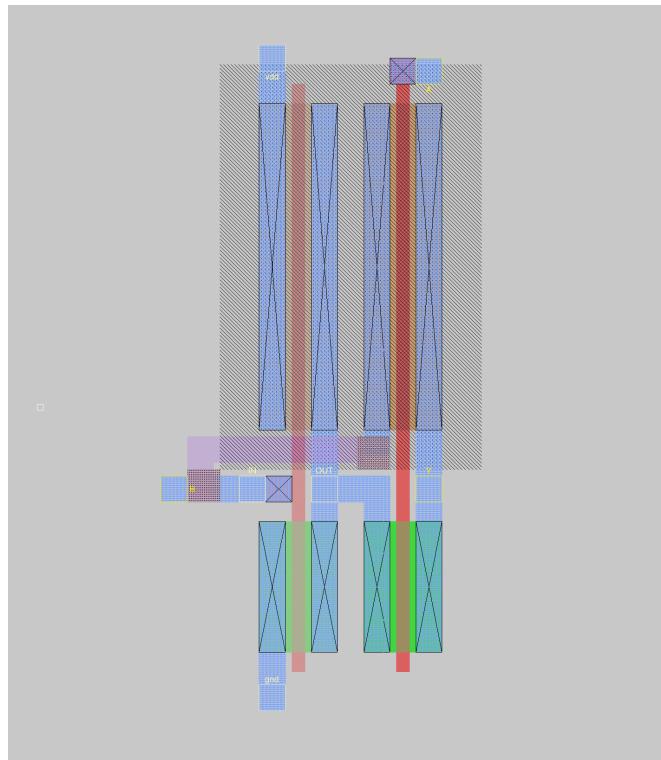


Fig. 20: MAGIC Layout of XOR Gate

E. Propagate/Generate Generator

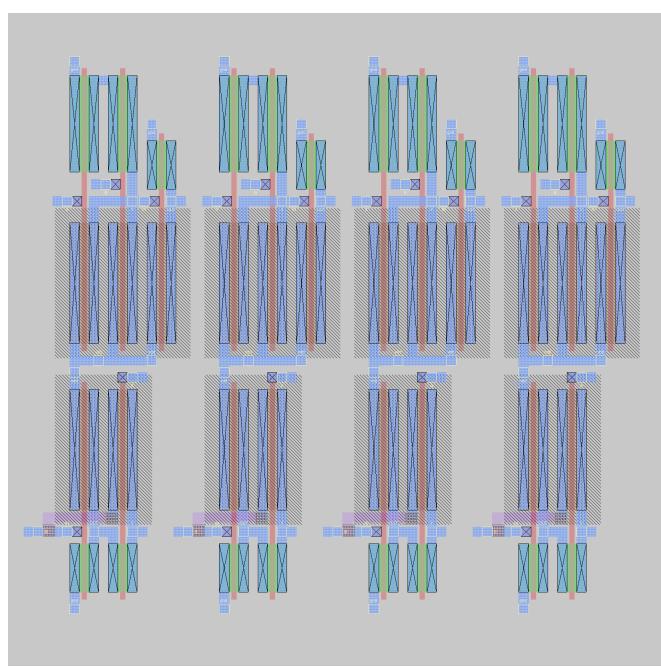


Fig. 21: MAGIC Layout of Propagate/Generate Generator

F. Carry Look Ahead Generator

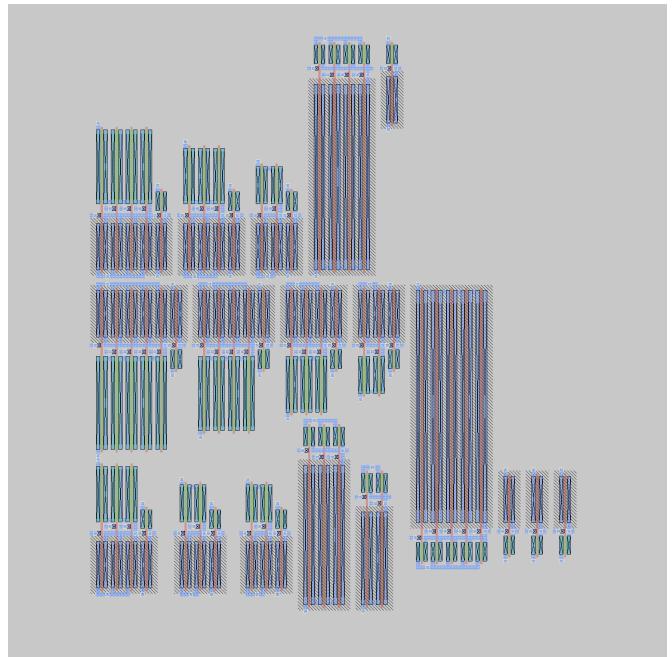


Fig. 22: MAGIC Layout of Carry Look Ahead Generator

G. Sum Generator

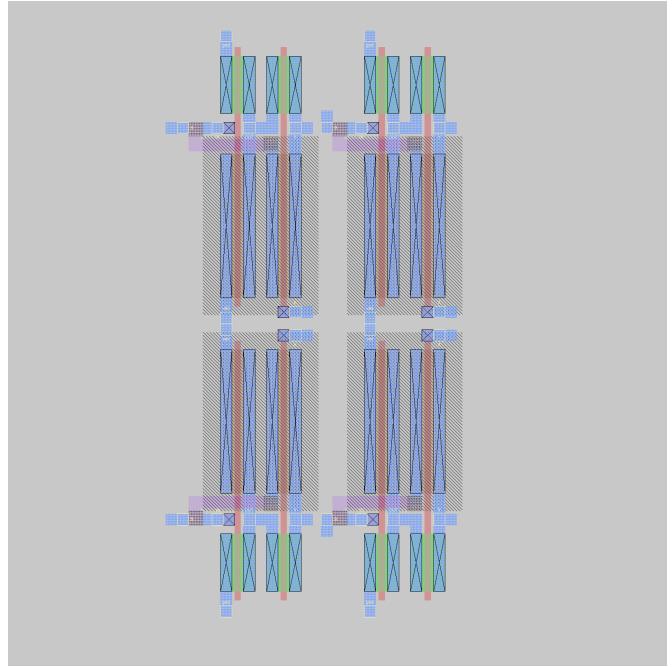


Fig. 23: MAGIC Layout of Sum Generator

## H. D Flop Flop

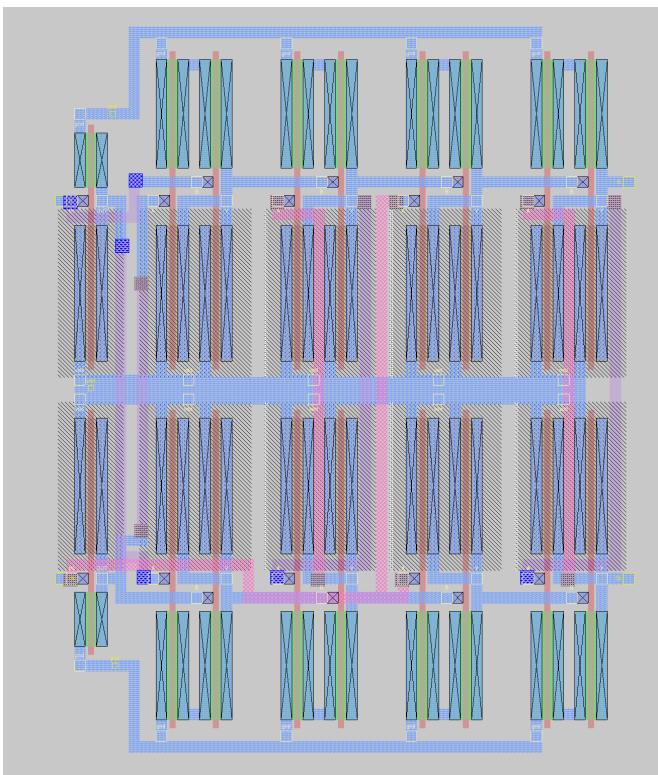


Fig. 24: MAGIC Layout of CMOS D Flip Flop

### 1) CMOS Implementation:

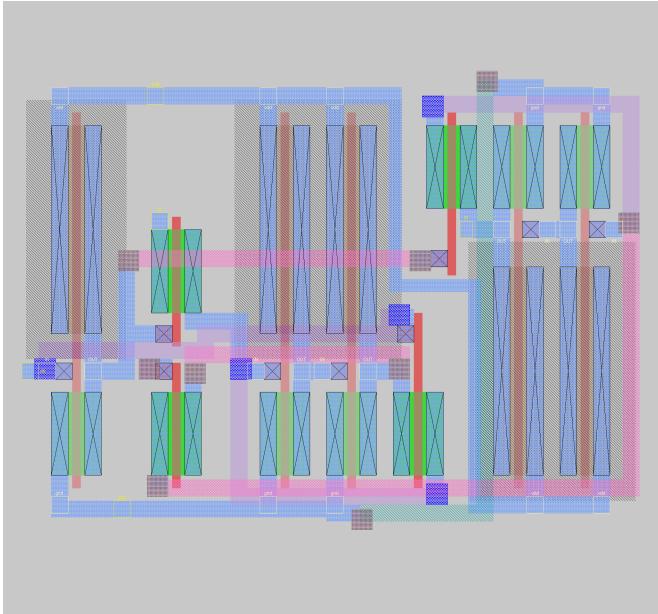


Fig. 25: MAGIC Layout of Optimized D Flip Flop

### 2) Optimized Implementation:

## I. Full Circuit

## VI. POST LAYOUT SIMULATION

### A. Inverter

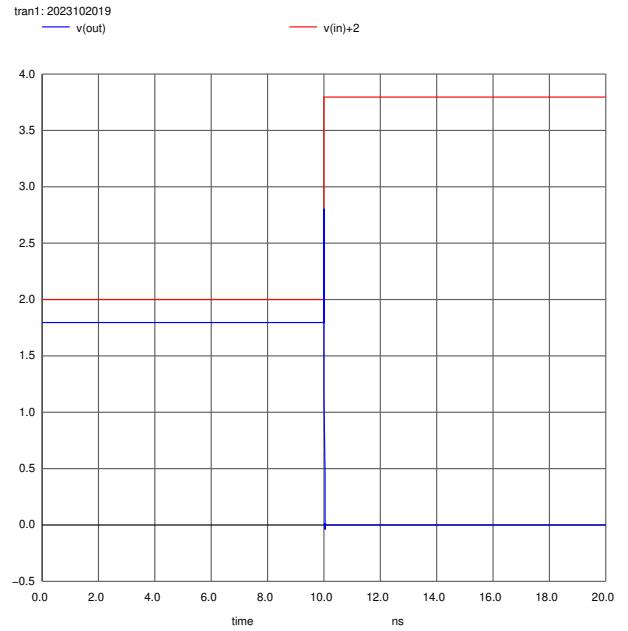


Fig. 27: Post Layout NGSPICE Plot of Inverter

### B. NAND Gate

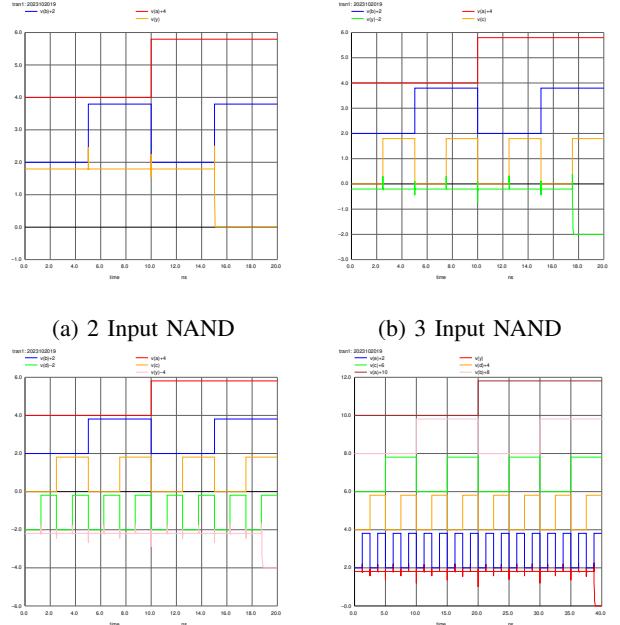


Fig. 28: Post Layout NGSPICE Plot of NAND Gates

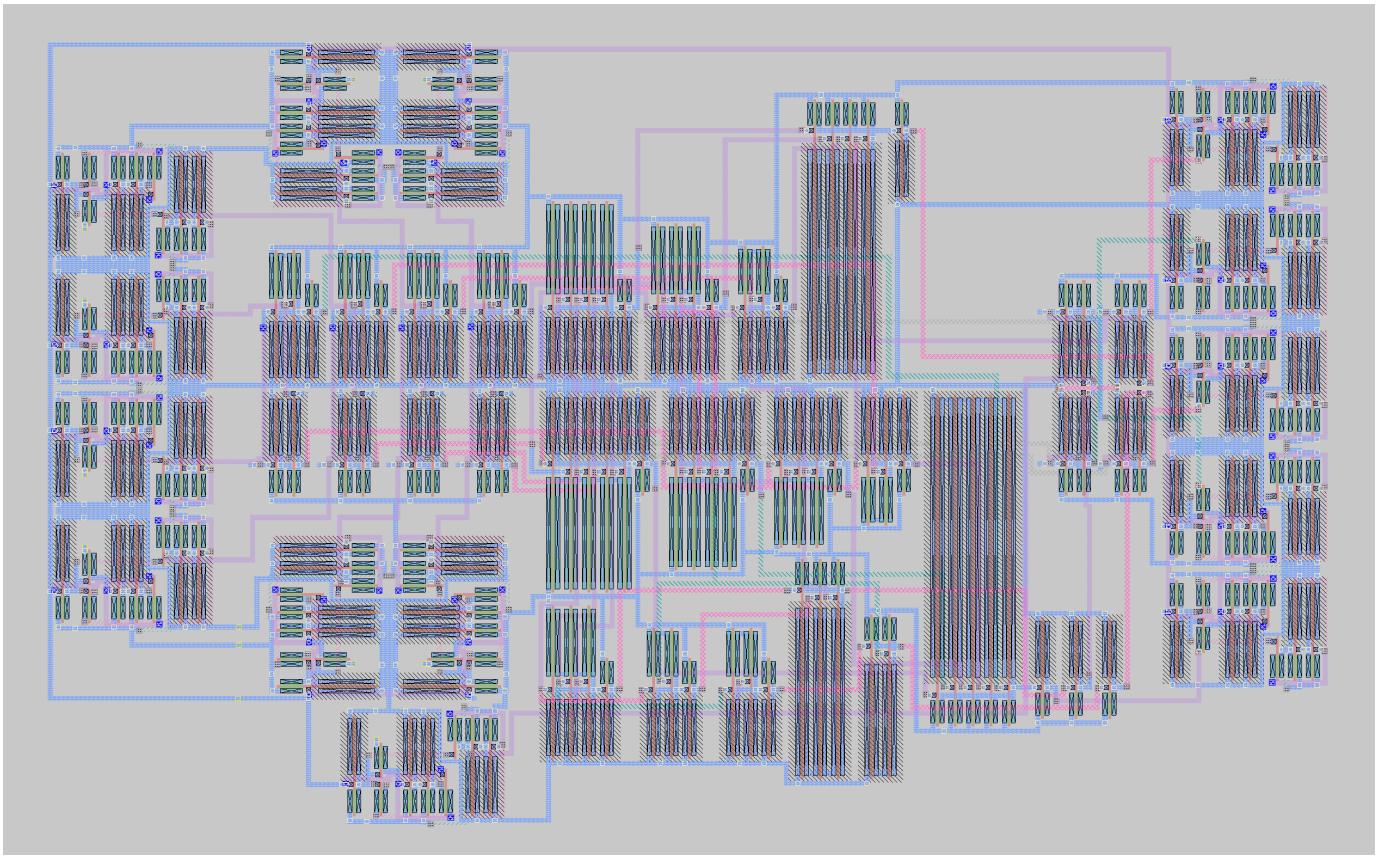
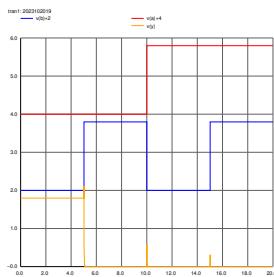
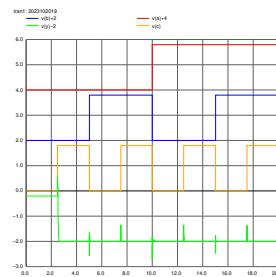


Fig. 26: MAGIC Layout of Full Circuit

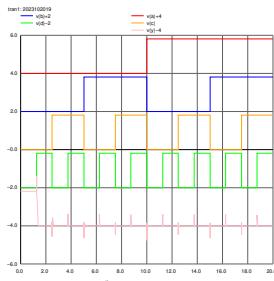
### C. NOR Gate



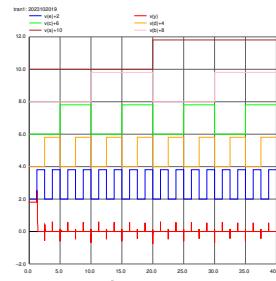
(a) 2 Input NOR



(b) 3 Input NOR



(c) 4 Input NOR



(d) 5 Input NOR

Fig. 29: Post Layout NGSPICE Plot of NOR Gates

### D. XOR Gate

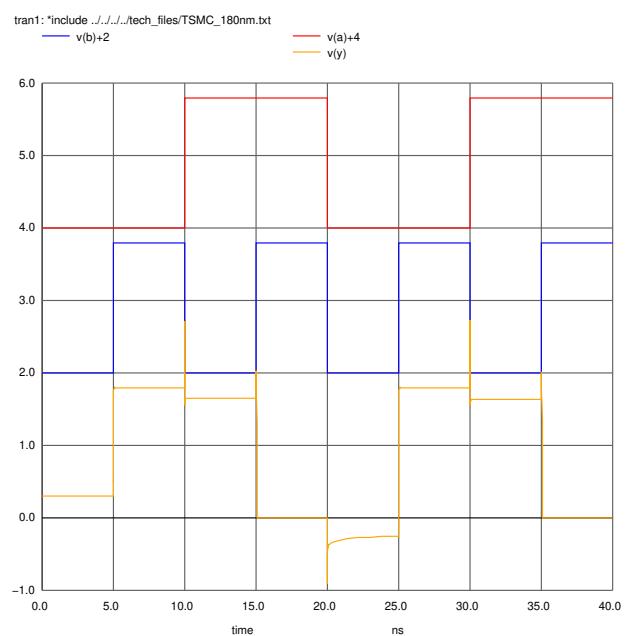


Fig. 30: Post Layout NGSPICE Plot of XOR Gate

### E. D Flip Flop

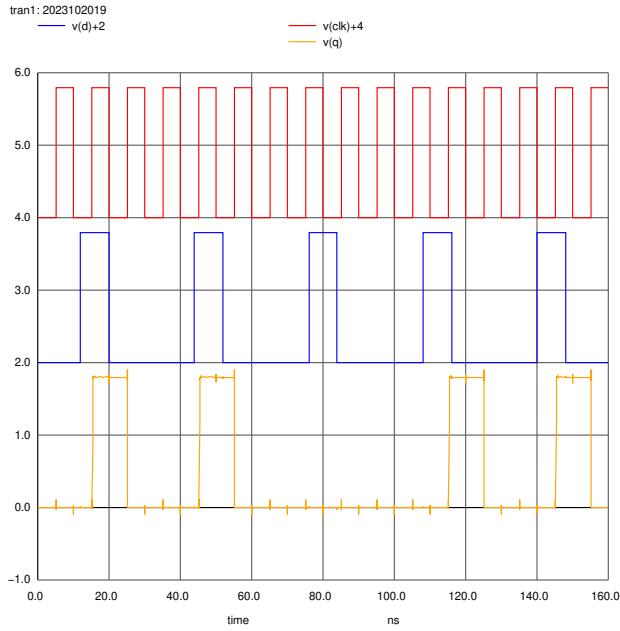


Fig. 31: Post Layout NGSPICE Plot of D Flip Flop

### F. Full Circuit (with Load Inverters)

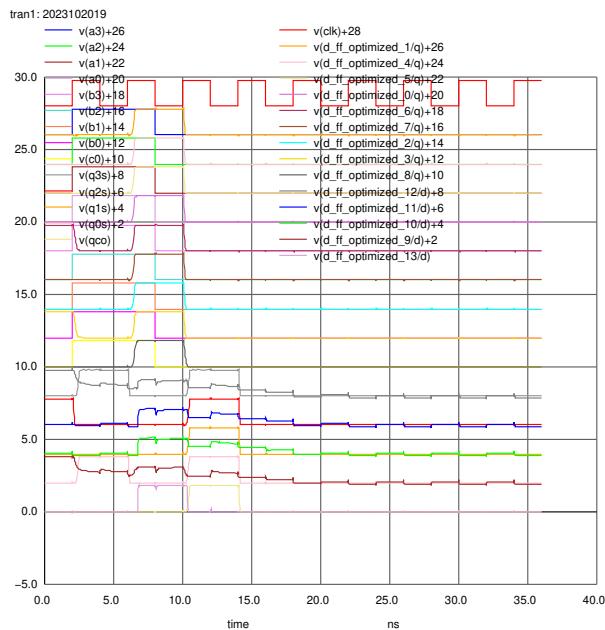
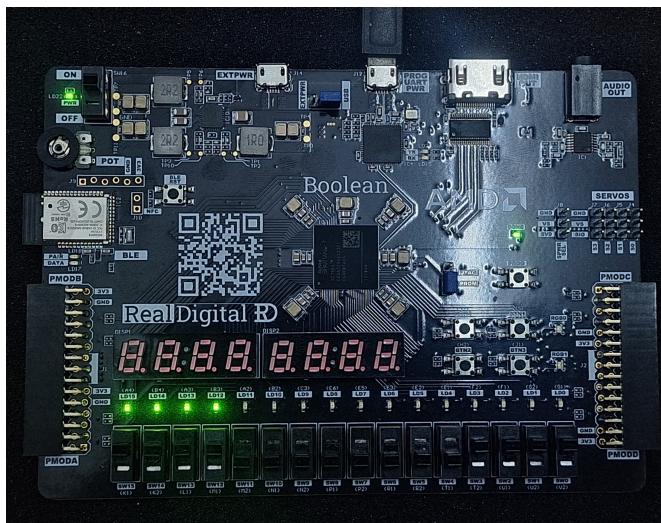


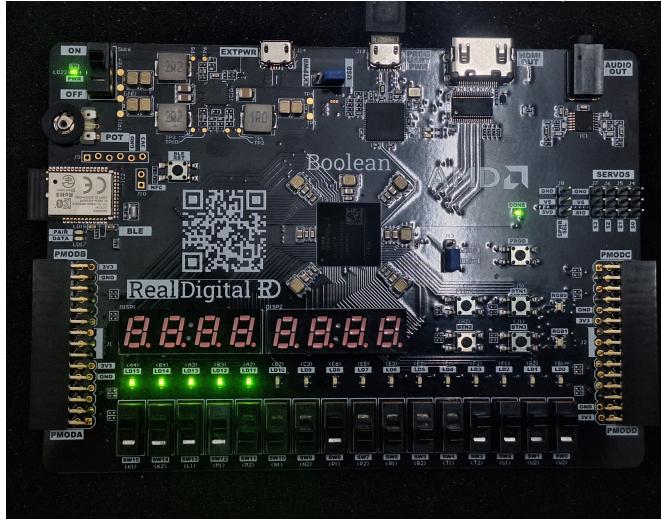
Fig. 32: Post Layout NGSPICE Plot of Full Circuit

## VII. FPGA SIMULATION

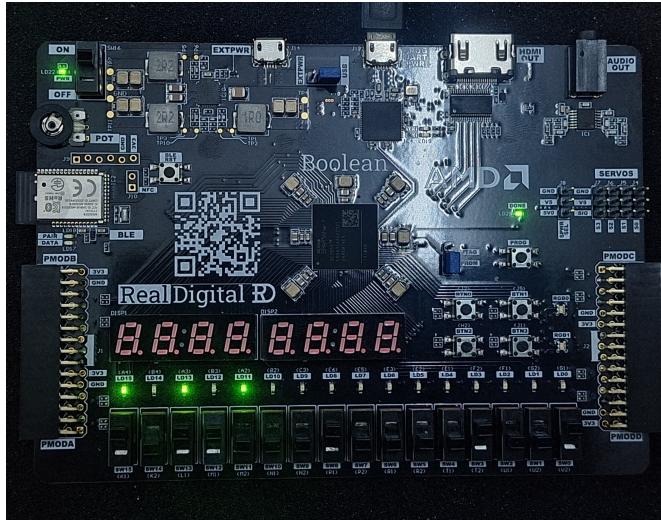
### A. On Board LEDs



$$(a) 1111 + 1111 + 0 = 11110$$



$$(b) 1111 + 1111 + 1 = 11111$$



$$(c) 1011 + 1001 + 1 = 10101$$

Fig. 33: FPGA Simulation

### B. Waveform Visualization

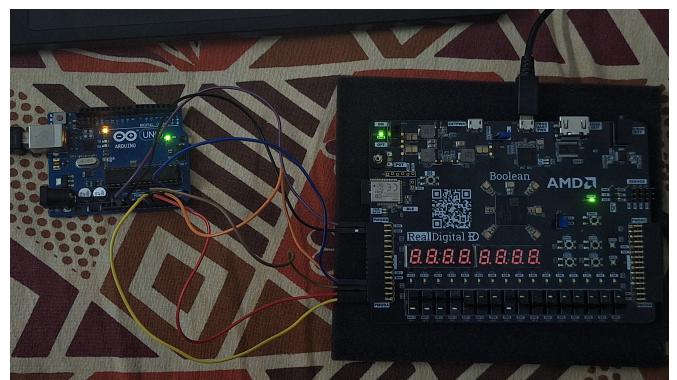


Fig. 34: Viewing Waveform of FPGA Simulation

### ACKNOWLEDGMENT

### REFERENCES

[1]