4-bit CLA Adder
VLSI Course Project

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***Abstract*—This document is a report on the Design and Simulation of a 4-bit Carry Look Ahead Adder.**

I. Introduction

The Carry Look Ahead Adder is a digital circuit that is used to add two 4 bit binary numbers. It is faster than the Ripple Carry Adder as it generates the carry signals for all the bits at the same time.

II. Proposed Design

A. CLA Adder

B. D Flip Flop

III. Verilog Simulation

A. CLA Adder

Fig. 1: GTKWave Plot of CLA Adder Verilog Simulation

B. D Flip Flop

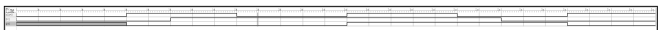


Fig. 2: GTKWave Plot of D Flip Flop Verilog Simulation

C. Full Circuit

IV. NGSPICE Simulation

A. Inverter

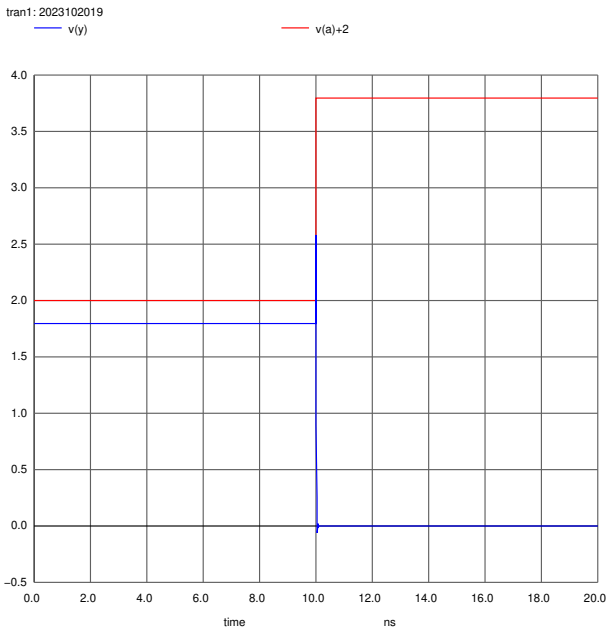
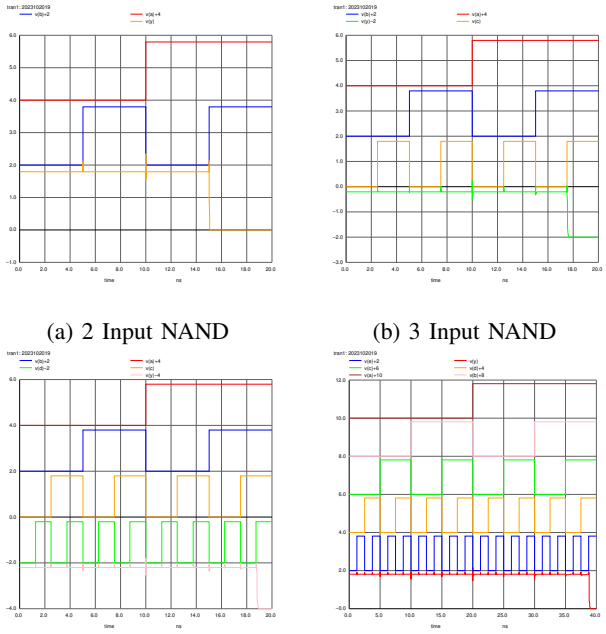


Fig. 3: NGSPICE Plot of Inverter

B. NAND Gate

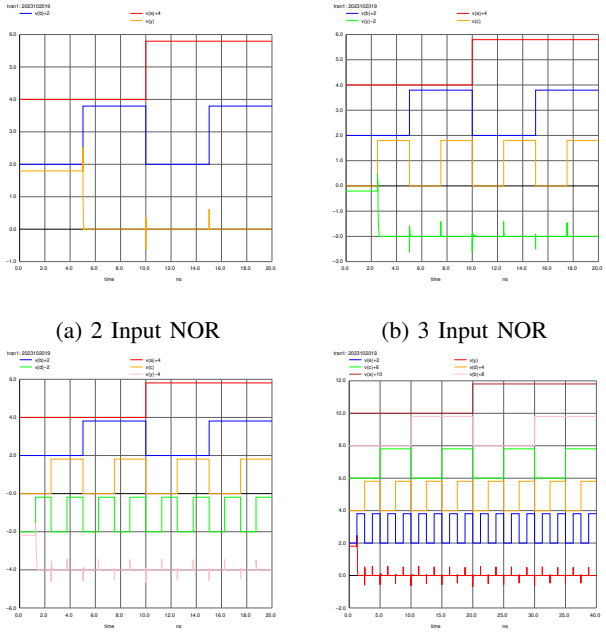


(a) 2 Input NAND (b) 3 Input NAND

(c) 4 Input NAND (d) 5 Input NAND

Fig. 4: NGSPICE Plot of NAND Gates

C. NOR Gate



(a) 2 Input NOR (b) 3 Input NOR

(c) 4 Input NOR (d) 5 Input NOR

Fig. 5: NGSPICE Plot of NOR Gates

D. XOR Gate

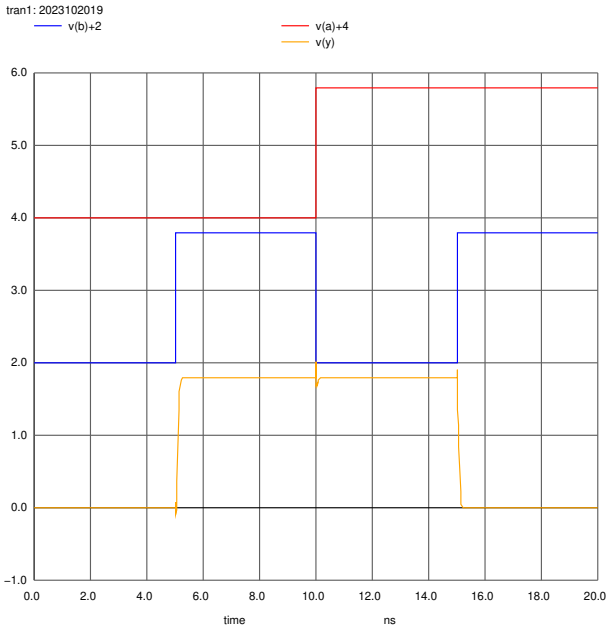


Fig. 6: NGSPICE Plot of CMOS XOR Gate

1) CMOS Implementation:

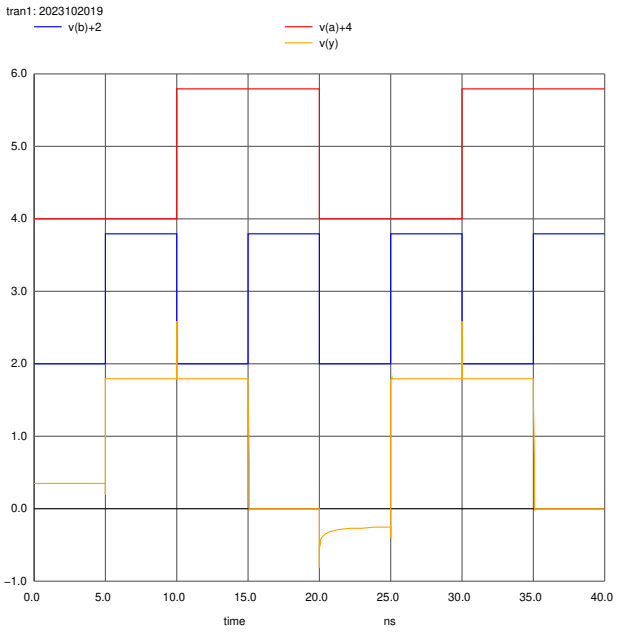


Fig. 7: NGSPICE Plot of CPTL XOR Gate

2) Complimentary Pass Transistor Implementation:

E. Propagate/Generate Generator

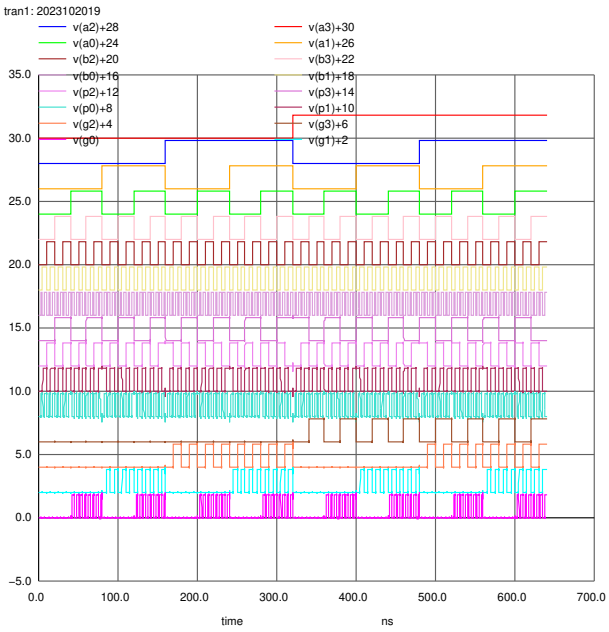


Fig. 8: NGSPICE Plot of CMOS Propagate/Generate Generator

1) CMOS Implementation:

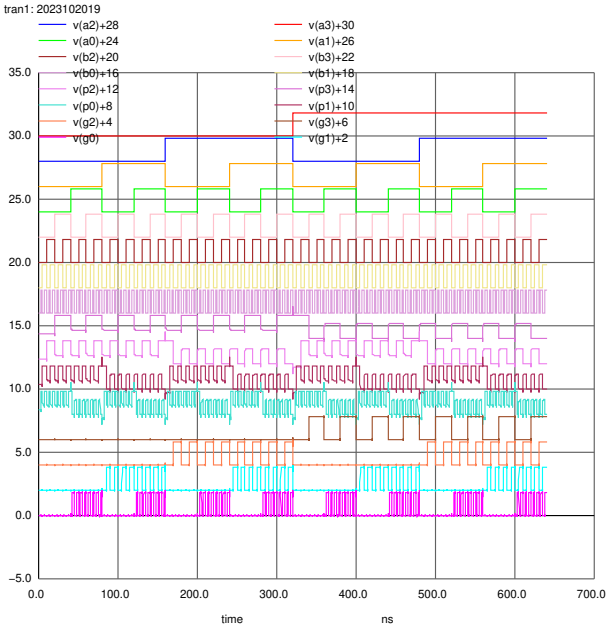


Fig. 9: NGSPICE Plot of CPTL Propagate/Generate Generator

2) Complimentary Pass Transistor Implementation:

F. Carry Look Ahead Generator

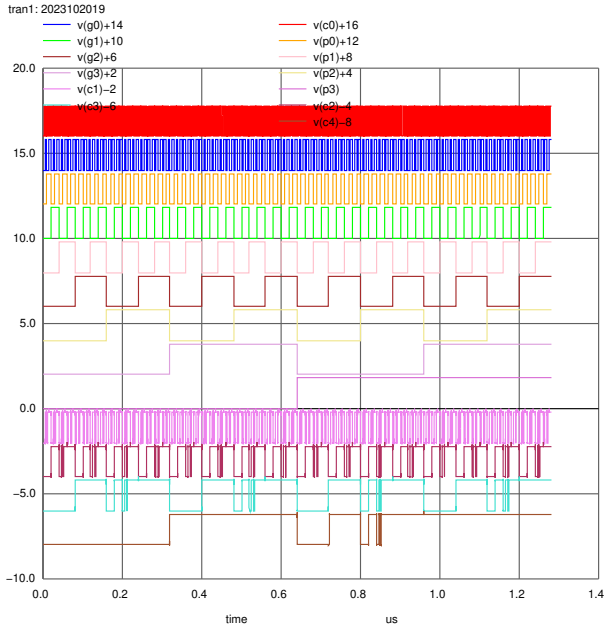


Fig. 10: NGSPICE Plot of CMOS Carry Look Ahead Generator

G. Sum Generator

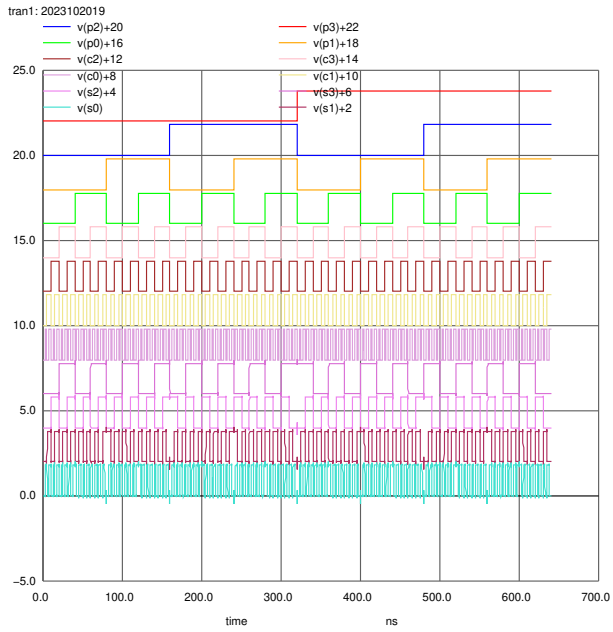


Fig. 11: NGSPICE Plot of CMOS Sum Generator

1) CMOS Implementation:

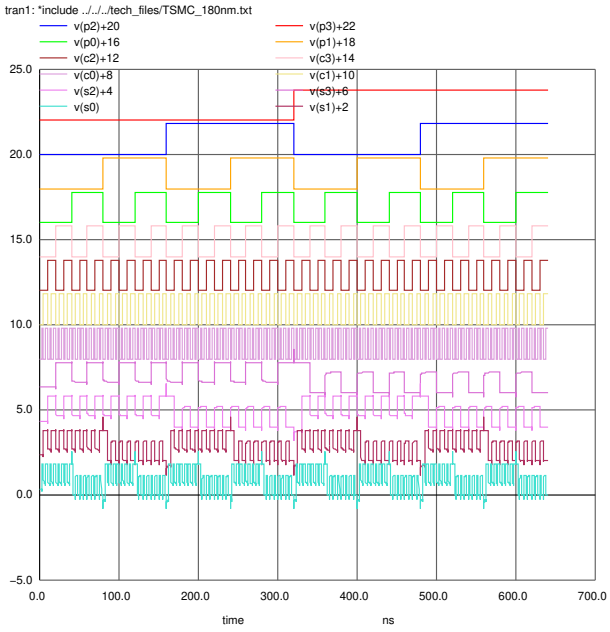


Fig. 12: NGSPICE Plot of CPTL Sum Generator

2) Complimentary Pass Transistor Implementation:

H. D Flop Flop

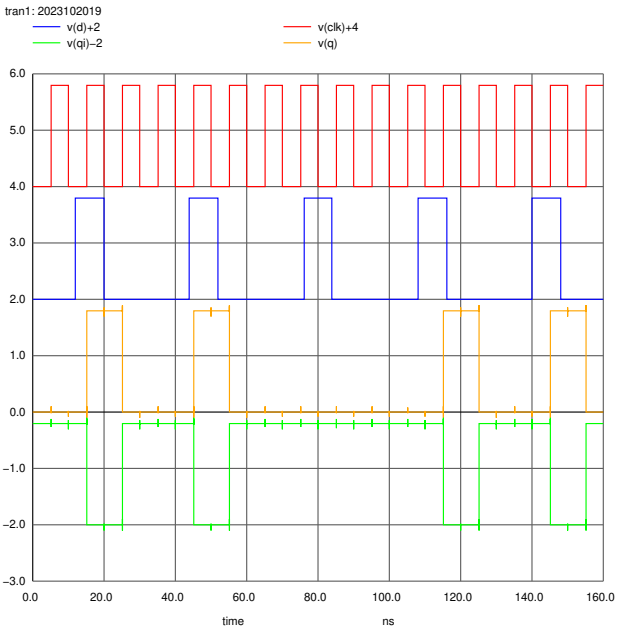


Fig. 13: NGSPICE Plot of CMOS D Flip FLop

1) CMOS Implementation:

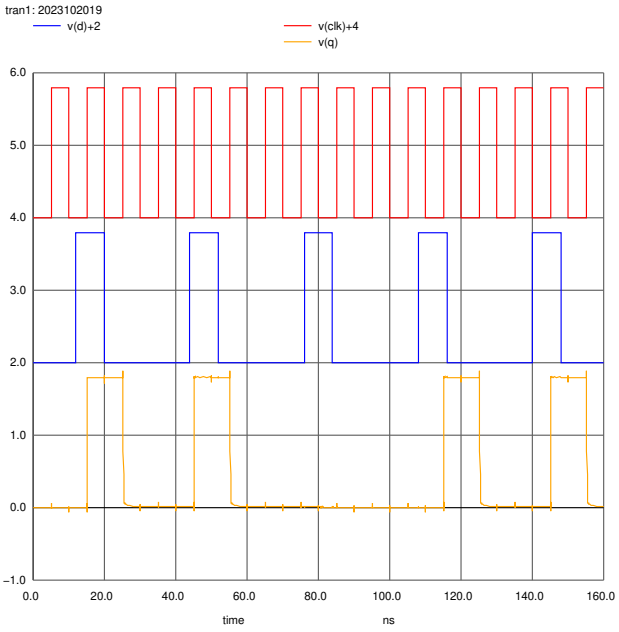


Fig. 14: NGSPICE Plot of Optimized D Flip Flop

2) Optimized Implementation:

I. Full Circuit

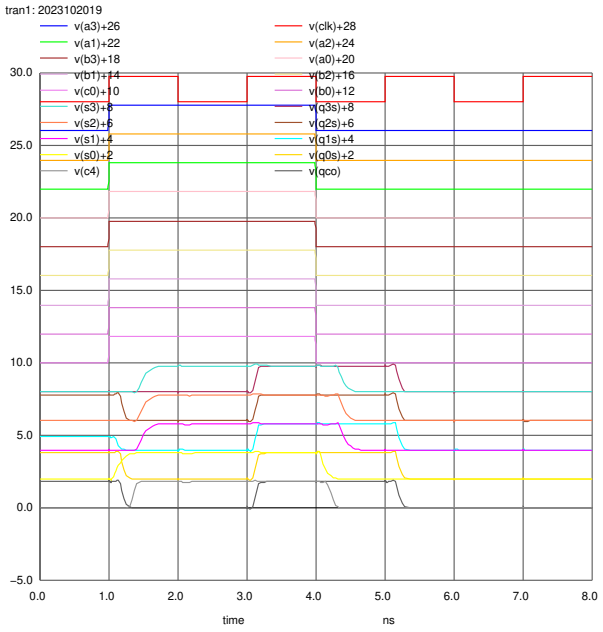


Fig. 15: NGSPICE Plot of CMOS Circuit

1) CMOS Implementation:

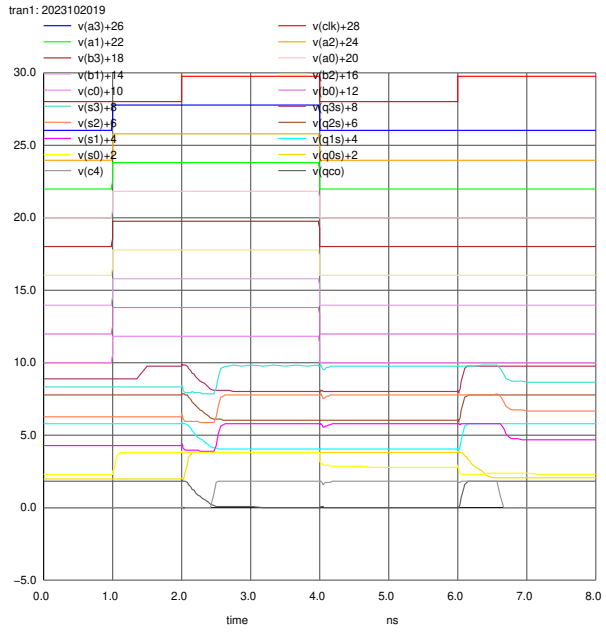


Fig. 16: NGSPICE Plot of Optimized Circuit

2) Optimized Implementation:

V. MAGIC Layout

A. Inverter

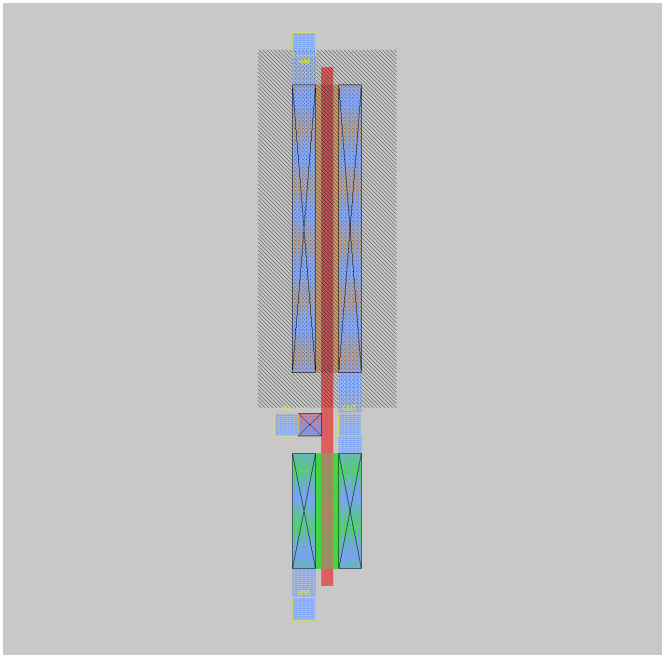
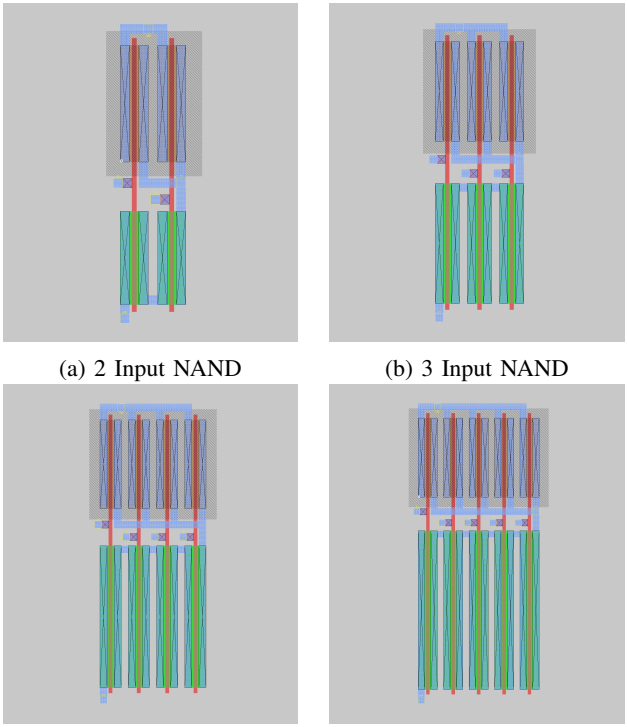


Fig. 17: MAGIC Layout of CMOS Inverter

B. NAND Gate

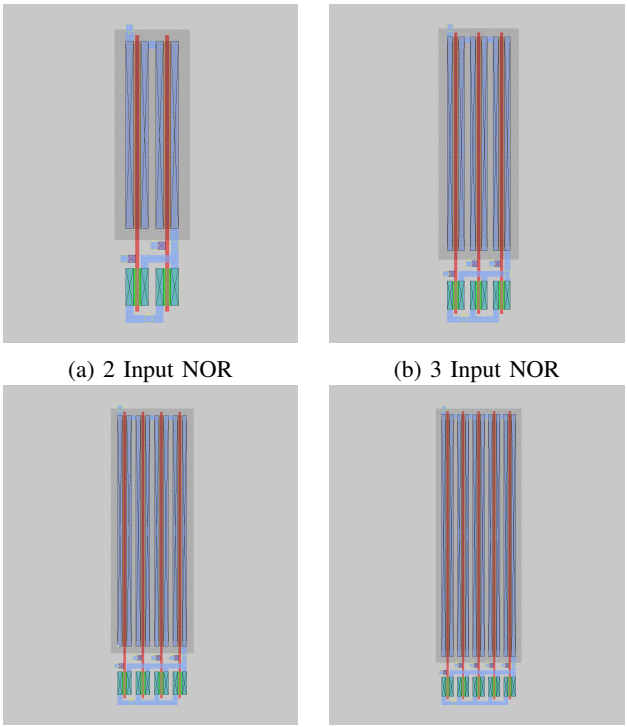


(a) 2 Input NAND (b) 3 Input NAND

(c) 4 Input NAND (d) 5 Input NAND

Fig. 18: MAGIC Layout of NAND Gates

C. NOR Gate



(a) 2 Input NOR (b) 3 Input NOR

(c) 4 Input NOR (d) 5 Input NOR

Fig. 19: MAGIC Layout of NOR Gates

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