

4-bit CLA Adder

VLSI Course Project

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Abstract—This document is a report on the Design and Simulation of a 4-bit Carry Look Ahead Adder.

I. INTRODUCTION

II. PROPOSED DESIGN

- A. *CLA Adder*
- B. *D Flip Flop*

III. VERILOG SIMULATION

- A. *CLA Adder*
- B. *D Flip Flop*
- C. *Full Circuit*

IV. NGSPICE SIMULATION

- A. *Inverter*
- B. *NAND Gate*
- C. *NOR Gate*
- D. *XOR Gate*
- E. *Propagate/Generate Generator*
- F. *Carry Look Ahead Generator*
- G. *Sum Generator*
- H. *D Flop Flop*
- I. *Full Circuit*

V. MAGIC LAYOUT

- A. *Inverter*
- B. *NAND Gate*
- C. *NOR Gate*
- D. *XOR Gate*
- E. *Propagate/Generate Generator*
- F. *Carry Look Ahead Generator*
- G. *Sum Generator*
- H. *D Flop Flop*
- I. *Full Circuit*

VI. POST LAYOUT SIMULATION

- A. *Inverter*
- B. *NAND Gate*
- C. *NOR Gate*
- D. *XOR Gate*
- E. *Propagate/Generate Generator*
- F. *Carry Look Ahead Generator*
- G. *Sum Generator*
- H. *D Flop Flop*
- I. *Full Circuit*

VII. FPGA SIMULATION

ACKNOWLEDGMENT

REFERENCES