

AWS with FPGA

Y V Sai Dinesh

yvsdinesh@ieee.org

July 13, 2020

Frame Title



AWS

Amazon Web Services



- Cloud computing is a term referred to storing, accessing and processing data over the internet.
- AWS is a comprehensive, easy to use computing platform offered Amazon. The platform is developed with a combination of infrastructure as a service (IaaS), platform as a service (PaaS) and packaged software as a service (SaaS) offerings.

Services offered in Cloud

- **Infrastructure as a Service (IAAS)** is a form of cloud computing that provides virtualized computing resources over the internet. Eg: hardware,servers, storage etc.
- **Platform as a Service (PAAS)** is a cloud computing model that delivers applications over the internet. Eg: hardware and software tools (API's & SDK's)
- **Software as a Service(SAAS)** is a software distribution model in which applications are hosted by a vendor or service provider and made available to customers over a network, typically the Internet. Eg: Website Hosting.
- Storage As A Service (SAAS): Google Drive, OneDrive, Communications As A Service (CAAS): Video Conferencing etc.

History of AWS

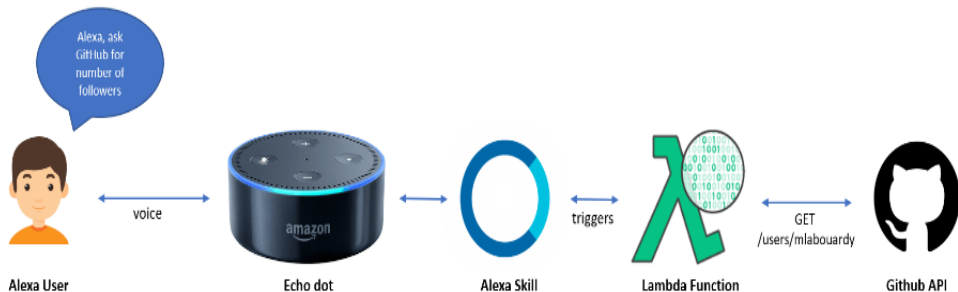
- 2002- AWS services launched
- 2006- Launched its cloud products
- 2012- Holds first customer event
- 2015- Reveals revenues achieved of \$4.6 billion
- 2016- Surpassed \$10 billion revenue target
- 2019- Offers nearly 100 cloud services

Applications of AWS services

Amazon Web services are widely used for various computing purposes like:

- Web site & Application hosting/SaaS hosting
- Media Sharing (Image/ Video)
- Mobile and Social Applications
- Content delivery and Media Distribution
- Storage, backup, and disaster recovery
- Development and test environments
- Academic Computing
- Search Engines
- Social Networking

Workflow of AWS



Companies using AWS

- Netflix: \$19 million
- Twitch: \$15 million
- LinkedIn: \$13 million
- Facebook: \$11 million
- Turner Broadcasting: \$10 million
- BBC: \$9 million
- Baidu: \$9 million
- ESPN: \$8 million
- Adobe: \$8 million
- Twitter: \$7 million

Advantages of AWS

- AWS allows organizations to use the already familiar programming models, operating systems, databases, and architectures.
- It is a cost-effective service that allows you to pay only for what you use, without any up-front or long-term commitments.
- Offers fast deployments
- Allows you to deploy your application in multiple regions around the world with just a few clicks
- You are allowed cloud access quickly with limitless capacity.

Disadvantages of AWS

- If you need more immediate or intensive assistance, you'll have to opt for paid support packages.
- Amazon Web Services may have some common cloud computing issues when you move to a cloud. For example, downtime, limited control, and backup protection.
- Hardware-level changes happen to your application which may not offer the best performance and usage of your applications.

Standards & Certifications

The following is a partial list of assurance programs with which AWS complies:

- SOC 1/ISAE 3402, SOC 2, SOC 3
- FISMA, DIACAP, and FedRAMP
- PCI DSS Level 1
- ISO 9001, ISO 27001, ISO 27017, ISO 27018

AWS with Vivado

- This AMI (Amazon Machine Image) is a CentOS Linux image provided by Xilinx Inc. The AMI is pre-built with FPGA and SoC development and runtime tools to program the latest and greatest Xilinx devices.
- Vivado & SDx 2020.1 Developer AMI- \$0.36/hr \approx Rs 27.07/hr
- Infrastructure Cost- \$0.192 EC2/hr \approx Rs 14.44/hr

FPGA with AWS

- The FPGA (field programmable gate array) AMI is a supported and maintained CentOS Linux image provided by Amazon Web Services. The AMI is pre-built with FPGA development tools and run time tools required to develop and use custom FPGAs for hardware acceleration.
- The FPGA Developer AMI along with the FPGA Developer Kit constitutes a development environment which includes scripts and tools for simulating your FPGA design, compiling code, building and registering your AFI (Amazon FPGA Image).

- Developers can deploy the FPGA developer AMI on an Amazon EC2 instance and quickly provision the resources they need to write and debug FPGA designs in the cloud.
- The AMI is designed to provide a stable, secure, and high performance development environment. The FPGA AMI is provided at no additional charge to Amazon EC2 users.

Xilinx ISE

- Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
- It is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.

- The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the ModelSim logic simulator is used for system-level testing.
- Other components shipped with the Xilinx ISE include the Embedded Development Kit (EDK), a Software Development Kit (SDK) and ChipScope Pro.

The design procedure consists of

- Design entry.

The design procedure consists of

- Design entry.
- Synthesis and implementation of the design.

The design procedure consists of

- Design entry.
- Synthesis and implementation of the design.
- Functional simulation.

The design procedure consists of

- Design entry.
- Synthesis and implementation of the design.
- Functional simulation.
- Testing and verification

The steps of this design procedure are listed below

- Create Verilog design input file(s) using template driven editor.

The steps of this design procedure are listed below

- Create Verilog design input file(s) using template driven editor.
- Compile and implement the Verilog design file(s).

The steps of this design procedure are listed below

- Create Verilog design input file(s) using template driven editor.
- Compile and implement the Verilog design file(s).
- Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA or CPLD).

The steps of this design procedure are listed below

- Create Verilog design input file(s) using template driven editor.
- Compile and implement the Verilog design file(s).
- Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA or CPLD).
- Assign input/output pins to implement the design on a target device.

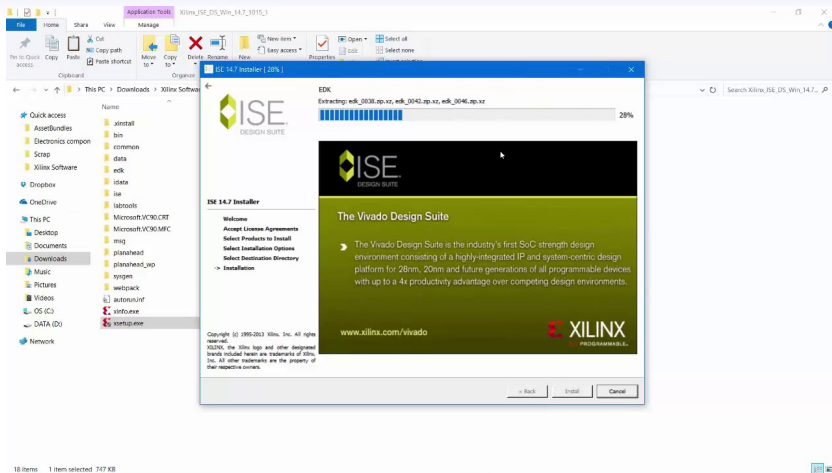
The steps of this design procedure are listed below

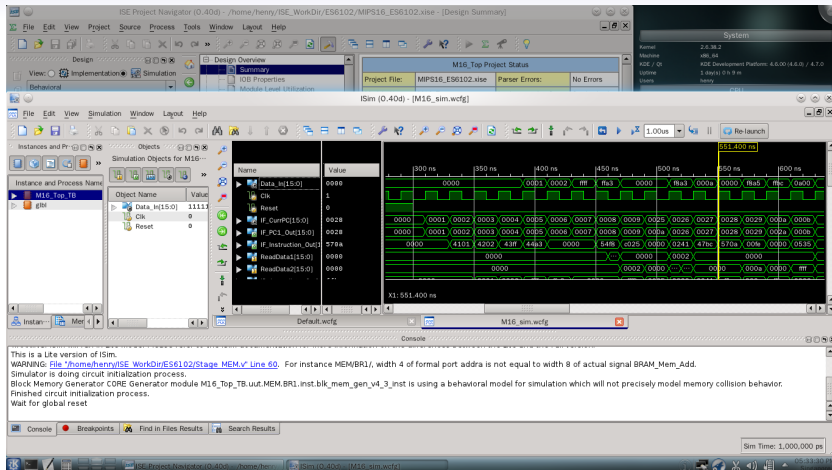
- Create Verilog design input file(s) using template driven editor.
- Compile and implement the Verilog design file(s).
- Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA or CPLD).
- Assign input/output pins to implement the design on a target device.
- Download bitstream to an FPGA or CPLD device.

The steps of this design procedure are listed below

- Create Verilog design input file(s) using template driven editor.
- Compile and implement the Verilog design file(s).
- Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA or CPLD).
- Assign input/output pins to implement the design on a target device.
- Download bitstream to an FPGA or CPLD device.
- Test design on FPGA/CPLD device.

- ISE design suite supports the Spartan-6, Virtex-6, and CoolRunner™ devices, as well as their previous generation families.
- ISE design suite runs on Windows 10 and Linux operating systems, click here for OS support details.
- Xilinx recommends Vivado Design Suite for new design starts with Virtex-7, Kintex-7, Artix-7, and Zynq-7000.





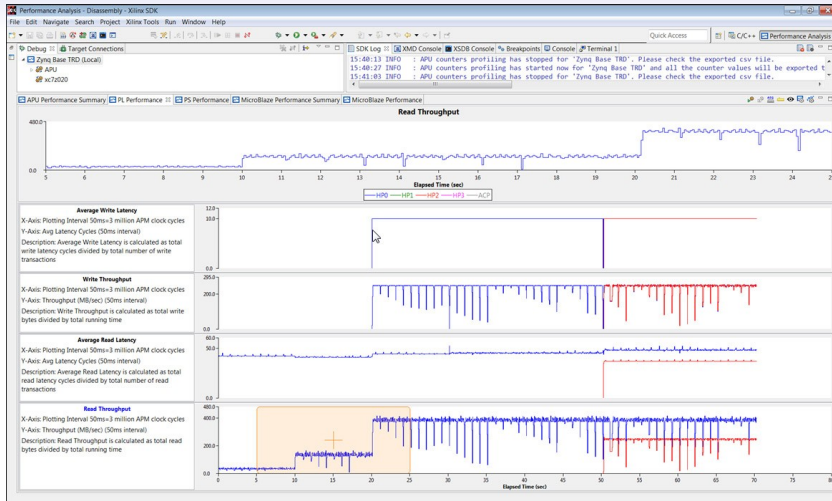
Xilinx SDK

- The Xilinx Software Development Kit (XSDK) is the Integrated Design Environment for creating embedded applications on Xilinx's microprocessors: Zynq UltraScale+ MPSoC, Zynq-7000 SoCs, and the industry-leading MicroBlaze™ soft-core microprocessor.
- The SDK is the first application IDE to deliver true homogenous and heterogeneous multi-processor design, debug, and performance analysis.

Benefits of Xilinx SDK

- Included with the Vivado Design Suite or available as a separate free download for embedded software developers
- Based on Eclipse 4.5.0 and CDT 8.8.0 (as of the 2016.3 release)
- Complete Integrated Design Environment (IDE) that directly interfaces to the Vivado embedded hardware design environment
- FreeRTOS integrated as RTOS available for all platforms
- Editor, compilers, build tools, flash memory management, and JTAG debug integration





Vivado Design Suite

- Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis.
- Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE), and has been described by reviewers as "well conceived, tightly integrated, blazing fast, scalable, maintainable, and intuitive".

- Since 2012, Xilinx ISE has been discontinued in favor of Vivado Design Suite, that serves the same roles as ISE with additional features for system on a chip development.
- Xilinx released the last version of ISE in October 2013 (version 14.7), and states that "ISE has moved into the sustaining phase of its product life cycle, and there are no more planned ISE releases."

project_1 - /opt2/Xilinx/Vivado/2016.4/bin/project_1/project_1.xpr - Vivado 2016.4

Implementation Complete

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Simulation
- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Implemented Design
- Constraints Wizard
- Edit Timing Constraints
- Report Timing Summary
- Report Clock Networks
- Report Clock Interaction
- Report Methodology
- Report DRC
- Report Noise
- Report Utilization
- Report Power

Program and Debug

- Bitstream Settings
- Generate Bitstream
- Open Hardware Manager

Netlist

- base_zynq_wrapper
- Nets (130)
- DOR_addr (15)
- DOR_ba (3)
- DOR_dm (4)
- DOR_dq (12)
- DOR_dqs_n (4)
- DOR_dqs_p (4)
- FIXED_IO_mio (54)
- led_4bits_tri_o (4)
- led_4bits_tri_o_OBUF (4)
- DOR_cas_n
- DOR_ck_n
- DOR_ck_p
- DOR_cke
- DOR_cs_n
- DOR_int2
- DOR_ras_n
- DOR_reset_n
- DOR_we_n
- FIXED_IO_ddr_vrn
- FIXED_IO_ddr_vrp
- FIXED_IO_ps_clk
- FIXED_IO_ps_porb
- FIXED_IO_ps_vrstb
- Leaf Cells (4)
- led_4bits_tri_o_OBUF[0]_inst (OBUF)
- led_4bits_tri_o_OBUF[1]_inst (OBUF)
- led_4bits_tri_o_OBUF[2]_inst (OBUF)
- led_4bits_tri_o_OBUF[3]_inst (OBUF)
- base_zynq_i (base_zynq)
- Nets (705)
- Leaf Cells (1)
- axi_bram_ctrl_0 (base_zynq_axi_bram_ctrl_0_0)
- axi_gpio_0 (base_zynq_axi_gpio_0_0)
- blk_mem_gen_0 (base_zynq_blk_mem_gen_0_0)
- processing_system7_0 (base_zynq_processing_system7_0)
- ps7_0_axi_periph (base_zynq_ps7_0_axi_periph_0)
- rst_ps7_0_50M (base_zynq_rst_ps7_0_50M_0)

Project Summary

Project Settings

Project name: project_1
Project location: /opt2/01hw/Vivado/2016.4/bin/project_1
Product family: Zynq-7000
Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045ffg900-2)
Top module name: base_zynq_wrapper
Target language: Verilog
Simulator language: ModelSim

Board Part

Display name: ZYNQ-7 ZC706 Evaluation Board
Board part name: xilinx.com:zc706:part0:1.3
Repository path: /opt2/01hw/Vivado/2016.4/data/boards/board_files
URL: www.xilinx.com/zc706
Board overview: ZYNQ-7 ZC706 Evaluation Board

Synthesis

Status: Complete
Messages: 20 warnings
Active run: synth_1
Part: xc7z045ffg900-2
Strategy: Vivado Synthesis Defaults

Implementation

Status: Complete
Messages: 4 warnings
Active run: impl_1
Part: xc7z045ffg900-2
Strategy: Vivado Implementation Defaults
Incremental compile: None
Summary Route Status

DRC Violations

No DRC violations were found.
[Implemented DRC Report](#)

Timing

Worst Negative Slack (WNS): 11.673 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 3795
[Implemented Timing Report](#)
Setup Hold Pulse Width

UTILIZATION - Post-Implementation

Power

Console

Warning: Constraints 18-500 could not create 'INSTANAME' constraint because net 'base_zynq_i/axi_gpio_0/gpio_is_o[2]' is not directly connected to tap level port. 'INSTANAME' is ignored by the tool.
Type a Tcl command here

It comes in three editions:

- Vivado HL WebPack Edition
- Vivado HL Design Edition
- Vivado HL System Edition

Vivado Design Suite HLx

- The new Vivado Design Suite HLx editions supply design teams with the tools and methodology needed to leverage C-based design and optimized reuse, IP sub-system reuse, integration automation and accelerated design closure.
- When coupled with the UltraFast™ High-Level Productivity Design Methodology Guide, this unique combination is proven to accelerate productivity by enabling designers to work at a high level of abstraction while facilitating design reuse.

HLx editions include HL System Edition, HL Design Edition and HL WebPACK™ Edition

Accelerating High Level Design

- Software-defined IP Generation with Vivado High-Level Synthesis
- Block-based IP Integration with Vivado IP Integrator
- On demand reconfiguration with Dynamic Function eXchange (DFX)
- Model-based Design Integration with Model Composer and System Generator for DSP

Accelerating Implementation

- 4X Faster Implementation
- 20% Better Design Density
- Up to 3-Speedgrade Performance Advantage for the low-end mid-range and 35% Power Advantage in the high-end

Xilinx ISE vs Vivado

- Xilinx ISE is a legacy IDE (Integrated Development Environment) for Xilinx brand FPGAs. The latest versions are ISE 14.7 and ISE 14.7 for Windows 10, and further versions are not expected. It supports primarily Series-6 devices (Spartan-6, Kintex-6, Virtex-6), and certain early models in the Series-7 line (certain Artix-7 models, for example).
- Xilinx Vivado is the newer IDE released by Xilinx to support its current FPGAs. It supports Series-7 FPGAs, but does not currently support some older devices, for example Spartan-6 devices which require ISE to work with. Vivado is the current development environment, with releases occurring once each quarter, with occasional maintenance releases.

References

- <https://github.com/aws/aws-fpga>
- <https://aws.amazon.com/marketplace/pp/Amazon-Web-Services-FPGA-Developer-AMI/B06VVYBLZZ>
- https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_1/ug1118-vivado-creating-packaging-custom-ip.pdf
- <https://s3.amazonaws.com/xilinx-documentation/How+to+Launch+a+Xilinx+AMI+Instance.pdf>

References

- <https://www.xilinx.com/products/design-tools/ise-design-suite.html>
- https://www.xilinx.com/html_docs/xilinx2019_1/SDK_Doc/sdk_getting_started/sdk_getting_started.html#:~:text=The%20Xilinx%C2%AE%20Software%20Development,the%20Eclipse%20open%20source%20standard.
- <https://www.xilinx.com/support/university/vivado.html>
- <https://www.xilinx.com/products/design-tools/vivado.html>