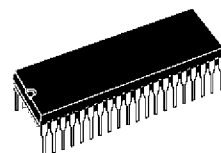
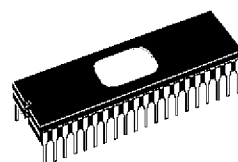


16K EPROM HCMOS MCUs WITH RAM

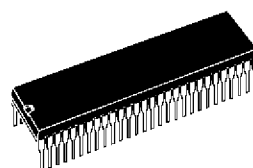
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- Internal Memory :
EPROM 16Kbytes
RAM 256bytes
224 general purpose registers available as RAM, accumulators or index pointers (Register File)
- 40-lead Dual In Line Plastic Package for ST90T27.
- 40-lead Windowed Ceramic Dual In Line Package for ST90E27.
- 44-lead Plastic Leaded Chip Carrier Package for ST90T28C.
- 44-lead Windowed Ceramic Leaded Chip Carrier Package for ST90E28L.
- 56-lead Dual In Line Plastic Package for ST90T28B.
- 56-lead Windowed Ceramic Dual In Line Package for ST90E28D.
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- One 16 bit Multifunction Timer, with an 8 bit prescaler and 12 operating modes
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9020 12K ROM and ST9027/28 16K ROM/256 RAM.



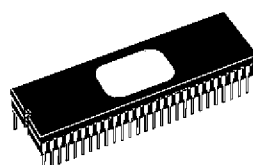
PDIP40



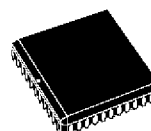
CDIP40-W



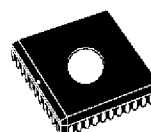
PSDIP56



CSDIP56-W



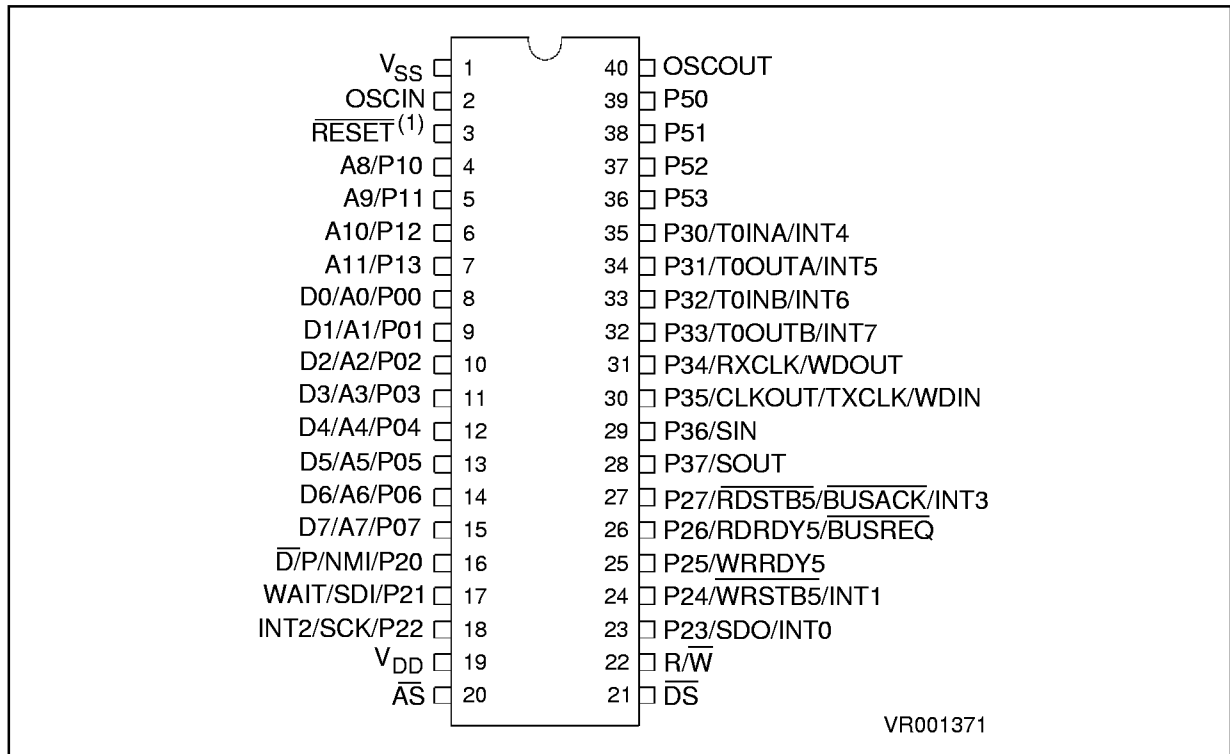
PLCC44



CLCC44-W

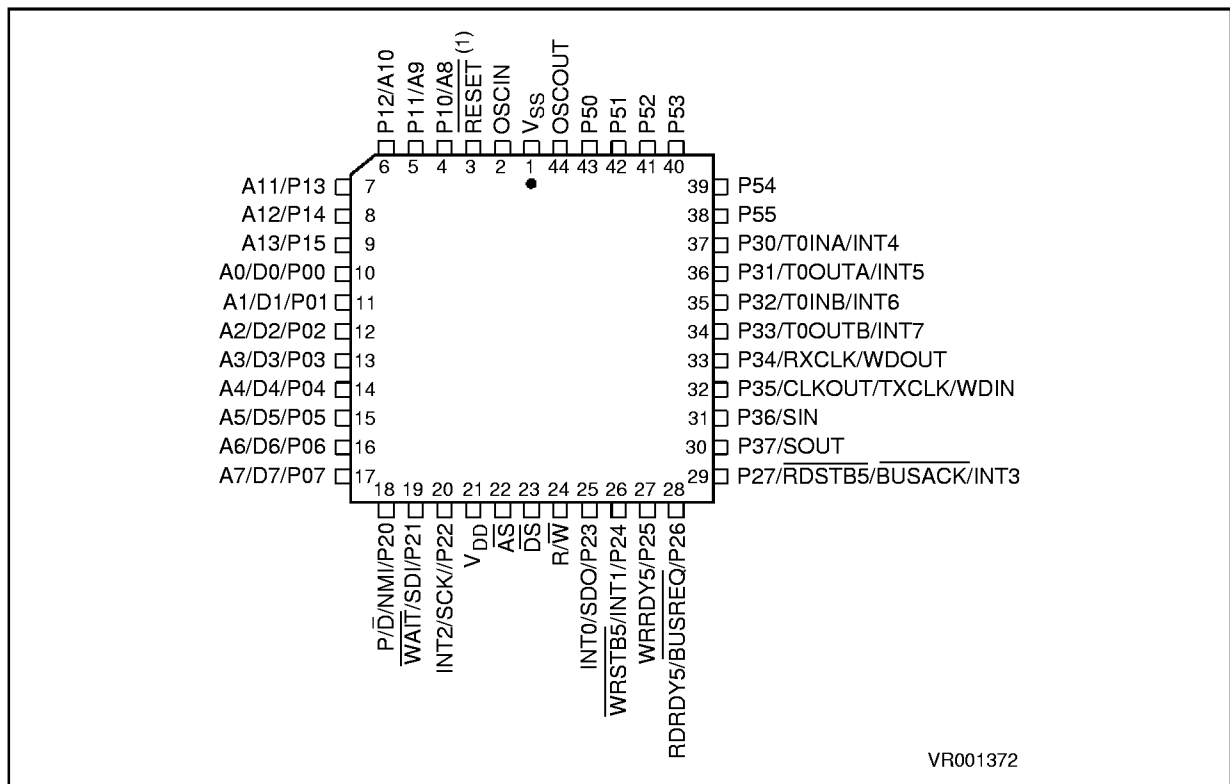
(Ordering Information at the end of the Datasheet)

Figure 1-1. 40 Pin DIP Package



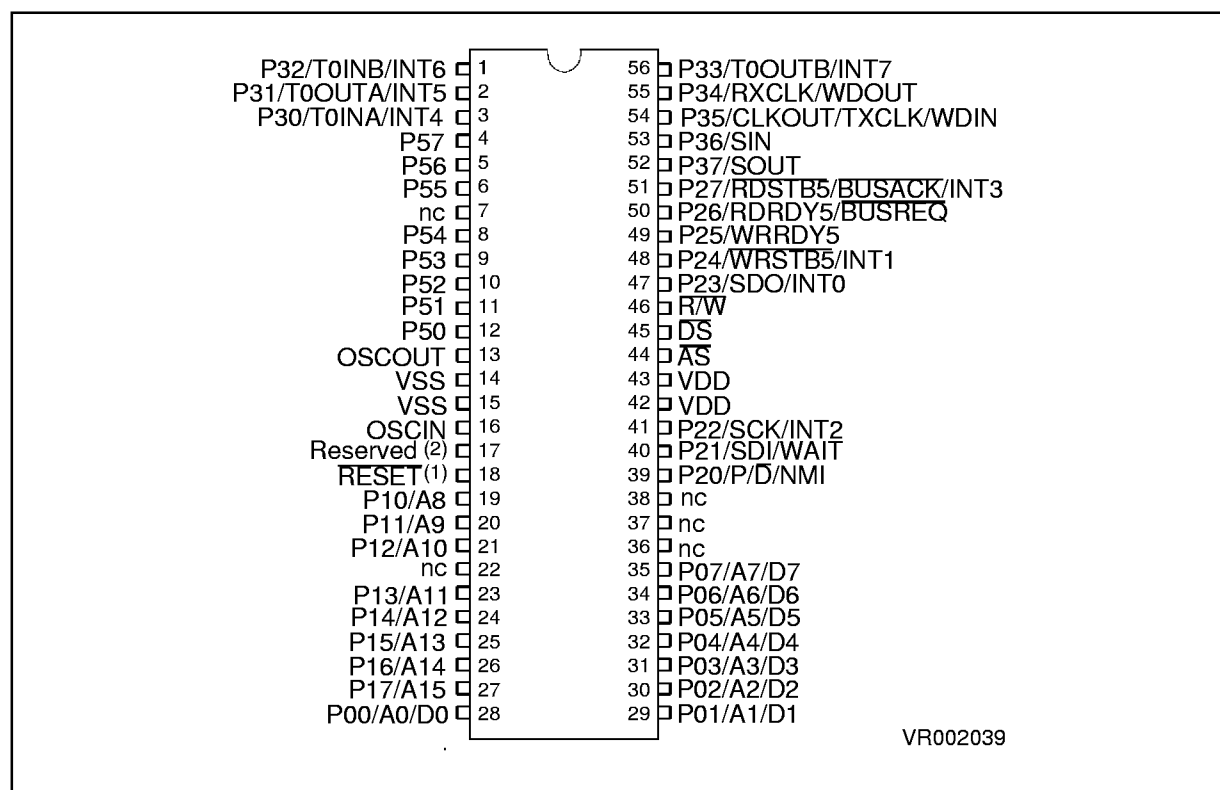
Note 1. This pin is also the VPP input for the EPROM based devices

Figure 1-2. 44 Pin PLCC Package



Note 1. This pin is also the VPP input for the EPROM based devices

Figure 1-3. 56 Pin DIP Package



Note 1. This pin is also the VPP input for the EPROM based devices

1.1 GENERAL DESCRIPTION

The ST90E27, E28 and ST90T27, T28 (following mentioned as ST90E2x) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

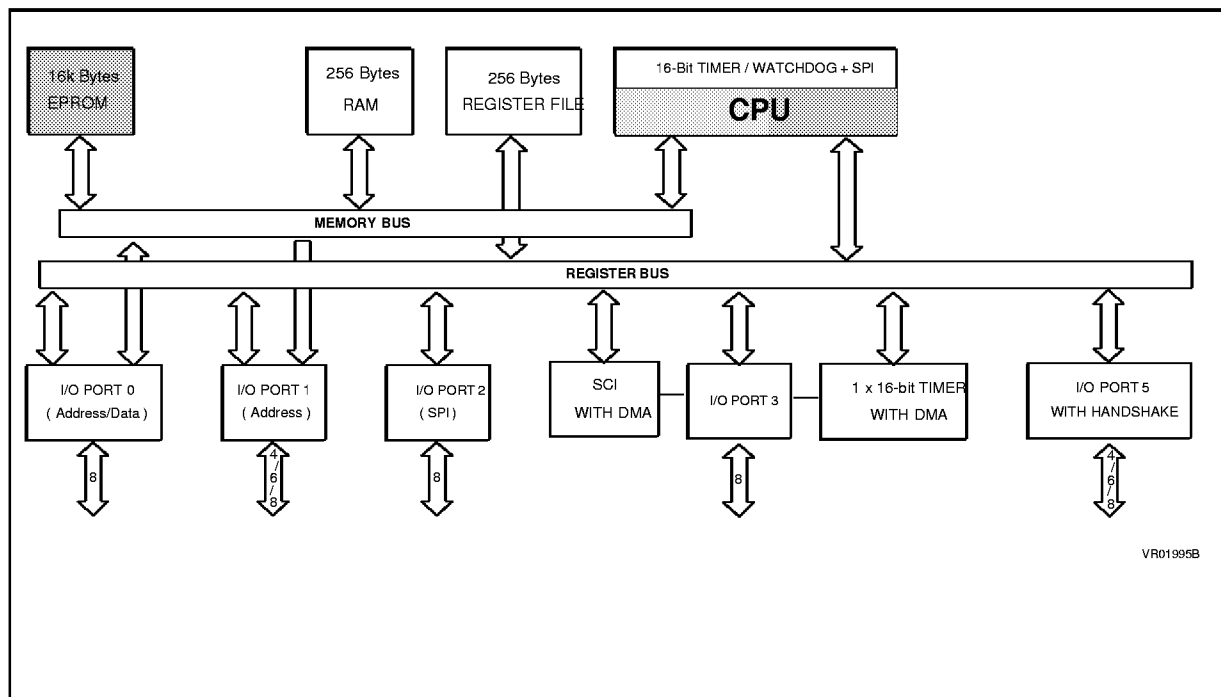
THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST902x ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E2x may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the modular design of the ST902X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I²C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST902X with up to 40 I/O lines dedicated to digital Input/Output. These lines are grouped into up to three 8-bit and two 4/6/8-bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/databus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Figure 1-4. ST90E27, E28 Block Diagram



GENERAL DESCRIPTION (Continued)

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allows simple use for complex waveform generation and measure-

ment, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

\overline{AS} . *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of \overline{AS} indicates that address, Read/Write (R/\overline{W}), and Data Memory signals are valid for program or data memory transfers. Under program control, \overline{AS} can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe (\overline{DS}) and R/\overline{W} .

\overline{DS} . *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of \overline{DS} . During a read cycle, Data In must be valid prior to the trailing edge of \overline{DS} . When the ST902x accesses on-chip memory, \overline{DS} is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, \overline{AS} and R/\overline{W} .

R/\overline{W} . *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/\overline{W} is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, \overline{AS} and \overline{DS} .

\overline{RESET}/V_{PP} . *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of \overline{RESET} , program execution begins from the Program memory location

pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input V_{PP} .

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

V_{DD} . Main Power Supply Voltage ($5V \pm 10\%$)

V_{SS} . Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P5.0-P5.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 40 lines grouped into I/O ports of 4/6/8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.3 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST902x may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1-1 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 1-1. ST902x I/O Port Alternate Function Summary

| I/O PORT Port.bit | Name | Function | Alternate Function | Pin Assignment | | |
|----------------------|---------------------|----------|---------------------------|----------------|--------|--------|
| | | | | SDIP56 | PDIP40 | PLCC44 |
| P0.0 | A0/D0 | I/O | Address/Data bit 0 mux | 28 | 8 | 10 |
| P0.1 | A1/D1 | I/O | Address/Data bit 1 mux | 29 | 9 | 11 |
| P0.2 | A2/D2 | I/O | Address/Data bit 2 mux | 30 | 10 | 12 |
| P0.3 | A3/D3 | I/O | Address/Data bit 3 mux | 31 | 11 | 13 |
| P0.4 | A4/D4 | I/O | Address/Data bit 4 mux | 32 | 12 | 14 |
| P0.5 | A5/D5 | I/O | Address/Data bit 5 mux | 33 | 13 | 15 |
| P0.6 | A6/D6 | I/O | Address/Data bit 6 mux | 34 | 14 | 16 |
| P0.7 | A7/D7 | I/O | Address/Data bit 7 mux | 35 | 15 | 17 |
| P1.0 | A8 | O | Address bit 8 | 19 | 4 | 4 |
| P1.1 | A9 | O | Address bit 9 | 20 | 5 | 5 |
| P1.2 | A10 | O | Address bit 10 | 21 | 6 | 6 |
| P1.3 | A11 | O | Address bit 11 | 23 | 7 | 7 |
| P1.4 | A12 | O | Address bit 12 | 24 | - | 8 |
| P1.5 | A13 | O | Address bit 13 | 25 | - | 9 |
| P1.6 | A14 | O | Address bit 14 | 26 | - | - |
| P1.7 | A15 | O | Address bit 15 | 27 | - | - |
| P2.0 | NMI | I | Non-Maskable Interrupt | 39 | 16 | 18 |
| P2.0 | P/ \overline{D} | O | Program/Data Space Select | 39 | 16 | 18 |
| P2.1 | SDI | I | SPI Serial Data In | 40 | 17 | 19 |
| P2.1 | \overline{WAIT} | I | External Wait Input | 40 | 17 | 19 |
| P2.2 | INT2 | I | External Interrupt 2 | 41 | 18 | 20 |
| P2.2 | SCK | O | SPI Serial Clock | 41 | 18 | 20 |
| P2.3 | INT0 | I | External Interrupt 0 | 47 | 23 | 25 |
| P2.3 | SDO | O | SPI Serial Data Out | 47 | 23 | 25 |
| P2.4 | INT1 | I | External Interrupt 1 | 48 | 24 | 26 |
| P2.4 | $\overline{WRSTB5}$ | I | Handshake Write Strobe P5 | 48 | 24 | 26 |
| P2.5 | WRRDY5 | O | Handshake Write Ready P5 | 49 | 25 | 27 |
| P2.6 | RDRDY5 | O | Handshake Read Ready P5 | 50 | 26 | 28 |

PIN DESCRIPTION (Continued)

Table 1-1. ST902x I/O Port Alternate Function Summary

| I/O PORT Port.bit | Name | Function | Alternate Function | Pin Assignment | | |
|----------------------|--------|----------|----------------------------|----------------|--------|--------|
| | | | | SDIP56 | PDIP40 | PLCC44 |
| P2.6 | BUSREQ | I | External Bus Request | 50 | 26 | 28 |
| P2.7 | INT3 | I | External Interrupt 1 | 51 | 27 | 29 |
| P2.7 | RDSTB5 | I | Handshake Read Strobe P5 | 51 | 27 | 29 |
| P2.7 | BUSACK | O | External Bus Acknowledge | 51 | 27 | 29 |
| P3.0 | INT4 | I | External Interrupt 4 | 3 | 35 | 37 |
| P3.0 | T0INA | I | MF Timer 0 Input A | 3 | 35 | 37 |
| P3.1 | INT5 | I | External Interrupt 5 | 2 | 34 | 36 |
| P3.1 | T0OUTA | O | MF Timer 0 Output A | 2 | 34 | 36 |
| P3.2 | INT6 | I | External Interrupt 6 | 1 | 33 | 35 |
| P3.2 | T0INB | I | MF Timer 0 Input B | 1 | 33 | 35 |
| P3.3 | INT7 | I | External Interrupt 7 | 56 | 32 | 34 |
| P3.3 | T0OUTB | O | MF Timer 0 Output B | 56 | 32 | 34 |
| P3.4 | RXCLK | I | SCI Receive Clock Input | 55 | 31 | 33 |
| P3.4 | WDOUT | O | T/WD Output | 55 | 31 | 33 |
| P3.5 | CLKOUT | O | SCI Byte Sync Clock Output | 54 | 30 | 32 |
| P3.5 | TXCLK | I | SCI Transmit Clock Input | 54 | 30 | 32 |
| P3.5 | WDIN | I | T/WD Input | 54 | 30 | 32 |
| P3.6 | SIN | I | SCI Serial Input | 53 | 29 | 31 |
| P3.7 | SOUT | O | SCI Serial Output | 52 | 28 | 30 |
| P5.0 | | O | I/O Handshake Port 5 | 12 | 39 | 43 |
| P5.1 | | O | I/O Handshake Port 5 | 11 | 38 | 42 |
| P5.2 | | O | I/O Handshake Port 5 | 10 | 37 | 41 |
| P5.3 | | O | I/O Handshake Port 5 | 9 | 36 | 40 |
| P5.4 | | O | I/O Handshake Port 5 | 8 | - | 39 |
| P5.5 | | O | I/O Handshake Port 5 | 6 | - | 38 |
| P5.6 | | O | I/O Handshake Port 6 | 5 | - | - |
| P5.7 | | O | I/O Handshake Port 7 | 4 | - | - |

1.4 MEMORY

The memory of the ST90E2x is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 64K bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E2x 16K bytes of on-chip EPROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T2x OTP version has the top 64 bytes of the EPROM reserved by SGS-THOMSON for testing purposes. The DATA space includes the 256 bytes of on-chip RAM memory at memory addresses 0000h through 00FFh.

WARNING. The ST90T2x has its 64 upper bytes in the internal EPROM reserved for testing purpose.

External data memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). Additional Data Memory may be decoded externally by using the P/D Alternate Function output. The on-chip general purpose (GP) Registers may also be used as RAM memory for minimum chip count systems.

1.5 EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E2x (16320 for the ST90T2x) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

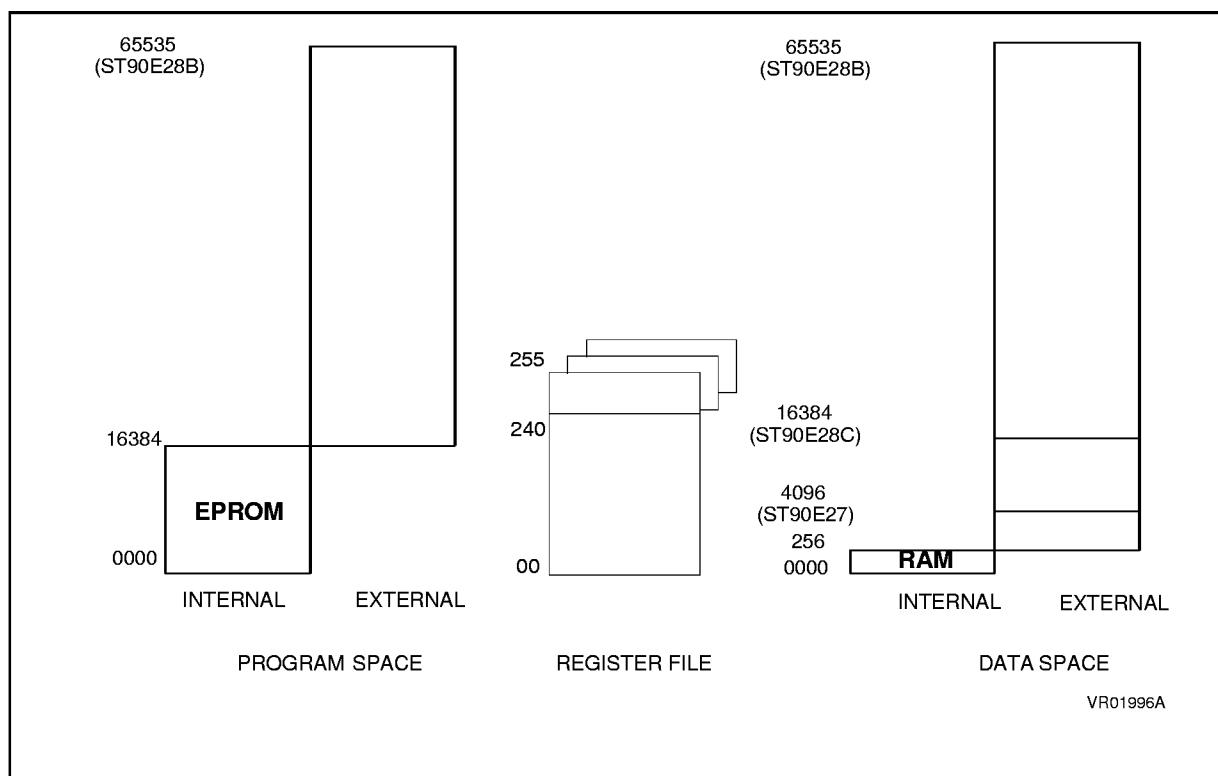
1.5.1 Eprom Erasing

The EPROM of the windowed package of the ST90E2x may be erased by exposure to Ultra-Violet light.

The erasure characteristic of the ST90E2x is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wave-lengths in the range 3000-4000Å. It is thus recommended that the window of the ST90E2x packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537Å. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm² power rating. The ST90E2x should be placed within 2.5cm (1inch) of the lamp tubes during erasure.

Figure 1-5. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{DD} | Supply Voltage | - 0.3 to 7.0 | V |
| V_I | Input Voltage | - 0.3 to $V_{DD} + 0.3$ | V |
| V_O | Output Voltage | - 0.3 to $V_{DD} + 0.3$ | V |
| V_{PP} | Input Voltage on V_{PP} Pin | -0.3 to 13.5 | V |
| T_{STG} | Storage Temperature | - 55 to + 150 | °C |
| I_{INJ} | Pin Injection Current Digital | -5 to 5 | mA |
| | Maximum accumulated pin injection Current in the device | -50 to 50 | mA |

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to VSS

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | | Unit |
|------------|-----------------------------------|-------|------|------|
| | | Min. | Max. | |
| T_A | Operating Temperature | - 40 | 85 | °C |
| V_{DD} | Operating Supply Voltage | 4.5 | 5.5 | V |
| f_{OSCE} | External Oscillator Frequency | | 24 | MHz |
| f_{OSCI} | Internal Clock Frequency (INTCLK) | | 12 | MHz |

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 10\%$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|------------|--|--|----------------|------|----------------|------|
| | | | Min. | Typ. | Max. | |
| V_{IHCK} | Clock Input High Level | External Clock | $0.7 V_{DD}$ | | $V_{DD} + 0.3$ | V |
| V_{ILCK} | Clock Input Low Level | External Clock | - 0.3 | | $0.3 V_{DD}$ | V |
| V_{IH} | Input High Level | TTL | 2.0 | | $V_{DD} + 0.3$ | V |
| | | CMOS | $0.7 V_{DD}$ | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Level | TTL | - 0.3 | | 0.8 | V |
| | | CMOS | - 0.3 | | $0.3 V_{DD}$ | V |
| V_{IHRS} | $\overline{\text{RESET}}$ Input High Level | | $0.7 V_{DD}$ | | $V_{DD} + 0.3$ | V |
| V_{ILRS} | $\overline{\text{RESET}}$ Input Low Level | | -0.3 | | $0.3 V_{DD}$ | V |
| V_{HYRS} | $\overline{\text{RESET}}$ Input Hysteresis | | 0.3 | | 1.5 | V |
| V_{OH} | Output High Level | Push Pull, $I_{load} = -0.8\text{mA}$ | $V_{DD} - 0.8$ | | | V |
| V_{OL} | Output Low Level | Push Pull or Open Drain, $I_{load} = 1.6\text{mA}$ | | | 0.4 | V |

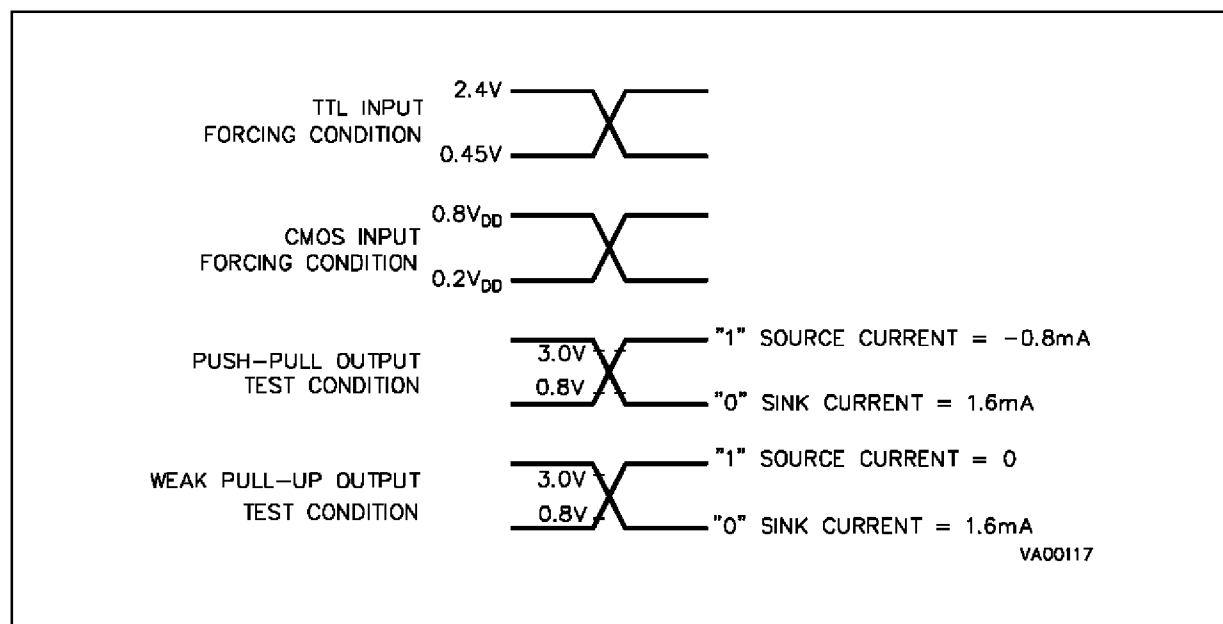
DC ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|------------|--|---|-------|-------|-------|---------|
| | | | Min. | Typ. | Max. | |
| I_{WPU} | Weak Pull-up Current | Bidirectional Weak Pull-up, $V_{OL} = 0V$ | - 50 | - 200 | - 420 | μA |
| I_{APU} | Active Pull-up Current, for INT0 and INT7 only | $V_{IN} < 0.8V$, under Reset | - 80 | - 200 | - 420 | μA |
| I_{LKIO} | I/O Pin Input Leakage | Input/Tri-State, $0V < V_{IN} < V_{DD}$ | - 10 | | + 10 | μA |
| I_{LKRS} | Reset Pin Input Leakage | $0V < V_{IN} < V_{DD}$ | - 30 | | + 30 | μA |
| I_{LKAP} | Active Pull-up Input Leakage | $0V < V_{IN} < 0.8V$ | - 10 | | + 10 | μA |
| I_{LKOS} | OSCIN Pin Input Leakage | $0V < V_{IN} < V_{DD}$ | - 10 | | + 10 | μA |
| V_{PP} | EPROM Programming Voltage | | 12.2 | 12.5 | 12.8 | V |
| I_{PP} | EPROM Programming Current | | | | 30 | mA |

Note:

1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working.

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS(V_{DD} = 5V ± 10% T_A = – 40°C to + 85°C, unless otherwise specified)

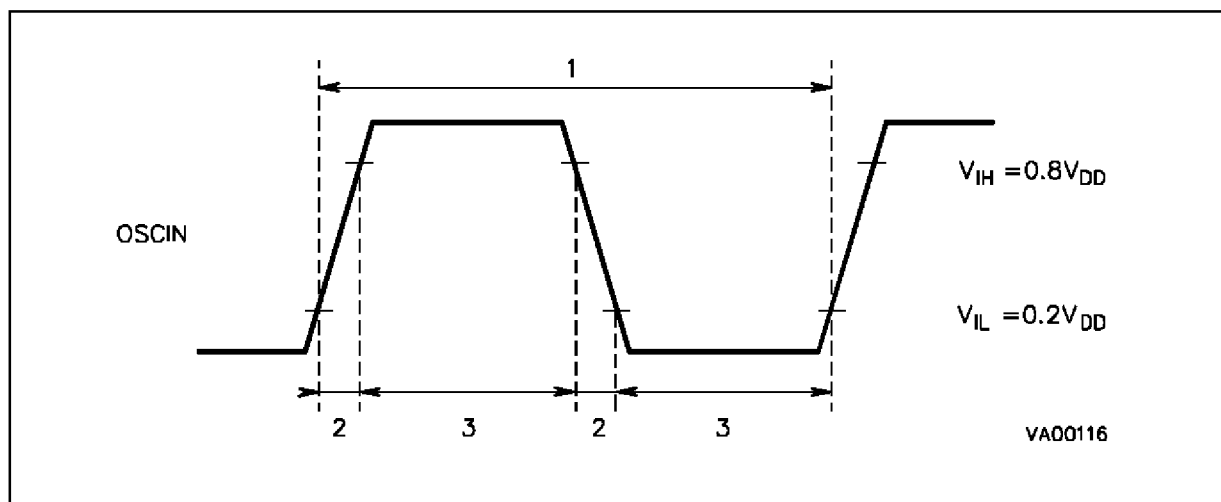
| Symbol | Parameter | Test Conditions | Value | | | Unit |
|-------------------|--|-----------------|-------|------|---------|------|
| | | | Min. | Typ. | Max. | |
| I _{DD} | Run Mode Current no CPUCLK prescale, Clock divide by 2 | 24MHz 4MHz | | | 40 | mA |
| I _{DP2} | Run Mode Current Prescale by 2 Clock divide by 2 | 24MHz 4MHz | | | 25 8 | mA |
| I _{WFI} | WFI Mode Current no CPUCLK prescale, Clock divide by 2 | 24MHz 4MHz | | | 15 5 | mA |
| I _{HALT} | HALT Mode Current | 24MHz | | | 10 | μA |

CLOCK TIMING TABLE
 $(V_{DD} = 5V \pm 10\%, T_A = -40^{\circ}C \text{ to } +85^{\circ}C)$

| N° | Symbol | Parameter | Value | | Unit | Note |
|----|------------|--------------------------|-------|------|------|------|
| | | | Min. | Max. | | |
| 1 | TpC | OSCIN Clock Period | 41.5 | | ns | 1 |
| | | | 83 | | ns | 2 |
| 2 | TrC, TfC | OSCIN Rise and Fall Time | | 12 | ns | |
| 3 | TwCL, TwCH | OSCIN Low and High Width | 17 | 25 | ns | 1 |
| | | | 38 | | ns | 2 |

Notes:

1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING


EXTERNAL BUS TIMING TABLE ($V_{DD} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_{load} = 50\text{pF}$, $\text{CPUCLK} = 12\text{MHz}$, unless otherwise specified)

| N° | Symbol | Parameter | Value (Note) | | | | Unit |
|----|-------------|---|-----------------------------|--|------|------|------|
| | | | OSCIN Divided By 2 | OSCIN Not Divided By 2 | Min. | Max. | |
| 1 | TsA (AS) | Address Set-up Time before $\overline{\text{AS}} \uparrow$ | $\text{TpC} (2P+1) - 22$ | $\text{TwCH} + \text{PTpC} - 18$ | 20 | | ns |
| 2 | ThAS (A) | Address Hold Time after $\overline{\text{AS}} \uparrow$ | $\text{TpC} - 17$ | $\text{TwCL} - 13$ | 25 | | ns |
| 3 | TdAS (DR) | $\overline{\text{AS}} \uparrow$ to Data Available (read) | $\text{TpC} (4P+2W+4) - 52$ | $\text{TpC} (2P+W+2) - 51$ | | 115 | ns |
| 4 | TwAS | $\overline{\text{AS}}$ Low Pulse Width | $\text{TpC} (2P+1) - 7$ | $\text{TwCH} + \text{PTpC} - 3$ | 35 | | ns |
| 5 | TdAz (DS) | $\overline{\text{DS}} \downarrow$ to Address Float | | | 12 | | ns |
| 6 | TwDSR | $\overline{\text{DS}}$ Low Pulse Width (read) | $\text{TpC} (4P+2W+3) - 20$ | $\text{TwCH} + \text{TpC} (2P+W+1) - 16$ | 105 | | ns |
| 7 | TwDSW | $\overline{\text{DS}}$ Low Pulse Width (write) | $\text{TpC} (2P+2W+2) - 13$ | $\text{TpC} (P+W+1) - 13$ | 70 | | ns |
| 8 | TdDSR (DR) | $\overline{\text{DS}} \downarrow$ to Data Valid Delay (read) | $\text{TpC} (4P+2W-3) - 50$ | $\text{TwCH} + \text{TpC} (2P+W+1) - 46$ | | 75 | ns |
| 9 | ThDR (DS) | Data to $\overline{\text{DS}} \uparrow$ Hold Time (read) | 0 | 0 | 0 | | ns |
| 10 | TdDS (A) | $\overline{\text{DS}} \uparrow$ to Address Active Delay | $\text{TpC} - 7$ | $\text{TwCL} - 3$ | 35 | | ns |
| 11 | TdDS (AS) | $\overline{\text{DS}} \uparrow$ to $\overline{\text{AS}} \downarrow$ Delay | $\text{TpC} - 18$ | $\text{TwCL} - 14$ | 24 | | ns |
| 12 | TsR/W (AS) | R/ $\overline{\text{W}}$ Set-up Time before $\overline{\text{AS}} \uparrow$ | $\text{TpC} (2P+1) - 22$ | $\text{TwCH} + \text{PTpC} - 18$ | 20 | | ns |
| 13 | TdDSR (R/W) | $\overline{\text{DS}} \uparrow$ to R/ $\overline{\text{W}}$ and Address Not Valid Delay | $\text{TpC} - 9$ | $\text{TwCL} - 5$ | 33 | | ns |
| 14 | TdDW (DSW) | Write Data Valid to $\overline{\text{DS}} \downarrow$ Delay (write) | $\text{TpC} (2P+1) - 32$ | $\text{TwCH} + \text{PTpC} - 28$ | 10 | | ns |
| 15 | ThDS (DW) | Data Hold Time after $\overline{\text{DS}} \uparrow$ (write) | $\text{TpC} - 9$ | $\text{TwCL} - 5$ | 33 | | ns |
| 16 | TdA (DR) | Address Valid to Data Valid Delay (read) | $\text{TpC} (6P+2W+5) - 68$ | $\text{TwCH} + \text{TpC} (3P+W+2) - 64$ | | 140 | ns |
| 17 | TdAs (DS) | $\overline{\text{AS}} \uparrow$ to $\overline{\text{DS}} \downarrow$ Delay | $\text{TpC} - 18$ | $\text{TwCL} - 14$ | 24 | | ns |

EXTERNAL WAIT TIMING TABLE ($V_{DD} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_{load} = 50\text{pF}$, $\text{INTCLK} = 12\text{MHz}$, Push-pull output configuration, unless otherwise specified)

| N° | Symbol | Parameter | Value (Note) | | | | Unit |
|----|-------------|---|---------------------------|---------------------------|------|------------|------|
| | | | OSCIN Divided By 2 | OSCIN Not Divided By 2 | Min. | Max. | |
| 1 | TdAs (WAIT) | $\overline{\text{AS}} \uparrow$ to $\overline{\text{WAIT}} \downarrow$ Delay | $2(P+1)\text{TpC} - 29$ | $2(P+1)\text{TpC} - 29$ | | 40 | ns |
| 2 | TdAs (WAIT) | $\overline{\text{AS}} \uparrow$ to $\overline{\text{WAIT}} \downarrow$ Min. Delay | $2(P+W+1)\text{TpC} - 4$ | $2(P+W+1)\text{TpC} - 4$ | 80 | | ns |
| 3 | TdAs (WAIT) | $\overline{\text{AS}} \uparrow$ to $\overline{\text{WAIT}} \downarrow$ Max. Delay | $2(P+W+1)\text{TpC} - 29$ | $2(P+W+1)\text{TpC} - 29$ | | $83W + 40$ | ns |

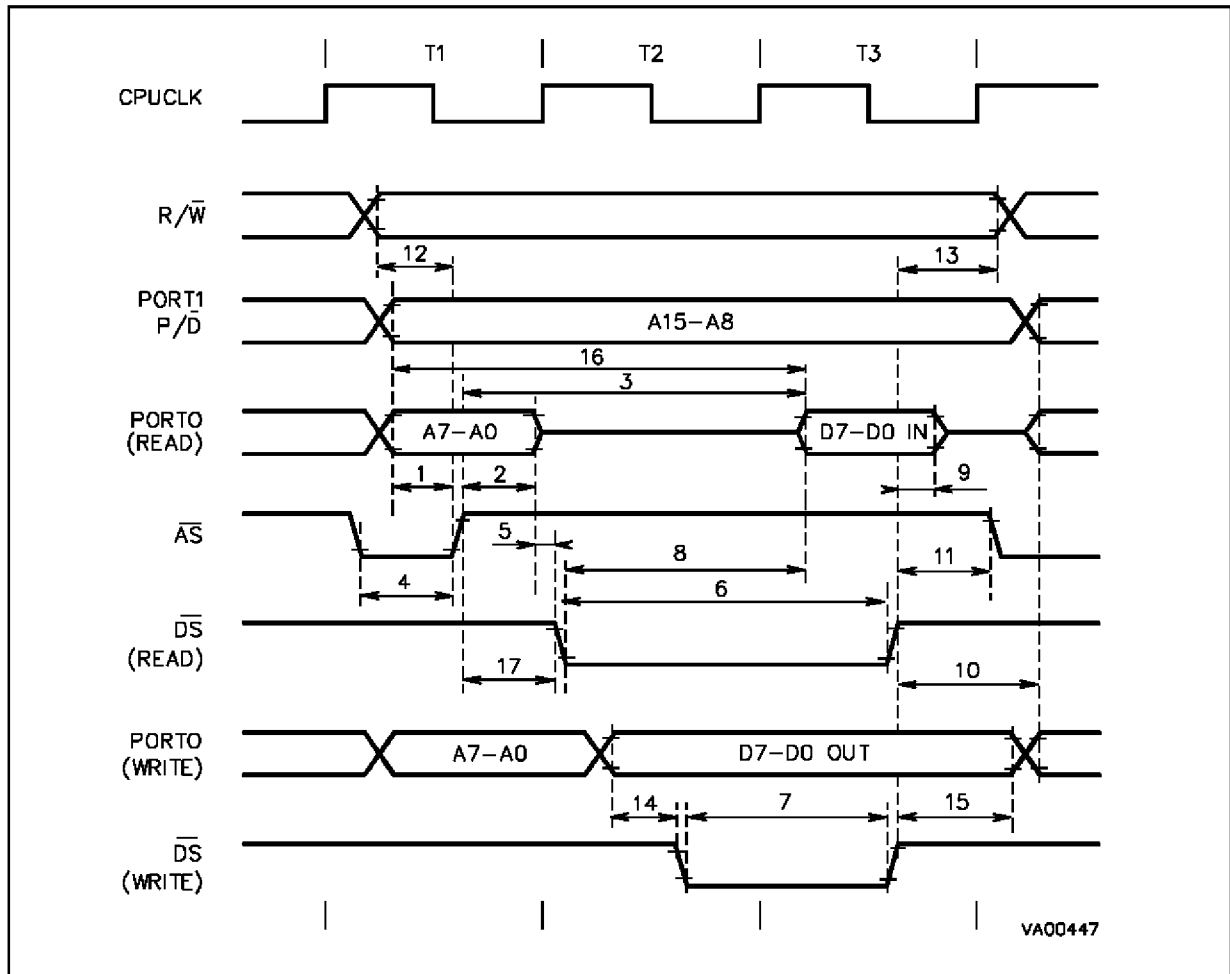
Note: (for both table) The value in the left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value in the right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:

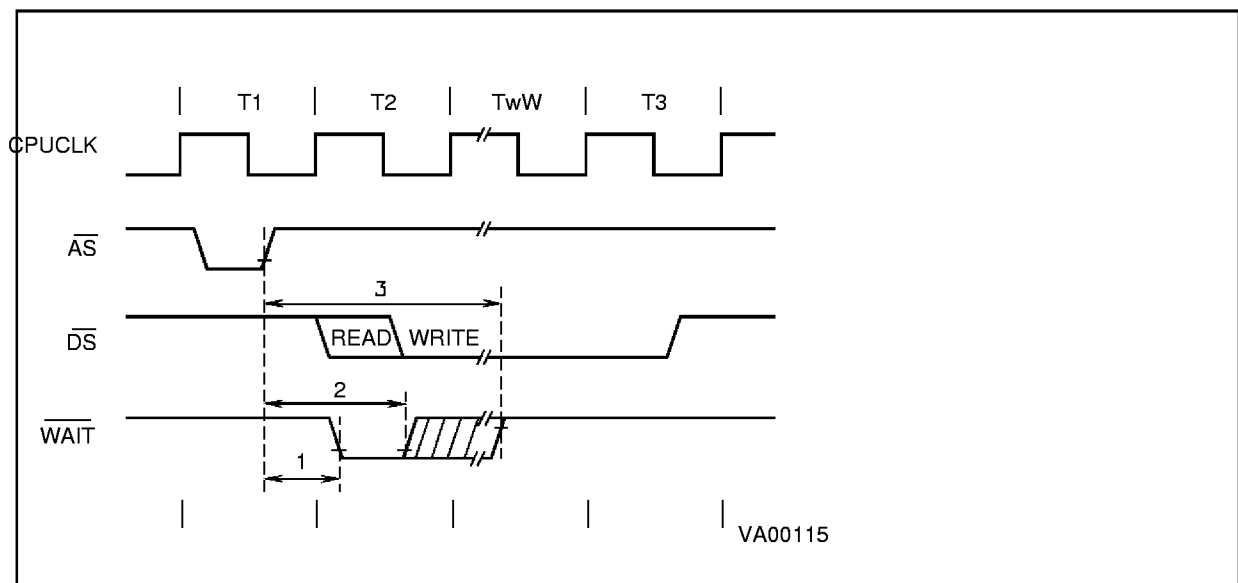
P = Clock Prescaling Value
W = Wait Cycles

TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING



HANDSHAKE TIMING TABLE ($V_{DD} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_{load} = 50\text{pF}$, $\text{INTCLK} = 12\text{MHz}$, Push-pull output configuration, unless otherwise specified)

| N° | Symbol | Parameter | Value (Note) | | | | Min. | Max. | Unit |
|----|-------------|--|---------------------|--------|------------------------|----------------|------|------|------|
| | | | OSCIN Divided By 2 | | OSCIN Not Divided By 2 | | | | |
| | | | Min. | Max. | Min. | Max. | | | |
| 1 | TwRDY | RDRDY, WRRDY Pulse Width in One Line Handshake | 2TpC (P+W+1) –18 | | TpC (P+W+1) – 18 | | 65 | | ns |
| 2 | TwSTB | \overline{RDSTB} , \overline{WRSTB} Pulse Width | 2TpC+12 | | TpC+12 | | 95 | | ns |
| 3 | TdST (RDY) | \overline{RDSTB} , or $\overline{WRSTB} \uparrow$ to RDRDY or WRRDY \downarrow | | TpC+45 | | (TpC-TwCL) +45 | | 87 | ns |
| 4 | TsPD (RDY) | Port Data to RDRDY \uparrow Set-up Time | (2P+2W+1) TpC –25 | | TwCH+ (W+P) TpC –25 | | 16 | | ns |
| 5 | TsPD (RDY) | Port Data to WRRDY \downarrow Set-up Time in One Line Handshake | 43 | | 43 | | 43 | | ns |
| 6 | ThPD (RDY) | Port Data to WRRDY \downarrow Hold Time in One Line Handshake | 0 | | 0 | | 0 | | ns |
| 7 | TsPD (STB) | Port Data to $\overline{WRSTB} \uparrow$ Set-up Time | 10 | | 10 | | 10 | | ns |
| 8 | ThPD (STB) | Port Data to $\overline{WRSTB} \uparrow$ Hold Time | 25 | | 25 | | 25 | | ns |
| 9 | TdSTB (PD) | $\overline{RDSTBD} \uparrow$ to Port Data Delay Time in Bidirectional Handshake | | 35 | | 35 | | 35 | ns |
| 10 | TdSTB (PHZ) | $\overline{RDSTB} \uparrow$ to Port High-Z Delay Time in Bidirectional Handshake | | 25 | | 25 | | 25 | ns |

Note: The value in the left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.

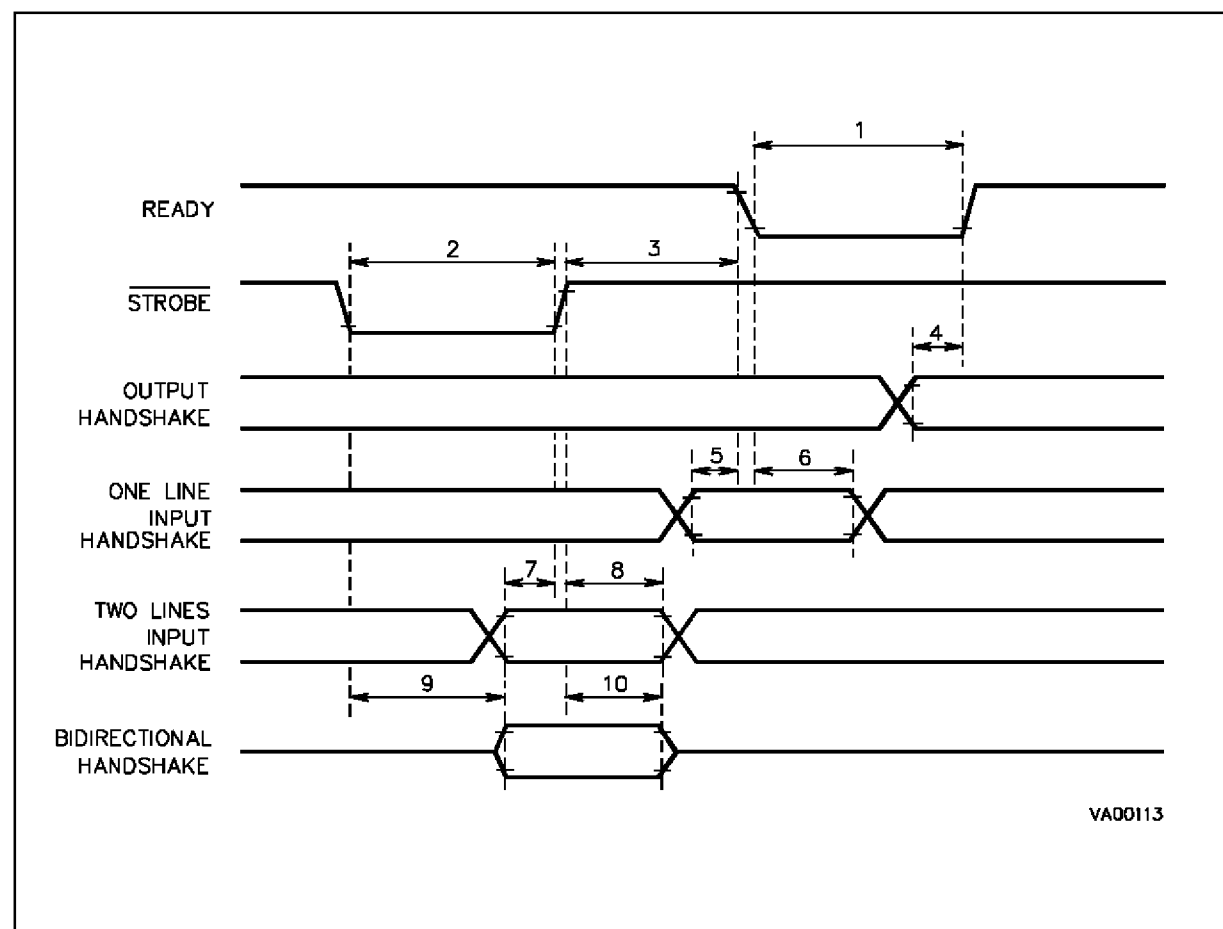
The value in the right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:

P = Clock Prescaling Value (R235.4,3,2)

W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

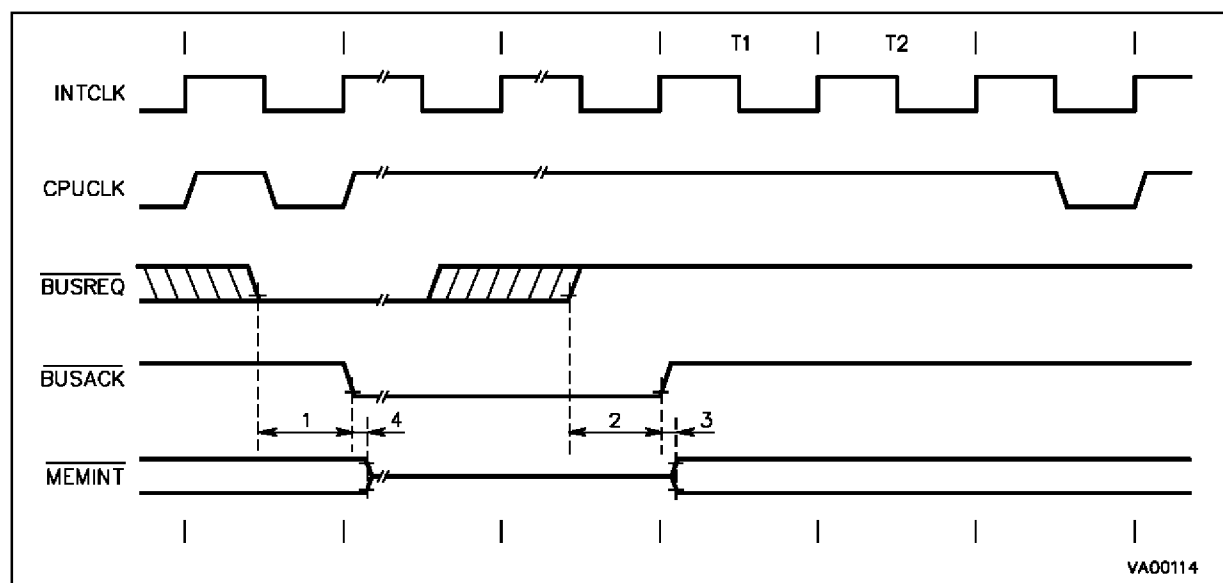


BUS REQUEST/ACKNOWLEDGE TIMING TABLE ($V_{DD} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_{load} = 50\text{pF}$, $\text{INTCLK} = 12\text{MHz}$, Push-pull output configuration, unless otherwise specified)

| N° | Symbol | Parameter | Value (Note) | | | | Unit |
|----|----------------------------|--|----------------------|-----------------------------|------|------|------|
| | | | OSCIN Divided By 2 | OSCIN Not Divided By 2 | Min. | Max. | |
| 1 | T _{dB} R (BACK) | $\overline{\text{BREQ}} \downarrow$ to $\overline{\text{BUSACK}} \downarrow$ | $T_{pC}+8$ | $T_{wCL}+12$ | 50 | | ns |
| | | | $T_{pC}(6P+2W+7)+65$ | $T_{pC}(3P+W+3)+T_{wCL}+65$ | | 360 | ns |
| 2 | T _{dB} R (BACK) | $\overline{\text{BREQ}} \uparrow$ to $\overline{\text{BUSACK}} \uparrow$ | $3T_{pC}+60$ | $T_{pC}+T_{wCL}+60$ | | 185 | ns |
| 3 | T _d BACK (BREL) | $\overline{\text{BUSACK}} \downarrow$ to Bus Release | 20 | 20 | | 20 | ns |
| 4 | T _d BACK (BACT) | $\overline{\text{BUSACK}} \uparrow$ to Bus Active | 20 | 20 | | 20 | ns |

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



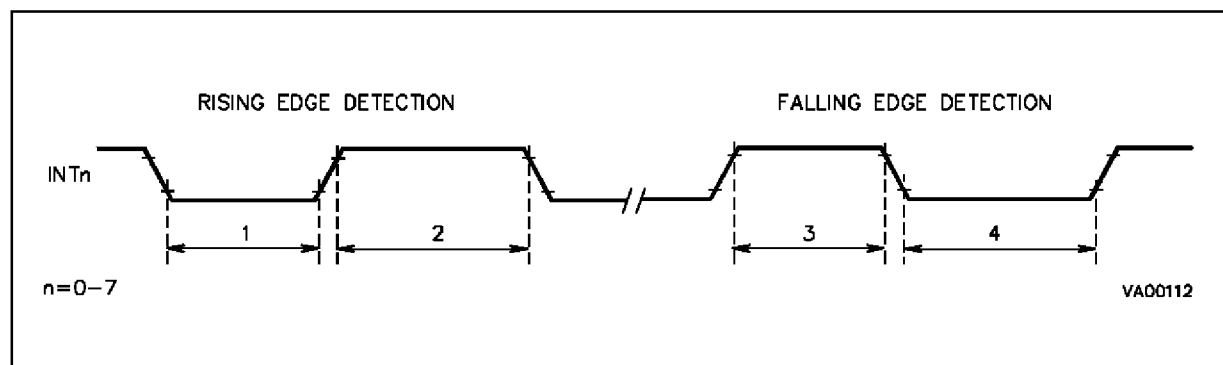
Note : MEMINT = Group of memory interface signals: AS, DS, R/W, P00-P07, P10-P17

EXTERNAL INTERRUPT TIMING TABLE ($V_{DD} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_{load} = 50\text{pF}$, $\text{INTCLK} = 12\text{MHz}$, Push-pull output configuration, unless otherwise specified)

| N° | Symbol | Parameter | Value (Note) | | | | Unit |
|----|-----------|---|-------------------------|-----------------------------|------|------|------|
| | | | OSCIN Divided By 2 Min. | OSCIN Not Divided By 2 Min. | Min. | Max. | |
| 1 | T_{wLR} | Low Level Minimum Pulse Width in Rising Edge Mode | $2T_{pC}+12$ | $T_{pC}+12$ | 95 | | ns |
| 2 | T_{wHR} | High Level Minimum Pulse Width in Rising Edge Mode | $2T_{pC}+12$ | $T_{pC}+12$ | 95 | | ns |
| 3 | T_{wHF} | High Level Minimum Pulse Width in Falling Edge Mode | $2T_{pC}+12$ | $T_{pC}+12$ | 95 | | ns |
| 4 | T_{wLF} | Low Level Minimum Pulse Width in Falling Edge Mode | $2T_{pC}+12$ | $T_{pC}+12$ | 95 | | ns |

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL INTERRUPT TIMING

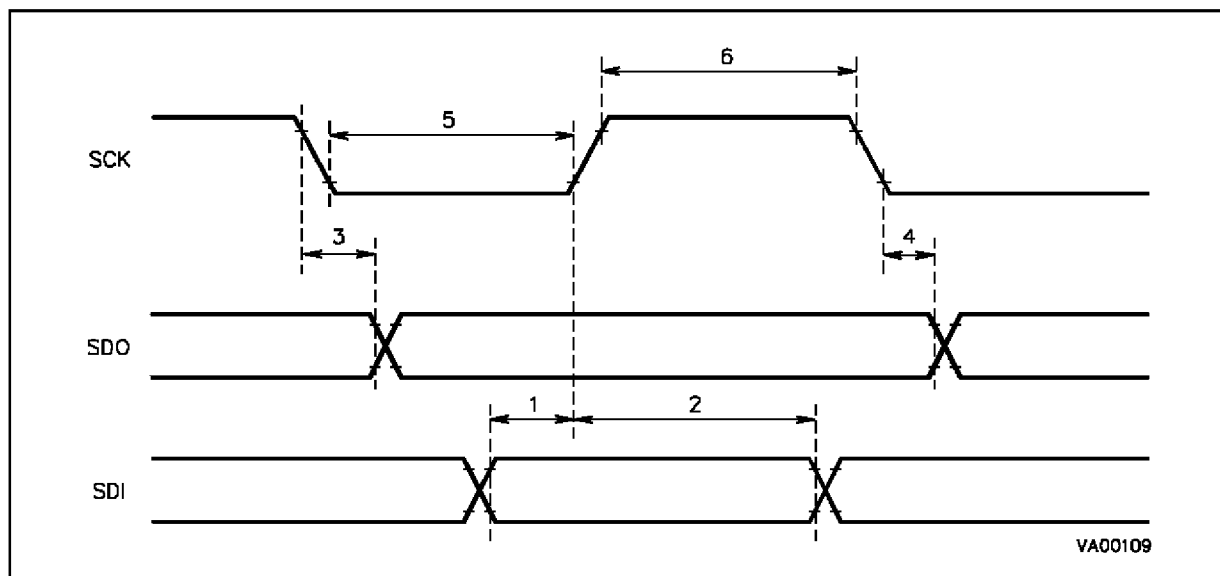


SPI TIMING TABLE ($V_{DD} = 5V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $C_{load} = 50pF$, $INTCLK = 12MHz$, Output Alternate Function set as Push-pull)

| N° | Symbol | Parameter | Value | | Unit |
|----|----------|--------------------------|--------------------|------|------|
| | | | Min. | Max. | |
| 1 | TsDI | Input Data Set-up Time | 100 | | ns |
| 2 | ThDI (1) | Input Data Hold Time | $1/2 T_{pC} + 100$ | | ns |
| 3 | TdOV | SCK to Output Data Valid | | 100 | ns |
| 4 | ThDO | Output Data Hold Time | -20 | | ns |
| 5 | TwSKL | SCK Low Pulse Width | 300 | | ns |
| 6 | TwSKH | SCK High Pulse Width | 300 | | ns |

Note: 1. T_{pC} is the OSCIN Clock period.

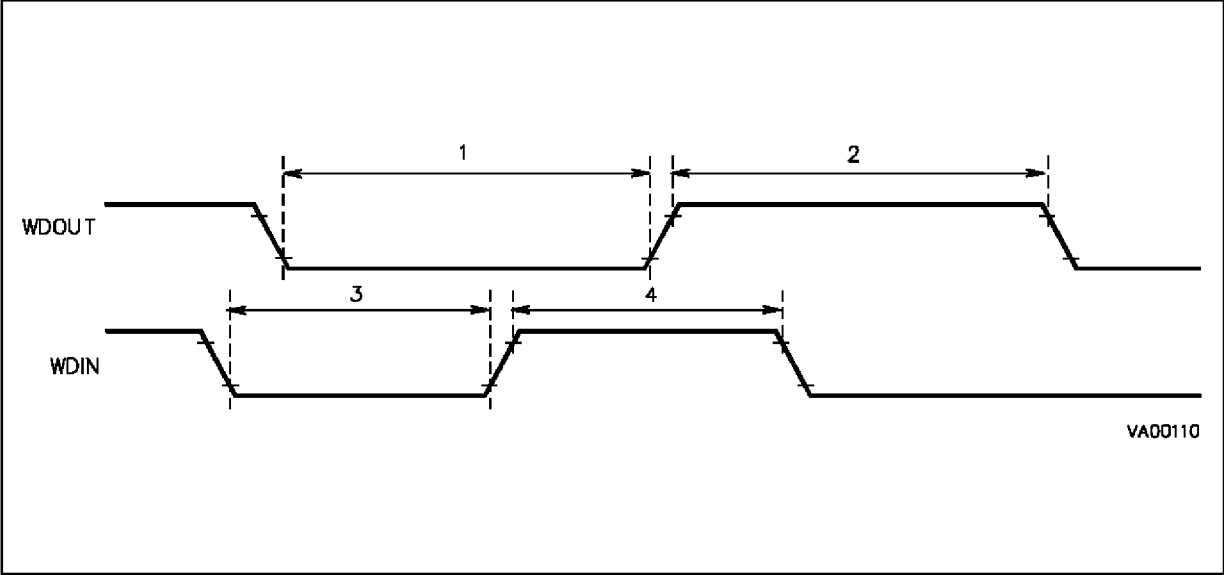
SPI TIMING



WATCHDOG TIMING TABLE($V_{DD} = 5V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $C_{load} = 50pF$, CPUCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

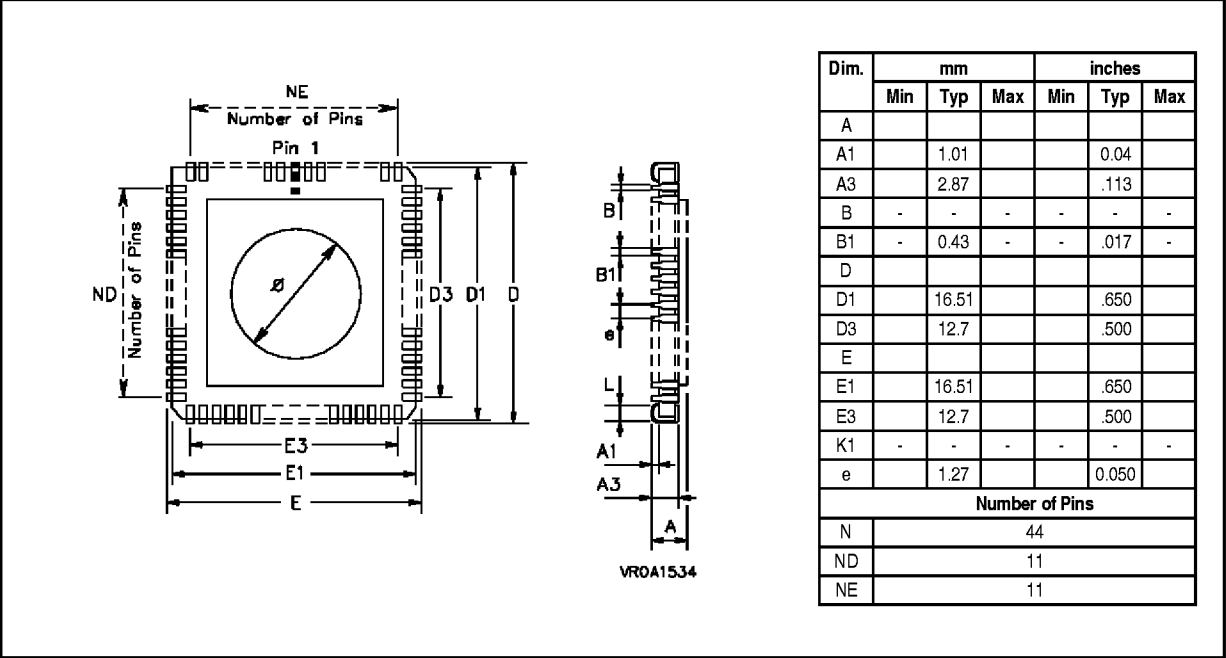
| N° | Symbol | Parameter | Values | | Unit |
|----|-------------|------------------------|--------|------|------|
| | | | Min. | Max. | |
| 1 | T_{wWDOL} | WDOUT Low Pulse Width | 620 | | ns |
| 2 | T_{wWDOH} | WDOUT High Pulse Width | 620 | | ns |
| 3 | T_{wWDIL} | WDIN High Pulse Width | 350 | | ns |
| 4 | T_{wWDIH} | WDIN Low Pulse Width | 350 | | ns |

WATCHDOG TIMING

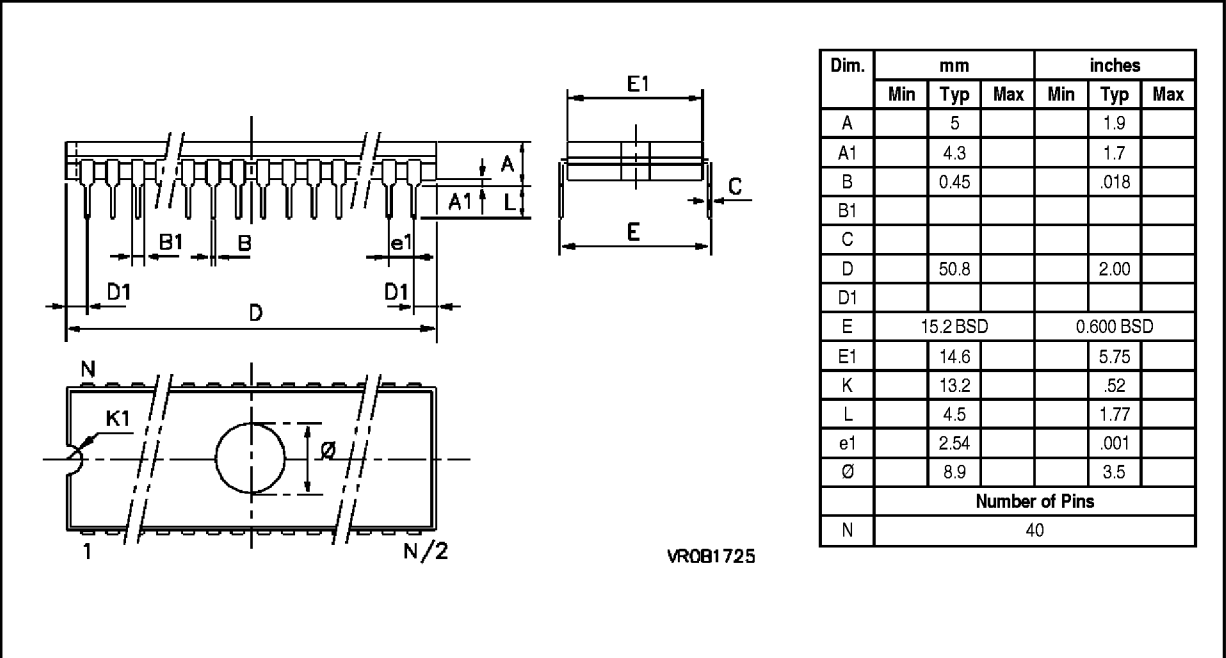


PACKAGE MECHANICAL DATA

44-Pin Ceramic Leadless Chip Carrier Package with Window

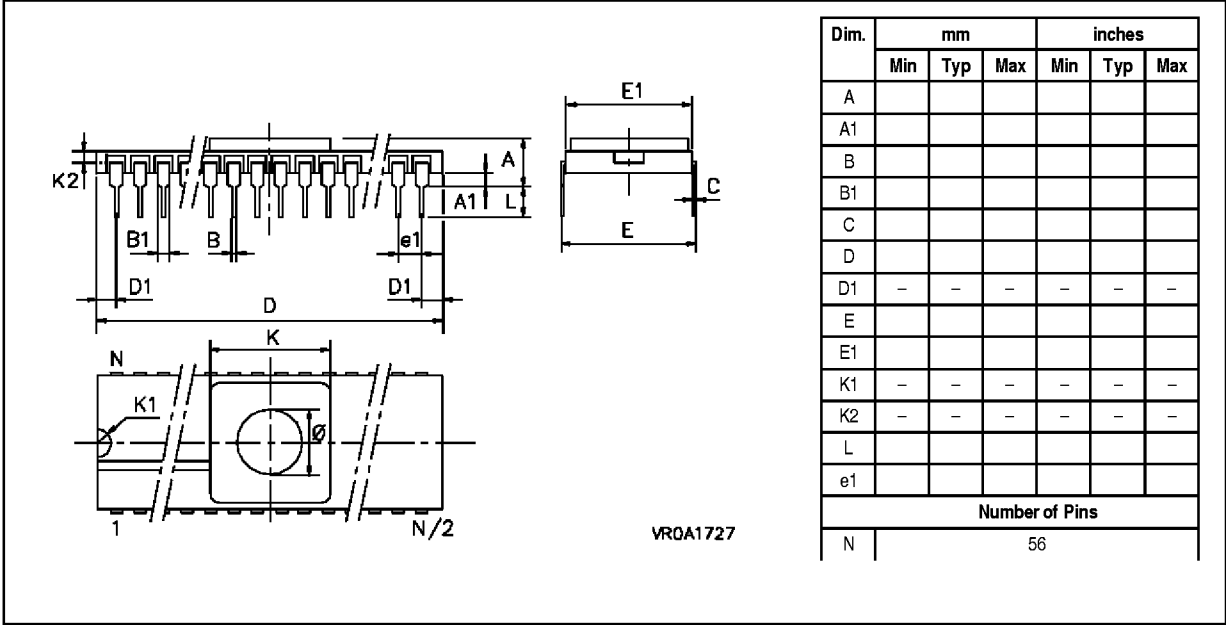


40-Pin Ceramic Dual In Line Package with Window



PACKAGE MECHANICAL DATA (Continued)

56-Pin Ceramic Dual In Line Package, 600 Mil Width



ORDERING INFORMATION

| Sales Type | Frequency | Temperature Range | Package |
|------------|-----------|-------------------|-----------|
| ST90E27D0 | 24MHz | 25°C | CDIP40-W |
| ST90E28L0 | | 25°C | CLCC44-W |
| ST90E28D0 | | 25°C | CSDIP56-W |
| ST90T27B6 | | -40°C to + 85°C | PDIP40 |
| ST90T28C6 | | -40°C to + 85°C | PLCC44 |
| ST90T28B6 | | -40°C to + 85°C | PDIP56 |