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Chapter 9 — CD-ROM Content

Supplemental Files

- Measuring Receiver Phase Noise
- "Oscillator Design Using *LTSpice"* by David Stockton, GM4ZNX (includes *LTSpice* simulation files in SwissRoll folder)
- Using the MC1648 in Oscillators
- "Novel Grounded Base Oscillator Design for VHF-UHF" by Dr Ulrich Rohde, N1UL
- "Optimized Oscillator Design" by Dr Ulrich Rohde, N1UL
- "Oscillator Phase Noise" by Dr Ulrich Rohde, N1UL
- "Some Thoughts On Crystal Oscillator Design" by Dr Ulrich Rohde, N1UL

Chapter 9

Oscillators and Synthesizers

RF signal paths all need to start somewhere. These starting places are oscillators — circuits that generate a periodic output signal without any input signal. In general, we use sinusoidal waveforms for communication signals, and square-wave outputs for digital signals (clocks). Ham operators care greatly about oscillator design. In a crowded band, a good oscillator is necessary for the receiver to resolve each of the signals present. Similarly, a good oscillator is needed for all transmitters so that our signals use only the amount of spectrum necessary for communication.

This chapter has been updated and rewritten for the 90th edition by Earl McCune, WA6SUH, from material originally written by David Stockton, GM4ZNX, and Frederick J. Telewski, WA7TZY. The sidebar on Phase-Locked Loops was contributed by Jerry DeHaven, WAØACF. Dr Ulrich Rohde, N1UL, contributed material on oscillator designs along with articles on phase noise and oscillator design which may be found on the *Handbook* CD-ROM. The section on Fractional-N Synthesizers was contributed to the 92nd edition by David Stockton, GM4ZNX.

The sheer number of different oscillator circuits seen in the literature can be intimidating, but their great diversity is an illusion that evaporates once their underlying pattern is seen. Despite the number of combinations that are possible, a manageably small number of oscillator types will cover all but very special requirements. Look at an oscillator circuit and "read" it: What form of filter — resonator — does it use? What form of amplifier? How have the amplifier's input and output been coupled into the filter? How is the filter tuned? These are simple, easily answered questions that put oscillator types into appropriate categories and make them understandable. The questions themselves make more sense when we understand the mechanics of oscillation, in which resonance plays a major role.

9.1 How Oscillators Work

Any oscillator is a fundamentally nonlinear device. Among other reasons, this circuit has an RF output even without any RF input. Any linear circuit can change the magnitude and phase shift on the signal only at its input.

9.1.1 Resonance

We are all familiar with pendulums. A weight (a mass in a gravitational field) hanging from some kind of string will swing back and forth with a very regular period. It has been known for millennia that this period does not change as long as the length of the string does not change, regardless of the amount of weight or how far it swings. Only a few centuries ago did Isaac Newton invent enough calculus to show why this is true. Yet even before Newton's seminal work, people were comfortable enough with this very predictable swinging period that pendulums were adopted as the basis of clocks and timekeeping.

Newton showed that the pendulum works by continuously exchanging its energy between potential (height) and kinetic (moving) forms. The mass moves fastest when it has minimum height (all energy is kinetic), and stops moving (all energy is potential) when it has maximum height. Further, when the energy is all in one form, the ingredients are in place to assure that conversion to the other form will happen. At the bottom, when the mass is moving fastest, its momentum assures that it will keep moving. The string constrains that movement and forces it to rise. When the mass stops rising, the string pulls on it in a different direction from gravity, which is pulling it down. This assures that the mass will fall and pick up speed — and the cycle repeats.

An electrical equivalent is created by the combination of an inductor and a capacitance. The inductor stores energy in a magnetic field when there is a current (motion of charge) flowing through it. The capacitor stores energy in an electric field when there is a voltage (presence of charge) in it. Connect the two together and the charge in the capacitor (electric potential energy) forces a current to begin flowing through the inductor. When the charge in the capacitor is zero, the current in the inductor is maximum (magnetic energy) and the magnetic field forces the current to continue, which recharges the capacitor with the opposite polarity. Just like the pendulum, the combination of inductor and capacitor trade energy back and forth between two types. Because energy is being stored in this circuit, we call this a *tank circuit*.

The common features between a pendulum and an electrical tank circuit are shown in **Fig 9.1**. For the pendulum, the speed of the mass and the displacement (height) are both sinusoidal with time and offset in phase by 90 degrees. Similarly, the voltage and current in

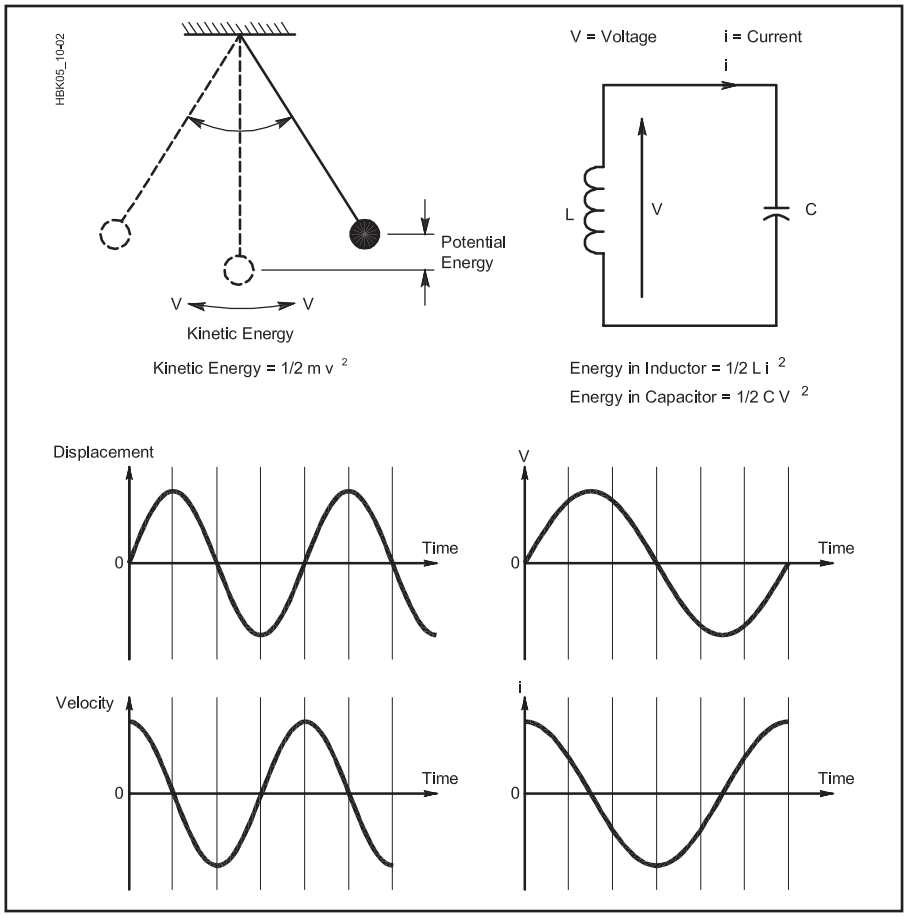


Fig 9.1 — A resonator lies at the heart of every oscillatory mechanical and electrical system. A mechanical resonator (here, a pendulum) and an electrical resonator (here, a tuned circuit consisting of L and C in parallel) share the same mechanism: the regular movement of energy between two forms — potential and kinetic in the pendulum, electric and magnetic in the tuned circuit. Both of these resonators share another trait: Any oscillations induced in them eventually die out because of losses — in the pendulum, due to drag and friction; in the tuned circuit, due to the resistance, coupling to other circuits, and radiation. Note that the curves corresponding to the pendulum's displacement vs velocity and the tuned circuit's voltage vs current differ by one-quarter of a cycle, or 90°.

the LC tank circuit are sinusoidal and offset by 90 degrees.

Unfortunately, these oscillations do not continue forever. When you pull a pendulum aside and let it go, it will swing for a while and eventually stop. This is due to losses that take a little bit of energy away from the pendulum each time it swings. For a pendulum, one major loss mechanism is air drag: As the mass moves through the air, some energy is spent to move the air out of its way. There are losses from the string as well: Every time the string is bent, it warms up just a little bit. This also takes energy away from the pendulum. With these losses, the energy conversion is not complete between kinetic and potential forms, and each cycle of the oscillation is slightly smaller than the one before. We say that the oscillation is *damped*.

The electrical tank circuit works similarly. When an oscillation is started, say with a spark charging the capacitance as shown in **Fig 9.2A**, we see that this oscillation is also damped. The primary losses include resistance in the inductor and interactions of the electric and magnetic fields with other conductors. There is also direct radiation of electromagnetic fields — exactly what we want to happen for radio communication, but counts as an energy loss from the resonator.

It was not hard to figure out that a damped oscillation is not very useful for radio communication. We need our signals to last for a longer time so they can carry useful information. The first attempt to solve this problem was to repeatedly apply sparks to the tank circuit in a manner like that of Fig 9.2B. This still is not a continuous sine wave and it is very noisy because, among other things, the timing of the sparks is extremely difficult to hold in exact synchronization with the tank oscillation. There has to be a better way…

9.1.2 Maintained Resonance (CW: Continuous Waves)

What we need is a way to make up for the resonator losses, but only just enough to maintain the oscillation indefinitely. Invention of the escapement achieved this for the pendulum, and that's what provides the distinctive "tick-tock" of a pendulum clock. Electrically we use an amplifier to do the same thing.

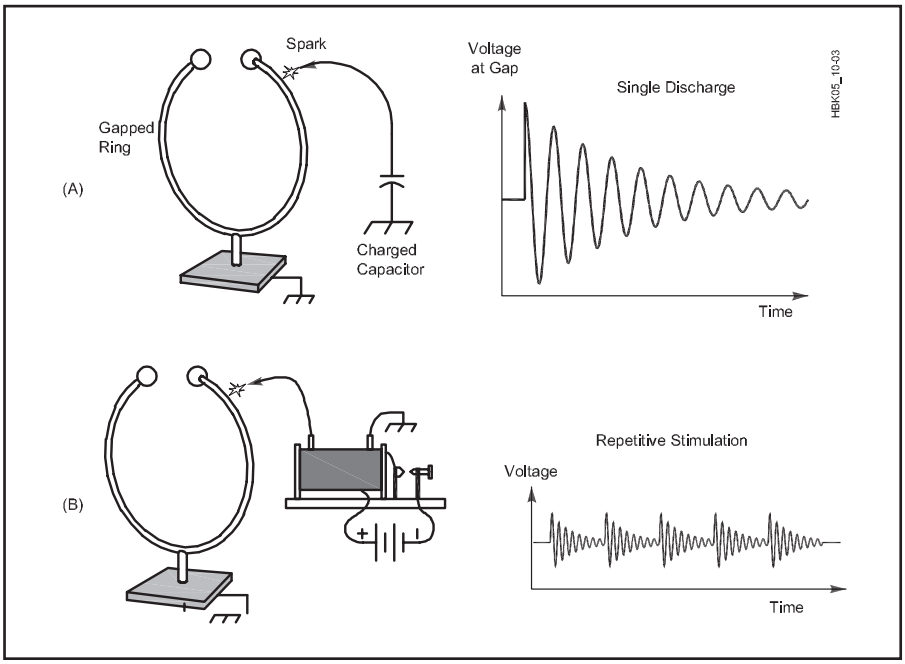


Fig 9.2 — Stimulating a resonance, 1880s style. Shock-exciting a gapped ring by a charged capacitor causes the ring to oscillate at its resonant frequency. The result is a damped wave, each successive alternation of which is weaker than its predecessor because of resonator losses. Repetitively stimulating the ring produces trains of damped waves, but oscillation is not continuous.

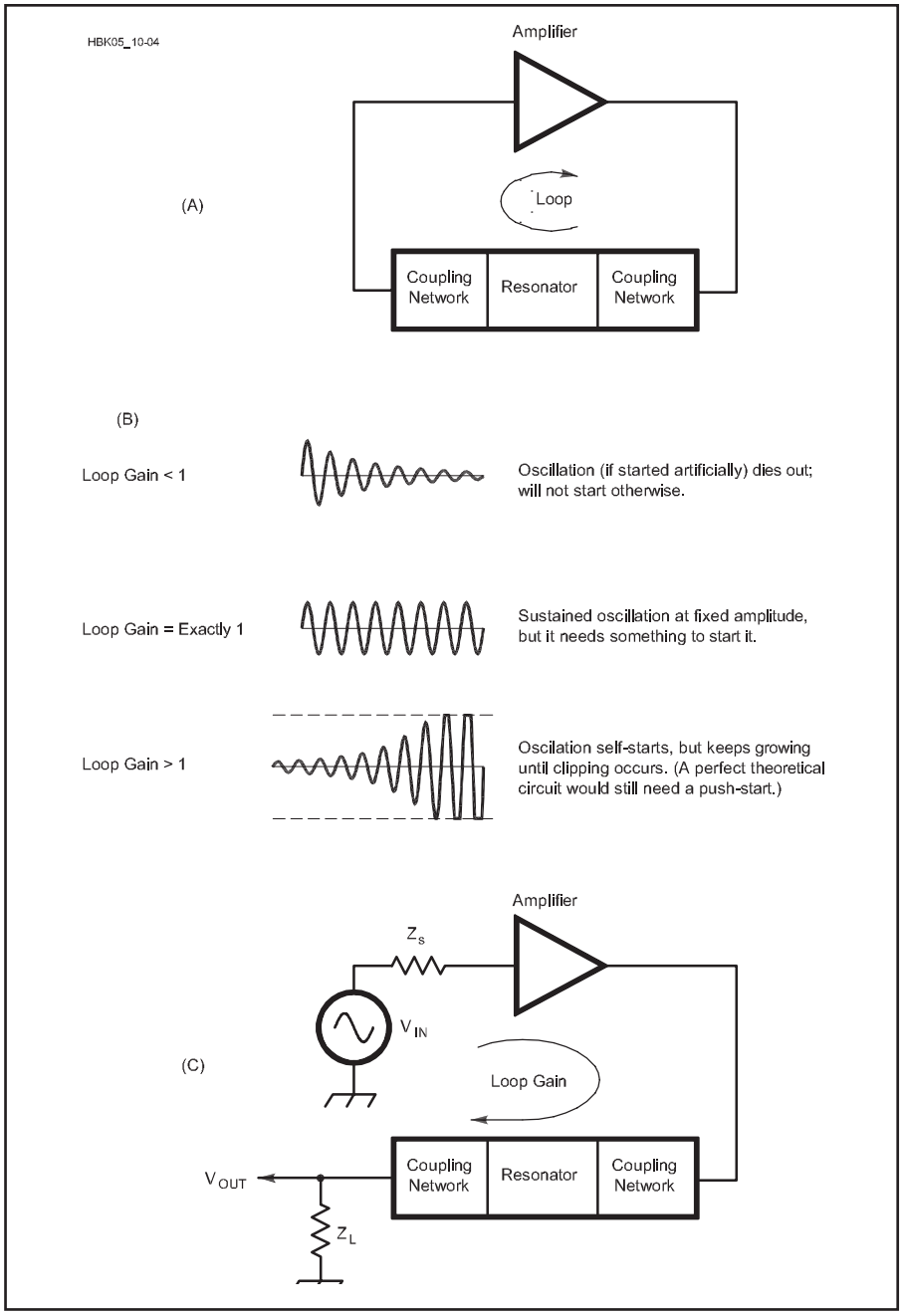


Fig 9.3 — A practical oscillator requires networks to couple power in and out of the resonator (A). At (B), we see the amount of loop gain determines whether the oscillations will die out (loop gain < 1), grow until the waveform is no longer a sine wave (>1), or sustain at a steady amplitude (=1). Breaking the loop, inserting a test signal and measuring the loop's overall gain allows us to determine whether the system can oscillate, sustain oscillation or clip (C).

By adding an amplifier to the tank circuit or *resonator*, we can take a small amount of the energy from the resonator, amplify it, and inject a part of the amplified tank signal back into the resonator. This process is shown in **Fig 9.3A**. Unlike in general amplifier design, here we are not interested in maximizing power transfer. Instead, we want to couple just enough energy into the resonator to overcome its losses, and to take only the minimum amount of energy out of the resonator needed to generate the restoring energy. Thus Fig 9.3A shows coupling networks instead of matching networks. We end up with a loop: The amplifier input comes from the output of the resonator, and the amplifier output goes to the input of the resonator.

The trick to oscillator design is to get the coupling networks and the amplifier gain working together just right. What this means is shown in Fig 9.3B. If we want to get a sine wave output, we need to get the loop gain — gain computed as the signal passes through the combination of amplifier, resonator, and both coupling networks — exactly equal to one, also called *unity*. If the loop gain is even slightly less than one, then not enough energy is supplied to overcome resonator losses and the damping still happens. If the loop gain is greater than one, then the magnitude of the sine wave will grow until the waveform is no longer sinusoidal.

There is more to making an oscillator work than getting the loop gain right. We also need to be sure that the energy from the amplifier output is applied to the resonator having the correct phase alignment with the oscillating signal in the resonator. Taken together these requirements are known as the *Barkhausen criteria*: to achieve oscillation the loop must 1) have a net zero phase shift (or some integer multiple of 360°) and 2) have a loop gain equal to one. Both of these are critically important. If either of these criteria is not met, the circuit will not oscillate.

How do we find out if we are meeting the Barkhausen criteria? We need to break the loop, usually at the input of the amplifier as shown in Fig 9.3C. We apply a signal slightly below the desired oscillation frequency, then sweep the frequency through and slightly past the desired oscillation frequency. During the sweep we monitor both the magnitude and phase response at the output of the resonator output coupling network. If everything is right, then at the desired frequency of oscillation the input and output signals will look exactly the same on an oscilloscope. If that doesn't happen, we have work to do.

Getting the phase response of the loop correct is usually the harder problem. Much of this difficulty comes from the many types of resonators that can be used, including:

- LC tank
- Quartz crystal (and other piezoelectric materials)
- Transmission line (stripline, microstrip, open-wire, coax, and so on)
- Microwave cavities, YIG spheres, dielectric resonators
- Surface-acoustic-wave (SAW) devices

Each of these also can be called a filter. It is true that any filter can also be used as a resonator in an oscillator. The more complicated phase responses of filters makes meeting both of the Barkhausen criteria more challenging, but certainly possible.

The phase response of the resonator is related to its Q (quality factor — see the **Electrical Fundamentals** chapter). If we have a parallel LC tank, then at frequencies well below resonance the tank looks inductive ($X_L << X_C$) and the current lags the voltage. At frequencies well above resonance the tank looks capacitive ($X_C << X_L$) so the current leads the voltage. In between, the phase shift of the current relative to the voltage depends on the actual frequency. The rapidity of the

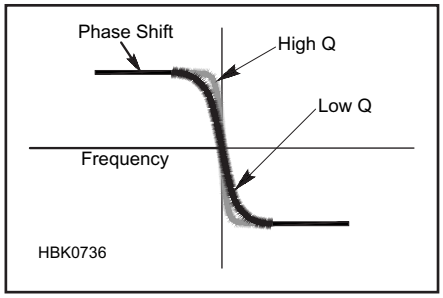


Fig 9.4 — Phase shift through the resonator depends on resonator Q. The higher resonator Q, the more abruptly phase changes through the resonator as frequency changes.

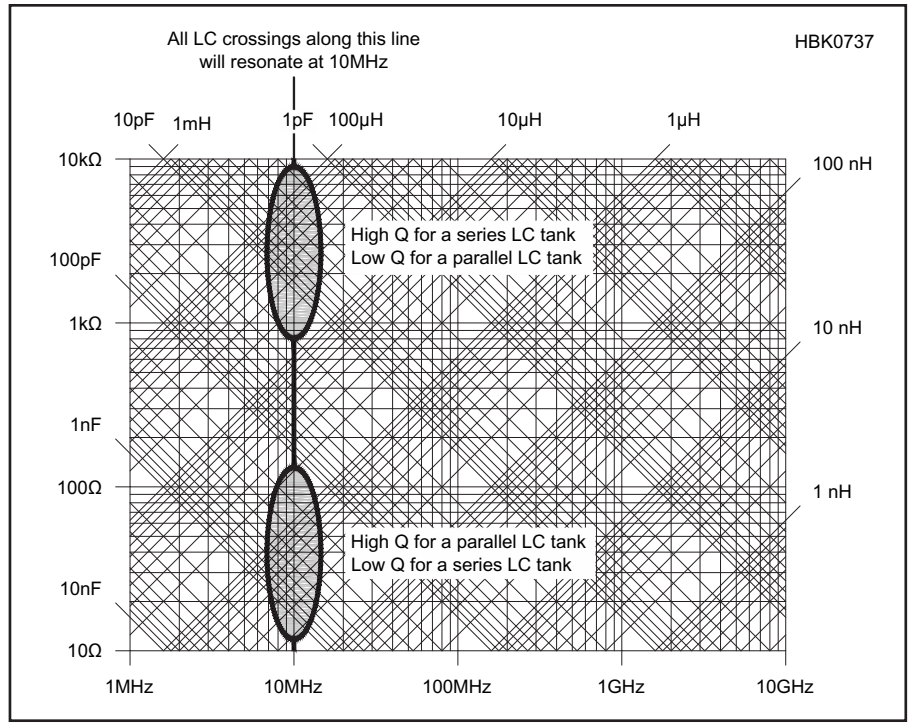


Fig 9.5 — There are an infinite number of combinations of L and C for a given resonant frequency. For a series-LC tank circuit, larger ratios of L to C result in higher values of Q and vice versa for parallel-LC tank circuits.

phase shift with changing frequency is governed by resonator Q: the phase shift happens very rapidly when Q is high. This is shown in **Fig 9.4**. When the resonator Q is low then the phase changes much more slowly at different frequencies.

If we have a series resonator then the phase change profile is reversed (capacitive to inductive) but otherwise the shape is the same. There are an infinite number of combinations of L and C values that provide the same resonant frequency. If we are interested in high Q, for a series tank we want to select large inductor values and small capacitor values. For a high-Q parallel tank we want the opposite — large capacitor values and small inductor values. **Fig 9.5**, a modified version of the reactance vs frequency chart in the **Electrical Fundamentals** chapter, shows these regions for a resonant frequency of 10 MHz.

9.1.3 Oscillator Start-Up

Looking at Fig 9.3B we see that the oscillation will build up in magnitude only when the loop gain is greater than unity. Thus this is an important additional criterion for oscillator design. The loop gain must be slightly greater than unity for it to start oscillating. Otherwise we have the undesired condition in which there is no signal in the resonator, so we sample nothing from it and put nothing back into it.

Still we need one more thing — noise. Some kind of signal needs to be injected into the resonator for the oscillation to start building up. We are fortunate that all amplifiers have output noise when power is applied, even if there is no input signal. It is this noise that allows any oscillator to start. Amplifier noise initiates a resonant signal in the tank, and if loop gain is slightly greater than unity, more signal is fed back into the resonator than the resonator loses. The output signal builds up until something stops it.

Here we take advantage of an amplifier characteristic where gain is reduced as the output reaches some predefined value. This is referred to as *compression*: when the output signal gets large enough, the amplifier gain is reduced a little bit. When compression balances steady output amplitude with a loop gain of exactly unity, the oscillator has reached steady state operation and we are ready to go!

Why don't we have noise at the oscillator output instead of a sine wave? Because of the filtering action of the resonator, the filtered noise waveform appears mostly sinusoidal. The narrower the bandwidth of the resonator (the higher its Q), the more sinusoidal the waveform, but it actually consists of very well-filtered noise. It is impossible to get only a pure sine wave. Noise is inevitable, and tremendous efforts are spent in reducing this noise. This is discussed in section 9.2.

9.1.4 Negative Resistance Oscillators

It is possible to build an oscillator without using an amplifier. Recognizing that losses in the tank are represented by a resistor, if the loss resistor is canceled with a negative resistance then there will be no operating losses and the tank oscillation will continue without damping. This structure is shown in **Fig 9.6**.

Negative resistance devices definitely exist. Anything that draws lower current as the applied voltage increases exhibits negative resistance. Gunn diodes are classic examples and are widely used in microwave oscillators. Lower frequency devices include tunnel diodes and lambda diodes. With this type of oscillator, the equivalent of having the loop gain slightly greater than unity at startup is for the negative resistance to be slightly more negative than the tank loss resistance is positive.

Amplitude limiting for this type of oscillator occurs when the signal amplitude increases enough to drive the negative resistance device to a less-negative value. All negative resistance devices listed here only exhibit their negative resistance over a finite range, so any signal approaching or exceeding this range will effectively reduce the negative resistance, as desired.

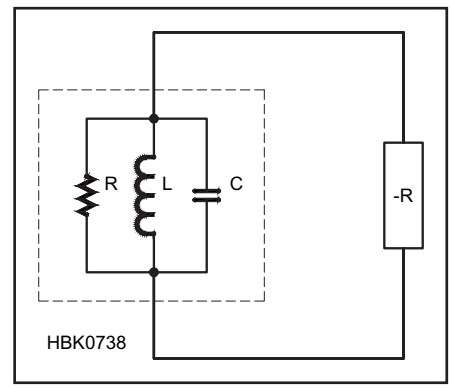


Fig 9.6 — The amplifier in an oscillator can be replaced by a device with negative resistance, such as a Gunn diode, and oscillation will still result.

9.2 Phase Noise

No oscillator output signal is perfect. Viewing an oscillator as a filtered-noise generator, as in the previous sections, is relatively modern. The older approach is to think of an oscillator making a pure sine wave with an added, unwanted noise signal. These are just different ways of visualizing the same thing. They are equally valid views which are used interchangeably, depending on which best makes some point clear.

For example, it is instructive to use the pure-sine-wave-plus-noise view to see relationships between AM noise and PM (phase) noise processes, shown in **Fig 9.7**. Adding Gaussian noise to a pure sine wave is usefully modeled using phasors as shown in Fig 9.7B. This generates both AM due to noise, and PM due to noise as shown in Fig 9.7C. Passing this signal through a limiter process, such as an amplifier in compression or through a switching mixer, leaves only the phase noise depicted in Fig 9.7D. Because it is so easy to remove AM noise but not phase noise, there is essentially no discussion about oscillator AM noise. Phase noise is the critical problem.

Phase modulation and frequency modulation are closely related. (See the **Modulation** chapter for a detailed description of each.) Phase is the integral of frequency, so phase modulation resembles frequency modulation, where the frequency deviation increases with increasing modulating frequency. Thus, there is no need to talk of "frequency noise" because phase noise already covers it.

A thorough analysis of oscillator phase noise is beyond the scope of this section. However, a detailed, state-of-the-art treatment by Dr Ulrich Rohde, N1UL, of free-running oscillators using nonlinear harmonic-balance techniques is presented as a supplement on the CD-ROM accompanying this book.

Because of the dynamic range required to measure phase noise, it is one of the most difficult measurements in all of electrical engineering. The sidebar "Transmitter Phase-Noise Measurement in the ARRL Lab" illustrates the lengths to which one must go to obtain repeatable, reliable measurements. An additional article on measuring receiver phase noise is included on the *Handbook* CD-ROM.

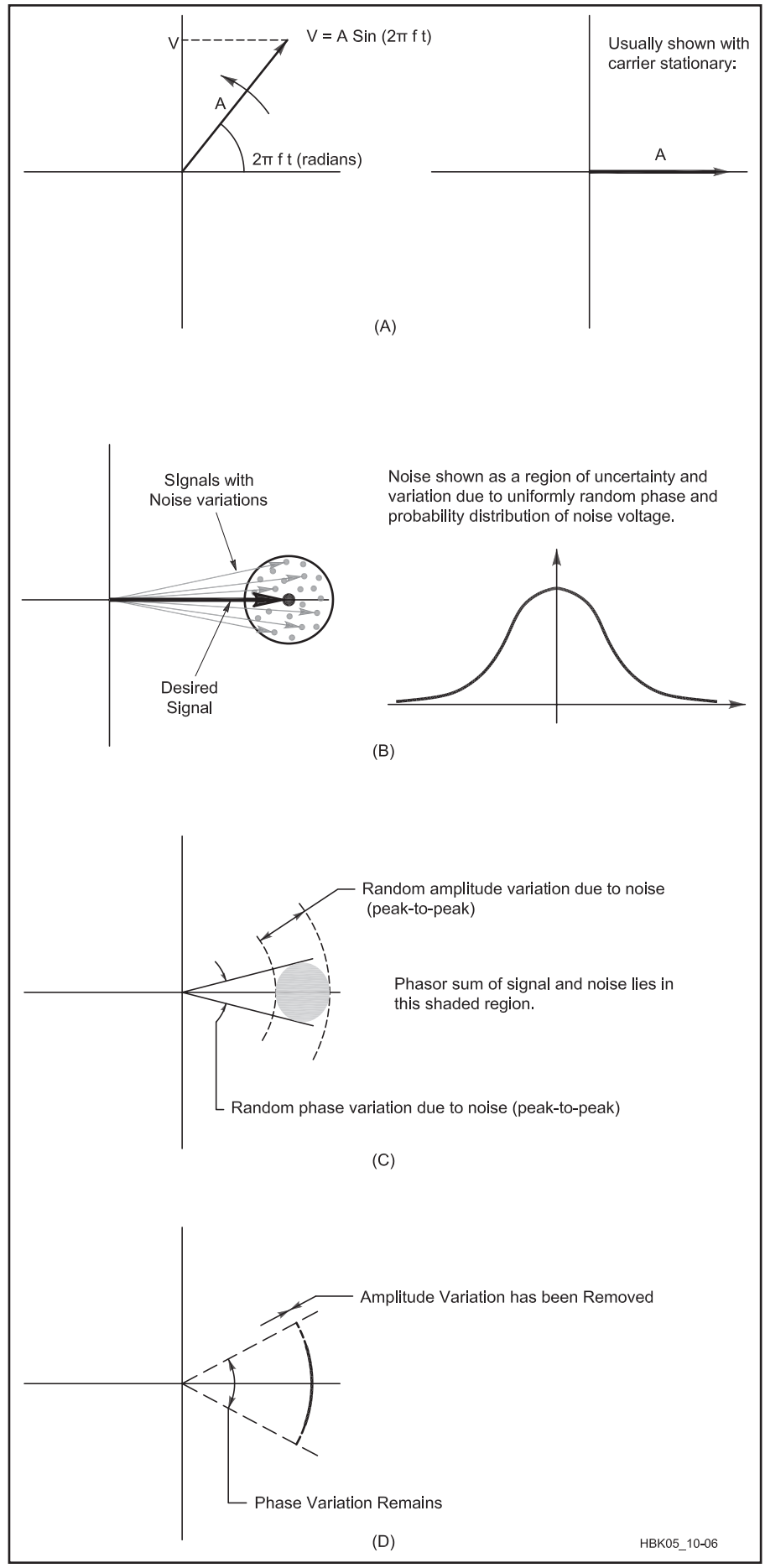


Fig 9.7 — At A, a vector (left) and phasor (right) diagram of an ideal oscillator with no noise. Added noise creates a region of uncertainty in the phasor's length and position (B). AM noise varies the phasor's length; PM noise varies the phasor's relative angular position (C). Limiting a signal that contains both AM and PM noise strips off the AM and leaves the PM (D).

Transmitter Phase-Noise Measurement in the ARRL Lab

Here is a brief description of the technique used in the ARRL Lab to measure transmitter phase noise. The system consists of a phase noise test set with low-noise variable crystal oscillators for reference signals. The test set zero-beats the oscillator to the transmitter signal using phase detectors on both signals. As shown in **Fig 9.A1**, we use an attenuator after the transmitter to bring the signal down to a suitable level for the phase noise test set. The crystal oscillator output is low level, so it does not require attenuation.

The phase noise test set is an automated system run by a PC that steps through the test, setting parameters in the spectrum analyzers and reading the data back from them, in addition to performing system calibration measurements at the start of the test. The computer screen displays the transmitted phase-noise spectrum, which can be printed or saved to a file on the hard drive. To test the baseline phase noise of the system, two identical crystal oscillators are tested against each other. It is quite important to be sure that the phase noise of the reference source is lower than that of the signal under test.

A sample phase-noise plot for an amateur transceiver is shown in **Fig 9.A2**. It was produced with the test setup shown in Fig 9.A1. These plots do not necessarily reflect the phase-noise characteristics of all units of a particular model.

The reference level (the top horizontal line on the scale in the plot) represents 0 dBc/Hz. Because each vertical division represents 20 dB, the plot shows the noise level between 0 dBc/Hz (the top horizontal line) and –160 dBc/Hz (the bottom horizontal line). The horizontal scale is logarithmic, with one decade per division (the first division shows noise from 100 Hz to 1000 Hz offset, whereas the last division shows noise from 100 kHz through 1 MHz offset).

What Do the Phase-Noise Plots Mean?

Although they are useful for comparing different radios, plots can also be used to calculate the amount of interference you may receive from a nearby

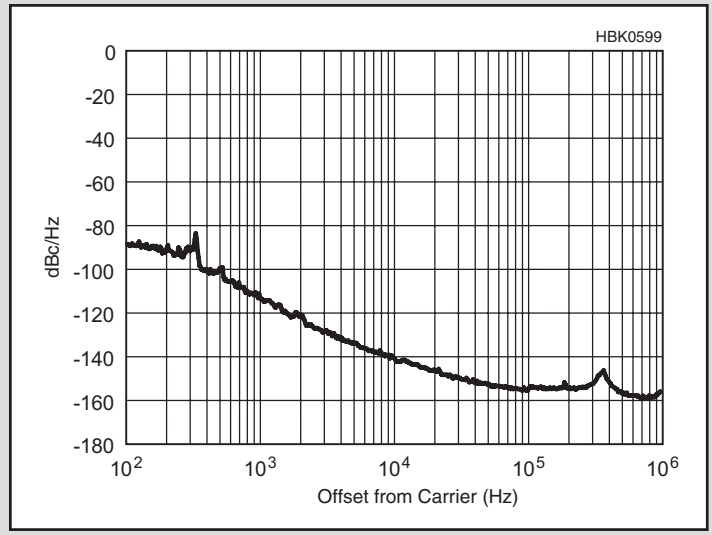


Fig 9.A2 — Sample phase noise plot for an amateur HF transceiver as published in Product Review in *QST*. This is the Elecraft K3.

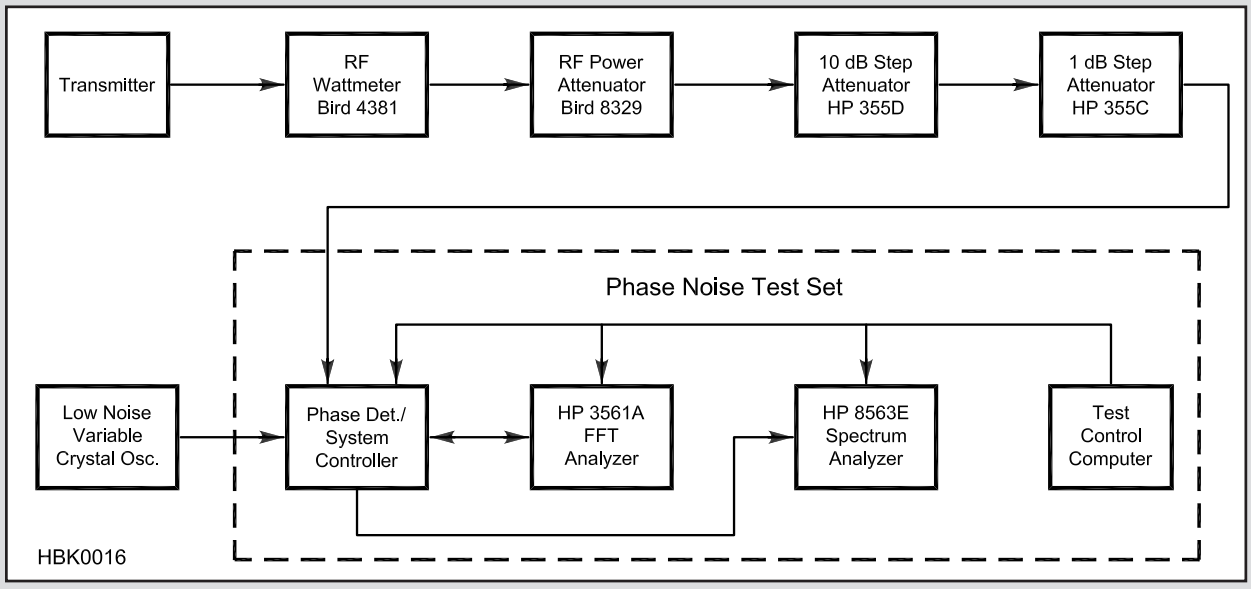


Fig 9.A1 — ARRL Lab phase-noise measurement setup.

transmitter with known phase-noise characteristics. An approximation is given by

$A_{QRM} = NL + 10 \times \log(BW)$

where

A_{QRM} = Interfering signal level, dBc
NL = noise level on the receive frequency, dBc
BW = receiver IF bandwidth, in Hz

For instance, if the noise level is –90 dBc/Hz and you are using a 2.5 kHz SSB filter, the approximate interfering signal will be –56 dBc. In other words, if the transmitted signal is 20 dB over S9, and each S unit is 6 dB, the interfering signal will be as strong as an S3 signal.

The measurements made in the ARRL Lab apply only to transmitted signals. It is reasonable to assume that the phase-noise characteristics of most transceivers are similar on transmit and receive because the same oscillators are generally used in local-oscillator (LO) chain.

In some cases, the receiver may have better phase noise characteristics than the transmitter. Why the possible difference? The most obvious reason is that circuits often perform less than optimally in strong RF fields, as anyone who has experienced RFI problems can tell you. A less obvious reason results from the way that many high-dynamic-range receivers work. To get good dynamic range, a sharp crystal filter called a *roofing filter* is often placed immediately after the first mixer in the receive line. This filter removes all but a small slice of spectrum for further signal processing. If the desired filtered signal is a product of mixing an incoming signal with a noisy oscillator, signals far away from the desired one can end up in this slice. Once this slice of spectrum is obtained, however, unwanted signals cannot be reintroduced, no matter how noisy the oscillators used in further signal processing. As a result, some oscillators in receivers don't affect phase noise.

The difference between this situation and that in transmitters is that crystal filters are seldom used for reduction of phase noise in transmitting because of the high cost involved. Equipment designers have enough trouble getting smooth, click-free break-in operation in transceivers without having to worry about switching crystal filters in and out of circuits at 40 WPM keying speeds! — *Zack Lau, W1VT, and Michael Tracy, KC1SX*

9.2.1 Effects of Phase Noise

Phase noise becomes a problem when it is more noticeable than other limitations. It degrades all signals, but whether it is important or not depends on the application. For voice signals it sounds like background "hiss" in headphones or speakers. It also limits the dynamic range of receivers with closely separated signals, or receiving signals with widely different input powers.

Phase noise became a significant problem for amateurs when the use of frequency synthesizers supplanted conventional LC VFOs in amateur equipment. For reasons discussed in the Synthesizers section of this chapter, it is a major task to develop a synthesizer that tunes in steps fine enough for use with SSB and CW operation while competing with the phase-noise performance of a reasonable-quality LC VFO. Many synthesizers fall far short of this target. Along with the problems with frequency synthesizers, phase noise always gets worse at higher frequencies. The trend toward general-coverage, up-converting architectures has required local oscillators to operate at higher and higher frequencies, making phase noise even more of a problem. Examples of phase noise and the problems it causes are detailed in the next two sections.

9.2.2 Reciprocal Mixing

All mixers are symmetrical, meaning that the output IF signal depends on the characteristics of both input signals: the local oscillator (LO) and the desired signal. A change to either signal shows up at the IF, where there is no way of knowing if the signal characteristics seen are from the input signal itself, or from the LO. We usually assume that the LO is very pure so only input signal modulations show up at the IF.

When there is phase noise on the LO signal, the situation changes. Noise on the LO transfers to *all* input signals at the mixer output as if it was originally present on each input signal and the LO was perfectly clean — the IF circuits can't tell the difference. This process is called *reciprocal mixing*, where noise on the LO appears as noise on the desired output signal. This is a serious limitation on a receiver's weak-signal ability.

How reciprocal mixing of LO phase noise can limit receiver dynamic range is shown in **Fig 9.8**. One possible scenario of band activity is shown as the set of input signals in Fig 9.8A. Fig 9.8B shows the phase noise profile for the LO of this receiver. Reciprocal mixing is illustrated in Fig 9.8C, showing that the LO phase noise is added to each of the signals in the band in proportion to its input power. The

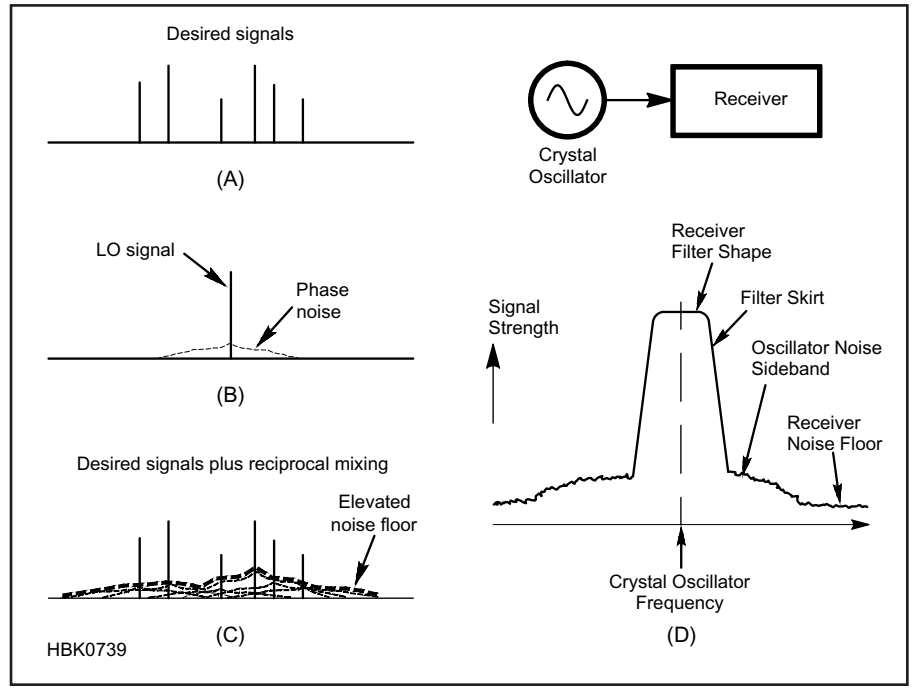


Fig 9.8 — A typical set of input signals is shown at A and an LO signal with phase noise at B. When the LO signal at B is mixed with the input signals at A, the result is a set of mixing products each having phase noise added, raising the noise floor across the band as shown at C. Phase noise in your receiver can be heard by tuning to a strong, clean crystal-oscillator signal as shown in D.

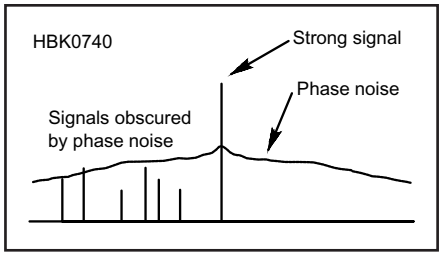


Fig 9.9 — A strong received signal can also cause such severe reciprocal mixing that desired signals are completely obscured by noise. If the signal is transmitted with phase noise from the transmitter LO, the effect is the same as noise covers the desired signals, sometimes across a very wide range of frequencies.

total noise seen by the receiver demodulator is the sum of all transferred phase noise profiles at the received frequency. This raises the apparent noise floor of the receiver.

Another receiver problem due to LO phase noise occurs if a very large signal appears in the receiver passband but at a frequency well removed from the desired signal. One example of this is shown in **Fig 9.9**. If the LO phase noise is excessive, then reciprocal mixing with this large signal can completely block the ability to demodulate the desired signals. Indeed, it is possible to make a wide swath of spectrum relatively useless. (If the strong signal is strong enough, it can result in *blocking* by causing a reduction of receiver gain. This is described in the **Receivers** and the **Test Equipment and Measurements** chapters.)

Reciprocal mixing in a receiver does not affect the operating ability of other stations. The solution is to reduce the phase noise on the receiver's LO.

9.2.3 A Phase Noise Demonstration

Healthy curiosity demands some form of demonstration so the scale of a problem can be judged "by ear" before measurements are attempted. We need to be able to measure the noise of an oscillator alone (to aid in the development of quieter ones) and we also need to be able to measure the phase noise of the oscillators in a receiver (a transmitter can be treated as an oscillator). Conveniently, a receiver contains most of the functions needed to demonstrate its own phase noise.

Because reciprocal mixing adds the LO's sidebands to clean incoming signals, in the same proportion to the incoming carrier as they exist with respect to the LO carrier, all we need do is to apply a strong, clean signal wherever we want within the receiver's tuning range. This signal's generator must have lower phase noise than the radio being evaluated. A general-purpose signal generator is unlikely to be good enough; a crystal oscillator is needed.

It's appropriate to set the oscillator's signal level into the receiver to about that of a strong broadcast carrier, say S9 + 40 dB. Set the receiver's mode to SSB or CW and tune around the test signal, looking for an increasing noise floor (higher hiss level) as you tune closer toward the signal, as shown in Fig 9.8D. Switching in a narrow CW filter allows you to hear noise closer to the carrier than is possible with an SSB filter. This is also the technique used to measure a receiver's effective selectivity, and some equipment reviewers kindly publish their plots in this format. *QST* reviews, done by the ARRL Lab, often include the results of specific phase-noise measurements.

9.2.4 Transmitted Phase Noise

Phase noise on an LO used to generate a transmitted signal will also be amplified and transmitted along with the desired output signal. This obscures reception by raising the noise floor even for receivers with low phase noise because they also receive the noise from the transmitter. In this case, the phase noise is generated externally to the receiver and must be removed at the transmitter.

If the transmitter is operating linearly, the strength of the transmitted noise is of the same proportion to transmitter output power as the phase noise is to the oscillator signal power. The noise may even extend well beyond the band in which the desired signal is transmitted unless the signal passes through narrow-band filtering that limits its bandwidth.

This transmitted noise is wasted power that is not useful for communication and unfortunately makes for a noisier band. If you are working a weak station and a nearby transmitter with a noisy oscillator comes on the air with a high power signal on a different frequency, it is possible that the output noise from this off-frequency transmitter may completely block your ability to continue working that weak station.

In bad cases, reception of nearby stations can be blocked over many tens of kilohertz above and below the frequency of the offending station. This is seen in **Fig 9.9**, where the offending signal and its associated noise are from a nearby transmitter. Frequencies close to that of the nearby transmitter are suddenly useless.

Transmitted phase noise can present serious problems for multi-station operation such as at Field Day or during emergency communications where several transmitters and receivers are in close proximity. This is a particular problem with transceivers that use early PLL-synthesized VFOs. If you are planning such an operation, be sure the level of transmitted phase noise is acceptable for the transceivers you plan on using.

At your receiver there is nothing you can do about transmitted phase noise. When there is noise power present at the same frequency as a weak (far) signal you are receiving, your receiver cannot separate them. The only solution is for the problem station to use a transmitter with a "cleaner" LO (less phase noise). This is a more serious problem than reciprocal mixing since this transmitted noise affects the ability of many other stations to use that band.

9.3 Oscillator Circuits and Construction

In this section we introduce some important oscillator circuits and provide well-tested guidelines on how to successfully build one. The following section presents a design example.

There are thousands of oscillator circuits, but just a few principal designs. One of the principal oscillator circuits is shown in **Fig 9.10**. An LC tank circuit is shown in Fig 9.10A. The usual single capacitance is replaced with two series capacitors having the same equivalent capacitance, C_{EQUIV}. The two capacitors act as an ac voltage divider, so that the voltage V1 at the midpoint is less than the total ac voltage of the tank, V_{TANK}.

What happens when we try to force V1 to be the same as V_{TANK} by adding an amplifier with unity voltage gain as shown in Fig 9.10B? The voltage division action of the capacitive divider does not change. If V1 is forced to be equal to V_{TANK} by the amplifier, then V_{TANK} will become greater than before. But then V1 will take on the new value of V_{TANK} and so forth. This is positive feedback and we have created an oscillator. Connecting an amplifier with low voltage gain to a split tank capacitance leads to the *Colpitts* group of oscillator designs.

It is certainly possible to "split" the inductor instead of the capacitor in a tank circuit and apply the same amplifier trick as before. This is shown in Fig 9.10C and describes the *Hartley* group of oscillators.

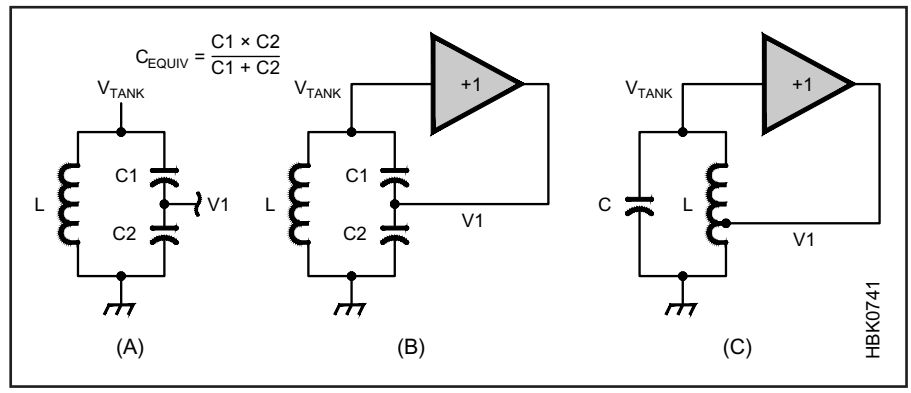


Fig 9.10 — The capacitor in an LC tank circuit (A) can be split into two capacitors with the same equivalent capacitance, C_{EQUIV}, so that the resonant frequency of the tank circuit is unchanged. (B) shows a unity-gain amplifier connected so that it forces V1 = V_{TANK}, creating positive feedback and a Colpitts oscillator results. (C) shows the same technique applied to the tank circuit inductor, creating a Hartley oscillator.

9.3.1 LC VFO Circuits

The LC oscillators used in radio equipment are usually designed to be variable frequency oscillators (VFOs). Tuning is achieved by either varying part of the capacitance of the resonator or, less commonly, by using a movable magnetic core to vary the inductance. Since the early days of radio, there has been a huge quest for the ideal, low-drift VFO. Amateurs and professionals have made immense efforts in this pursuit. A brief search of the literature reveals a large number of VFO designs, many accompanied by claims of high stability. The quest for stability has been solved by the development of low-cost frequency synthesizers, which give crystal-controlled stability. Synthesizers are generally noisier than a good VFO, so the VFO still has much to offer in terms of signal cleanliness, cost, and power consumption, making it attractive for homebrew construction. No single VFO circuit has any overwhelming advantage over any other — component quality, mechanical design and the care taken in assembly are much more important.

Fig 9.11 shows three popular oscillator circuits stripped of any non-essential components so they can be more easily compared. The original Colpitts circuit (Fig 9.11A) is now often referred to as the parallel-tuned Colpitts because its series-tuned derivative (Fig 9.11B) has become the most common. All three of these circuits use an amplifier with a voltage gain less than unity, but large current gain. The N-channel JFET source follower shown appears to be the most popular current choice.

PARALLEL-TUNED COLPITTS VFO

In the parallel-tuned Colpitts, C3 and C4 are large values, perhaps 10 times larger than typical values chosen for C1 and C2 to resonate L at the desired frequency. This means only a small fraction of the total tank voltage is applied to the FET gate, and the FET can be considered to be only lightly coupled into the tank. Equally important, the values of C3 and C4 must be much larger than the FET device internal capacitances to provide good stability for the output frequency. This keeps small variations in the FET capacitances from having a significant effect on oscillator operation.

The FET is driven by the sum of the voltages across C3 and C4, while it drives the voltage across C4 alone. This means that the tank operates as a resonant, voltage-step-up transformer compensating for the less-than-unity-voltage-gain amplifier. The resonant circuit consists of L, C1, C2, C3 and C4. The resonant frequency can be calculated by using the standard formulas for capacitors in series and parallel to find the resultant capacitance effectively connected across the inductor, L, and then use the standard formula for LC resonance:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (9.1)$$

where

f = frequency in hertz
L = total inductance in henries
C = total capacitance in farads.

Equation 9.1 holds for all cases. Its accuracy is dependent on the designer's ability to account for all of the contributions to tank inductance and capacitance. There are several rules of thumb that help a VFO designer identify the various "stray" contributions to tank inductance and capacitance:

1. Wherever there is voltage, stray capacitance must be considered.
2. Wherever there is current, stray mutual inductance must be considered.
3. All currents form loops, creating inductance.

These "rules" will help point out where to look for contributions to inductance and capacitance. At frequencies below 10 MHz the actual components you see and touch tend to be all you need to consider. As the oscillator frequency increases, consideration of stray capacitance and stray inductance — reactance effects that are not associated directly with a visible component — becomes increasingly important. If the oscillator frequency is noticeably lower than what you predict from using Eq 9.1, it is almost certain that there are important stray reactances that you need to account for.

Getting back to the circuit of Fig 9.11A, for a wide tuning range C2 must be kept small to reduce the swamping effect of C3 and C4 on the variable capacitor C1. (For more information on component selection, the chapters on oscillators in *Experimental Methods for RF Design* and *Introduction to Radio Frequency Design* listed in the References provide excellent material.) "Swamping" refers to a much larger value component reducing the effect of a small component connected to it.

A parallel-tuned Colpitts oscillator is the subject of the detailed paper "A Design Example for an Oscillator for Best Phase Noise and Good Output Power" by Dr Ulrich

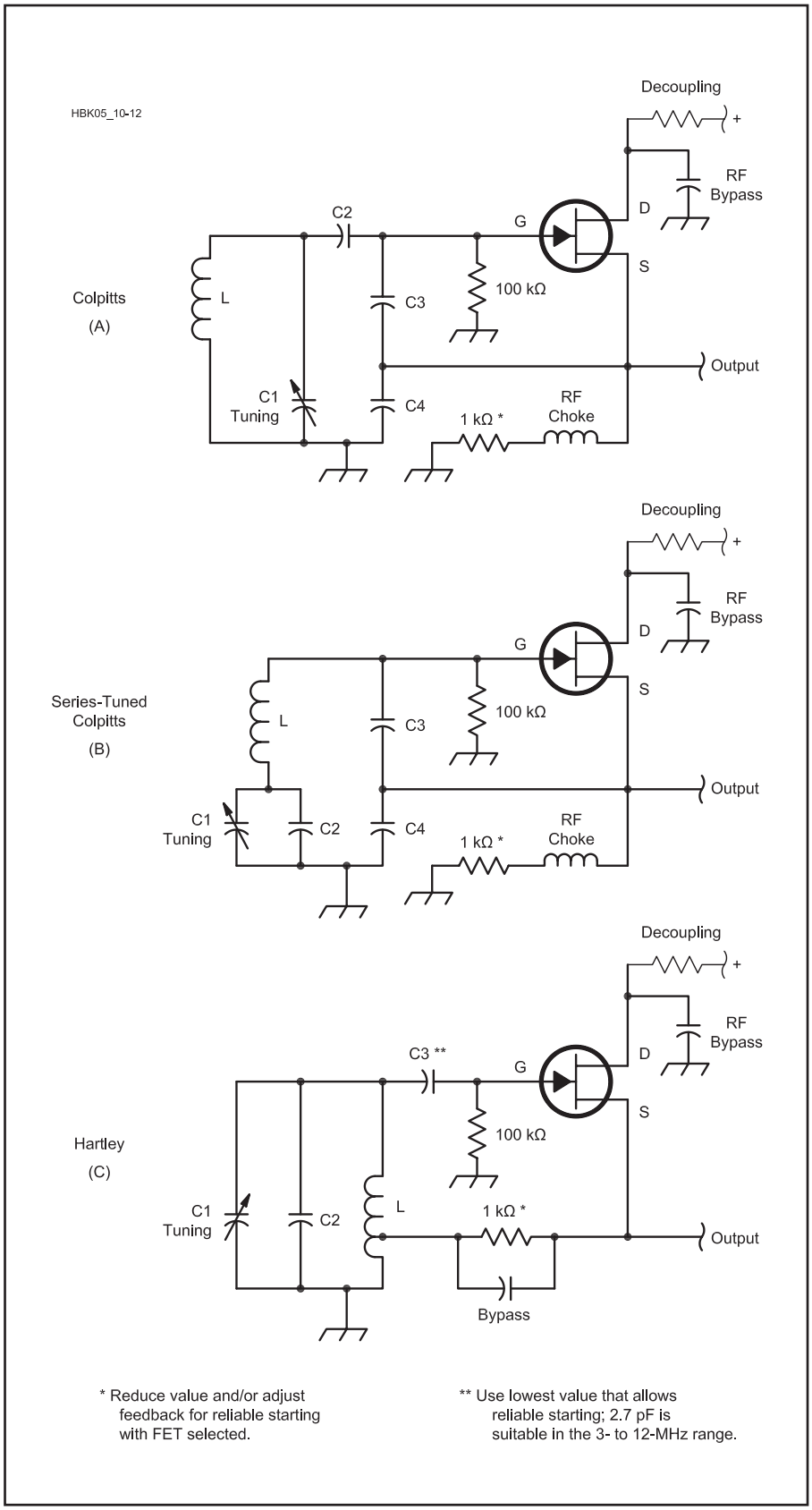


Fig 9.11 — The Colpitts (A), series-tuned Colpitts (B) and Hartley (C) oscillator circuits. Rules of thumb: C3 and C4 at A and B should be equal and valued such that their X_C = 45 Ω at the operating frequency; for C2 at A, X_C = 100 Ω. For best stability, use C0G or NP0 units for all capacitors associated with the FETs' gates and sources. Depending on the FET chosen, the 1-kΩ source-bias-resistor value shown may require adjustment for reliable starting.

Rohde, N1UL, available on the CD-ROM accompanying this book. The paper shows the design process by which both noise and power can be optimized in a simple oscillator.

SERIES-TUNED COLPITTS VFO

The series-tuned Colpitts circuit works in much the same way. The difference is that the variable capacitor, C1, is positioned so that it is well-protected from being swamped by the large values of C3 and C4. In fact, small values of C3, C4 would act to limit the tuning range. Fixed capacitance, C2, is often added across C1 to allow the tuning range to be reduced to that required without interfering with C3 and C4, which set the amplifier coupling. The series-tuned Colpitts has a reputation for better stability than the parallel-tuned original. Note how C3 and C4 swamp the capacitances of the amplifier in both versions.

HARTLEY VFO

The Hartley oscillator of Fig 9.11C is similar to the parallel-tuned Colpitts, but the JFET amplifier source is connected to a tap on the tank inductance instead of the tank capacitance. A typical tap placement is 10% to 20% of the total turns up from the cold end of the inductor. (It's usual to refer to the lowest-signal-voltage end of an inductor as "cold" and the other, with the highest signal voltage as "hot".) C2 limits the tuning range as required.

C3 is reduced to the minimum value that allows reliable starting. This is necessary because the Hartley's lack of the Colpitts' capacitive divider would otherwise couple the FET's internal capacitances to the tank more strongly than in the Colpitts, potentially affecting the circuit's frequency stability.

VFO DESIGN NOTES

Generally, VFOs can be adapted to work at other frequencies (within the limits of the active device). To do so, compute an adjustment factor: f_{old} / f_{new}. Multiply the value of each frequency determining or feedback L or C by that factor. As frequency increases and amplifier gain drops, it may be required to increase feedback more than indicated by the factor.

In all three circuits, there is a 1 kΩ resistor in series with the source bias circuit. This resistor does a number of desirable things. It spoils (lowers) the Q of the inevitable low-frequency resonance of the choke with the tank tap circuit. It reduces tuning drift due to choke impedance and winding capacitance variations. It also protects against spurious oscillation at undesired frequencies due to internal choke resonances. Less obviously, it acts to stabilize the loop gain of the built-in AGC action of this oscillator. Stable operating conditions act to reduce frequency drift.

Some variations of these circuits may be found with added resistors providing a dc bias to stabilize the system quiescent current. More elaborate still are variations characterized by a constant-current source providing bias. This can be driven from a separate AGC detector system to give very tight level control. The gate-to-ground clamping diode (1N914 or similar) long used by radio amateurs as a means of avoiding gate-source conduction has been shown by Dr Ulrich Rohde, N1UL, to degrade oscillator phase-noise performance, and its use is virtually unknown in professional circles.

Fig 9.12 shows two more VFOs to illustrate the use of different devices. The vacuum-tube triode Hartley shown features permeability tuning, which has no sliding contact like that of a capacitor's rotor and can be made reasonably linear by artfully spacing the coil turns. The slow-motion drive can be done with a screw thread. The disadvantage is that special care is needed to avoid backlash and eccentric rotation of the core. If a non-rotating core is used, the slides have to be carefully designed to prevent motion in unwanted directions. The Collins Radio Company made extensive use of tube-based permeability tuners, and a semiconductor version can still be found in a number of Ten-Tec radios.

Vacuum tubes cannot run as cool as competitive semiconductor circuits, so care is needed to keep the tank circuit away from the tube heat. In many amateur and commercial vacuum-tube oscillators, oscillation drives the tube into grid current at the positive peaks, causing rectification and producing a negative grid bias. The oscillator thus runs in Class C, in which the conduction angle reduces as the signal amplitude increases until the amplitude stabilizes. As in the FET circuits of Fig 9.11, better stability and phase-noise performance can be achieved in a vacuum-tube oscillator by moving its operating point out of true Class C — that is, by including a bypassed cathode-bias resistor (the resistance appropriate for Class A operation is a good starting value). Vacuum-tube radios are still maintained in operation and occasionally constructed for enjoyment but the semiconductor long ago achieved dominance in VFOs.

Compared to the more frequently used JFET, bipolar transistors like the one used in Fig 9.12B are relatively uncommon in oscillators because their relatively low input and output impedances are more difficult to couple into a high-Q tank without loading it excessively. Bipolar devices do tend to give better sample-to-sample amplitude uniformity for a given oscillator circuit, because many of the bipolar transistor characteristics are due less to manufacturing than physics. This is not true for JFETs of any given type; JFETs tend to vary more in their characteristics because manufacturing variations directly affect their threshold or pinch-off voltage.

SQUEGGING

The effect called *squegging* (or *squeeging*) can be loosely defined as oscillation on more than one frequency at a time, but may also manifest itself as RF oscillation interrupted at an audio frequency rate, as in a superregenerative detector. One form of squegging occurs when an oscillator is fed from a power supply with high source impedance. The power supply charges up the decoupling capacitor until oscillation starts. The oscillator draws current and pulls down the capacitor voltage until it has starved itself of power and oscillation stops. The oscillator stops drawing current and the decoupling capacitor then recharges until oscillation restarts. The process, the low-frequency cycling of which is a form of relaxation oscillation, repeats indefinitely. The oscillator output can clearly be seen to be pulse modulated with an oscilloscope.

Squegging can be a consequence of poor design in battery-powered radios. As the cells become exhausted, their internal resistance often rises and circuits that they power can begin to misbehave. In audio stages, such misbehavior may manifest itself in the "putt-putt" sound of the slow relaxation oscillation called "motorboating."

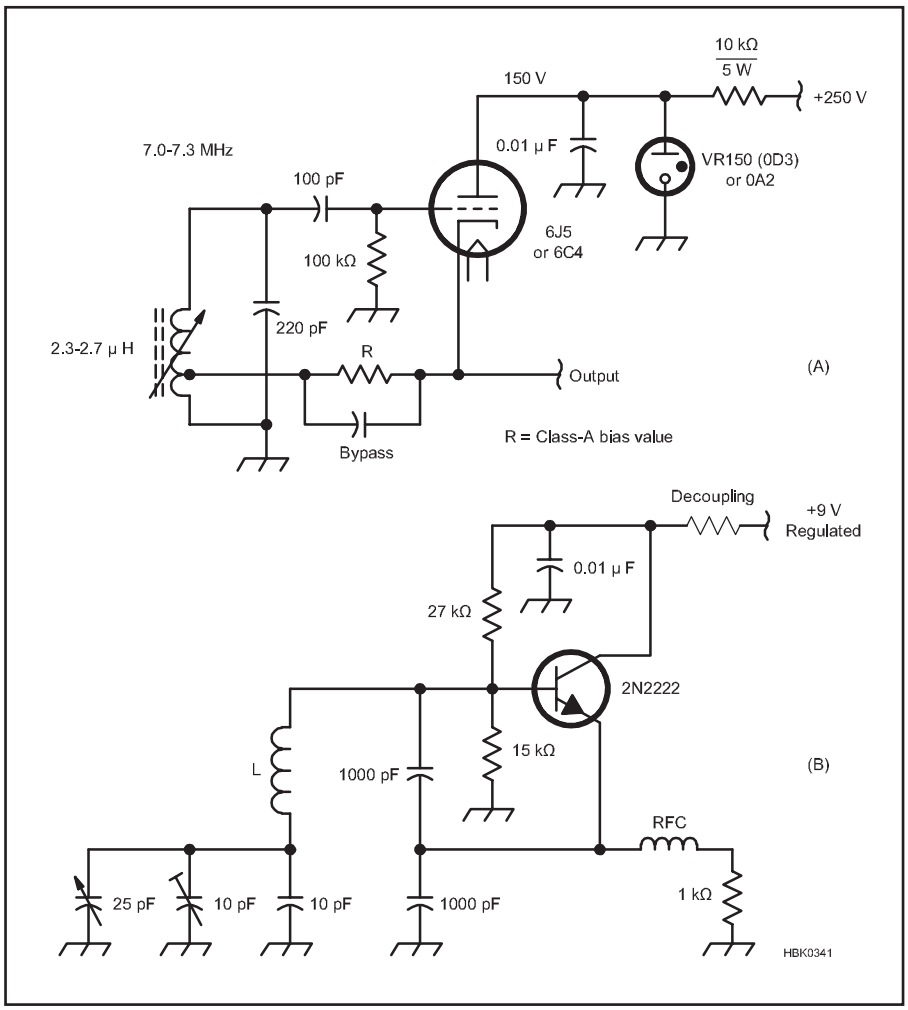


Fig 9.12 — Two additional oscillator examples: at A, a triode-tube Hartley; at B, a bipolar junction transistor in a series-tuned Colpitts.

9.3.2 RC VFO Circuits

Due to the requirements for physical length and area to create inductance, actual inductors cannot be reduced in size to the degree required for use in RF integrated circuits. Resistors and capacitors can be made very small, a fraction of a percent of the size of any inductor. Since size is money in RF integrated circuits, there is a great motivation to eliminate inductors. The problem is that any oscillator without an inductor must use resistors to develop the necessary phase shift, and resistors add loss and noise.

A 180° phase-shift network and an inverting amplifier can be used to make an oscillator with the required 360° of phase shift. A single-stage RC low-pass network cannot

produce more than 90° of phase shift and only approaches that as the signal becomes infinitely attenuated. Two stages can only approach 180° and then also with immense attenuation. A practical RC phase-shift oscillator requires three stages to produce 180° of phase shift without destroying the loop gain. **Fig 9.13A** shows the basic form of the phase-shift oscillator; Fig 9.13B is an example of a phase-shift oscillator commonly used in commercial transceivers as an audio sidetone oscillator.

An RC oscillator can be made extremely small and to tune over a huge bandwidth (1000:1 is common). Unfortunately, Q of the phase-shift circuit is less than one, giving very poor noise performance that's unsuitable even to the least-demanding RF application.

RC oscillators are common though in digital clock generators. A common example uses a Schmitt trigger inverter as shown in Fig 9.13C. (See the discussion of comparators in the **Analog Basics** chapter.) This oscillator alternately charges and discharges the capacitor through the feedback resistor. Oscillation is assured because the inverter has hysteresis: the threshold at which output switches high is lower than the threshold at which the output switches low. The voltage across the capacitor moves between these two switching thresholds. The tuning bandwidth is the ratio of the fixed feedback resistor value to its sum with the potentiometer at full value. This ratio can be as high as 1000:1.

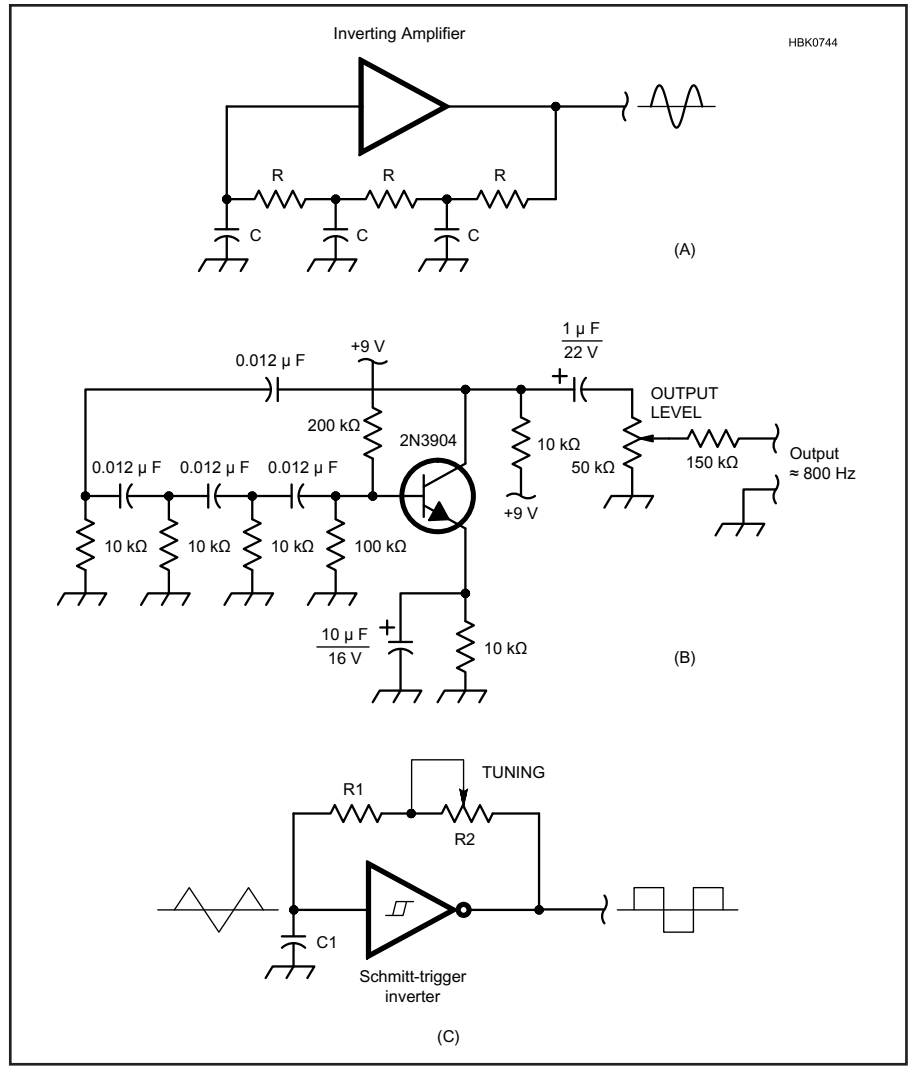


Fig 9.13 — In the basic phase-shift oscillator (A), a chain of RC networks — three or more — provide the feedback and phase shift necessary for oscillation, at the cost of low Q and considerable loop loss. Many commercial transceivers have used a phase-lead oscillator similar to that shown at B as a sidetone generator. Using a single RC circuit with a Schmitt trigger at C produces a simple oscillator with a very wide tuning range and a square wave output.

9.3.3 Three High-Performance HF VFOs

THE N1UL MODIFIED VACKAR VFO

The oscillator circuit of **Fig 9.14A** is contributed by Dr Ulrich Rohde, N1UL. It is a modified Vackar design (see the sidebar) in which a small coupling capacitor (8 pF) and voltage divider capacitor (18 pF) isolate the resonator circuit (10 µH and 50 pF tuning capacitor) from the oscillator transistor.

The oscillator transistor is followed by a buffer stage to isolate the oscillator from the load. Because the coupling between the transistor base and the resonator is fixed and light, stability of the oscillator is high across a wide tuning range from 5.5 to 6.6 MHz. Either the inductor or capacitor may be varied to tune the oscillator, but a variable capacitor is recommended as more practical and gives better performance.

Because of the oscillator transistor's large capacitors from base to ground (220 pF) and collector to ground (680 pF), the various parameters of the oscillator transistor have little practical influence on circuit performance. The widely available 2N3904 performs well for both the oscillator and buffer transistors.

Practical resonator coil and the tuning capacitors will have a positive temperature coefficient. The 8 pF and the 18 pF capacitors should have an N150 temperature coefficient to partially compensate for their drift. After 1 hour, the observed frequency drift for this circuit was less than 10 Hz / hour.

THE K7HFD LOW-NOISE DIFFERENTIAL OSCILLATOR

The other high performance oscillator example, shown in **Fig 9.15**, is designed for low-noise performance by Linley Gumm, K7HFD, and appears on page 126 of the ARRL's *Solid State Design for the Radio Amateur* (out of print, but available used and through libraries). This circuit uses no unusual components and looks simple, yet it is a subtle and sophisticated circuit.

The effects of limiting in reducing AM oscillator noise were covered previously. However, because AM noise sidebands can

The Vackar Oscillator

The original Vackar oscillator is named for Jirí Vackár, who invented the circuit in the late 1940s. The circuit's description — a refinement of the Clapp oscillator — can be found in older editions of the Radio Society of Great Britain's *Radio Communication Handbook*, with some further comments on the oscillator in RSGB's *Amateur Radio Techniques*. The circuit is also described in the Nov 1955 *QST* "Technical Correspondence" column by W9IK. The Vackar circuit optimized the Clapp oscillator for frequency stability: the oscillator transistor is isolated from the resonator, tuning does not affect the feedback coupling, and the transistor's collector output impedance is kept low so that gain is the minimum necessary to sustain oscillation.

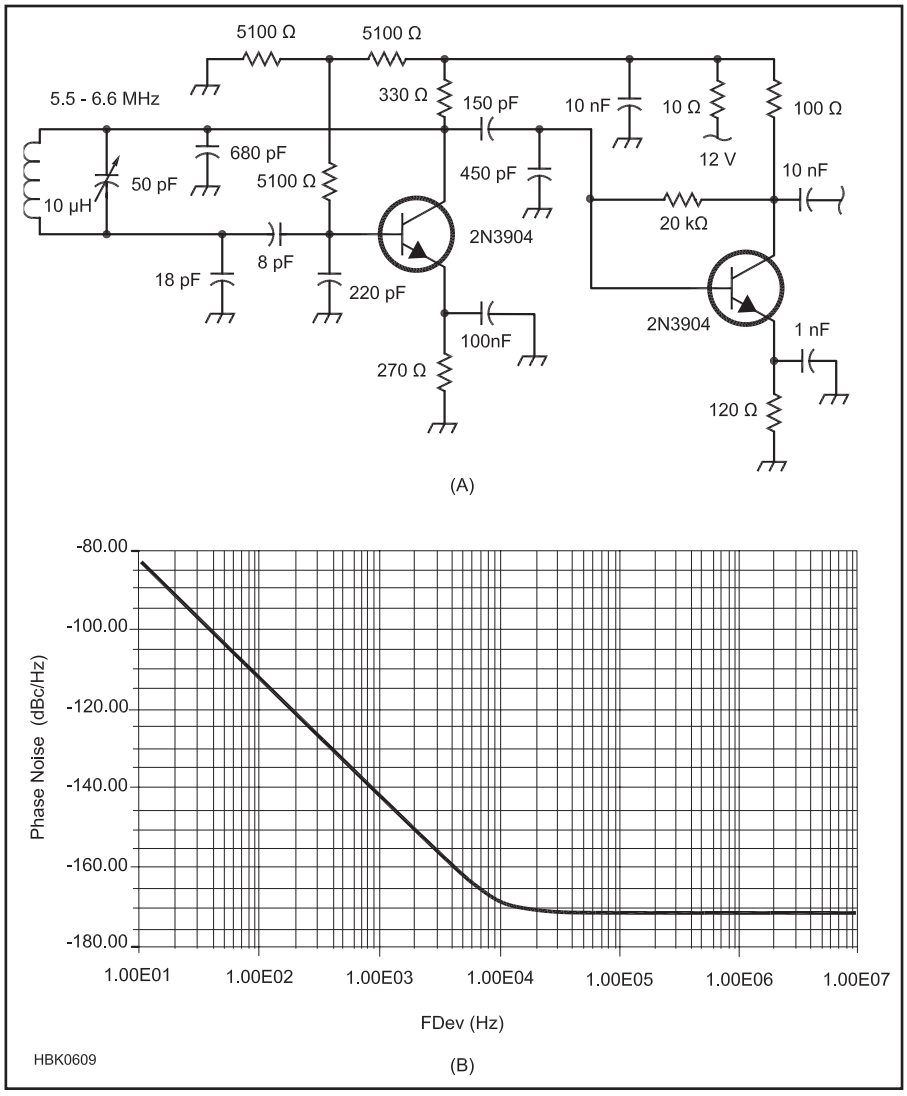


Fig 9.14 — At A, N1UL's Modified Vackar VFO is tuned from 5.5 to 6.6 MHz using the 50 pF capacitor. Tuning may be restricted to narrower ranges by placing a fixed capacitor in parallel with a smaller variable capacitor. The resonant frequency of the oscillator is determined by the 10 µH inductor and 50 pF tuning capacitor. B shows the excellent phase noise performance of the modified Vackar VFO in this *Harmonica* simulation. At 1 kHz from the carrier, noise is –144 dBc.

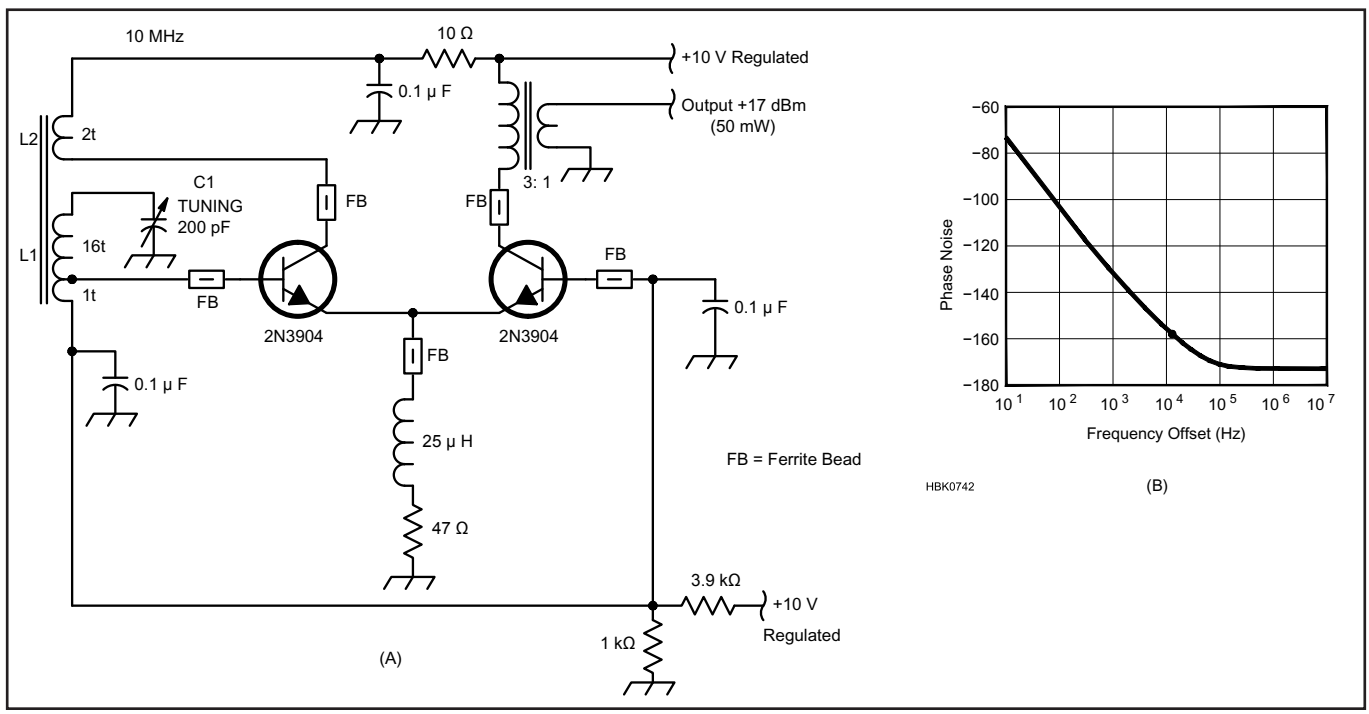


Fig 9.15 — At A, this low-noise oscillator design by K7HFD operates at an unusually high power level to achieve a high C/N (carrier-to-noise) ratio. L1 is 1.2 µH and uses 17 turns of wire on a T-68-6 toroid core. The tap is at 1 turn. Q at 10 MHz is 160. L2 is a 2 turn link over L1. At B, modeling of the differential oscillator by Dr Ulrich Rohde, N1UL, shows its excellent phase-noise performance.

get translated into PM noise sidebands by imperfect limiting, there is an advantage to stripping off the AM as early as possible, in the oscillator itself. An ALC system in the oscillator will counteract and cancel only the AM components within its bandwidth, but an oscillator based on a limiter will do this over a broad bandwidth. K7HFD's oscillator uses a differential pair of bipolar transistors as a limiting amplifier. The dc bias voltage at the bases and the resistor in the common emitter path to ground establishes a controlled dc bias current, here 25 to 27 mA. The ac voltage between the bases switches this current between the two collectors. This applies a rectangular pulse of current into link winding L2, which drives the series-resonant tank L1-C1. The output impedance of the collector is high in both the current-on and current-off states. Along with the small number of turns of the link winding, this presents very high impedance to the tank circuit, which minimizes degradation of the tank Q. The input impedance of this limiter is also quite high and is applied across only a one-turn tap of L1, which similarly minimizes any impact on the tank Q. The input transistor base is driven into conduction only on one peak of the tank waveform. The output transformer has the inverse of the current pulse applied to it, so the output is not a low distortion sine wave, although the output harmonics will not be as extensive as simple theory would suggest because the circuit's high output impedance allows stray capacitances to attenuate high-frequency components. The low-frequency transistors used here also act to reduce the harmonic power.

With an output of +17 dBm, this is a power oscillator, running with nearly 300 mW of dc input power, so appreciable heating is present that can cause temperature-induced drift. The circuit's high-power operation is a deliberate ploy to create a high signal-to-noise ratio by having as high a signal power as possible. This also reduces the problem of the oscillator's broadband noise output. The limitation on the signal level in the tank is the transistors' base-emitter-junction breakdown voltage. The circuit runs with a few volts peak-to-peak across the one-turn tap, so the full tank is running at over 50 V_{P-P}.

Excessive voltage levels for the transistors can easily be generated by this circuit. The single easiest way to damage a bipolar transistor is to reverse bias the base-emitter junction until it avalanches. Most devices are rated to withstand only 5 V applied this way, the current needed to do damage is small, and very little power is needed. If the avalanche current is limited to less than that needed to perform immediate destruction of the transistor, it is likely that there will be some degradation of the device, a reduction in its bandwidth and gain along with an increase in its noise. These changes are irreversible and cumulative. Small, fast signal diodes have breakdown voltages of over 30 V and less capacitance than the transistor bases, so one possible experiment would be to try the effect of adding a fast signal diode in series with the base of each transistor and running the circuit at even higher levels.

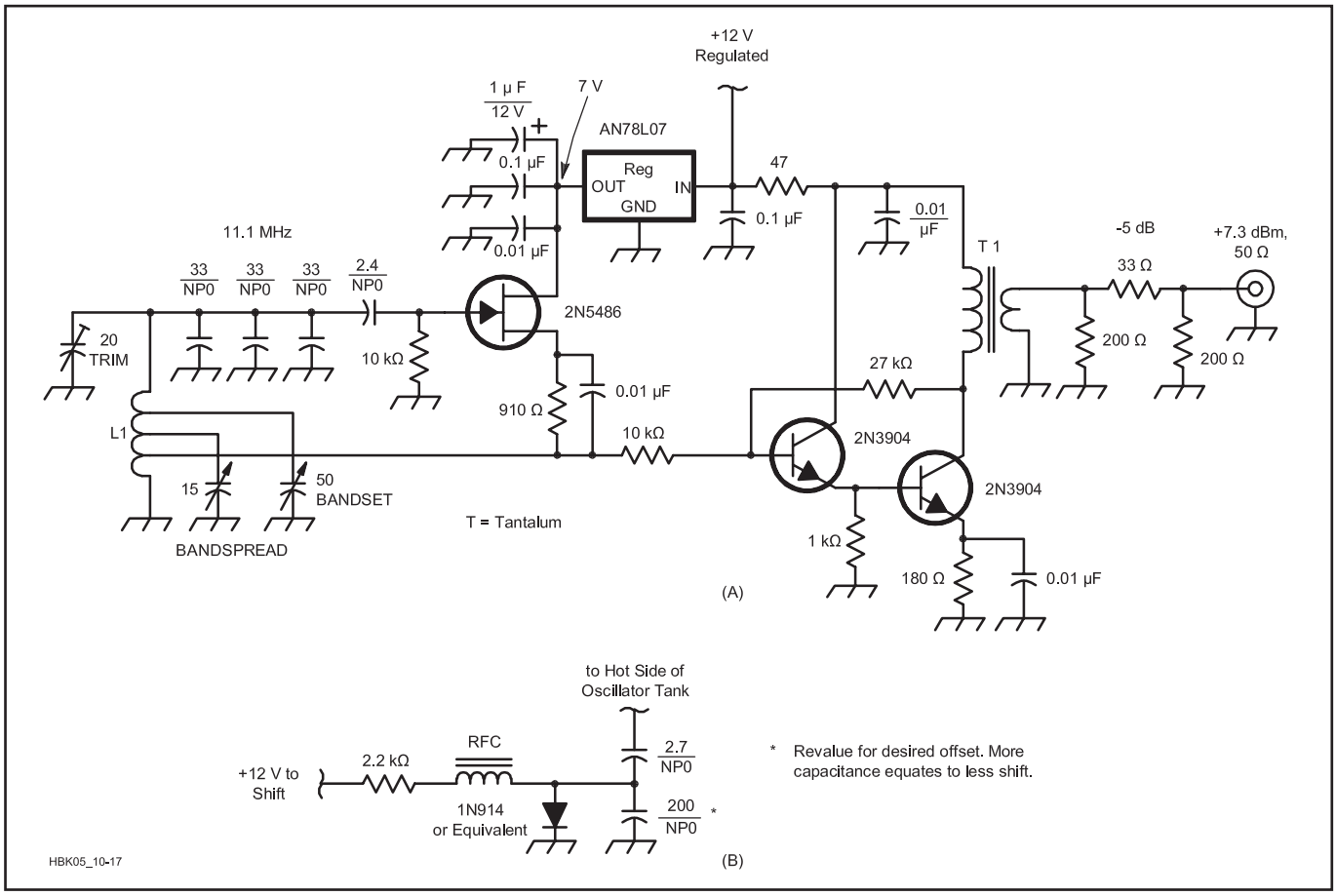


Fig 9.16 — Incorporating ideas from N1UL, KA7EXM, W7ZOI and W7EL, the oscillator at A achieves excellent stability and output at 11.1 MHz without the use of a gate-clamping diode, as well as end-running the shrinking availability of reduction drives through the use of bandset and bandspread capacitors. L1 consists of 10 turns of B & W #3041 Miniductor (#22 tinned wire, ⅝ inch in diameter, 24 turns per inch). The source tap is 2½ turns above ground; the tuning-capacitor taps are positioned as necessary for bandset and bandspread ranges required. T1's primary consists of 15 turns of #28 enameled wire on an FT-37-72 ferrite core; its secondary, 3 turns over the primary. B shows a system for adding fixed TR offset that can be applied to any LC oscillator. The RF choke consists of 20 turns of #26 enameled wire on an FT-37-43 core.

The oscillation amplitude is controlled by the drive current limit. The voltage on L2 must never allow the collector of the transistor driving it to go into saturation, for if this happens the transistor presents very low impedance to L2 and badly loads the tank, wrecking the Q and the noise performance. The circuit can be checked to verify the margin from saturation by probing the hot end of L2 and the emitter with an oscilloscope. Another, less obvious, test is to vary the power-supply voltage and monitor the output power. While the circuit is under current control, there is very little change in output power, but if the supply is low enough to allow saturation, the output power will change significantly with varying supply voltage.

The use of the 2N3904 is interesting, as it is not normally associated with RF oscillators. It is a cheap, plain, general-purpose type more often used at dc or audio frequencies. There is evidence that suggests some transistors that have good noise performance at RF have worse noise performance at low frequencies, and that the low-frequency noise they create can modulate an oscillator, creating noise sidebands. Experiments with low-noise audio transistors may be worthwhile, but many such devices have high junction capacitances.

In the description of this circuit in *Solid State Design for the Radio Amateur*, the results of a phase-noise test made using a spectrum analyzer with a crystal filter as a preselector are given. Ten kilohertz out from the carrier, in a 3 kHz measurement bandwidth, the noise was more than 120 dB below the carrier level. This translates into better than –120 – 10 log (3000), which equals –154.8 dBc/Hz, SSB, consistent with the modeled phase noise performance shown in Fig 9.15B. At this offset, –140 dBc is usually considered to be excellent. This VFO provides state-of-the art performance by today's standards — in a 1977 publication.

A JFET HARTLEY VFO

Fig 9.16 shows an 11.1 MHz version of a VFO and buffer closely patterned after that used in 7 MHz transceiver designs published by Roger Hayward, KA7EXM, and Wes Hayward, W7ZOI ("The Ugly Weekender") and Roy Lewallen, W7EL ("The Optimized QRP Transceiver"). In it, a Hartley oscillator using a 2N5486 JFET drives the two-2N3904 buffer attributed to Lewallen. This version diverges from the originals in that its JFET uses source bias (the bypassed 910 Ω resistor) instead of a gate-clamping diode and is powered from a low-current 7 V regulator IC instead of a Zener diode and dropping resistor. The 5 dB pad sets the buffer's output to a level appropriate for "Level 7" (+7 dBm LO) diode ring mixers.

The circuit shown was originally built with a gate-clamping diode, no source bias and a 3 dB output pad. Adjusting the oscillator bias as shown increased its output by 2 dB without degrading its frequency stability (200 to 300 Hz drift at power up, stability within ±20 Hz thereafter at a constant room temperature).

In recognition that precision mechanical tuning components are hard to obtain, the resonator uses "Bandset" and "Bandspread" variable capacitors. These terms are from the early days of radio: bandset is for coarse-tuning and bandspread is for fine-tuning.

VFO Construction

These suggestions by G3PDM can be applied to any analog VFO circuit. Following these guidelines minimizes the effects of temperature change and mechanical vibration (microphonics) on the VFO.

- Use silvered-mica or other highly-stable capacitors for all fixed-value capacitors in the oscillator circuit. Power-supply decoupling capacitors may be any convenient type, such as ceramic or film.
- Tuning capacitors should be a high-quality component with double ball-bearings and silver-plated surfaces and contacts.
- The resonant circuit inductor should be wound on a ceramic form and solidly mounted.
- All oscillator components should be clean and attached to a solid support to minimize thermal changes and mechanical vibration.
- The enclosure should be solid and isolated from mechanical vibration.
- The power supply should be well-regulated, liberally decoupled and free of noise.
- Keep component leads short and if point-to-point wiring is employed, use heavy wire (#16 to #18 AWG).
- Single-point grounding of the oscillator components is recommended to avoid stray inductance and to minimize noise introduced from other sources. If a PCB is used, include a ground-plane.

9.4 Building an Oscillator

We've covered a lot of ground about how oscillators work, their limitations and a number of interesting circuits, so the inevitable question arises of how to design one. Let's make an embarrassing confession right here: Very few oscillators you see in published circuits or commercial equipment were designed by the equipment's designer. Almost all have been adopted from other sources. While recycling in general is important for the environment, it means in this case that very few professional or amateur designers have ever designed an oscillator from scratch. We all have collections of circuits we've "harvested," and we adjust a few values or change a device type to produce something to suit a new project.

Oscillators aren't designed, they evolve. They seem to have a life of their own. The Clarke & Hess book listed in the references contains one of the few published classical design processes. The ARRL book *Experimental Methods in RF Design* contains extensive material on oscillator circuits that is well worth reading. A demonstration by David Stockton, GM4ZNX, of oscillator design based on a simulation of how oscillators start up by the free *LTSpice* simulation program is available on the CD-ROM.

9.4.1 VFO Components and Construction

TUNING CAPACITORS AND REDUCTION DRIVES

As most commercially made radios now use frequency synthesizers, it has become increasingly difficult to find certain key components needed to construct a good VFO. Slow-motion drives and variable capacitors are available from *QST* advertiser National RF (**www.nationalrf.com**), Dan's Small Parts and Kits (**www.danssmallpartsandkits.net**), and Antique Electronic Supply (**www.tubesandmore.com**). An alternate approach is also available: Scavenge suitable parts from old equipment; use tuning diodes instead of variable capacitors — an approach that, if uncorrected through phase locking, generally degrades stability and phase-noise performance; or use two tuning capacitors, one with a capacitance range ⅕ to ⅒ that of the other, in a bandset/bandspread approach.

Assembling a variable capacitor to a chassis and its reduction drive to a front panel

can result in *backlash* — an annoying tuning effect in which rotating the capacitor shaft deforms the chassis and/or panel rather than tuning the capacitor. One way of minimizing this is to use the reduction drive to support the capacitor, and use the capacitor to support the oscillator circuit board, which is then attached to the chassis.

FIXED CAPACITORS

Traditionally, silver-mica fixed capacitors have been used extensively in oscillators, but their temperature coefficient is not as low as can be achieved with other types, and some silver micas have been known to behave erratically. Polystyrene film has become a proven alternative. One warning is worth noting: polystyrene capacitors exhibit a permanent change in value should they ever be exposed to temperatures much above 70 °C; they do not return to their old value on cooling. Particularly suitable for oscillator construction are the low-temperature-coefficient ceramic capacitors, often described as NP0 or C0G types. (NP0 and C0G are equivalent) These names are actually temperature-coefficient codes. **Fig 9.17** contains graphs showing the behavior of three common temperature coefficients. Some ceramic capacitors are available with deliberate, controlled temperature coefficients so that they can be used to compensate for other causes of frequency drift with temperature. For example, the code N750 denotes a part with a temperature coefficient of –750 parts per million per degree Celsius. These parts are now somewhat difficult to obtain, so other methods are needed. (Values for temperature coefficients and other attributes of capacitors are presented in the **Component Data and References** chapter.)

In a Colpitts circuit, the two large-value capacitors that form the voltage divider for the active device still need careful selection. It is tempting to use any available capacitor of the right value, because the effect of these components on the tank frequency is reduced by the proportions of the capacitance values in the circuit. This reduction is not as great as the difference between the temperature stability of an NP0 ceramic part and some of the low-cost, decoupling-quality X7R-dielectric ceramic capacitors. It's worth using low-temperature coefficient parts even in the seemingly less-critical parts of a VFO circuit — even for the bypass capacitors. Chasing the cause of temperature drift is more challenging than fun. Buy critical components like high-stability capacitors from trustworthy sources.

TUNING CAPACITOR NETWORKS

Often an available variable capacitor has greater capacitance than required for a desired frequency range. While plates can sometimes be removed, a better solution embeds the variable capacitor in a network of fixed capacitors. The evolution of this network is shown in the middle section of **Fig 9.18**. The variable capacitor, C_V, and C_2 are paralleled to form the equivalent C_{2V}. This is then placed in series with C_1 for the equivalent C_{12V}. This

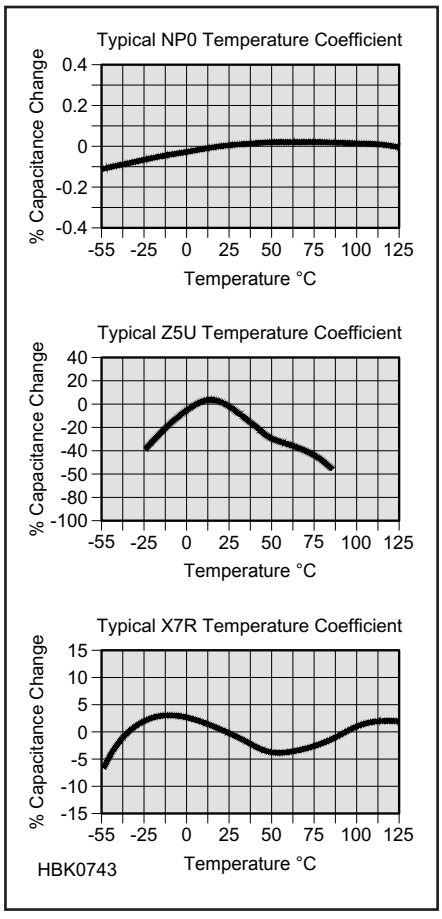


Fig 9.17 — EIA capacitor temperature coefficients specify change in capacitance with temperature. See the Component Data and References chapter for a complete table of temperature coefficient identifiers and characteristics.

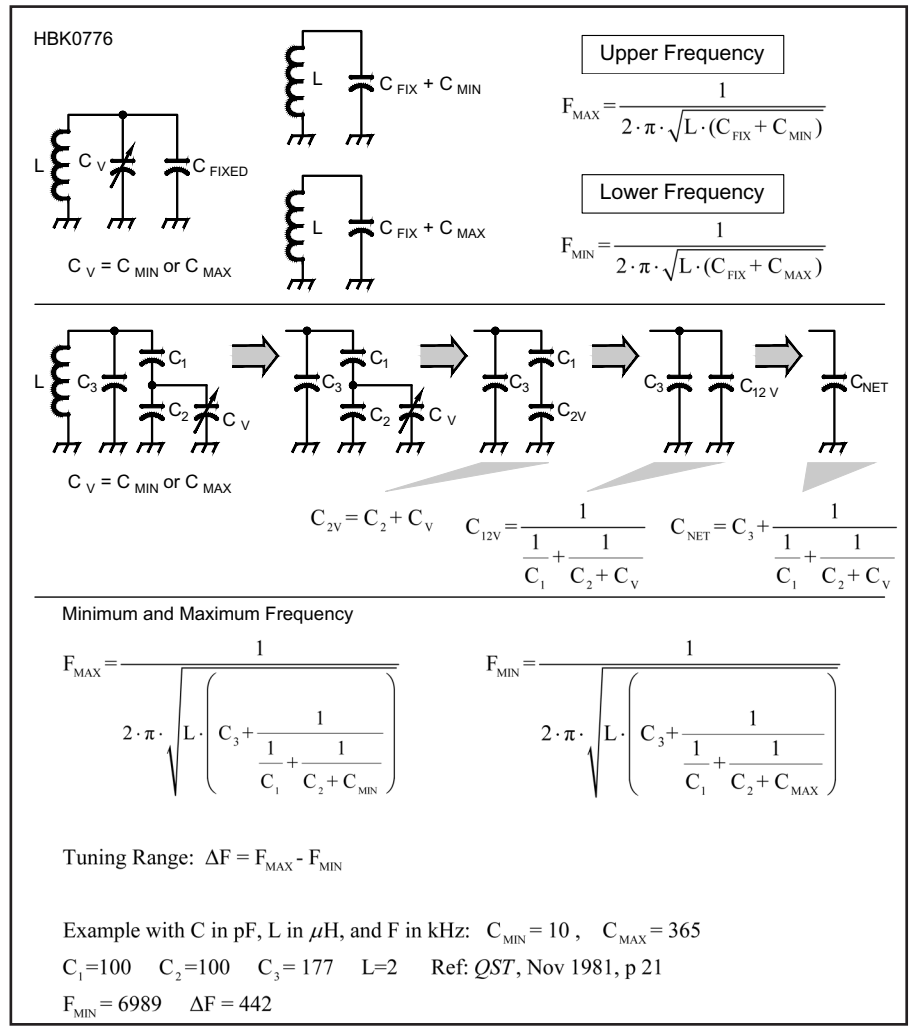


Fig 9.18 — A simple resonant circuit is tuned with parallel capacitors as shown in the top section. The tuning range is controlled by the ratio of the variable capacitance to the fixed capacitance.

is, in turn, paralleled by C_3 to form the total capacitor, C_{NET}. The overall frequency is calculated from the usual resonance relationship. The equations are shown, with capacitance in farads, inductance in henries, and frequency in Hz.

There is considerable flexibility available to the designer, afforded by picking C_1 and C_2 values. Some combinations with C_1 much smaller than the variable capacitor can produce highly nonlinear tuning.

INDUCTORS

Ceramic coil forms can give excellent results, as can self-supporting air-wound coils (Miniductor). If you use a magnetic core, support it securely and use powdered iron. Do not use ferrite because of its temperature instability. Stable VFOs have been made using toroidal cores. Micrometals mix #6 has a low temperature coefficient and works well in conjunction with NP0 ceramic capacitors. Coil forms in other materials have to be assessed on an individual basis.

A material's temperature stability will not be apparent until you try it in an oscillator, but you can apply a quick test to identify those nonmetallic materials that are lossy enough to spoil a coil's Q. Put a sample of the coil-form material into a microwave oven along with a glass of water and cook it about 10 seconds on low power. Do not include any metal fittings or ferromagnetic cores. Good materials will be completely unaffected; poor ones will heat and may even melt, smoke, or burst into flame. (This operation is a fire hazard if you try more than a tiny sample of an unknown material. Observe your experiment continuously and do not leave it unattended!)

W7ZOI suggests annealing toroidal VFO coils after winding. W7EL reports achieving success with this method by boiling his coils in water and letting them cool in air.

VOLTAGE REGULATORS

VFO circuits are often run from locally regulated power supplies, usually from resistor/Zener diode combinations. Zener diodes have some idiosyncrasies that could spoil the oscillator. They are noisy, so decoupling is needed down to audio frequencies to filter this out. Zener diodes are often run at much less than their specified optimum bias current. Although this saves power, it results in a lower output voltage than intended and the diode's impedance is much greater, increasing its sensitivity to variations in input voltage, output current and temperature. Some common Zener types may be designed to run at as much as 20 mA; check the data sheet for your diode family to find the optimum current.

True Zener diodes are low-voltage devices; above a couple of volts, so-called Zener diodes are actually avalanche types. The temperature coefficient of these diodes depends on their breakdown voltage and crosses through zero for diodes rated at about 5 V. If you intend to use nothing fancier than a common-variety Zener, designing the oscillator to run from 5 V and using a 5.1 V Zener will give you a free advantage in voltage-versus-temperature stability.

There are some diodes available with especially low temperature coefficients, usually referred to as reference or temperature-compensated diodes. These usually consist of a series pair of diodes designed to cancel each other's temperature drift. The 1N821A diode has a temperature coefficient of ±100 ppm/°C. Running at 7.5 mA, the 1N829A provides 6.2 V ±5% and a temperature coefficient of just ±5 parts per million (ppm) maximum per degree Celsius. A change in bias current of 10% will shift the voltage less than 7.5 mV, but this increases rapidly for greater current variation. The curves in **Fig 9.19** show how the temperature coefficients of these diodes are dependent on bias current.

The LM399 is a complex IC that behaves like a superb Zener at 6.95 V, ±0.3 ppm/°C. Precision, low-power, three-terminal regulators are also available that are designed to be used as voltage references, some of which can provide enough current to run a VFO. There are comprehensive tables of all these devices between pages 334 and 337 of Horowitz and Hill, *The Art of Electronics, 2nd ed*.

OSCILLATOR DEVICES

The 2N3819 FET, a classic from the 1960s, has proven to work well in VFOs but, like the MPF102 which is also long-popular with ham builders, it is manufactured to wide tolerances. Considering an oscillator's importance in receiver stability, you should not hesitate to spend a bit more on a better device. The 2N5484, 2N5485 and 2N5486 are worth considering; together, their transconductance ranges span that of the MPF102, but each is a better-controlled subset of that range. The 2N5245 is a more recent device with better-than-average noise performance that runs at low currents like the 2N3819. The 2N4416/A, also available as the plastic-cased PN4416, is a low-noise device, designed for VHF/UHF amplifier use, which has been featured in a

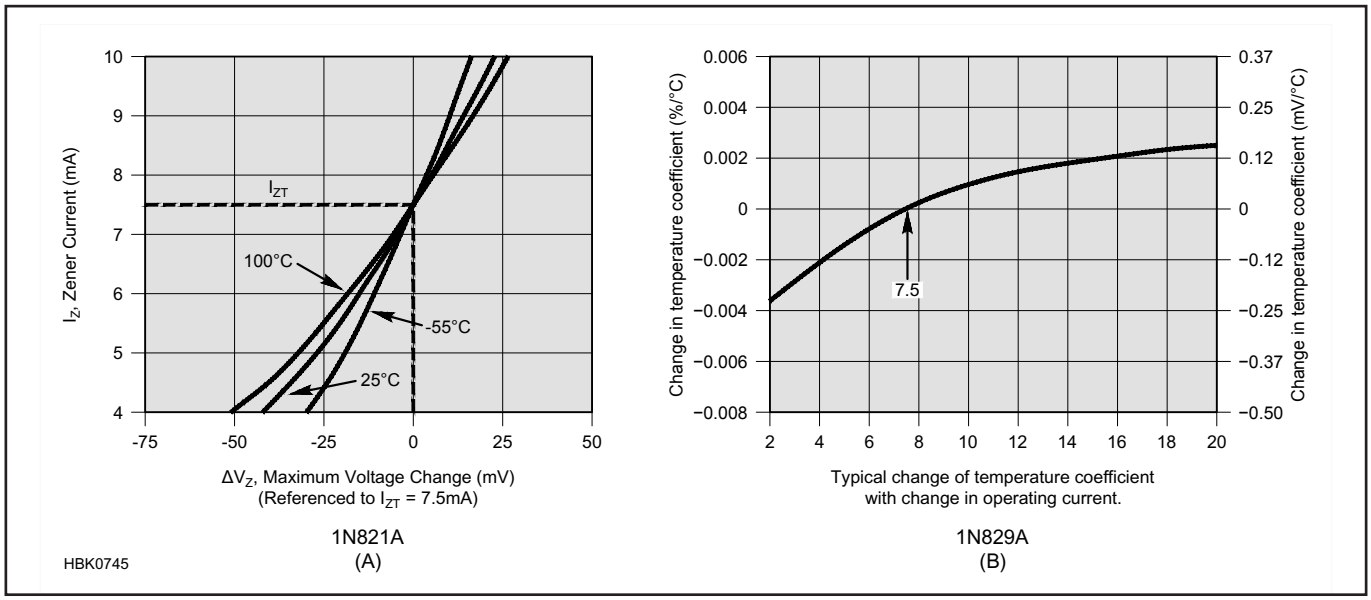


Fig 9.19 — The temperature coefficient of temperature-compensated diodes varies with bias current. To obtain the best temperature performance, use the specific bias current for the diode.

number of good oscillators up to the VHF region. Its low internal capacitance contributes to low frequency drift. The J310 (plastic; the metal-cased U310 is similar) is another popular JFET for use in oscillators.

The 2N5179 (plastic, PN5179 or MPS5179) is a bipolar transistor capable of good performance in oscillators up to the top of the VHF region. Care is needed because its absolute-maximum collector-emitter voltage is only 12 V, and its collector current must not exceed 50 mA. Although these characteristics may seem to convey fragility, the 2N5179 is sufficient for circuits powered by stabilized 6 V power supplies.

VHF-UHF capable transistors are not really necessary in LC VFOs because such circuits are rarely used above 10 MHz. (High-bandwidth transistors also increase high-frequency harmonic content in the output signal.) Absolute frequency stability is progressively harder to achieve with increasing frequency, so free-running oscillators are used only rarely to generate VHF-UHF signals for radio communication. Instead, VHF-UHF radios usually use voltage-tuned, phase-locked oscillators in some form of synthesizer. Bipolar devices like the BFR90 and MRF901, with f_T in the 5 GHz region and mounted in stripline packages, are needed for successful oscillator design at UHF.

The popular SA/NE602 mixer IC has a built-in oscillator and can be found in many published circuits. This device has separate input and output pins to the tank and has proved to be quite tame. It may not have been "improved" yet (so far, it has progressed from the SA/NE602 to the SA/NE602A, the A version affording somewhat higher dynamic range than the original SA/NE602). It might be a good idea for anyone laying out a board using one to take a little extra care to keep PCB traces short in the oscillator section to build in some safety margin so that the board can be used reliably in the future. Experienced (read: "bitten") professional designers know that their designs are going to be built for possibly more than 10 years and have learned to make allowances for the progressive improvement of semiconductor manufacture.

9.4.2 Temperature Compensation

The general principle for creating a high-stability VFO is to use components with minimal temperature coefficients in circuits that are as insensitive as possible to changes in components' secondary characteristics. Even after careful minimization of the causes of temperature sensitivity, further improvement can still be desirable. The traditional method was to split one of the capacitors in the tank so that it could be apportioned between low-temperature-coefficient parts and parts with deliberate temperature dependency. Only a limited number of different, controlled temperature coefficients are available, so the proportioning between low coefficient and controlled coefficient parts was varied to "dilute" the temperature sensitivity of a part more sensitive than desired. This is a tedious process, involving much trial and error, an undertaking made more complicated by the difficulty of arranging means of heating and cooling the unit being compensated. (Hayward described such a means in December 1993 *QST*.) As commercial and military equipment have been based on frequency synthesizers for some time, supplies of capacitors with controlled temperature sensitivity are drying up. An alternative approach is needed.

A temperature-compensated crystal oscillator (TCXO) is an improved-stability version of a crystal oscillator that is used widely in industry. Instead of using controlled-temperature coefficient capacitors, most TCXOs use a network of thermistors and normal resistors to control the bias of a tuning diode. Manufacturers measure the temperature vs. frequency characteristic of sample oscillators, and then use a computer program to calculate the optimum normal resistor values for production. This can reliably achieve at least a tenfold improvement in stability. We here are not interested in mass manufacture, but the idea of a thermistor tuning a varactor is worth adopting. The parts involved are likely to be available for a long time.

Browsing through component suppliers' catalogs shows ready availability of 4.5 to 5 kΩ bead thermistors intended for temperature-compensation purposes, at less than a dollar each. **Fig 9.20** shows a circuit based on this form of temperature compensation. Commonly available thermistors have negative temperature coefficients, so as temperature rises, the voltage at the counterclockwise (CCW) end of R8 increases, while that at the clockwise (CW) end drops. Somewhere near the center there is no change. Increasing the voltage on the tuning diode decreases its capacitance, so settings toward R8's CCW end simulate a negative-temperature-coefficient capacitor; toward its clockwise end, a positive-temperature- coefficient part. Choose R1 to pass 8.5 mA from whatever supply voltage is available to the 6.2 V reference diode, D1. The 1N821A/1N829A-family diode used has a very low temperature coefficient and needs 7.5 mA bias for best performance; the bridge takes the other 1 mA. R7 and R8 should be good-quality multi-turn trimmers. D2 and C1 need to be chosen to suit the oscillator circuit. Choose the least capacitance that provides enough compensation range. This reduces the noise added to the oscillator. (It is possible, though tedious, to solve for the differential varactor voltage with respect to R2 and R5, via differential calculus and circuit theory. The equations in Hayward's 1993 article can then be modified to accommodate the additional capacitors formed by D2 and C1.) Use a single ground point near D2 to reduce the influence of ground currents from other circuits. Use good-quality metal-film components for the circuit's fixed resistors.

The novelty of this circuit is that it is designed to have an easy and direct adjustment process. The circuit requires two adjustments, one at each of two different temperatures, and achieving them requires a stable frequency

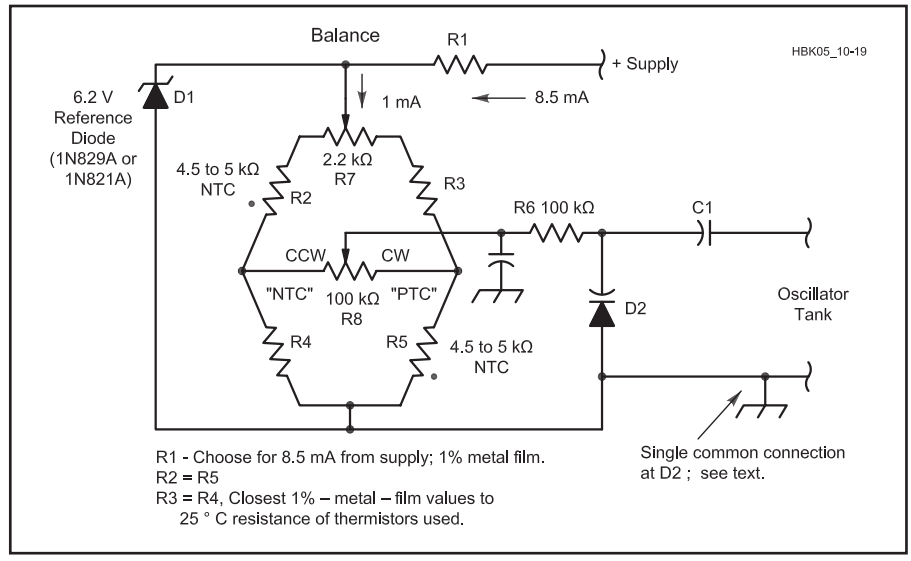


Fig 9.20 — Oscillator temperature compensation is difficult because of the scarcity of negative-temperature-coefficient capacitors. This circuit by GM4ZNX uses a bridge containing two identical thermistors to steer a tuning diode for drift correction. The 6.2 V Zener diode used (a 1N821A or 1N829A) must be a temperature-compensated part; just any 6.2 V Zener will not do.

counter that can be kept far enough from the radio so that the radio, not the counter, is subjected to the temperature extremes. (Using a receiver to listen to the oscillator under test can speed the adjustments.) After connecting the counter to the oscillator to be corrected, run the radio containing the oscillator and compensator in a room-temperature, draft-free environment until the oscillator's frequency reaches its stable operating temperature (rise over the ambient temperature). Lock its tuning, if possible. Adjust R7 to balance the bridge. This causes a drop of 0 V across R8, a condition you can reach by winding R8 back and forth across its range while slowly adjusting R7. When the bridge is balanced and 0 V appears across R8, adjusting R8 causes no frequency shift. When you've found this R7 setting, leave it there, set R8 to the exact center of its range and record the oscillator frequency.

Run the radio in a hot environment and allow its frequency to stabilize. Adjust R8 to restore the frequency to the recorded value. The sensitivity of the oscillator to temperature should now be significantly reduced between the temperatures at which you performed the adjustments. You will also have somewhat improved the oscillator's stability outside this range.

For best results with any temperature-compensation scheme, it's important to group all the oscillator and compensator components in the same enclosure, avoiding differences in airflow over components. A good oscillator should not dissipate much power, so it's feasible, even advisable, to mount all of the oscillator components in an unventilated box. In the real world, temperatures change and if the components being compensated and the components doing the compensating have different thermal time constants, a change in temperature can cause a temporary change in frequency until the slower components have caught up. One cure for this is to build the oscillator in a thick-walled metal box that's slow to heat or cool, and so dominates and reduces the possible rate of change of temperature of the circuits inside. This is sometimes called a *cold oven*.

9.4.3 Shielding and Isolation

It is important to remember that any inductor acts as half of a transformer. Oscillators contain inductors running at moderate power levels and so can radiate strong enough signals to cause interference with other parts of a radio, or with other radios. This is the tank (or other) inductor behaving as a transformer primary. Oscillators are also sensitive to radiated signals or other nearby varying magnetic fields. This is the tank (or other) inductor also behaving as a transformer secondary. Effective shielding is therefore vital.

Any oscillator is particularly sensitive to interference on the same or very nearby frequency. If this interference is strong enough an effect called *injection locking* will occur. The oscillator effectively stops oscillating and instead directly follows the interfering signal. This situation is very bad. For example, a VFO used to directly drive a power amplifier and antenna (to form a simple CW transmitter) can prove surprisingly difficult to shield well enough because of injection locking from any leakage of the power amplifier's high-level signal back into the oscillator. Even if injection locking does not fully kick in, the wrestling inside the VFO between its own oscillation and the interference can affect its frequency, resulting in a very poor transmitted note. If the radio gear is in the station antenna's near field, there are also strong fields that are coherent with the VFO oscillation, making sufficient shielding even more difficult.

The following rules of thumb continue to serve ham builders well:

- Use a complete metal box, with as few holes drilled in it as possible, with good contact around surface(s) where its lid(s) fit(s) on.
- Use feedthrough capacitors on power and control lines that pass in and out of the VFO enclosure and on the transmitter or transceiver enclosure as well.
- Use buffer amplifier circuitry that amplifies the signal by the desired amount and provides sufficient attenuation of signal energy flowing in the reverse direction. This is known as *reverse isolation* and is a frequently overlooked loophole in shielding. Figs 9.15 and 9.16 include buffer circuitry of proven performance. Another (and higher-cost) option is to consider using a high-speed buffer-amplifier IC (such as the LM6321N by National Semiconductor, a part that combines the high input impedance of an op amp with the ability to drive 50-Ω loads directly up into the VHF range).
- Use a mixing-based frequency-generation scheme instead of one that operates straight through or by means of multiplication. Such a system's oscillator stages can operate on frequencies with no direct frequency relationship to its output frequency. This essentially eliminates the possibility of injection locking the VFO.
- Use the time-tested technique of running your VFO at a sub-harmonic of the output signal desired — say, 3.5 MHz in a 7 MHz transmitter — and multiply its output frequency in a suitably nonlinear stage for further amplification at the desired frequency. This does reduce the tendency to injection lock.

9.5 Crystal Oscillators

Because crystals afford Q values and frequency stabilities that are orders of magnitude better than those achievable with LC circuits, fixed-frequency oscillators usually use quartz crystal resonators. Master references for frequency counters and synthesizers are always based on crystal oscillators.

So glowing is the executive summary of the crystal's reputation for stability that newcomers to radio experimentation naturally believe that the presence of a crystal in an oscillator will force oscillation at the frequency stamped on the can. This impression is usually revised after the first few experiences to the contrary! There is no sure-fire crystal oscillator circuit (although some are better than others); reading and experience soon provide a learner with plenty of anecdotes to the effect that:

- Some circuits have a reputation of being temperamental, even to the point of not always starting.
- Crystals sometimes mysteriously oscillate on unexpected frequencies.

Even crystal manufacturers have these problems, so don't be discouraged from building crystal oscillators. The occasional uncooperative oscillator is a nuisance, not a disaster, and it just needs a little individual attention. Knowing how a crystal behaves is the key to a cure.

Dr Ulrich Rohde, N1UL, has generously contributed a pair of detailed papers that discuss the crystal oscillator along with several HF and VHF designs. Both papers, "Quartz Crystal Oscillator Design" and "A Novel Grounded Base Oscillator Design for VHF/UHF Frequencies" are included on the CD-ROM accompanying this book.

9.5.1 Quartz and the Piezoelectric Effect

Quartz is a crystalline material with a regular atomic structure that can be distorted by the simple application of force. Remove the force, and the distorted structure springs back to its original form with very little energy loss. This property allows *acoustic waves* — sound — to propagate rapidly through quartz with very little attenuation, because the velocity of an acoustic wave depends on the elasticity and density (mass/volume) of the medium through which the wave travels.

If you heat a material, it expands. Heating may cause other characteristics of a material to change — such as elasticity, which affects the speed of sound in the material. In quartz, however, expansion and change in the speed of sound are very small and tend to cancel, which means that the transit time for sound to pass through a piece of quartz is very stable.

The third property of this wonder material is that it is *piezoelectric*. Apply an electric field to a piece of quartz and the crystal lattice distorts just as if a force had been applied. The electric field applies a force to electrical charges locked in the lattice structure. These charges are captive and cannot move around in the lattice as they can in a semiconductor, for quartz is an insulator. A capacitor's dielectric stores energy by creating physical distortion on an atomic or molecular scale. In a piezoelectric crystal's lattice, the distortion affects the entire structure. In some piezoelectric materials, this effect is sufficiently pronounced that special shapes can be made that bend *visibly* when a field is applied.

Consider a rod made of quartz. Any sound wave propagating along it eventually hits an end, where there is a large and abrupt change in acoustic impedance. Just as when an RF wave hits the end of an unterminated transmission line, a strong reflection occurs. The rod's other end similarly reflects the wave. At some frequency, the phase shift of a round trip will be such that waves from successive round trips exactly coincide in phase and reinforce each other, dramatically increasing the wave's amplitude. This is *resonance*.

The passage of waves in opposite directions forms a standing wave with antinodes at the rod ends. Here we encounter a seeming ambiguity: not just one, but a family of different frequencies, causes standing waves — a family fitting the pattern of ½, ⅔, ⅝, ⅞ and so on, wavelengths into the length of the rod. And this is the case: A quartz rod can resonate at any and all of these frequencies.

The lowest of these frequencies, where the crystal is ½ wavelength long, is called the *fundamental* mode. The others are named the third, fifth, seventh and so on, *overtones*. There is a small phase-shift error during reflection at the ends, which causes the frequencies of the overtone modes to differ slightly from odd integer multiplies of the fundamental. Thus, a crystal's third overtone is very close to, but not exactly, three times its fundamental frequency. Many people are confused by overtones and harmonics. Harmonics are additional signals at exact integer multiples of the fundamental frequency. Overtones are not signals at all; they are additional resonances that can be exploited if a circuit is configured to excite them.

The crystals we use most often resonate in the 1 to 30 MHz region and are of the *AT-cut, thickness shear* type, although these last two characteristics are rarely mentioned. A 15 MHz fundamental crystal of this type is about 0.15 mm thick. Because of the widespread use of reprocessed war-surplus, pressure-mounted FT-243 crystals, you may think of crystals as small rectangles on the order of a half-inch in size. The crystals we commonly use today are discs, etched and/or doped to their final dimensions, with metal electrodes deposited directly on the quartz. A crystal's diameter does not directly affect its frequency; diameters of 8 to 15 mm are typical. (Quartz crystals are also discussed in the **RF and AF Filters** chapter.)

AT-cut is one of a number of possible standard designations for the orientation at which a crystal disc is sawed from the original quartz crystal. The crystal lattice atomic structure is asymmetric, and the orientation of this with respect to the faces of the disc influences the crystal's performance. *Thickness shear* is one of a number of possible orientations of the crystal's mechanical vibration with respect to the disc. In this case, the crystal vibrates perpendicularly to its thickness. This is not easy to visualize, and diagrams don't help much, but **Fig 9.21** is an attempt at illustrating this. Place a moist bathroom sponge between the palms of your hands, move one hand up and down, and you'll see thickness shear in action.

There is a limit to how thin a disc can be made, given requirements of accuracy and price. Traditionally, fundamental-mode crystals have been made up to 20 MHz, although 30 MHz is now common at a moderately raised price. Using techniques pioneered in the semiconductor industry, crystals have been made with a central region etched down to a thin membrane, surrounded by a thick ring for robustness. This approach can push fundamental resonances to over 100 MHz, but these are more lab curiosities than parts for everyday use. The easy solution for higher frequencies is to use a nice, manufacturably-thick crystal on an overtone mode. All crystals have multiple modes, so if you order a 28.060 MHz, third-overtone unit for a little QRP transmitter, you'll get a crystal with a fundamental resonance somewhere near 9.353333 MHz, but its manufacturer will have adjusted the thickness to plant the third overtone exactly on the ordered frequency. An accomplished manufacturer can do tricks with the flatness of the disc faces to make the wanted overtone mode a little more active and the other modes a little less active. (As some builders discover, however, this does not *guarantee* that the wanted mode is the most active!)

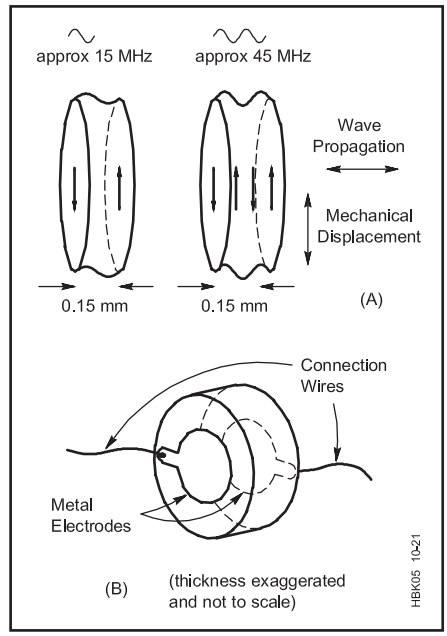


Fig 9.21 — Thickness-shear vibration at a crystal's fundamental and third overtone (A); B shows how the modern crystals commonly used by radio amateurs consist of etched quartz discs with electrodes deposited directly on the crystal surface.

Quartz's piezoelectric property provides a simple way of driving the crystal electrically. Early crystals were placed between a pair of electrodes in a case. This gave amateurs the opportunity to buy surplus crystals, open them and grind them a little to reduce their thickness, thus moving them to higher frequencies. The frequency could be reduced very slightly by loading the face with extra mass, such as by blackening it with a soft pencil. Modern crystals have metal electrodes deposited directly onto their surfaces (Fig 9.21B), and such tricks no longer work.

The piezoelectric effect works both ways. Deformation of the crystal produces voltage across its electrodes, so the mechanical energy in the resonating crystal can also be extracted electrically by the same electrodes. Seen electrically, at the electrodes, the mechanical resonances look like electrical resonances. Their Q is very high. A Q of 10,000 would characterize a *poor* crystal today; 100,000 is often reached by high-quality parts. For comparison, a Q of over 200 for an LC tank is considered good.

9.5.2 Frequency Accuracy

A crystal's frequency accuracy is as outstanding as its Q. Several factors determine a crystal's frequency accuracy. First, the manufacturer makes parts with certain tolerances: ±200 ppm for a low-quality crystal for use as in a microprocessor clock oscillator, ±10 ppm for a good-quality part for professional radio use. Anything much better than this starts to get expensive! A crystal's resonant frequency is influenced by the impedance presented to its terminals, and manufacturers assume that once a crystal is brought within several parts per million of the nominal frequency, its user will perform fine adjustments electrically.

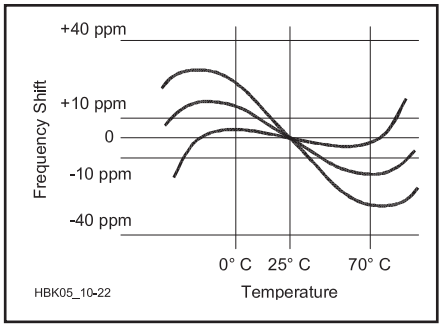
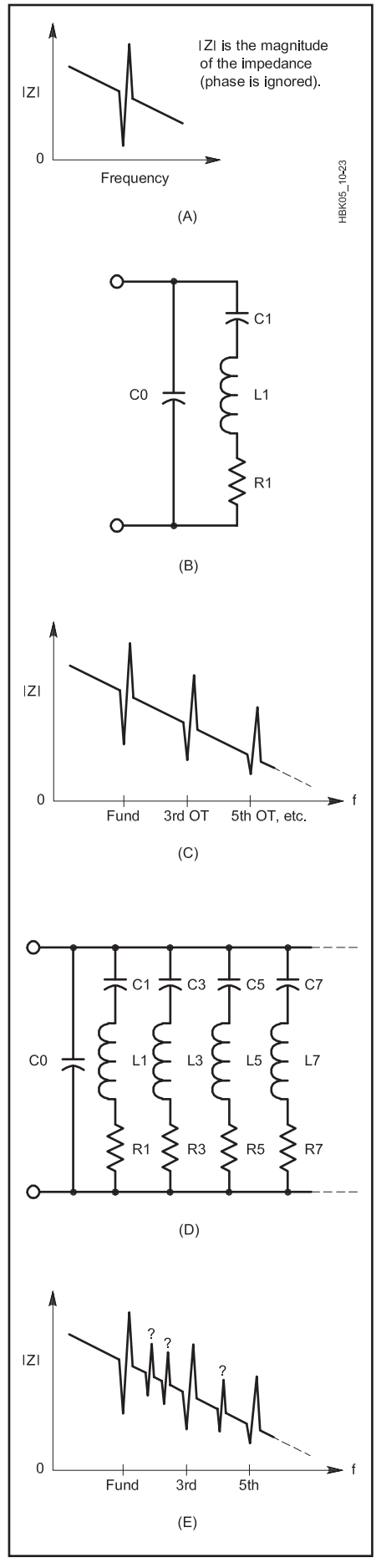


Fig 9.22 — Slight changes in a crystal cut's orientation shift its frequency-versus-temperature curve.

Second, a crystal ages after manufacture. Aging could give increasing or decreasing frequency; whichever, a given crystal usually keeps aging in the same direction. Aging is rapid at first and then slows down. Aging is influenced by the care in polishing the surface of the crystal (time and money) and by its holder style. The cheapest holder is a soldered-together, two-part metal can with glass bead insulation for the connection pins. Soldering debris lands on the crystal and affects its frequency. Alternatively, a two-part metal case can be made with flanges that are pressed together until they fuse, a process called *cold-welding*. This is much cleaner and improves aging rates roughly fivefold compared to soldered cans. An all-glass case can be made in two parts and fused together by heating in a vacuum. The vacuum raises the Q, and the cleanliness results in aging that's roughly 10 times slower than that achievable with a soldered can. The best crystal holders borrow from vacuum-tube assembly processes and have a *getter*, a highly reactive chemical substance that traps remaining gas molecules, but such crystals are used only for special purposes.

Third, temperature influences a crystal. A reasonable, professional quality part might be specified to shift not more than ±10 ppm over 0 to 70 °C. An AT-cut crystal has an *S*-shaped frequency-versus-temperature characteristic, which can be varied by slightly changing the crystal cut's orientation. **Fig 9.22** shows the general shape and the effect of changing the cut angle by only a few seconds of arc. Notice how all the curves converge at 25 °C. This is because this temperature is normally chosen as the reference for specifying a crystal. The temperature stability specification sets how accurate the manufacturer must make the cut. Better stability may be needed for a crystal used as a receiver frequency standard, frequency counter clock and so on. A crystal's temperature characteristic shows a little hysteresis. In other words, there's a bit of offset to the curve depending on whether temperature is increasing or decreasing. This is usually of no consequence except in the highest-precision circuits.



It is the temperature of the quartz that is important, and as the usual holders for crystals all give effective thermal insulation, only a couple of milliwatts dissipation by the crystal itself can be tolerated before self-heating becomes troublesome. Because such heating occurs in the quartz itself and does not come from the surrounding environment, it defeats the effects of temperature compensators and ovens.

The techniques shown earlier for VFO temperature compensation can also be applied to crystal oscillators. An after-compensation drift of 1 ppm is routine and 0.5 ppm is good. The result is a *temperature-compensated crystal oscillator* (*TCXO*). Recently, oscillators have appeared with built-in digital thermometers, microprocessors and ROM look-up tables customized on a unit-by-unit basis to control a tuning diode via a digital-to-analog converter (DAC) for temperature compensation. These *digitally temperature-compensated oscillators* (*DTCXOs*) can reach 0.1 ppm over the temperature range. With automated production and adjustment, they promise to become the cheapest way to achieve this level of stability.

Oscillators have long been placed in temperature-controlled *ovens*, which are typically held at 80 °C. Stability of several parts per billion can be achieved over temperature, but this is a limited benefit as aging can easily dominate the accuracy. These are usually called *oven-controlled crystal oscillators* (*OCXOs*).

Fourth, the crystal is influenced by the impedance presented to it by the circuit in which it is used. This means that care is needed to make the rest of an oscillator circuit stable, in terms of impedance and phase shift.

Gravity can slightly affect crystal resonance. Turning an oscillator upside down usually produces a small frequency shift, usually much less than 1 ppm; turning the oscillator back over reverses this. This effect is quantified for the highest-quality reference oscillators.

9.5.3 The Equivalent Circuit of a Crystal

Because a crystal is a passive, two-terminal device, its electrical appearance is that of an impedance that varies with frequency. **Fig 9.23A** shows a very simplified sketch

Fig 9.23 — Exploring a crystal's impedance (A) and equivalent circuit (B) through simplified diagrams. C and D extend the investigation to include overtones; E, to spurious responses not easily predictable by theory or controllable through manufacture. A crystal may oscillate on any of its resonances under the right conditions.

of the magnitude (phase is ignored) of the impedance of a quartz crystal. The general trend of dropping impedance with increasing frequency implies capacitance across the crystal. The sharp fall to a low value resembles a series-tuned tank, and the sharp peak resembles a parallel-tuned tank. These are referred to as series and parallel resonances. Fig 9.23B shows a simple circuit that will produce this impedance characteristic. The impedance looks purely resistive at the exact centers of both resonances, and the region between them has impedance increasing with frequency, which looks inductive.

C1 (sometimes called *motional capacitance*, C_m, to distinguish it from the lumped capacitance it approximates) and L1 (*motional inductance,* L_m) create the series resonance, and as C0 and R1 are both fairly small, the impedance at the bottom of the dip is very close to R1. At parallel resonance, L1 is resonating with C1 and C0 in series, hence the higher frequency. The impedance of the parallel tank is extremely high; the terminals are connected to a capacitive tap, which causes them to see only a small fraction of what is still a very large impedance. The overtones should not be neglected, so Figs 9.23C and 9.23D include them. Each overtone has series and parallel resonances and so appears as a series tank in the equivalent circuit. C0 again provides the shifted parallel resonance.

This is still simplified, because real-life crystals have a number of spurious, unwanted modes that add yet more resonances, as shown in Fig 9.23E. These are not well controlled and may vary a lot even between crystals made to the same specification. Crystal manufacturers work hard to suppress these spurs and have evolved a number of recipes for shaping crystals to minimize them. Just where they switch from one design to another varies from manufacturer to manufacturer.

Always remember that the equivalent circuit is just a representation of crystal behavior and does not represent circuit components actually present. Its only use is as an aid in designing and analyzing circuits using crystals. **Table 9.1** lists typical equivalent-circuit values for a variety of crystals. It is impossible to build a circuit with 0.026 to 0.0006 pF capacitors; such values would simply be swamped by strays. Similarly, the inductor must have a Q that is orders of magnitude better than is practically achievable, and impossibly low stray C in its winding.

The values given in Table 9.1 are nothing more than rough guides. A crystal's frequency is tightly specified, but this still allows inductance to be traded for capacitance. A good manufacturer could hold these characteristics within a ±25% band or could vary them over a 5:1 range by special design. Similarly marked parts from different sources vary widely in motional inductance and capacitance.

Quartz is not the only material that behaves in this way, but it is the best. Resonators can be made out of lithium tantalate and a group of similar materials that have lower Q, allowing them to be *pulled* over a larger frequency range in VCXOs. Much more common, however, are ceramic resonators based on the technology of the well-known ceramic IF filters. These have much lower Q than quartz and much poorer frequency precision. They serve mainly as clock resonators for cheap microprocessor systems in which every last cent must be saved. A ceramic resonator could be used as the basis of a wide range, cheap VXO, but its frequency stability would not be as good as a good LC VFO.

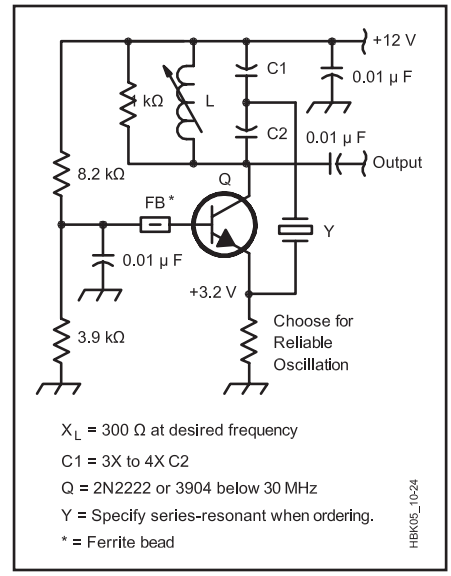


Fig 9.24 — A basic series-mode crystal oscillator. A 2N5179 can be used in this circuit if a lower supply voltage is used; see text.

9.5.4 Crystal Oscillator Circuits

(See also the papers "Quartz Crystal Oscillator Design" and "A Novel Grounded Base Oscillator Design for VHF/UHF Frequencies" by Dr Ulrich Rohde, N1UL, included on the CD-ROM accompanying this book.)

Crystal oscillator circuits are usually categorized as series- or parallel-mode types, depending on whether the crystal's low- or high-impedance resonance comes into play at the operating frequency. The series mode is now the most common; parallel-mode operation was more often used with vacuum tubes. **Fig 9.24** shows a basic series-mode oscillator. Some people would say that it is an overtone circuit, used to run a crystal on one of its overtones, but this is not necessarily true. The tank (L-C1-C2) tunes the collector of the common-base amplifier. C1 is larger than C2, so the tank is tapped in a way that transforms to lower impedance, decreasing signal voltage, but increasing current. The current is fed back into the emitter via the crystal. The common-base stage provides a current gain of less than unity, so the transformer in the form of the tapped tank is essential to give loop gain. There are *two* tuned circuits, the obvious collector tank and the series-mode one "in" the crystal. The tank kills the amplifier's gain away from its tuned frequency, and the crystal will only pass current at the series resonant frequencies of its many modes. The tank resonance is much broader than any of the crystal's modes, so it can be thought of as the crystal setting the frequency, but the tank selecting which of the crystal's modes is active. The tank could be tuned to the crystal's fundamental, or one of its overtones.

Fundamental oscillators can be built without a tank quite successfully, but there is always the occasional one that starts up on an overtone or spurious mode. Some simple oscillators have been known to change modes while running (an effect triggered by changes in temperature or loading) or to not always start in the same mode! A series-mode oscillator should present low impedance to the crystal at the operating frequency. In Fig 9.24, the tapped collector tank presents a transformed fraction of the 1-kΩ collector load resistor to one end of the crystal, and the emitter presents a low impedance to the other. To build a practical oscillator from this circuit, choose an inductor with a reactance of about 300 Ω at the wanted frequency and calculate C1 in series with C2 to resonate with it. Choose C1 to be 3 to 4 times larger than C2. The amplifier's quiescent ("idling") current sets the gain and hence the operating level. This is not easily calculable, but can be found by experiment. Too little quiescent current and the oscillator will not start reliably; too much and the transistor can drive

Table 9.1
Typical Equivalent Circuit Values for a Variety of Crystals

Crystal Type	*Series L*	*Series C (pF)*	*Series R (Ω)*	*Shunt C (pF)*
1 MHz fundamental	3.5 H	0.007	340	3.0
10 MHz fundamental	9.8 mH	0.026	7	6.3
30 MHz third overtone	14.9 mH	0.0018	27	6.2
100 MHz fifth overtone	4.28 mH	0.0006	45	7.0

itself into saturation. If an oscilloscope is available, it can be used to check the collector waveform; otherwise, some form of RF voltmeter can be used to allow the collector voltage to be set to 2 to 3 V RMS. 3.3 kΩ would be a suitable starting point for the emitter bias resistor. The transistor type is not critical; 2N2222A or 2N3904 would be fine up to 30 MHz; a 2N5179 would allow operation as an overtone oscillator to over 100 MHz (because of the low collector voltage rating of the 2N5179, a supply voltage lower than 12 V is required). The ferrite bead on the base gives some protection against parasitic oscillation at UHF.

If the crystal is shorted, this circuit should still oscillate. This gives an easy way of adjusting the tank; it is even better to temporarily replace the crystal with a small-value (tens of ohms) resistor to simulate its *equivalent series resistance* (ESR), and adjust L until the circuit oscillates close to the wanted frequency. Then restore the crystal and set the quiescent current. If a lot of these oscillators were built, it would sometimes be necessary to adjust the current individually due to the different equivalent series resistance of individual crystals. One variant of this circuit has the emitter connected directly to the C1/C2 junction, while the crystal is a decoupler for the transistor base (the existing capacitor and ferrite bead not being used). This works, but with a greater risk of parasitic oscillation.

We commonly want to trim a crystal oscillator's frequency. While off-tuning the tank a little will pull the frequency slightly, too much detuning spoils the mode control and can stop oscillation (or worse, make the circuit unreliable). The answer to this is to add a trimmer capacitor, which will act as part of the equivalent series tuned circuit, in series with the crystal. This will shift the frequency in one way only, so the crystal frequency must be re-specified to allow the frequency to be varying around the required value. It is common to specify a crystal's frequency with a standard load (30 pF is commonly specified), so that the manufacturer grinds the crystal such that the series resonance of the specified mode is accurate when measured with a capacitor of this value in series. A 15 to 50 pF trimmer can be used in series with the crystal to give fine frequency adjustment. Too little capacitance can stop oscillation or prevent reliable starting. The Q of crystals is so high that marginal oscillators can take several seconds to start!

This circuit can be improved by driving the crystal's lower series-resonant impedance with an emitter follower as in **Fig 9.25**. This is the *Butler* oscillator. Again the tank controls the mode to either force the wanted overtone or protect the fundamental mode. The tank need not be tapped because Q2 provides current gain, although the circuit is sometimes seen with C split, driving Q2

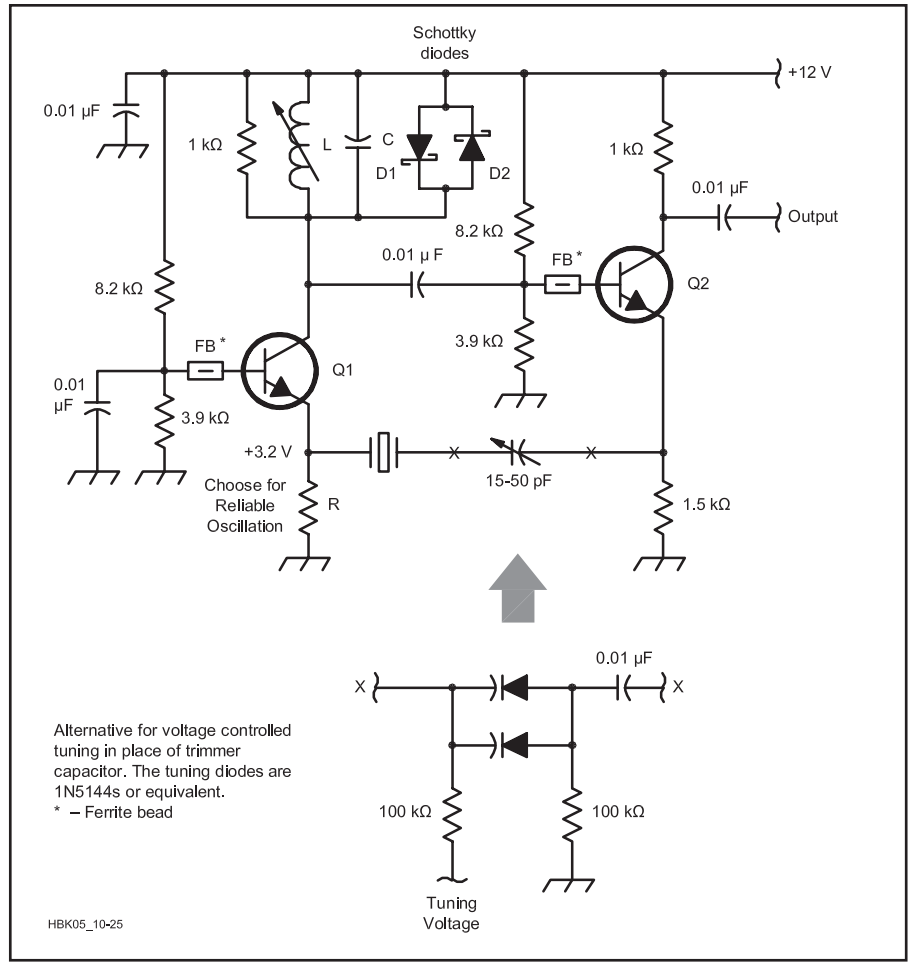


Fig 9.25 — A Butler crystal oscillator with Q2 connected as an emitter follower to drive the crystal's low series-resonant impedance.

from a tap. The position between the emitters offers a good, low-impedance environment to keep the crystal's in-circuit Q high. R, in the emitter of Q1, is again selected to give reliable oscillation. The circuit has been shown with a capacitive load for the crystal, to suit a unit specified for a 30 pF load. An alternative circuit to give electrical fine tuning is also shown. The diodes across the tank act as limiters to stabilize the operating amplitude and limit the power dissipated in the crystal by clipping the drive voltage to Q2. The tank should be adjusted to peak at the operating frequency, not used to trim the frequency. The capacitance in series with the crystal is the proper frequency trimmer.

The Butler circuit works well, and has been used in critical applications to 140 MHz (seventh-overtone crystal, 2N5179 transistor). Although the component count is high, the extra parts are cheap ones. Increasing the capacitance in series with the crystal reduces the oscillation frequency but has a progressively diminishing effect. Decreasing the capacitance pulls the frequency higher, to a point at which oscillation stops; before this point is reached, start-up will become unreliable. The possible amount of adjustment, called *pulling range*, depends on the crystal; it can range from less than 10 to several hundred parts per million. Overtone crystals have much less pulling range than fundamental crystals on the same frequency; the reduction in pulling is roughly proportional to the square of the overtone number.

LOW-NOISE CRYSTAL OSCILLATORS

Fig 9.26A shows a crystal operating in its series mode in a series-tuned Colpitts circuit. Because it does not include an LC tank to prevent operation on unwanted modes, this circuit is intended for fundamental mode operation only and relies on that mode being the most active. If the crystal is ordered for 30 pF loading, the frequency trimming capacitor can be adjusted to compensate for the loading of the capacitive divider of the Colpitts circuit. An unloaded crystal without a trimmer would operate slightly off the exact series resonant frequency in order to create an inductive impedance to resonate

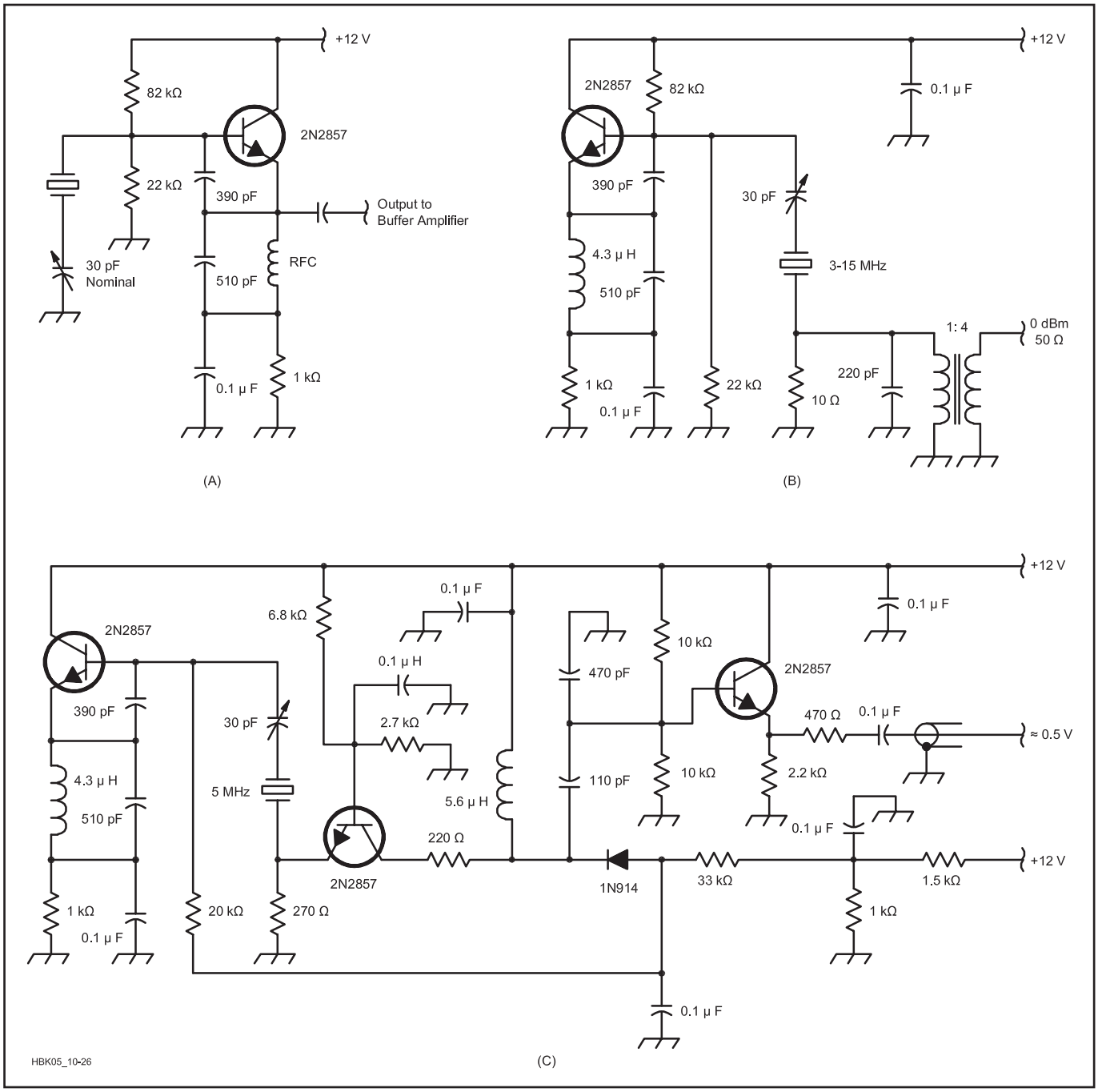


Fig 9.26 — The crystal in the series-tuned Colpitts oscillator at A operates in its series-resonant mode. B shows N1UL's low-noise version, which uses the crystal as a filter and features high harmonic suppression (from Rohde, *Microwave and Wireless Synthesizers Theory and Design*; see references). The circuit at C builds on the B version by adding a common-base output amplifier and ALC loop.

with the divider capacitors. Dr Ulrich Rohde, N1UL, in Figure 4-47 of his book *Digital PLL Frequency Synthesizers — Theory and Design*, published an elegant alternative method of extracting an output signal from this type of circuit, shown in Fig 9.26B. This taps off a signal from the current in the crystal itself. This can be thought of as using the crystal as a band-pass filter for the oscillator output. The RF choke in the emitter keeps the emitter bias resistor from loading the tank and degrading the Q. In this case (3 MHz operation), it has been chosen to resonate close to 3 MHz with the parallel capacitor (510 pF) as a means of forcing operation on the wanted mode. The 10-Ω resistor and the transformed load impedance will reduce the in-circuit Q of the crystal, so a further development substituted a common base amplifier for the resistor and transformer. This is shown in Fig 9.26C. The common-base amplifier is run at a large quiescent current to give a very low input impedance. Its collector is tuned to give an output with low harmonic content and an emitter follower is used to buffer this from the load. This oscillator sports a simple ALC system, in which the amplified and rectified signal is used to reduce the bias voltage on the oscillator transistor's base. This circuit is described as achieving a phase noise level of –168 dBc/Hz a few kilohertz out from the carrier. This may seem far beyond what may ever be needed, but frequency multiplication

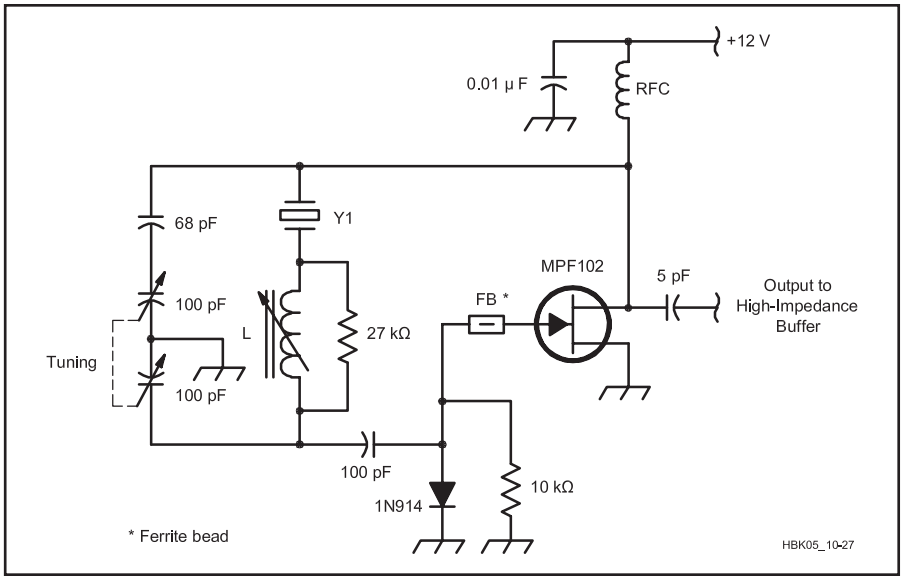


Fig 9.27 — A wide-range variable-crystal oscillator (VXO) by W7ZOI and W1FB. It was originally designed for use in low-power radios without the usual wide-range VFO.

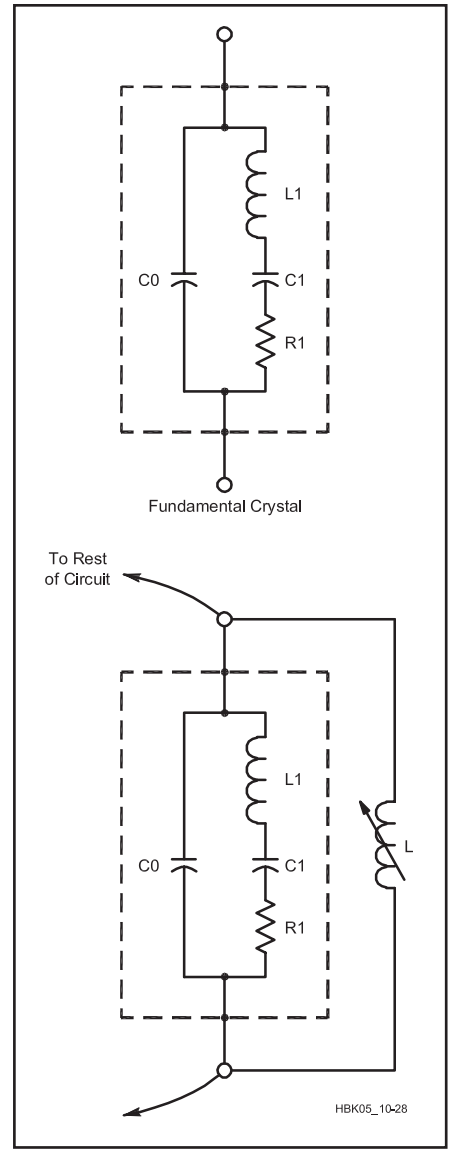


Fig 9.28 — Using an inductor to "tune out" C0 can increase a crystal oscillator's pulling range.

to high frequencies, whether by classic multipliers or by frequency synthesizers, multiplies the deviation of any FM/PM sidebands as well as the carrier frequency. This means that phase noise worsens by 20 dB for each tenfold multiplication of frequency. A clean crystal oscillator and a multiplier chain is still the best way of generating clean microwave signals for use with narrow-band modulation schemes.

It has already been mentioned that overtone crystals are much harder to pull than fundamental ones. This is another way of saying that overtone crystals are less influenced by their surrounding circuit, which is helpful in a frequency-standard oscillator like this one. Even though 5 MHz is in the main range of fundamental-mode crystals and this circuit will work well with them, an overtone crystal has been used. To further help stability, the power dissipated in the crystal is kept to about 50 µW. The common-base stage is effectively driven from a higher impedance than its own input impedance, under which conditions it gives a very low noise figure.

9.5.5 VXOs

Some crystal oscillators have frequency trimmers. If the trimmer is replaced by a variable capacitor as a front-panel control, we have a *variable crystal oscillator* (*VXO*): a crystal-based VFO with a narrow tuning range, but good stability and noise performance. VXOs are often used in small, simple QRP transmitters to tune a few kilohertz around common calling frequencies. Artful constructors, using optimized circuits and components, have achieved 1000-ppm tuning ranges. Poor-quality "soft" crystals are more pull-able than high-Q ones. Overtone crystals are not suited to VXOs. For frequencies beyond the usual limit for fundamental mode crystals, use a fundamental unit and frequency multipliers.

ICOM and Mizuho made some 2 meter SSB transceivers based on multiplied VXO local oscillators. This system is simple and can yield better performance than many expensive synthesized radios. SSB filters are available at 9 or 10.7 MHz, to yield sufficient image rejection with a single conversion. Choice of VXO frequency depends on whether the LO is to be above or below signal frequency and how much multiplication can be tolerated. Below 8 MHz, multiplier filtering is difficult. Above 15 MHz, the tuning range per crystal narrows. A 50-200 kHz range per crystal should work with a modern front-end design feeding a good 9 MHz IF, for a contest quality 2 meter SSB receiver.

The circuit in **Fig 9.27** is a JFET VXO from Wes Hayward, W7ZOI, and Doug DeMaw, W1FB, optimized for wide-range pulling. Published in *Solid State Design for the Radio Amateur*, many have been built and its ability to pull crystals as far as possible has been proven. Dr Ulrich Rohde, N1UL, has shown that the diode arrangement as used here to make signal-dependent negative bias for the gate confers a phase-noise disadvantage, but oscillators like this that pull crystals as far as possible need any available means to stabilize their amplitude and aid start-up. In this case, the noise penalty is worth paying. This circuit can achieve a 2000-ppm tuning range with amenable crystals. If you have some overtone crystals in your junk box whose fundamental frequency is close to the wanted value, they are worth trying.

This sort of circuit doesn't necessarily stop pulling at the extremes of the possible tuning range; sometimes the range is set by the onset of undesirable behavior such as jumping mode or simply stopping oscillating. L was a 16 µH slug-tuned inductor for 10 MHz operation. It is important to minimize the stray and interwinding capacitance of L since this dilutes the range of impedance presented to the crystal.

One trick that can be used to aid the pulling range of oscillators is to tune out the C0 of the equivalent circuit with an added inductor. **Fig 9.28** shows how. L is chosen to resonate with C0 for the individual crystal, turning it into a high-impedance parallel-tuned circuit. The Q of this circuit is orders of magnitude less than the Q of the true series resonance of the crystal, so its tuning is much broader. The value of C0 is usually just a few picofarads, so L has to be a fairly large value considering the frequency at which it is resonated. This means

that L has to have low stray capacitance or else it will self-resonate at a lower frequency. The tolerance on C0 and the variations of the stray C of the inductor means that individual adjustment is needed. This technique can also work wonders in crystal ladder filters.

9.5.6 Logic-Gate Crystal Oscillators

The frequency-determining network of an RC oscillator has a Q of less than one, which means that phase shift changes very slowly with different frequencies (see section 9.3.2 on RC Oscillators above). The Pierce crystal oscillator discussed previously is a converted phase-shift oscillator, with the crystal taking the place of one series resistor. The crystal provides a much faster phase shift than an RC stage, so the crystal "controls" the frequency of oscillation.

The actual frequency of oscillation is the frequency at which the Barkhausen criteria are met. The crystal must operate near its series resonance in order for the loop gain to be unity. Oscillation then settles at the frequency where the crystal phase shift, added to the RC phase shifts, equals 180 degrees. The crystal usually provides between 45 and 60 degrees of phase shift, so the oscillation frequency is above the series resonance and below the parallel resonance of the crystal where the crystal behaves as a large inductor. (See the figure showing crystal response in the section Quartz Crystal Filters in the **RF and AF Filters** chapter.)

The Pierce circuit is rarely seen in this full form. Instead, a cut-down version is the most common circuit in many microprocessors and other digital ICs that need a crystal-controlled clock. **Fig 9.29** shows this minimalist Pierce, using a CMOS logic inverter as the amplifier. R_{bias} provides dc negative feedback to bias the gate into its linear region. This value is not critical, anything between 100 kΩ and 10 MΩ works fine. The RC phase shifts needed to make this work come from R_{out}-C1 and $R_{crystal}$-C2. This circuit has a reputation of being temperamental, mainly because neither R_{out} nor $R_{crystal}$ are well documented or controlled in manufacturing. There is also a general belief that this circuit requires C1 = C2, which is not true.

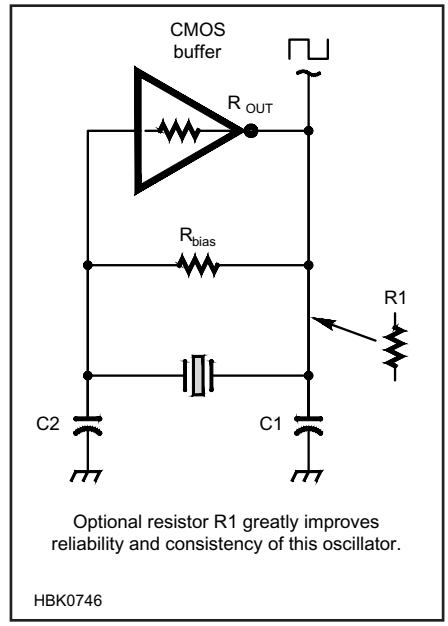


Fig 9.29 — The simplified Pierce oscillator using a logic-gate for the inverting amplifier. Adding R1 improves oscillator design and reliability.

A great improvement in performance is achieved by adding one resistor, R1, as shown in Fig 9.29. R_{bias} remains connected directly across the CMOS inverter. R1 is inserted in series from the gate output to the feedback network. The benefits are multiple:

- The edge speed of modern CMOS gates is extremely fast, so R1C1 eliminates the possibility of this fast edge exciting overtone operation.
- Phase shift into the crystal can be intentionally designed by R1 and C1 value selection.
- Drive from the inverter output is reduced into the crystal, possibly saving it from being damaged.
- Loop gain can now be controlled for best waveform and startup characteristics.

Design values are strongly dependent on the actual crystal frequency needed. C2 is selected first, to provide around 60 degrees of phase shift working against the crystal equivalent series resistance (usually a few tens of ohms, but the value needs to be verified!). The time constant R1 C1 is usefully chosen to be the reciprocal of the crystal radian frequency ($1/2\varpi f_{XTAL}$). Higher values of R1 reduce the loop gain and provide better protection for the crystal, until the loop gain gets too small and oscillation stops.

9.6 Oscillators at UHF and Above

The traditional way to make signals at higher frequencies is to make a signal at a lower frequency (where oscillators are easier) and multiply it up to the wanted range. Frequency multiplication is still one of the easiest and best ways of making a clean UHF/microwave signal. The design of a multiplier depends on whether the multiplication factor is an odd or even number. For odd multiplication, a Class-C biased amplifier can be used to create a series of harmonics; a filter selects the one wanted. For even multiplication factors, a full-wave-rectifier arrangement of distorting devices can be used to create a series of harmonics with strong even-order components, with a filter selecting the wanted component. At higher frequencies, diode-based passive circuits are commonly used. Oscillators using some of the LC circuits already described can, with care in construction, be used in the VHF range. At UHF, different approaches become necessary.

9.6.1 UHF Oscillators: Intentional and Accidental

The biggest change when working at UHF and microwave frequencies is that lumped circuit elements effectively disappear. Stray reactances and resistance dominates everything. Success at these high frequencies requires making peace with the situation and developing a very good sense of where "stray" circuit elements reside in your layout and their approximate magnitude.

Fig 9.30 shows a pair of oscillators based on a resonant length of line, which is a distributed circuit element. The first one is a return to basics: a resonator, an amplifier and

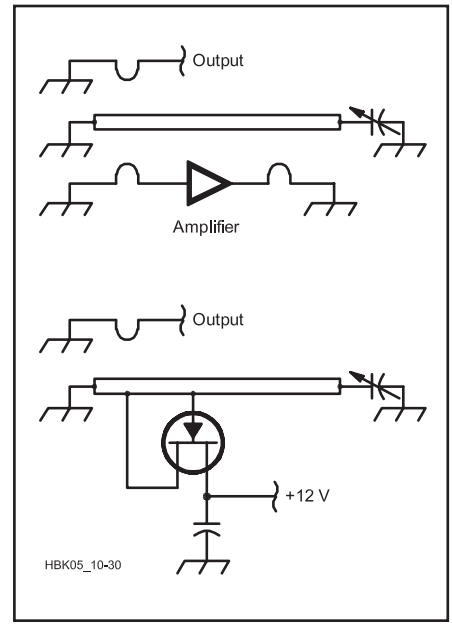


Fig 9.30 — Oscillators that use transmission-line segments as resonators. Such oscillators are more common than many of us may think, as Fig 9.31 reveals.

a pair of coupling loops. The amplifier can be a single bipolar or FET device or one of the monolithic microwave integrated circuit (MMIC) amplifiers. The second circuit is really a Hartley oscillator, and one is made as a test oscillator for the 70 cm band from a 10 cm length of wire suspended 10 mm over an unetched PC board as a ground plane, bent down and soldered at one end, with a trimmer at the other end. The FET is a BF981 dual-gate device used as a source follower.

No free-running oscillator is really stable enough on these bands. Oscillators in this range are almost invariably tuned with tuning diodes controlled by phase-locked-loop synthesizers, which are themselves controlled by a crystal oscillator. This transfers the same stability of the crystal oscillator to the UHF oscillator.

There is one extremely common UHF oscillator that is almost always an undesired accident, being a very common form of spurious VHF/UHF oscillation in circuitry intended to process lower-frequency signals. **Fig 9.31A** shows the circuit in its simplest form. Analyzing this circuit using a comprehensive model of the UHF transistor reveals that the emitter presents an impedance that is small, resistive, and negative to the outside world. If this negative resistance is large enough to more than cancel the effective series resistance of a tank placed on the emitter, oscillation will occur.

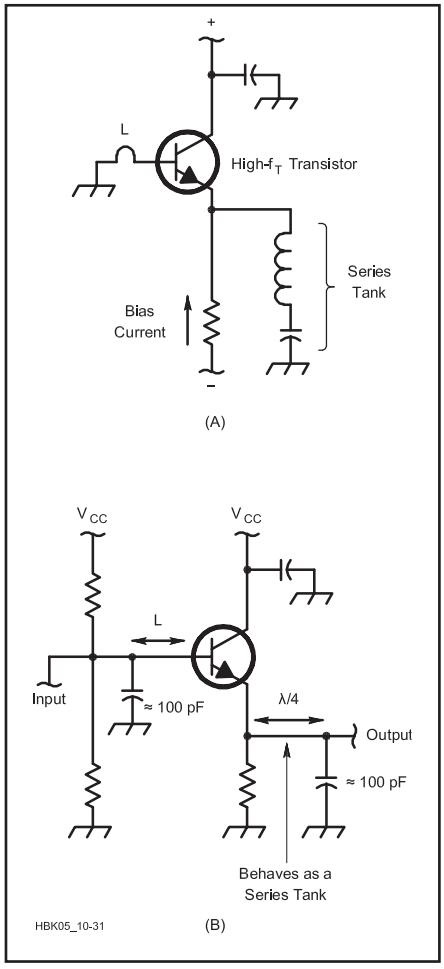


Fig 9.31 — High device gain at UHF and resonances in circuit board traces can result in spurious oscillations even in non-RF equipment.

At UHF your schematic diagram probably will not show a tank circuit is present. But the high frequency transistor will know it is there, since it "sees" all of the stray reactances present in the layout. Fig 9.31B shows a very basic emitter-follower circuit with some capacitance to ground on both the input and output. If the capacitor shunting the input is a distance away from the transistor, the trace to the transistor's base looks like an inductor. The trace at the emitter of the transistor also looks like an inductor, and any nearby conductor will look like a capacitor to that trace (two conductors separated by a dielectric, which here is air and the PC board material). Any intentional capacitors add to this. If the transistor has gain at any frequency where the phasing from all of these stray reactances is right for oscillation (see Barkhausen criteria in previous sections) then oscillation will happen. This circuit is effectively the same as that in Fig 9.31A. This is a good reason to use the lowest-frequency transistor that you can for any application.

Stray reactances do not always have to cause headaches. Indeed you can use them, knowing that they are there. The circuit of Fig 9.31A can be deliberately built as a useful wide-tuning oscillator covering say, 500 MHz to 1 GHz! This circuit is well-suited to construction with printed-circuit inductors. Common FR4 glass-epoxy board is lossy at these frequencies; better performance is achieved by using (the much more expensive) glass-Teflon board. If you can get surplus pieces of this type of material, it has many uses at UHF and microwave, but it is difficult to use as the adhesion between the copper and the substrate can be weak. A high-UHF transistor with a 5 GHz f_T such as the BFR90 is suitable; the base inductor can be 30 mm of 1 mm trace folded into a hairpin shape (inductance, less than 10 nH).

The upshot of this is that there is no longer any branch of electronics where RF design and layout techniques can be ignored safely. A circuit must not just be designed to do what it should do; it must also be designed so that it cannot do what it should not do.

If you have an accidental oscillator, there are three ways of taming such a circuit: adding a small resistor of perhaps 50 to 100 Ω in the collector lead close to the transistor, or adding a similar resistor in the base lead, or by fitting a ferrite bead over the base lead under the transistor. Extra resistors can disturb dc conditions, depending on the circuit and its operating currents. Ferrite beads have the advantage that they can be easily added to existing equipment and have no effect at dc and low frequencies. Beware of some electrically conductive ferrite materials that can short transistor leads! If an HF oscillator uses beads to prevent any risk of spurs (such as shown in Fig 9.15), the beads should be anchored with a spot of adhesive to prevent movement which can cause small frequency shifts. Ferrite beads of Fair-Rite #43 material are especially suitable for this purpose; they are specified in terms of impedance, not inductance. Ferrites at frequencies above their normal usable range become very lossy and can make a lead look not inductive, but like a few tens of ohms, resistive.

9.6.2 Microwave Oscillators

Using conventional PC-board techniques with surface-mount components and extraordinarily careful layout allows the construction of circuits up to 4 GHz or so. Above this, commercial techniques and fancier materials become necessary unless we take the step to the ultimate distributed circuit — the cavity resonator.

Older than stripline techniques and far more amenable to home construction, cavity-based oscillators can give the highest possible performance at microwave frequencies. Air is a very low-loss dielectric with a dielectric constant of 1, so it gives high Q and does not force excessive miniaturization. **Fig 9.32** shows a series of structures used by G. R. Jessop, G6JP, to illustrate the evolution of a cavity from a tank made of lumped components. All cavities have a number of different modes of resonance, the orientation of the

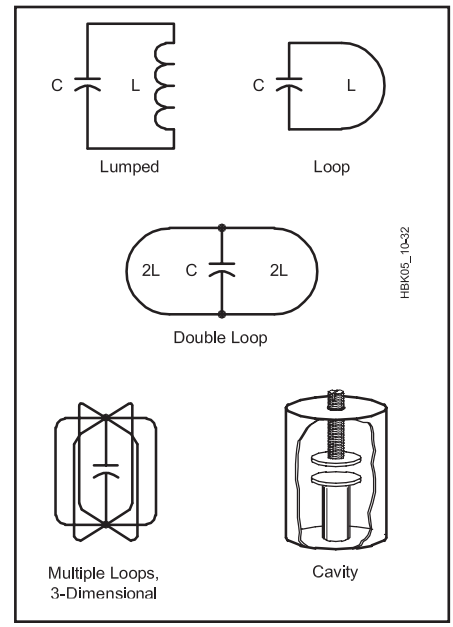


Fig 9.32 — Evolution of the cavity resonator.

currents and fields are shown in **Fig 9.33**. The cavity can take different shapes, but the one shown here has proven to suppress unwanted modes well. The gap need not be central and is often right at the top. A screw can be fitted through the top, protruding into the gap, to adjust the frequency.

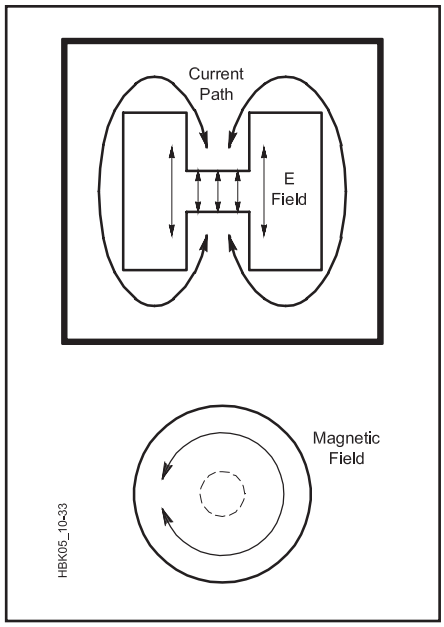


Fig 9.33 — Currents and fields in a cavity.

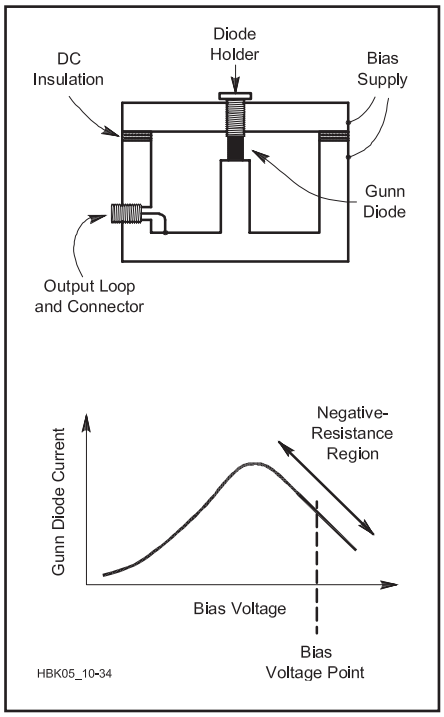


Fig 9.34 — A Gunn diode oscillator uses negative resistance and a cavity resonator to produce radio energy.

SEMICONDUCTOR CAVITY OSCILLATORS

To make an oscillator using a cavity, an amplifier is needed. Gunn and tunnel diodes have regions in their characteristics where their current falls with increasing bias voltage. This is negative resistance. If such a device is mounted in a loop in a cavity and bias is applied, the negative resistance can more than cancel the effective loss resistance of the cavity, causing oscillation. These diodes are capable of operating at extremely high frequencies and were discovered long before transistors were developed that had any gain at microwave frequencies.

A Gunn-diode cavity oscillator is the basis of many of the Doppler radar modules used to detect traffic or intruders and of the Gunnplexer 10 GHz transceiver modules used by amateurs. **Fig 9.34** shows a common configuration. The coupling loop and coax output connector could be replaced with a simple aperture to couple into waveguide or a mixer cavity. **Fig 9.35** shows a transistor cavity oscillator version using a modern microwave transistor, which can be either a FET or bipolar device. The two coupling loops are electrically completed by the capacitance of the feedthrough capacitors.

DIELECTRIC-RESONATOR OSCILLATORS (DRO)

The dielectric-resonator oscillator (DRO) is a very common microwave oscillator, as it is used in the downconverter of satellite TV receivers. The dielectric resonator itself is a ceramic cylinder, like a miniature hockey puck, several millimeters in diameter. The ceramic has a very high dielectric constant, so the surface (where ceramic meets air in an abrupt dielectric mismatch) reflects electromagnetic waves and makes the ceramic body act as a resonant cavity. It is mounted on a substrate and coupled to the active device of the oscillator by a stripline that runs past it. At 10 GHz, a FET made of gallium arsenide (GaAsFET), rather than silicon, is normally used. The dielectric resonator elements are made at frequencies appropriate to mass applications like satellite TV. The setup charge to manufacture small quantities at special frequencies is likely to be prohibitive for the foreseeable future.

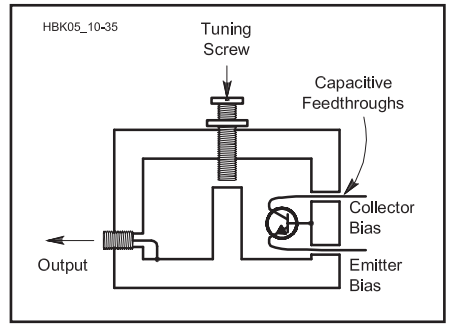


Fig 9.35 — A transistor can also directly excite a cavity resonator.

The challenge with these devices is to devise new ways of using oscillators on industry standard frequencies. Their chief attraction is their low cost in large quantities and compatibility with microwave stripline (microstrip) techniques. Frequency stability and Q are competitive with good cavities, but are inferior to that achievable with a crystal oscillator and chain of frequency multipliers.

YIG TUNED OSCILLATORS (YTO)

The yttrium-iron garnet (YIG) oscillator is a fundamental microwave source with a very wide tuning range and a linear tuning characteristic. Many YIG oscillators can be tuned over more than an octave and some tune more than 5 octaves! They are complete units that appear as heavy blocks of metal with low-frequency connections for power supplies and tuning, and an SMA connector for the RF output. The manufacturer's label usually states the tuning range and often the power supply voltages. This is very helpful because, with new units being very expensive, it is important to be able to identify the characteristics of surplus units. The majority of YTOs operate within the 2 to 18 GHz region, although units down to 500 MHz and up to 40 GHz are occasionally found. At microwave frequencies there is no octave-tunable device that can equal their signal cleanliness and stability. A typical stability for a 3 GHz YTO is less than 1 kHz per second drift. This may seem poor — until we realize that this is 0.33 ppm per second. Still, any YIG application involving narrow-band modulation will require some form of frequency stabilizer.

Nearly all surplus RF spectrum analyzers use YTOs as their first LO. For example, a 0 to 1500 MHz analyzer usually uses a 2 to 3.5 GHz YTO with a 2.0 GHz first IF. To understand the YTO tuning circuits, should there be need for troubleshooting and repair, a basic understanding of YIG oscillators definitely helps.

Fig 9.36 shows the construction of a YIG oscillator. A YTO is based on a YIG sphere that is carefully oriented within a coupling loop. This resonator is connected to a negative-resistance device and the whole assembly is placed between the poles of an electromagnet. Negative-resistance (Gunn) diodes were originally used in these oscillators, but transistor circuits are now essentially universal and use much less power. The support for the YIG sphere often contains a controlled heater to reduce temperature variation. YIG spheres are resonant at a frequency controlled not only by their physical dimensions, but also by any magnetic field around them. Hence the electromagnet: by varying

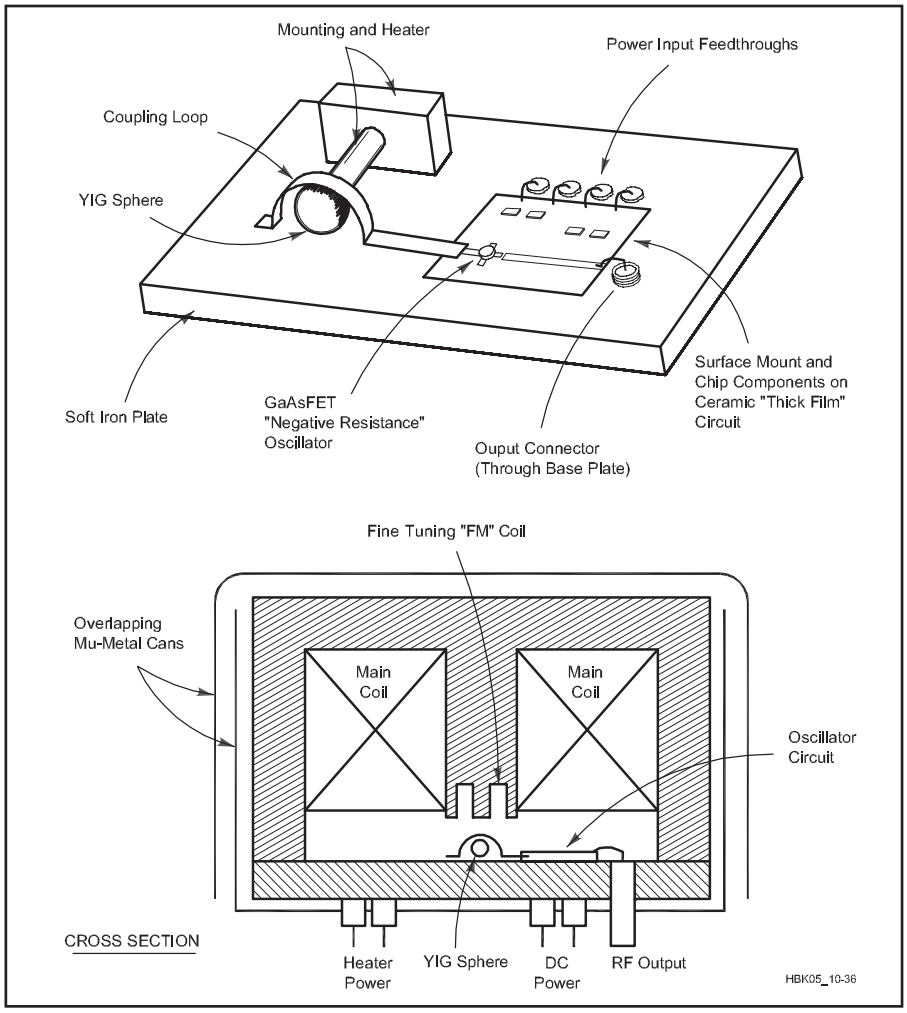


Fig 9.36 — A yttrium-iron-garnet (YIG) sphere serves as the resonator in the sweep oscillators used in many spectrum analyzers.

the current through the electromagnet's windings, a controlled variable magnetic field is applied across the YIG sphere. This tunes the oscillator across a very wide range. The frequency/current relationship can have excellent linearity, typically around 20 MHz/mA.

Magnetically tuned oscillators bring some unique problems with them. The first problem is that magnetic fields, especially at low frequencies, are extremely difficult to shield. Therefore YTO tuning is influenced by any local magnetic fields, causing frequency modulation. The YTO's magnetic core must be carefully designed to be all-enclosing in an attempt at self-shielding, and then one or more nested mu-metal cans are fitted around everything. It is still important to place the YTO away from obvious sources of magnetic fields, like power transformers. Cooling fans are also sources of fluctuating magnetic fields, with some fans generating fields 20 dB than from a well-designed 200 W 50/60-Hz transformer.

The second new problem is that the YTO's internal tuning coil needs significant current from the power supply to create the strong tuning field. This can be eased by adding a permanent magnet as a fixed "bias" field, but the bias shifts as the magnet ages. The main tuning coil still has many turns, and therefore high inductance (often more than 0.1 henrys). Large inductances require a high supply voltage for rapid tuning, with correspondingly high power consumption. The usual compromise is to have dual coils: One with many turns for slow tuning over a wide range, and a second coil with far fewer turns for fast tuning or FM over a limited range. This "FM coil" has a sensitivity around 1% to 2% of the main coil, perhaps 500 kHz/mA.

9.6.3 Klystrons, Magnetrons, and Traveling Wave Tubes

There are a number of thermionic (vacuum-tube) devices that are widely used as amplifiers or fundamental oscillators at microwave frequencies. Standard vacuum tubes (see the **RF Amplifiers** chapter for an introduction to vacuum tubes) work well for frequencies up to hundreds of megahertz. At frequencies higher than this, the amount of time that the electrons take to move between the cathode and the plate becomes a limiting factor. There are several special tubes designed to work at microwave frequencies, usually providing more power than can be obtained from solid-state devices.

Two of the following tubes (klystrons and traveling wave tubes) use the principle of *velocity-modulation* to extract RF energy from an electron beam. The general principles of velocity modulation and basic properties of devices using it are presented in the online tutorial **www.radartutorial.eu/druck/Book5.pdf**. Additional resources are described below.

THE KLYSTRON

The klystron tube uses the principle of velocity modulation of the electrons to avoid transit time limitations. The beam of electrons travels down a metal drift tube that has interaction gaps along its sides. RF voltages are applied to the gaps and the electric fields that they generate accelerate or decelerate the passing electrons. The relative positions of the electrons shift due to their changing velocities, causing the electron density of the beam to vary. This variation of electron beam density is used to perform amplification or oscillation.

Klystron tubes can be relatively large, and they can easily provide hundreds of watts to hundreds of kilowatts of microwave power. These power levels are useful for UHF broadcasting and particle accelerators, for example. Unfortunately klystrons have relatively narrow bandwidths, and may not be re-tunable for operation on amateur frequencies. A video titled "How a Klystron Tube Works" can be found at the YouTube online video service and a detailed history and tutorial is available at **www.slac.stanford.edu/cgi-wrap/getdoc/slac-pub-7731.pdf**.

THE MAGNETRON

The magnetron tube is an efficient oscillator for microwave frequencies. Magnetrons are most commonly found in microwave ovens and high-powered radar equipment. The anode of a magnetron is made up of a number of coupled resonant cavities that surround the cathode. The applied magnetic field causes the electrons to rotate around the cathode and the energy that they give off as they approach the anode adds to the RF electric field. The RF power is obtained from the anode through a vacuum window.

Magnetrons are self-oscillating with the frequency determined by the construction of their anodes; however, they can be tuned by coupling either inductance or capacitance to the resonant anode. The range of frequencies depends on how fast the tuning must be ac-

complished. The tube may be tuned slowly over a range of approximately 10% of the center frequency. If faster tuning is necessary, such as is required for frequency modulation, the range decreases to about 5%.

Excellent drawings showing how magnetrons work are available at **hyperphysics.phy-astr.gsu.edu/hbase/waves/magnetron.html** and a thorough introduction for the interested reader is can be downloaded from **www.cpii.com/docs/related/2/Mag%20tech%20art.pdf**.

THE TRAVELING WAVE TUBE

A third type of tube operating in the microwave range is the traveling wave tube (TWT). For wide-band amplifiers in the microwave range this is the tube of choice. Either permanent magnets or electromagnets are used to focus the beam of electrons that travels through the TWT. This electron beam passes through a helical slow-wave structure, in which electrons are accelerated or decelerated, providing density modulation due to the applied RF signal, similar to that in the klystron. The modulated electron beam induces voltages in the helix that provides an amplified output signal whose gain is proportional to the length of the slow-wave structure. After the RF energy is extracted from the electron beam by the helix, the electrons are collected and recycled to the cathode. Traveling wave tubes can often be operated outside their designed frequencies by carefully optimizing the beam voltage.

9.7 Frequency Synthesizers

Like many of our modern technologies, the origins of frequency synthesis can be traced back to WW II. The driving force was the desire for stable, rapidly switchable and accurate frequency control technology to meet the demands of narrow-band, frequency-agile HF communications systems without resorting to large banks of switched crystals. Early synthesizers were cumbersome and expensive, and therefore their use was limited to only the most sophisticated communications systems. With the help of the same technologies that have taken computers from room-sized to now fitting into the palms of our hands, frequency synthesis techniques have become one of the most enabling technologies in modern communications equipment.

Every communications device manufactured today, be it a handheld transceiver, cell phone, pager, AM/FM entertainment radio, scanner, television, HF communications equipment, or test equipment, contains a frequency synthesizer. Synthesis is the technology that allows an easy interface with both computers and microprocessor controllers. It provides amateurs with many desirable features, such as the feel of an analog knob with precision 10-Hz frequency increments, wide-band accuracy and stability determined by a single precision crystal oscillator, frequency memories, and continuously variable precision frequency splits. Now reduced in size to small integrated circuits, frequency synthesizers have long replaced the cumbersome chains of frequency multipliers and filters in VHF, UHF and microwave equipment, giving rise to the highly portable communications devices we use today. Frequency synthesis has also had a major impact in lowering the cost of modern equipment, particularly by reducing manufacturing complexity.

Frequency synthesizers are categorized in two general types: *direct synthesizers*, where the output signal is the result of operations directly performed on the input signal; and *indirect synthesizers*, where selected characteristics of the input signal are transferred onto a separately generated output signal. One defining feature of any direct synthesizer is that no feedback is used, so there is never any dynamic stability problem. Indirect synthesizers always include feedback control loops, so dynamic stability is a major design concern.

Direct synthesizers include the major techniques of *direct analog synthesis* (DAS) and *direct digital synthesis* (DDS). Direct analog synthesizers consist primarily of frequency multipliers, frequency dividers, mixers, and filters. DAS is very useful for generating small numbers of signals, with widely spaced frequencies, from a reference oscillator. DAS is particularly useful when more than one output signal is required at the same time. Direct digital synthesizers are essentially dedicated microprocessors that have one program, to create an output signal waveform given a desired frequency (in digital form) using the applied reference signal. Unlike DAS, the output frequencies from a DDS can easily be separated by millihertz (0.001 Hz) while keeping all of the stability of the reference oscillator. Both being direct techniques, neither DAS nor DDS use feedback control loops, so switching from one frequency to another happens in nanoseconds.

Indirect synthesizers include the major techniques of frequency-locked loops (FLL) and phase-locked loops (PLL). The whole idea behind any indirect synthesizer is to transfer characteristics of one signal onto another separate signal. An FLL transfers only frequency characteristics of the input signal onto the output signal. Major FLL applications used by radio amateurs include *automatic frequency control* (AFC) loops and tone decoders. PLLs are more precise because not only frequency characteristics of the reference oscillator, but also its phase characteristics, are transferred to the oscillator generating the output signal. There are two main application classes in which PLLs find wide use. The first is as a *frequency generator*, where we call it a *frequency synthesizer*. In transmitters this synthesizer may also include modulation, particularly for FM and FSK signals. The second PLL application class is as an angle (frequency or phase) demodulator, where we call it a *tracking demodulator* or *synchronizer*. Tracking demodulators used in deep space communication and clock recovery used in digital communication are major applications today.

It is curious to note that using modern digital circuitry, it actually is easier to make a PLL than an FLL. This turns out to be fortuitous! This section will focus on the PLL used as a frequency synthesizer. For readers interested in PLL use as a demodulator or as a synchronizer, there are many textbooks available that discuss these applications in great detail.

9.7.1 Phase-Locked Loops

As mentioned above, the PLL is a key component of any indirect synthesizer. The sidebar "An Introduction to Phase-Locked Loops" provides an overview of this technology. This section presents a detailed discussion of design and performance topics of PLL synthesizers and the circuits used to construct them. The digital logic circuits and terms included in this discussion are covered in the **Digital Basics** chapter.

ARCHITECTURE

The principle of the PLL synthesizer is straightforward. A tunable oscillator is first built to cover the required output frequency range; then the PLL system is constructed around this oscillator to keep it tuned to the desired frequency. This is done by continuously comparing the phase of the oscillator to a stable reference, such as a crystal oscillator, and using the result to steer tuning of the oscillator. If the oscillator frequency is too high, the phase of its output will start to lead that of the reference by an increasing amount. This is detected and is used to decrease the frequency of the oscillator. Too low a frequency causes an increasing phase lag, which is detected and used to increase the frequency of the oscillator. In this way,

An Introduction to Phase-Locked Loops

By Jerry DeHaven, WAØACF

Phase locked loops (PLLs) are used in many applications from tone decoders, to stabilizing the pictures in your television set, to demodulating your local FM station or 2 meter repeater. They are used for recovering weak signals from deep space satellites and digging out noisy instrumentation signals. Perhaps the most common usage for PLLs in Amateur Radio is to combine the variability of an LC oscillator with the long term stability and accuracy of a crystal oscillator in PLL frequency synthesizers. Strictly speaking a PLL is not necessarily a frequency synthesizer and a frequency synthesizer is not necessarily a PLL, although the terms are used interchangeably.

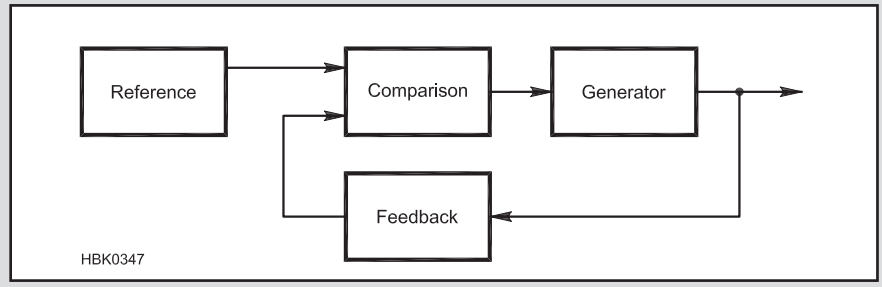


Fig 9.A3 — Simple control loop. The Comparison block creates a control signal for the Generator by comparing the output of the Reference and Feedback blocks.

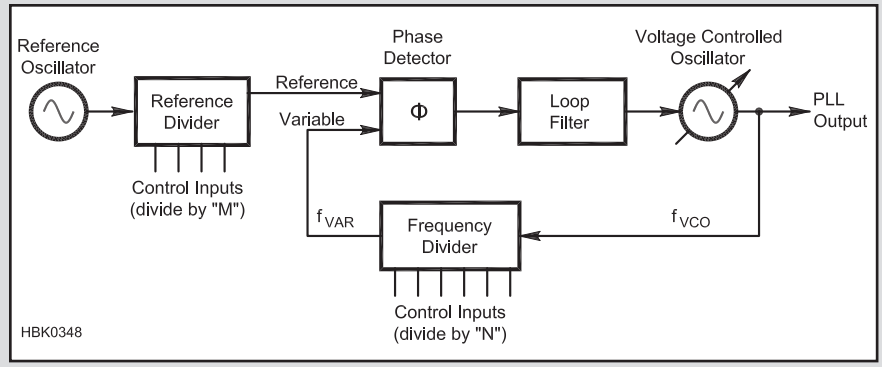


Fig 9.A4 — PLL frequency synthesizer block diagram. The PLL is locked when the frequency PLL Output / N is the same as that of the Reference Oscillator / M.

PLL Block Diagram

The block diagram in **Fig 9.A3** shows a basic *control loop*. An example of a control loop is the furnace or air conditioning system in your house or the cruise control in your car. You input a desired output and the control loop causes the system output to change to and remain at that desired output (called a *setpoint*) until you change the setpoint. Control loops are characterized by an input, an output and a feedback mechanism as shown in the simple control loop diagram in Fig 9.A3. The setpoint in this general feedback loop is called the *reference*.

In the case of a heating system in your house, the reference would be the temperature that you set at the thermostat. The feedback element would be the temperature sensor inside the thermostat. The thermostat performs the comparison function as well. The generator would be the furnace which is turned on or off depending on the output of the comparison stage. In general terms, you can see that the reference input is controlling the output of the generator.

Like other control loops, the design of a PLL is based on feedback, comparison and correction as shown in Fig 9.A3. In this section we will focus on the concepts of using a phase locked loop to generate (synthesize) one or more frequencies based on a single reference frequency.

In a typical PLL frequency synthesizer there are six basic functional blocks as shown in **Fig 9.A4**. The PLL frequency synthesizer block diagram is only slightly more complicated than the simple control loop diagram, so the similarity should be evident. After a brief description of the function of each block we will describe the operational behavior of a PLL frequency synthesizer.

In Fig 9.A4, the general control loop is implemented with a bit more detail. The Reference block is composed of the Reference Oscillator and the Reference Divider. The Comparison block consists of the Phase Detector and Loop Filter. The Generator is replaced by the Voltage-Controlled Oscillator (or VCO) and the Feedback block is replaced by the Frequency Divider. The two signals being compared are both frequencies; the reference frequency and variable frequency signals. The output of the Loop Filter is made up of dc and low frequency ac components that act to change the VCO frequency. The output of the PLL is an integer multiple of the reference frequency (the output of the Reference Divider). It is probably not obvious why, but read on to find out!

The Reference Oscillator — The reference oscillator is usually a crystal oscillator with special attention paid to thermal stability and low mechanical and electronic noise. The main function of the reference oscillator is to generate a stable frequency for the PLL. Let us make a distinction between the reference oscillator frequency and the reference frequency. The output of the reference oscillator is at the crystal frequency, say 5.000 MHz. The choice of the actual crystal frequency depends on the PLL design, the availability of another oscillator in the radio, the avoidance of spurious responses in the receiver, and so on.

The *reference frequency* is the output of the reference (crystal) oscillator divided by the integer M to a relatively low frequency, say 10 kHz. In this case, 10 kHz is the reference frequency. The reference frequency equals the step size between the PLL output frequencies. In this simple example the crystal frequency can be any frequency that is an integer multiple of 10 kHz and within the operating range of the Reference Divider.

The Phase Detector — There are many types of phase detectors, but for now let us consider just a basic mixer, or a multiplier. The phase detector has two inputs and one output. In its simplest form, the output of the phase detector is a dc voltage proportional to the phase difference between the two inputs. In practice, a phase detector can be built using a diode double-balanced mixer or an active multiplier.

The output of the mixer consists of products at many frequencies both from multiplication and from nonlinearities. In this application, the desired output is the low frequency and dc terms so all of the RF products are

[continued on next 2 pages]

terminated in a load and the low frequency and dc output is passed to the PLL loop filter.

When the PLL is locked — meaning that the output frequency is the desired multiple of the reference frequency — the phase detector output is a steady dc voltage somewhere between ground and the PLL power supply voltage. When the PLL is commanded to change to another frequency, the phase detector output will be a complex, time-varying signal that gradually settles in on its final value.

The Loop Filter —The loop filter is a low-pass filter that filters the output of the phase detector. The loop filter can be a simple resistor-capacitor (RC) low-pass filter or an active circuit built with bipolar transistors or operational amplifiers. The cutoff frequency of the low pass filter is on the order of 100 Hz to 10 kHz. Although the frequencies involved are dc and low audio frequencies the design of the loop filter is critical for good reference suppression and low noise performance of the PLL frequency synthesizer.

The output of the loop filter is a dc voltage that "steers" the following stage, the Voltage Controlled Oscillator. The dc value can vary over a substantial portion of the PLL power supply. For example, if the loop filter runs off a 9 V power supply you may expect to see the output voltage range from about 2 V to 7 V depending on the VCO frequency range.

The Voltage Controlled Oscillator (*VCO*)—The VCO is probably the most critical stage in the PLL frequency synthesizer. This stage is the subject of many conflicting design goals. The VCO must be electrically tunable over the desired frequency range with low noise and very good mechanical stability. Ideally, the output frequency of the VCO will be directly proportional to the input control voltage. A key characteristic is the *VCO constant* or *tuning gain*, usually expressed in MHz per volt (MHz/V). The VCO has one input, the dc voltage from the loop filter, and usually two outputs; one for the PLL output, the other driving the feedback stage — the frequency divider.

The Frequency Divider — The VCO frequency divider that acts as the feedback block is a programmable frequency divider or counter. The division ratio N is set either by thumbwheel switches, diode arrays or a microprocessor. The input to the divider is the VCO output frequency. The output of the divider is the VCO output frequency divided by N.

When the PLL is unlocked, such as when the PLL is first turned on, or commanded to change to another frequency, the frequency divider's output frequency will vary in a nonlinear manner until the PLL locks. Under locked conditions, the divider's output frequency (VCO Output / N) is the same as the reference frequency (Reference Oscillator / M).

The function of the frequency divider as the feedback element is easier to understand with an example. Let's assume that the desired PLL output frequency is 14.000 MHz to 14.300 MHz and it should change in steps of 10 kHz (0.010 MHz). A step size of 10 kHz means that the reference frequency must be 10 kHz. There are 31 output frequencies available — one at a time, not simultaneously. (Don't forget to count 14.000 MHz.) Let us arbitrarily choose the reference oscillator as a 5.000 MHz crystal oscillator. To generate the 10 kHz reference frequency, the reference divider must divide by M = 500 = 5.000 MHz / 0.010 MHz. (Use the same units, don't divide MHz by kHz.)

To generate a matching 10 kHz signal from the VCO output frequency, the Frequency Divider (the feedback stage) must be programmable to divide by N = 1400 to 1430 = 14.000 to 14.300 MHz / 0.010 MHz. The reference divisor (M = 500) is fixed, but the Frequency Divider stage needs to be programmable to divide by N = 1400 to 1430 in steps of 1. In this way, the output frequency of the PLL is compared and locked to the stable, crystal-generated value of the reference frequency.

PLL Start-up Operation

Let's visualize the PLL start-up from power on to steady state, visualizing in sequence what each part of the PLL is doing. Some portions of the loop will act quickly, in microseconds; other parts will react more slowly, in tens or hundreds of milliseconds.

The reference oscillator and its dividers will probably start oscillating and stabilize within tens of microseconds. The reference oscillator divider provides the reference frequency to one input of the phase detector.

The VCO will take a bit longer to come up to operation because of extensive power supply filtering with high-value capacitors. The VCO and the programmable dividers will probably reach full output within a few hundred microseconds, although the VCO will not yet be oscillating at the correct frequency.

At this point the phase detector has two inputs but they are at different frequencies. The mixer action of the phase detector produces a beat note at its output. The beat note, which could be tens or hundreds of kHz, is low-pass filtered by the PLL loop filter. That low-pass filter action averages the beat note and applies a complicated time-varying ac/dc voltage to the VCO input.

Now the VCO can begin responding to the control voltage applied to its input. An important design consideration is that the filtered VCO control signal must steer the VCO in the correct direction. If the polarity of the control signal is incorrect, it will steer the VCO *away* from the right frequency and the loop will never lock. Assuming correct design, the control voltage will begin steering the VCO in such a direction that the VCO divider frequency will now get closer to the reference frequency.

With the phase detector inputs a little bit closer in frequency, the beat note will be lower in frequency and the low pass filtered average of the phase detector output will change to a new level. That new control voltage will continue to steer the VCO in the right direction even closer to the "right" frequency. With each successive imaginary trip around the loop you can visualize that eventually a certain value of VCO control voltage will be reached at which the VCO output frequency, when divided by the frequency divider, will produce zero frequency difference at the inputs to the phase detector. In this state, the loop is *locked*. Once running, the range over which a PLL can detect and lock on to a signal is its *capture range*.

PLL Steady-state Operation

When the divided-down VCO frequency matches the reference frequency, the PLL will be in its steady-state condition. Since the comparison stage is a phase detector, not just a frequency mixer, the control signal from the loop filter to the VCO will act in such a way that maintains a constant relationship between the *phase* of the reference frequency and the frequency divider output. For example, the loop might stabilize with a 90° difference between the inputs to the phase detector. As long as the phase difference is constant, the reference frequency and the output of the frequency divider (and by extension, the VCO output) must also be the same.

As the divisor of the frequency divider is changed, the loop's control action will keep the divided-down VCO output phase locked to the reference frequency, but with a phase difference that gets closer to 0 or 180°, depending on which direction the input frequency changes. The range over which the phase difference at the phase detector's input varies between 0° and 180° is the widest range over which the PLL can keep the input and VCO signals locked together. This is called the loop's *lock range*.

If the divisor of the frequency divider is changed even further, the output of the loop filter will actually start to move in the opposite direction and the loop will no longer be able to keep the VCO output locked to the reference frequency and the loop is said to be *out of lock* or *lost lock*.

Loop Bandwidth

Whether you picture a control loop

such as the thermostat in your house, the speed control in your car or a PLL frequency synthesizer, they all have "bandwidth," that is, they can only respond at a certain speed. Your house will take several minutes to heat up or cool down, your car will need a few seconds to respond to a hill if you are using the speed control. Likewise, the PLL will need a finite time to stabilize, several milliseconds or more depending on the design.

This brings up the concept of *loop bandwidth*. The basic idea is that disturbances outside the loop have a low-pass characteristic up to the loop bandwidth, and that disturbances inside the loop have a high-pass characteristic up to the loop bandwidth. The loop bandwidth is determined by the phase detector gain, the loop filter gain and cutoff frequency, the VCO gain and the divider ratio. Loop bandwidth and the phase response of the PLL determine the stability and transient response of the PLL.

PLLs and Noise

Whether the PLL frequency synthesizer output is being used to control a receiver or a transmitter frequency, the spectral cleanliness of the output is important. Since the loop filter output voltage goes directly to the VCO, any noise or spurious frequencies on the loop filter output will modulate the VCO causing FM sidebands. On your transmitted signal, the sidebands are heard as noise by adjacent stations. On receive, they can mix with other signals, resulting in a higher noise floor in the receiver.

A common path for noise to contaminate the loop filter output is via the power supply. This type of noise tends to be audible in your receiver or transmitter audio. Use a well-regulated supply to minimize 120-Hz power supply ripple. Use a dedicated low-power regulator separate from the receiver audio stages so you do not couple audio variations from the speaker amplifier into the loop filter output. If you have a computer / sound card interface, be careful not to share power supplies or route digital signals near the loop filter or VCO.

A more complicated spectral concern is the amount of reference frequency feed-through to the VCO. This type of spurious output is above the audio range (typically a few kHz) so it may not be heard but it will be noticed, for example, in degraded receiver adjacent channel rejection. In the example above, Fig 9.A4, the reference frequency is 10 kHz. High amounts of reference feed-through on the VCO control input will result in FM sidebands on the VCO output.

Loop filter design and optimization is a complicated subject with many trade-offs. This subject is covered in detail in the PLL references, but the basic trade-off is between loop bandwidth (which affects the speed at which a PLL can change frequency and lock) and reference rejection. Improved phase detectors can be used which will minimize the amount of reference feed-through for the loop filter to deal with. Another cause of high reference sidebands is inadequate buffering between the VCO output and the frequency divider stage.

One indication of PLL design difficulty is the spread of the VCO range expressed either in percent or in octaves. It is fairly difficult to make a VCO that can tune over one octave, a two-to-one frequency spread. Typically, the greater the spread of the VCO tuning range, the worse the noise performance gets. The conflicting design requirements can sometimes be conquered by trading off complexity, cost, size, and power consumption.

A common source of noise in the VCO is microphonics. Very small variations in capacitance can frequency modulate the VCO and impose audible modulation on the VCO output. Those microphonic products will be heard on your transmit audio or they will be superimposed on your receiver audio output. Under vibration, an air-wound inductor used in a VCO can move slightly relative to a metal shield for example. A common technique to minimize microphonics is to cover the sensitive parts with wax, Q-Dope, epoxy or a silicone sealer. As with the loop filter use a well-filtered, dedicated regulator for the VCO to minimize modulation by conducted electrical noise.

Types of PLLs

One of the disadvantages of a single loop PLL frequency synthesizer is that the reference frequency determines the step size of the output frequency. For two-way radio and other systems with fixed channel spacing that is generally not a problem. For applications like amateur radio CW and SSB operation, tuning steps smaller than 10 Hz is almost a necessity. Like so many design requirements, there are trade-offs with making the reference frequency smaller and smaller. Most evident is that the loop filter bandwidth would have to keep getting lower and lower to preserve spectral cleanliness and loop stability. Because low frequency filters take longer to settle, a single-loop PLL with a 10 Hz loop bandwidth would take an unacceptably long time to settle to the next frequency.

Creative circuit architectures involving two or more PLLs operating together achieve finer tuning increments with only moderate complexity. Once you understand the basics of a single loop PLL you will be able to learn and understand the operation of a multi-loop PLL.

the oscillator is locked into a fixed-phase relationship with the reference, which means that their frequencies are held exactly equal.

A representative block diagram of a PLL is shown in **Fig 9.37**. Measurement of any error in the output signal phase is made by the *phase detector* (PD). The measured error is supplied to the *loop filter* and *loop amplifier* which work together to tune the *voltage controlled oscillator* (VCO) just enough to make the error go to zero. The phase detector determines the actual frequency and phase of the VCO through the *feedback divider* (N). The phase detector operates at a lower frequency which is a sub-multiple of both the crystal oscillator frequency reference (f_{XO}) and the output frequency (f_{OUT}). This lower frequency is correctly called the PLL *reference frequency* (f_{REF}) because it sets the operating conditions of the PLL.

There is unfortunate history about the term reference frequency. It is often used to refer to both the operating frequency of the phase detector and to the frequency reference applied to the PLL. If the *reference divider* (R) is not present then of course these two frequencies are the same. But in general, the reference divider is present and these frequencies are different. Ambiguity here is widespread and a big problem, even today many decades into the widespread use of PLLs. We must be very careful in the words we choose to use!

FREQUENCY RESOLUTION (STEP SIZE)

Frequency of the output signal can be easily changed by changing the divide ratio of the feedback divider. For example if the reference frequency (at the phase detector!) is 100 kHz and the output frequency is 147.5 MHz, the feedback divider number must be N = 1475. If we changed the value of N to 1474, the frequency at the output of the feedback divider becomes 100.068 kHz. The phase detector notices that the frequency of the VCO is too high, and "tells" the loop filter to reduce the frequency of the VCO until the frequency out of the feedback divider becomes exactly 100.000 kHz. This will happen when the VCO is retuned to a frequency of 147.4 MHz.

By changing the value of N by 1, we have just tuned the frequency synthesizer by its smallest available step. This is called the *frequency resolution* of the synthesizer, or equivalently the synthesizer *step size*. Here we note that this step size is (147.5 – 147.4) = 0.1 MHz. It is no accident that this frequency is exactly equal to the PLL reference frequency f_{REF}. This result is an important reason to avoid all ambiguity in the term "reference frequency." f_{REF} is equal to the synthesizer output frequency step size.

There certainly are applications where we want the step size to be a small number, say 10 Hz. You might guess — correctly — that there are problems in building a PLL synthe-

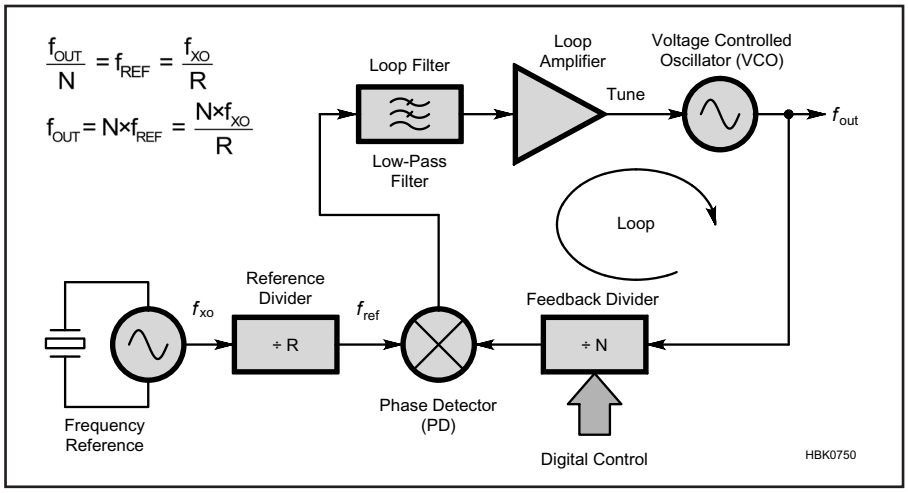


Fig 9.37 — A basic phase-locked-loop (PLL) synthesizer acts to keep the divided-down signal from its voltage-controlled oscillator (VCO) phase-locked to the divided-down signal from its reference oscillator. Fine tuning steps are therefore possible without the complication of direct synthesis.

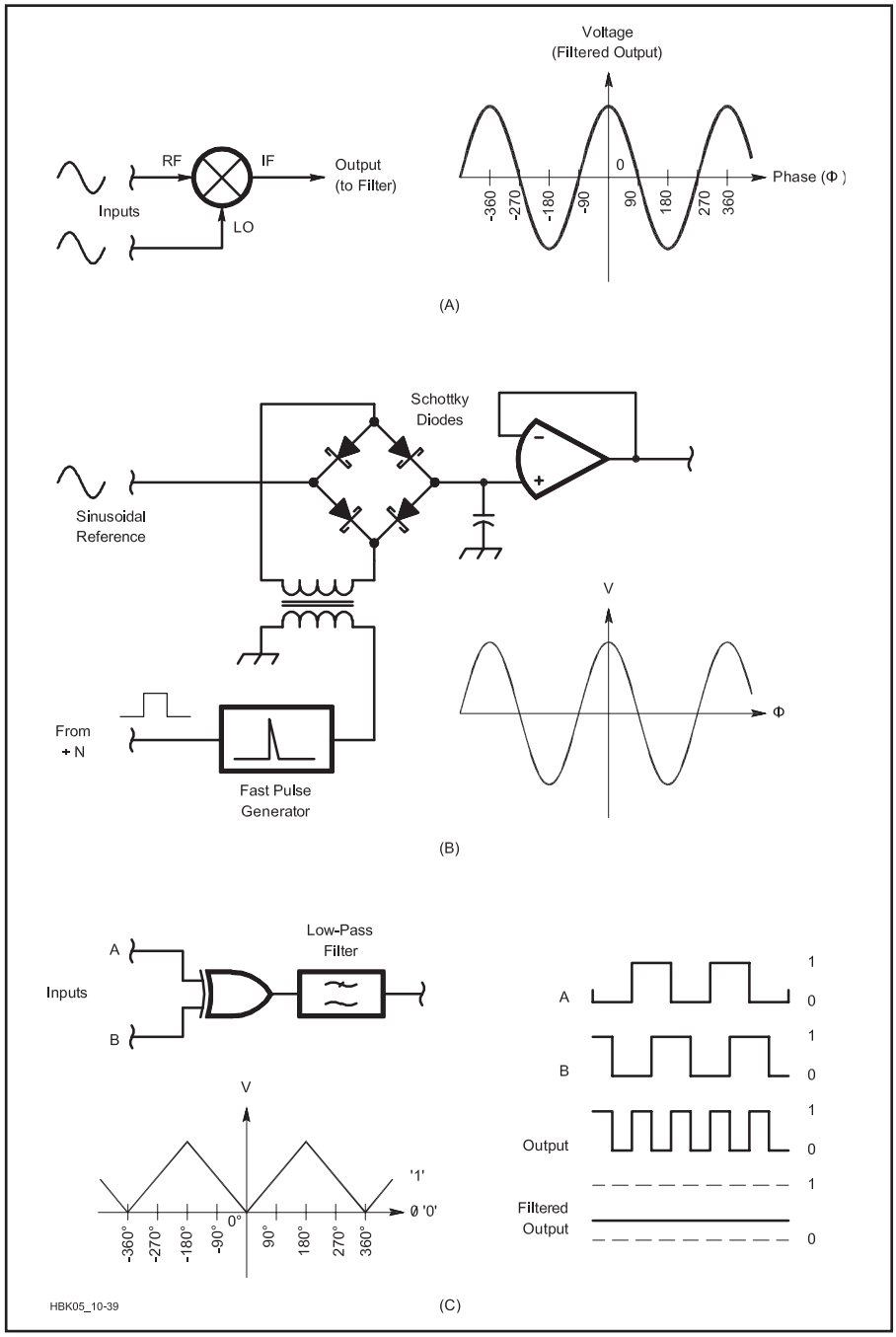


Fig 9.38 — Simple phase detectors: a mixer (A), a sampler (B) and an exclusive-OR gate (C).

sizer for a very low f_{REF}. The usual solution is to combine multiple PLLs with some DAS techniques to get around these problems.

DYNAMIC STABILITY AND LOOP BANDWIDTH

Because feedback control is required to transfer the frequency and phase characteristics from the crystal oscillator onto the VCO, all of the stability problems inherent in feedback control apply to PLL design. If the gain and phase responses are not well designed the PLL can oscillate. In this case instead of getting the stability transfer we want, the output is essentially a frequency modulated signal spread across the entire tuning bandwidth of the synthesizer — clearly a very bad thing. How to perform this design is discussed in section 9.7.2.

For the moment let us assume that our PLL dynamics are properly designed. One other characteristic of feedback control is now important: how fast can the output frequency be changed from one value to another? This is controlled by the *loop bandwidth* of the PLL. For practical reasons the loop bandwidth should be less than 5% of f_{REF}. Using the example above in which f_{REF} = 100 kHz, the loop bandwidth we design for cannot exceed 5 kHz. To answer our question, we can use the rule of thumb that in a well-designed loop, the settling time should be between 1 and 2 times the reciprocal of the loop bandwidth. For a 5 kHz loop bandwidth the settling time should not exceed 2/5000 = 400 μs. We can begin to see one problem with PLL design if f_{REF} is very small: To get a 1 kHz step size from a PLL synthesizer the maximum loop bandwidth available is 50 Hz. This is impractically small.

This loop bandwidth also influences how we can modulate our PLL synthesizer in an FM transmitter. Imagine now that we apply a very small amount of FM to the reference oscillator f_{XO}. The amount of deviation will be amplified by N/R — but this is true only for low modulating frequencies. If the modulating frequency is increased, the VCO has to change frequency at a higher rate. As the modulating frequency continues to increase, eventually the VCO has to move faster than

the available *settling time*. The PLL now acts as a low-pass filter, reducing the available deviation from higher modulating frequencies. The cut-off frequency of this PLL low-pass action is equal to this same loop bandwidth.

PLL COMPONENTS

Let us continue our discussion of phase-locked loop synthesizers by examining the role of each of the component pieces of the system. They are the phase detector, the VCO, the dividers (with possible prescalers), the loop filter, and of course the reference oscillator.

Phase Detectors

Phase detection is the key operation in any PLL. Remembering that we are making a phase locked loop, what we really need is not *absolute* phase measurement but a *relative* phase measurement. We need to know only how the phase of the VCO output signal f_{OUT} is changing with respect to the phase of the crystal reference f_{XO}.

As usual, there are both analog and digital circuit techniques available to perform phase detection. For frequency synthesizer design the analog techniques are seldom used. Analog phase detectors are used only in receiver and demodulator applications. There are two that sometimes still appear in ham equipment, the multiplier/mixer of **Fig 9.38A** and the sampling phase detector shown in Fig 9.38B.

The mixer is a very low noise device when used as a phase detector, which explains why it is not yet completely gone from synthesizer design. It remains only in PLL designs where f_{REF} is very high, greater than 10-100 MHz. The main reason for this is that a PLL using a mixer for the PD is subject to a phenomenon called *false lock*, where the PLL may act like it is locked even though it really isn't. Detecting and eliminating a false lock condition is much easier to do at higher frequencies. The sampling phase detector is now used only in synthesizers with output frequencies in the high microwave region, typically well above 10 GHz. The gain of this sampling circuit is very low, so it is used only if there is no viable alternative.

The most widely used digital phase detector is the exclusive-OR (XOR) gate shown in Fig 9.38C. (See the **Digital Basics** chapter for XOR gate operation.) If inputs A and B in Fig 9.38C are almost in phase, the output will be low most of the time, and its average filtered value will be close to the logic 0 level. If inputs A and B are almost in phase opposition, the output will be high most of the time, and its average voltage will be close to logic 1. The average voltage is near its mid-value when the inputs are shifted in phase by 90 degrees. In this respect the XOR gate is much like the analog mixer. To achieve this circuit's full output-voltage range, it's important that the reference and VCO signals at its input have a 50% duty cycle.

Phase-Frequency Detector

One problem common to *all* phase detectors is the possibility of false lock. This happens because the output of any phase detector can have an average value of zero even when the frequencies at its inputs are not equal. This is a very serious problem that requires any PLL using them to have additional circuitry to serve as an acquisition aid. If the PLL

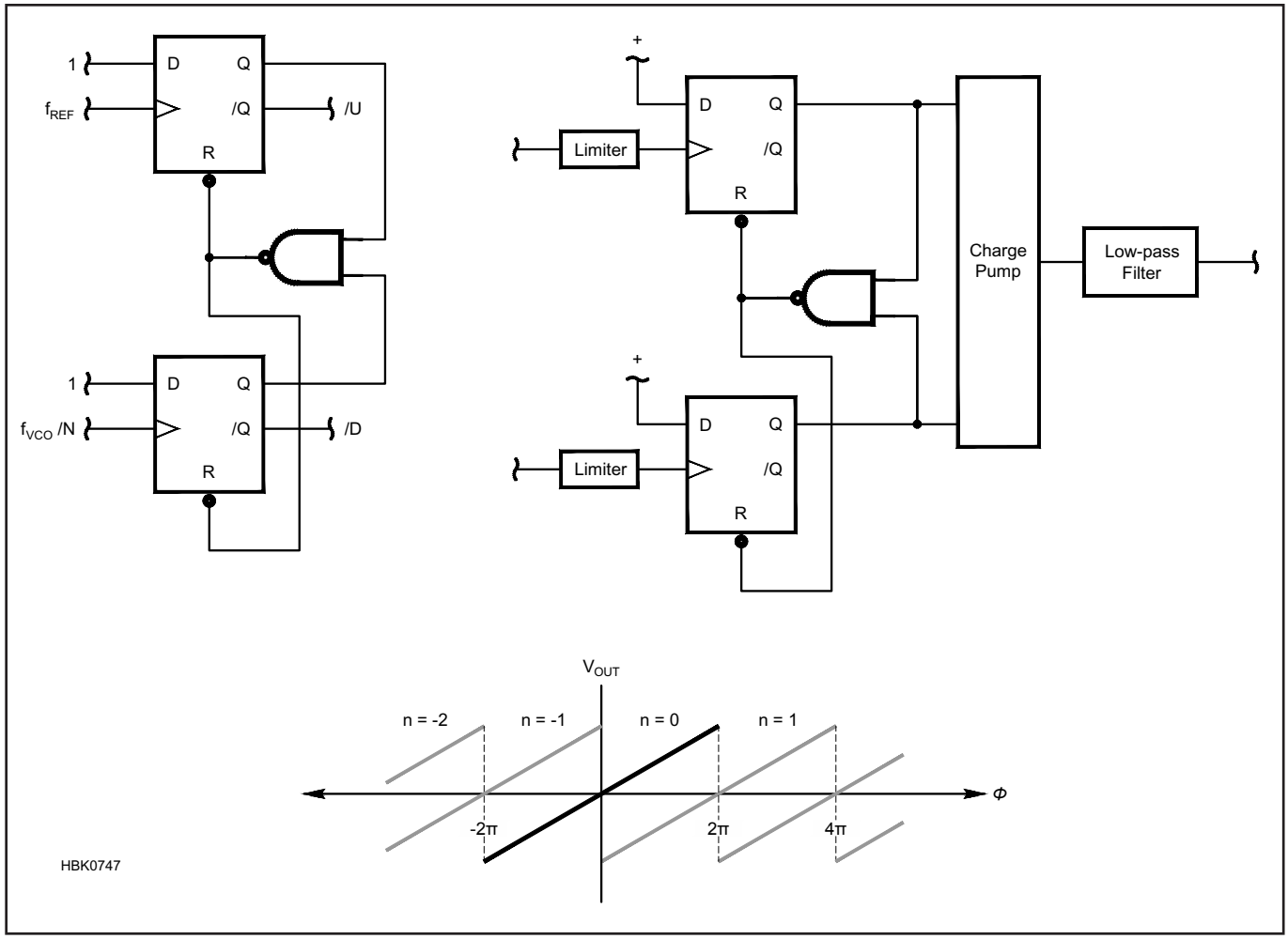


Fig 9.39 — The phase frequency detector (PFD) makes a measurement of the time difference between two rising edges of the input signals.

tries to settle when the PD inputs are not at the same frequency, this acquisition aid must prod the PLL to keep moving toward the true lock frequency. Such acquisition aids are not needed when a *phase-frequency detector* (PFD) is used.

The benefit of the PFD is that if the input signals are at different frequencies, even if they are at very different frequencies, the output is never zero. The PFD output always produces a dc shift in the direction the PLL needs to move until the lock condition is achieved. No acquisition aids are ever needed. This alone is enough to explain its nearly universal adoption today.

As seen in **Fig 9.39A**, the PFD is a simple digital circuit. This also helps make it attractive to use in this era of CMOS integrated circuits. Other designs for the PFD exist, but they all follow the logic shown in Fig 9.39A. Of particular importance is that the PFD has two outputs.

The PFD operates by measuring the time difference between the rising edges of the reference signal and the divided VCO. The first signal to arrive sets its flip-flop. The second edge to arrive also sets its flip-flop, which immediately causes both flip-flops to be reset, ready for the next set of signal edges. By operating at high speed, the PFD is very sensitive to phase differences between the input signals. The PFD does require an equal number of edges for each signal, so it is not useful when the signals have varying numbers of edges, such in a receiver's demodulator or a synchronizer.

If the VCO frequency is too low only the /U output is active, causing the loop filter to raise the VCO frequency. On the other hand, when the VCO frequency is high only the /D output is active, causing the loop filter to lower the VCO frequency. It is interesting to note that unlike the mixer and XOR phase detectors, which require the inputs to be in phase quadrature, the PFD locks when the input signals are in exact phase alignment.

Being an edge triggered circuit, PFD operation is essentially independent of input signal duty cycle. This eliminates the need for input waveform processing. If the input frequencies are different, the time differences measured by the PFD will be either constantly increasing or decreasing. As a result only one of the PFD output signals will be active, informing the PLL unambiguously which way to correct the controlled source to achieve phase lock.

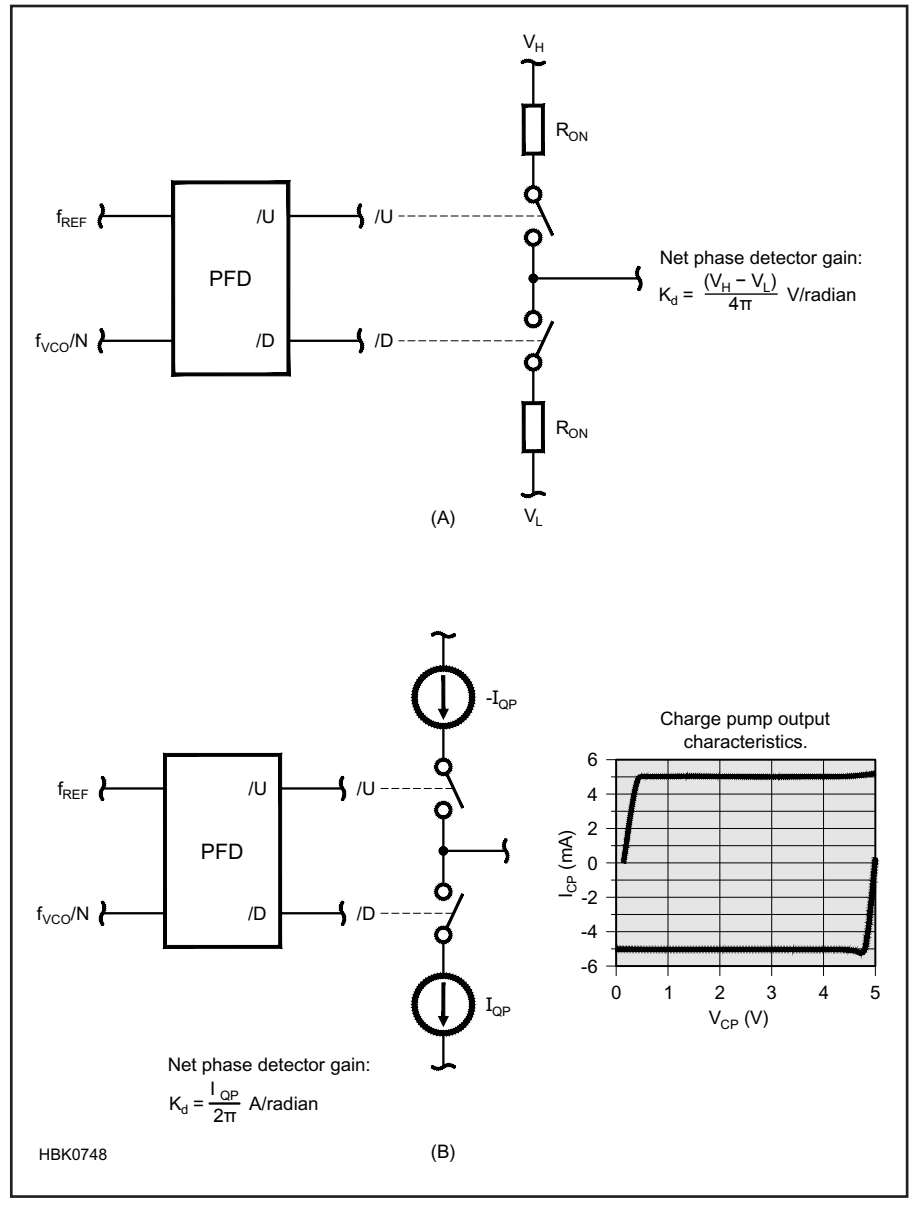


Fig 9.40 — The charge pump delivers short bursts of current to the loop filter under the control of the phase frequency detector (PFD) outputs. A voltage mode charge pump is shown at A and a current mode charge pump at B.

Charge Pumps

Because the PFD has two outputs and most loop filters have only one input, something is needed to bridge the PFD and the loop filter. The usual technique is the *charge pump*, shown in Fig 9.39B. The charge pump gets its name by allowing current to flow only for the brief interval, here when the /D or /U outputs are active. Current flow in short bursts is equivalent to a finite charge transfer.

Charge pumps come in two configurations, voltage mode and current mode, as shown in **Fig 9.40**. Voltage mode (Fig 9.40A) was the original version, though now current mode (Fig 9.40B) is most widely used with integrated circuit PLLs.

The voltage mode charge pump directly connects voltage sources to the loop filter when the PFD output signals are active. When the PFD output signals are at rest (both high) both voltage sources are disconnected from the loop filter. These voltage spikes transfer charge to the integrator in accordance with the PLL loop filter time constant. One voltage source inputs current to the loop filter and the other removes it.

The current mode charge pump is architecturally similar to the voltage mode charge pump, with voltage sources replaced by current sources. Like the voltage mode charge pump, this circuit disconnects both sources when the PFD output signals are at rest. In this case, current spikes transfer charge to and from the loop filter integrator. This transfer is independent of the loop filter series resistances.

The current mode charge pump has some advantages to the frequency synthesizer designer. Three are particularly significant:

- Pump current flows at a constant value independent of the loop filter voltage. Unless V_H and V_L are both very large compared with any possible loop filter voltage, the amount of charge transfer will vary with different loop

filter voltage values.

• During the PFD reset time, both output sources are active. The voltage mode charge pump will attempt to connect both voltage sources to the loop filter during this brief period, which can generate some undesirably large power supply current spikes. During PFD reset, the current mode charge pump loads the power supply with a single current value of I_{QP}. If both current sources are well matched, their currents completely cancel at the loop filter input, effectively disconnecting them that much earlier.

• At low offset frequencies, the loop gain flattens out with a voltage mode charge pump. Loop gain continues to increase with a current mode charge pump, effectively matching active filter performance.

VCO

The design and characteristics of oscillators, including tunable oscillators, is the major topic of this chapter so it will not be repeated here. Of particular importance to PLL design are the tuning characteristic of the VCO and the VCO tuning bandwidth.

The tuning characteristic of an oscillator shows the output frequency versus the tuning voltage, such as the example of **Fig 9.41A**. The slope of this curve is called the VCO's *modulation gain* (K_0) and it is this modulation gain that is most important to PLL design. For wideband VCOs the variation of K_0 can exceed 5:1 from minimum to maximum frequency. In section 9.7.2 the design method shows how a wide gain variation such as this is handled with a single loop filter design.

It is important to realize that the VCO has no idea that it is controlled by a PLL. While it is oscillating it continues to drift and jitter with time and temperature like any other oscillator. You must characterize these variations to be assured that the tuning capability has sufficient range for the PLL to "find" a tuning voltage value that will retune the VCO to the required frequency, under all circumstances.

The primary VCO characteristic of interest to the synthesizer designer is the tuning gain "constant," K_0. Almost never a constant, K_0 is a local measure of how much the VCO output frequency changes with a change in tuning voltage.

VCO designers go to great lengths to make K_0 an actual constant. This additional effort often increases the VCO design complexity and usually results in a more expensive design. If no linearization effort is undertaken, K_0 can easily vary from 3:1 to 10:1 over the tuning band. This also complicates the frequency synthesizer design. Specific applications will dictate where effort needs to be expended: in the VCO design or the PLL design.

All PLL design algorithms assume that there is no delay between when the loop filter presents a tuning change command to the VCO and when the VCO frequency actually changes. This situation is true when the VCO tuning bandwidth is much greater than the PLL loop bandwidth. If the VCO tuning bandwidth is not much greater than the PLL loop bandwidth, there are additional phase shifts that will cause problems with PLL stability. It is usually much easier to narrow the loop bandwidth than to redesign the VCO. If redesigning the VCO is a possibility, reduce the capacitance seen at the tuning input to increase the tuning bandwidth.

The VCO tuning bandwidth is important mainly for PLL designs that have wide loop bandwidths. Measuring the frequency deviation as the modulating frequency varies is best done by looking at the FM sidebands on a spectrum analyzer, as shown in Fig 9.41B. For constant deviation, FM sidebands follow the top profile. When the modulating frequency doubles, the sidebands drop below the profile by 6 dB, and if it triples, by 10 dB. The first FM sideband must exceed all other sidebands by 10 dB for proper VCO *characterization* — the process of determining the VCO's characteristic parameters such as the tuning sensitivity, noise spectrum, dynamic

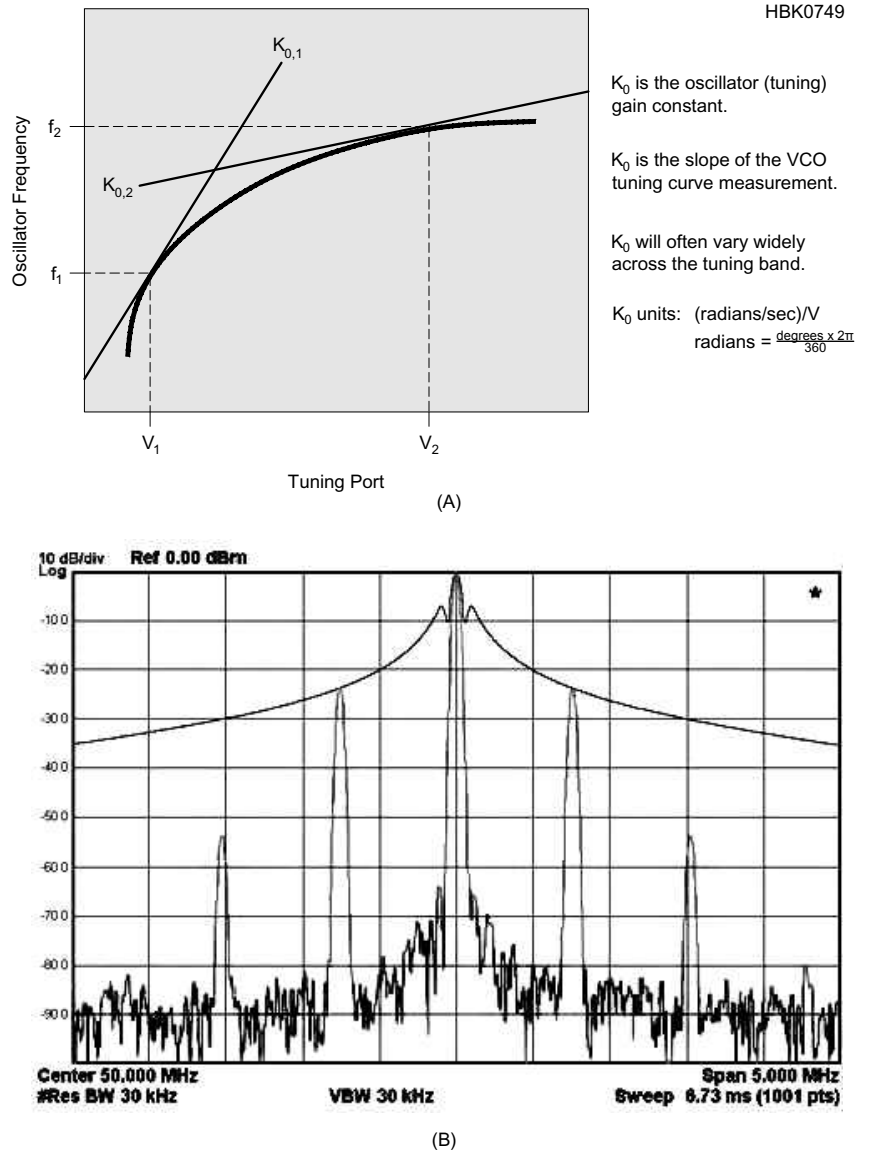


Fig 9.41 — (A) Measurement of the VCO tuning characteristic provides a curve describing frequency versus tuning voltage. The VCO tuning gain at a particular frequency (or tuning voltage) is the slope of this curve at that point. (B) A spectrum analyzer is used to measure frequency deviation of the VCO and the modulating frequency varies. FM sideband peak amplitudes follow the top profile when deviation is constant. VCO tuning bandwidth is determined by increasing the modulating frequency until the first sidebands are no longer 10 dB greater than all other sidebands.

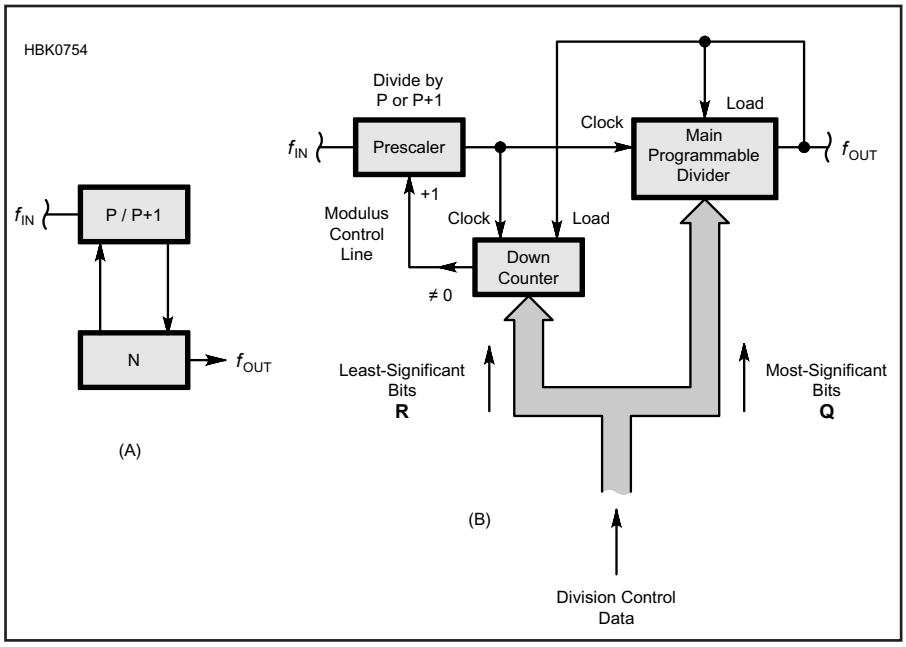


Fig 9.42 — A typical implementation of a dual-modulus prescaler.

response to changes in the tuning input signal, and so on. (See the Agilent application note "Boosting PLL Design Efficiency" in the References section.) VCO tuning bandwidth is determined by the point at which increasing the modulating frequency deviates from (drops below) the profile shown in Fig 9.41B.

Reference Divider

The reference divider is one of the easiest parts of a PLL to design, though technically is it outside the PLL. The input frequency is well known — it is the crystal reference. The output frequency is also well known, being the phase detector frequency f_{REF}. The ratio of these two frequencies is the required counter divide-by ratio or *modulus*.

When designing PLL synthesizers, f_{REF} is usually specified but f_{XO} is not. This provides some flexibility in design to use easy counter implementations if the resulting f_{XO} is also easy to get. The easiest digital counters to use for any divider are those operating with binary numbers (divide by 2, 4, 8, 16, …, 128, …). For example, if f_{REF} = 20 kHz and you choose R = 512 then f_{XO} = 10.24 MHz, which is a readily available crystal frequency.

Feedback Divider and Prescalers

The feedback divider is more of a challenge. First and foremost, this divider must work properly with whatever possible frequency it may ever see at its input. Whatever the highest and lowest frequencies the VCO may be, the divider must handle them all.

The feedback divider is almost always programmable so that the output frequency can be changed. Programmable counters are always slower than non-programmable designs, so some speed limitation occurs. Fortunately in this era of tiny CMOS integrated circuits the problems of past years in getting programmable counters to operate at hundreds of MHz are nearly over. Older equipment still has feedback divider designs that are carefully crafted to handle the frequencies at which they must operate.

Fixed Prescaler

When the programmable counter does not have sufficient speed to handle the frequencies required, then the VCO frequency must be divided down ahead of the programmable counter to assure that everything works reliably. This additional divider usually has a fixed binary value so it will go fast enough without using too much power. Called a *prescaler*, as long as the output frequency from the prescaler is always within the operating range of the programmable divider the PLL will be reliable.

Of course, there are consequences: when a prescaler is used, the PLL step size is multiplied by the prescaler divider value. For our f_{REF} = 100 kHz, if we adopt a divide-by-16 prescaler then the step size increases by a factor of 16 to 1.6 MHz. The direct way to correct for this is to reduce f_{REF} by the same factor of 16, which unfortunately means that the PLL loop bandwidth is also reduced by a factor of 16. Is there a solution with fewer compromises?

Dual-Modulus Prescaling

Yes, there is such a solution. If the prescaler is designed to divide by two values separated by 1, say 16 and 17, or 8 and 9, then we call this a *dual-modulus P/P+1 prescaler*. Using dual-modulus prescaling we can leave f_{REF} unchanged, keeping our step size and loop bandwidth while gaining much higher operating frequency for the feedback divider.

Dual modulus prescaling is a cooperative effort between a high speed prescaler and a much lower speed programmable counter. The result of this cooperation is a programmable counter that operates at a very high input frequency while maintaining unit division resolution. Dual-modulus prescaling works by allocating quotient and remainder values from the division N/P as shown in **Fig 9.42A**.

The improvement comes from viewing the operation of division in a slightly different way. The division ratio (N) of any two integers will always provide a quotient (Q) and a remainder (R). If Q counts of prescaled f_{in}/P are followed by R counts of f_{in} directly, then N = QP + R. One way to build this counter would be to first count a quotient's worth of prescaled input, and then count a remainder's amount of the input frequency directly. This last step is hard because of the high frequency.

A second approach is to add the remainder counts to the prescaled output as follows: If Q – R counts of prescaled f_{in}/P are followed by R counts of prescaled $f_{in}/(P + 1)$, then N = (Q – R) P + R (P + 1). This is the same as N = QP – RP + RP + R = QP + R.

If the remainder counts are distributed among the quotient counts by increasing the prescaler modulus by one from P to P + 1 for the remainder's amount of cycles, then returning the prescaler to its nominal division ratio while the rest of the quotient counts are made, the same result is achieved. This design always operates the programmable counter at a much lower frequency than the input frequency, which is a much more robust design.

The catch, however, is that there have to be enough quotient counts over which to distribute any amount of remainder counts. If you run out of quotient counts before remainder counts the technique falls apart and that particular loop divisor will not be *realizable*. For real dividers, all of the terms — Q, P, and R — must be positive integers, so Q – R must be greater than zero for N = QP+R to be realizable.

The maximum remainder, $R_{max} = P - 1$. The minimum quotient is equal to R_{max}. So the minimum remainder, $R_{min} = 0$. That means:

$$N_{min} = Q_{min} P + R_{min} = (P - 1) P + 0$$
$$= P^2 - P$$

If the PLL design always requires N to be greater than $P^2 - P$ then there are no problems. If N does need to go below $P^2 - P$, then the only solution is to choose a dual modulus

prescaler with a smaller value of P. Various values of P and N_{min} are:

P	N_{min}
8	56
16	240
64	4032
128	16256

Dual-modulus prescaling therefore implies a minimum divisor value before continuous divider value coverage is realized. The value of this minimum divisor depends on the base modulus of the prescaler, P, and increases quadratically. Proper choice of prescaler modulus is one of the important decisions the frequency synthesizer designer has to make.

Fig 9.42B shows how a typical dual-modulus prescaler is implemented. Each cycle of the system begins with the last output pulse having loaded the frequency control word, shown as "Division Control Data," into both the main divider and the prescaler controller. If the division control data's least significant bits (which make up R) loaded into the prescaler controller are not zero, the prescaler is set to divide by P + 1, 1 greater than its normal ratio, P. The main divider counts Q pulses from the prescaler.

Each cycle out of the prescaler then clocks the down counter. Eventually, the down counter reaches zero, and two things happen: The counter is designed to hold (stop counting) at zero (and it will remain held until it is next reloaded) and the prescaler is switched back to its normal ratio, P, until the next reload.

Because the technique is widely used, dual-modulus prescaler ICs are widely used and widely available. Devices for use to a few hundred megahertz are cheap, and devices in the 2.5 GHz region are commonly available. Common prescaler IC division ratio pairs are: 8-9, 10-11, 16-17, 32-33, 64-65 and so on. Many ICs containing programmable dividers are available in versions with and without built-in prescaler controllers.

Loop Filter

When designing PLL synthesizers we usually just have to measure and accept the VCO characteristics of K_0 and the PFD output characteristics. Output frequency range and step size are also not flexible. We pull all of these together into a working and stable synthesizer by proper design of the loop filter.

Loop filter design is usually shrouded in mystery, which has given PLL synthesizer design an aura of a "black art." This is not at all warranted because very reliable design algorithms have been around for decades. Unfortunately these have usually been published in obscure places so they are not well known. The best algorithms known to this author are presented in section 9.7.2. These methods have served extremely well for over 30 years and should provide you with fast design times and very stable PLL synthesizers. No iteration should be needed.

Loop filters come in active and passive structures. In general the easiest designs use passive (RC) loop filters if the output voltage range from the phase detector (including the PD or PFD and its charge pump) is sufficient to tune the VCO over its required frequency range. If the VCO needs a larger tuning voltage range then an active loop filter structure is necessary.

Passive loop filter circuits for current mode charge pump outputs are shown in **Fig 9.43**. The loop filter time constant is set by the charge pump current and C1, independent of R and of the loop filter output voltage. R provides a phase leading zero for PLL stability. The first-order filter in Fig 9.43A has a minimum parts count and results in loop dynamics that are consistent with the output frequency.

A second-order filter has the undesirable characteristic of allowing step and impulse changes in the input to appear at the output. This results in significant reference sidebands — a bad thing. Fig 9.43B shows a third-order filter in which C2 changes step changes at the input to slower ramps by rolling off the high frequency response of the loop filter. This results in a significant reduction in reference sidebands.

Active loop filters offer more structures that work well and are easier to design, though more complicated to build. When a voltage mode charge pump is being used, an active loop filter is strongly desired since it removes the PLL response variations with different loop filter voltage values.

In **Fig 9.44**, the gain of the op-amp isolates the actual loop filter output voltage from the charge pump output voltage, controlling the loop so that the charge pump output voltage is V_{REF}. Each passive component has the same basic function here as in the passive filter.

The third-order active filter in Fig 9.44 adds an additional pole within the feedback loop and reference frequency sidebands are significantly reduced. Charge pump current impulses now cause ramps instead of steps in the output voltage, but they still cause problems at the amplifier inputs. Good design algorithms include this extra pole as part of the fundamental dynamics — not as a disturbance of conventional second-order dynamics.

Though the design in **Fig 9.45** adds another capacitor by splitting the input resistor, the added complexity is usually well worth it. Charge pumps put out very narrow, spiky signals that are usually of sufficient amplitude and duration to temporarily drive the op-amp input into saturation. If this happens the PLL response becomes non-linear and problems often arise.

The improvement of this design is to low-pass filter the charge pump pulses before being applied to the op-amp input. The op-amp far prefers the resulting ramps, remaining linear and therefore predictable in behavior. This results in further reduction in reference frequency sidebands and is easily adapted to difference-output digital PDs, including the PFD.

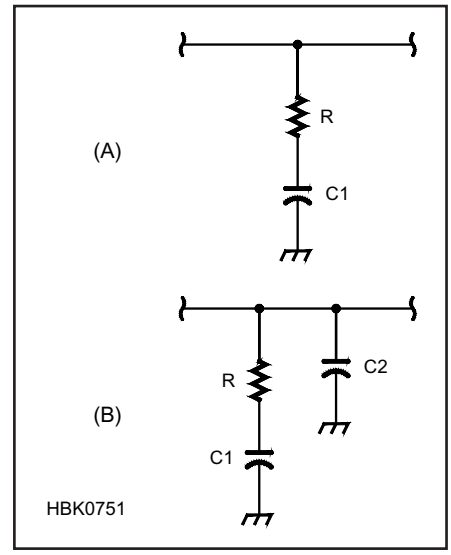


Fig 9.43 — Passive loop filters for current mode charge pump PFD outputs.

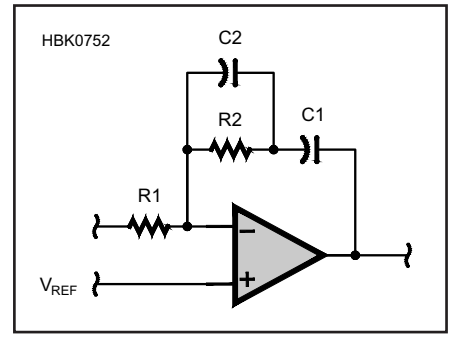


Fig 9.44 — Third-order active loop filter isolates the loop filter output voltage from the charge pump outputs.

Design equations for these loop filters will be presented after the remaining PLL component blocks are discussed.

Reference Oscillator

Any PLL is simply a stability transfer mechanism, so the behavior of the reference oscillator will not be improved on. The fractional frequency error of the overall frequency synthesizer will match that of the reference oscillator. For example if the output of the PLL synthesizer changes 1 kHz at an output frequency of 1 GHz [1000/1,000,000,000 = 1:1 million, or 1 part per million (ppm)] then the reference has changed that same fractional amount. If the crystal reference

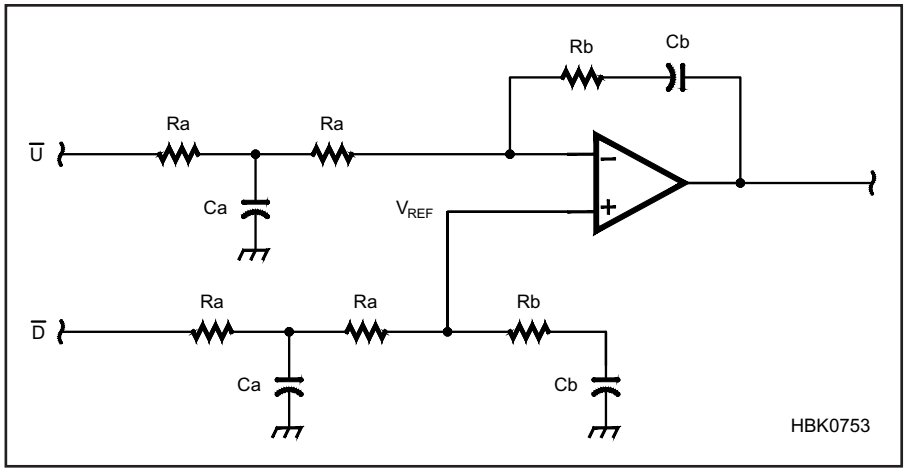


Fig 9.45 — Adding additional low-pass filtering by splitting the input resistor and adding C_A improves loop stability and reduces reference frequency sidebands. This design is well-suited for differential-output PFDs.

is 10 MHz (a very common frequency for crystal references) its frequency drift was (1 ppm) × (10 MHz) = 10 Hz. This is not much frequency drift, but it is significant to the ultimate output frequency.

9.7.2 PLL Loop Filter Design

When it is time to design a PLL synthesizer, it is best to do it in steps. Begin with knowing how the hardware you are using behaves:

- VCO tuning characteristics, K_0
- PFD characteristic (with charge pump), K_d
- Crystal reference frequency, f_{XO}

Next, list the requirements of your application

- Output frequency range, f_{OUT}
- Output frequency step size, f_{STEP}

Now you are ready to choose the two main design parameters:

- Loop bandwidth — this should not exceed 5% of $f_{REF} = f_{STEP}$.
- Phase Margin — this sets the overall stability of the PLL and can be any value between 50 and 60 degrees. A good value is 54 degrees.

With all of this information in place it is time to calculate the values for the two frequency dividers and the loop filter components. Begin with the divider values:

$R = f_{XO}/f_{REF}$

$N = f_{OUT}/f_{REF}$

$N_{MIN} = f_{OUT,MIN}/f_{REF}$

$N_{MAX} = f_{OUT,MAX}/f_{REF}$

The best design algorithm for stable PLL design calls for using the geometric mean of the feedback divider value range in the loop filter design. This same idea is used to manage the range of VCO gain values for K_0.

$$N_{DESIGN} = \sqrt{N_{MAX} \times N_{MIN}}$$

K_0 design target value =

$$\sqrt{K_{0,MAX} \times K_{0,MIN}}$$

PFD gain depends on whether the charge pump is voltage mode or current mode:

(voltage mode) $K_d = (V_H - V_L)/4\pi$

(current mode) $K_d = I_{QP}/2\pi$

For all of the active loop filter structures use the voltage mode value.

Everything is now ready. Place these design values into the appropriate design equations for the selected loop filter structure. For a passive loop filter use **Fig 9.46**. If you are using an active loop filter the appropriate equations are in **Fig 9.47** or **Fig 9.48**. The resistor and capacitor values from these calculations are not critical. Choose values within 30% of what you calculate and the design will be fine. Truly!

Following any loop filter design, it is always a good idea to check the results by directly calculating the filter time constants from the components chosen. Compare these time constants with those derived theoretically. If they match within 10-20%, there should be no problem with loop stability.

The passive third order loop filter design equations of Fig 9.46 look very similar to those of its active filter counterpart. The major difference is that this procedure yields two time constants instead of three, and a term equaling the sum of both filter capacitances.

Unlike the active filter form, there are no arbitrary component choices with the passive filter. From the time constants and the total capacitance, all three loop filter components are uniquely determined.

Since the concepts of natural frequency and damping no longer apply (by definition) in a third-order filter, the more general stability concepts of gain crossover and phase margin are used. A value of 50-60 degrees is usually used for the design phase margin.

The equations for Fig 9.47 and Fig 9.48 include the rolloff pole within the loop dynamics, rather than treating it as a loop perturbation. This allows a greater amount of high frequency rolloff to be achieved as it "kicks in" at a much lower frequency than perturbation techniques would allow.

A usual design strategy is to choose the

$$\tau_2 = \frac{\sec\phi_0 - \tan\phi_0}{\omega_0} = \frac{1 - \sin\phi_0}{\omega_0 \cdot \cos\phi_0}$$

$$\tau_1 = \frac{1}{\omega_0^{\,2} \cdot \tau_2}$$

$$C_T = \frac{K_0 \cdot K_d}{N \cdot \omega_0^{\,2}} \cdot \sqrt{\frac{1+(\omega_0 \cdot \tau_1)^2}{1+(\omega_0 \cdot \tau_2)^2}} = \frac{K_0 \cdot K_d}{N} \cdot \frac{\tau_1}{\omega_0}$$

ϕ_0= phase margin (°)
ω_0 = open loop gain crossover frequency (radians/sec)

$$\tau_1 = RC_1 \qquad C_2 = \frac{\tau_2}{\tau_1} \times C_T$$

$$\tau_2 = R\left(\frac{C_1 \times C_2}{C_1 + C_2}\right) \qquad C_1 = C_T - C_2$$

$$C_T = C_1 + C_2 \qquad R = \frac{\tau_1}{C_1}$$

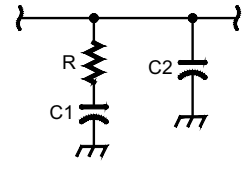


Fig 9.46 — Design equations for passive loop filters.

$$\tau_3 = \frac{\sec\phi_0 - \tan\phi_0}{\omega_0} = \frac{1 - \sin\phi_0}{\omega_0 \cdot \cos\phi_0}$$

$$\tau_2 = \frac{1}{\omega_0^{\,2} \cdot \tau_3}$$

$$\tau_1 = \frac{K_0 \cdot K_d}{N \cdot \omega_0} \cdot \left| \frac{-j\omega_0\tau_2 - 1}{j\omega_0\tau_3 + 1} \right| = \frac{K_0 \cdot K_d}{N} \cdot \frac{\tau_2}{\omega_0}$$

$$\tau_1 = R_1 C_1$$

$$\tau_2 = R_2 (C_1 + C_2) \qquad \frac{R_2}{R_1} = \frac{\tau_2 - \tau_3}{\tau_1}$$

$$\tau_3 = R_2 C_2$$

ϕ_0= phase margin (°)
ω_0 = open loop gain crossover frequency (radians/sec)

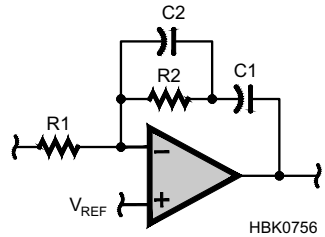


Fig 9.47 — Design equations for third-order active loop filters

$$\tau_c = \frac{\sec\phi_0 + \tan\phi_0}{\omega_0} = \frac{1 + \sin\phi_0}{\omega_0 \cdot \cos\phi_0}$$

$$\tau_a = \frac{2}{\omega_0^{\,2} \cdot \tau_c}$$

$$\tau_b = \frac{K_0 \cdot K_d}{N \cdot \omega_0} \cdot \frac{\tau_c}{2}$$

$$\tau_a = R_a \cdot C_a \qquad \frac{R_b}{R_a} = \frac{\tau_c}{\tau_b}$$

$$\tau_b = R_a \cdot C_b$$

$$\tau_c = R_b \cdot C_b$$

ϕ_0= phase margin (°)
ω_0 = open loop gain crossover frequency (radians/sec)

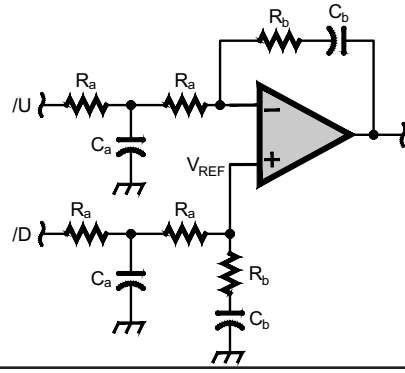


Fig 9.48 — Design equations for differential-input active loop filters

resistors first to achieve the design ratio. This may provide several possible resistor pairs. Calculate the resulting capacitor values for each resistor pair possibility, and choose the set that provides the closest realizable values.

9.7.3 Fractional-N Synthesizers

The simplest frequency synthesizer is the single PLL with a programmable counter as a frequency divider in the feedback path. It can now all be integrated onto a single semiconductor device, though better performance may be available with some sections done discretely. These synthesizers are well suited to channelized radios where the channel spacing is fairly wide. Millions of them can be found in VHF/UHF radios, cell phones, TV tuners and so on. However, apart from VHF/UHF FM transceivers, most Amateur Radio operation requires fine-resolution synthesizers to simulate the look and feel of a free-tuning VFO.

To this point in the chapter, the PLL synthesizer designs have assumed that the feedback divider operates as a single programmed integer value. This design is referred to as an *integer-N PLL*. These PLLs have an unavoidable trade-off of the step size versus every other performance parameter. Making a fine resolution loop by using a very high value of N forces a very low phase detector frequency and low open loop gain. This leads to extremely slow settling, bad phase noise, and poor suppression of spurs.

Multiple PLL loops can be used to give fine resolution without invoking other performance limitations other than cost, size and power consumption. PLL/DDS hybrids can do the same job and save some cost, size, and power consumption. The holy grail is a fine resolution synthesizer with a clean output, small size, low cost and low power consumption but that has not yet been attained. There is another thread of development particularly suited to high levels of integration, although it, too, has limitations. It is called *fractional-N* or *frac-N synthesis*.

THE ORIGIN

A single PLL would have fine resolution, if the divide-by-N stage in its feedback path weren't constrained to divide only by integers. The dividers are implemented as digital counters, counting cycles of the VCO frequency. Counting in anything smaller than integers would need something running faster than the VCO to act as an interpolator. To get steps much finer than the increments given by integers would need an interpolator running at a very large multiple of the VCO frequency, which is impractical.

One solution is to vary the value of N so that the average value of N, taken over a long enough time period, gives the required resolution. This can be done, and it doesn't need impossibly fast logic. For example, consider the 2 meter synthesizer discussed in the previous section on Frequency Resolution: if N is varied in a repeating pattern of 8 divisions by 1474 followed by 2 divisions by 1475, the average is $(8 \times 1474 + 2 \times 1475)/10 = 1474.2$. A PLL operating with this type of variable division in the feedback loop is called a *fractional-N PLL*.

The resulting problem with such a PLL is that it is never exactly on the desired frequency. It switches between too-high and too-low, even though its average might be just right. We could view this as wide deviation FM, where the modulation is a rectangular pulse of controlled mark-space ratio. Such a spectrum will have high noise levels and huge sidebands which are quite undesirable.

Nevertheless, designers of such systems have tried to slow the loops so that they could not follow the switching and sat on the average frequency. The problem with obtaining sufficient filtering of the sidebands was that the loop became too slow and all the problems mentioned above appeared, making the solution worse than single-N synthesis.

ANALOG PHASE INTERPOLATION

Variable-N synthesizers were not used in Amateur Radio transceivers, but it was common in test equipment from the 1980s and 1990s without the tuning and noise requirements of radio equipment. This type of synthesizer is described in the context of using or repairing test equipment. (For example, see the HP 3335A Synthesizer service manual's Theory of Operation section.)

PLLs can be phase modulated, quite easily, within their bandwidths by summing in a modulating voltage after the phase detector. The phase effect of the switching of the N number can easily be calculated. A digital system can be made to do this, but an extra analog system must be added to interpolate the results of the digital system. This hybrid circuit can compute a phase modulation waveform which cancels all the effects of the frequency switching, but leaves the average intact. Cancellation is never perfect but

manufactured synthesizers were developed that suppressed the unwanted sidebands to around –80 dBc (decibels with respect to the carrier level).

This is a complex system and can be hard to understand. Sometimes a second way of viewing it may be easier: If a ramp waveform is added after a phase detector in a PLL, the loop will be phase modulated with a ramping phase, or in other words, a frequency offset. If the ramp slope is controlled, any amount of resolution is possible. The problem is that ramps cannot go on forever, and the phase detector will soon hit the end of its range. The solution is to increase the N number of the divider just once at the same time that the ramp is reset by a cycle's worth of phase. A sampling system is used to disguise the disturbance of the transient phase shift and ramping resumes.

This is a large system needing careful, individual, trimming to get the analog circuitry to mesh seamlessly with the digital circuitry. The digital parts are integrated into a custom IC, but the discrete analog parts require a lot of board space. The performance was acceptable for mid-range equipment at the time. State of the art equipment used it as part of a hybrid structure as the least significant of three PLLs. The resulting fractional-N loop gave the system much finer resolution than the previous generation of 5-loop hybrids.

NOISE SHAPING

These early schemes switched the PLL divider between N and N+1 in simple, repetitive patterns, so the inevitable sideband energy was concentrated into large, obvious components. One variant of the filtering scheme used "rate multiplier" logic devices to control N to N+1 switching and reduced the amplitude of the unwanted components by spreading them out. While still not clean enough to be generally useful, other technologies were maturing: oversampling 1-bit DACs for audio, pseudo-random binary sequences for simulating telephone traffic for error rate testing, and the addition of dither to ADCs.

An integer-N PLL is a sort of DAC. You put data in as modulation, and the result is a change of frequency rather than voltage. The principles of an extreme oversampling DAC can be applied to it just as much as to the output buffer of a 1-bit DAC in a CD player. These systems scramble the sideband energy and make it much less conspicuous — a good thing. The sideband energy is also spread over a wider frequency range than the bandwidth of the loop filter. This is even better because it means more energy can be filtered out. Further, the scrambling process can be engineered to control the spectrum of the noise-like sidebands, called *noise shaping*, pushing most of the noise energy high enough in frequency that filtering can do a good job. The logic systems which shape the noise are higher-order delta modulators. They take up a lot of logic elements on an IC, but can be highly integrated and are therefore small, cheap, and have low power consumption. As a result, the noise-shaped fractional-N synthesizer looks like a simple PLL with a large amount of logic processing the data fed to its programmable divider.

Delta-modulators above the second order are inherently unstable. Audio converters have various proprietary schemes to stabilize them, and these little subtleties are carefully guarded secrets. The MASH (Multi-stAge noise Shaping) DAC arrangement adds together a series of low-order modulators, rather than trying to make one very high-order modulator. Fixing the stability problem requires that the output doesn't just jump between two states, N and N+1 in PLL terms, but it dances over a limited range.

LIMITATIONS

With the division factor varying in a pseudo-random way, the operating point of the phase detector is also varying over a wide range and the phase detector needs to have a similarly wide operating range. Since filtering only happens *after* the phase detector and large amounts of noise at high offset frequencies are present, the phase detector must be very linear.

The noise-shaping scrambler keeps the close-in frequency range clean, but any non-linearity in the phase detector allows the strong high frequency noise components to intermodulate. Intermodulation creates products at close-in frequencies, spoiling the noise performance of the close-in range.

This limits how clean the noise-shaping synthesizer can be made. The best examples are useful for many purposes but still aren't good enough for a high-grade HF receiver or any system requiring superior adjacent channel rejection. For such uses, they are combined with a high performance integer-N PLL in a hybrid structure similar to how the original fractional-N loop was used.

AVAILABILITY

Fractional-N synthesizers have been available in chip form for several years. Analog Devices, National Semiconductor, and other manufacturers have offered families of PLL ICs for a long time, and their ranges include devices with all the noise shaping logic on-board. Some even have GHz VCOs on-board as well, with dividers down to more mundane frequency ranges.

These synthesizers have become an RF design building block. The RFMD RFFC2071, for example has a pair of medium-level active mixers with an entire synthesizer all on one die. Handheld transceivers that also receive 0.5 to 999.999999 MHz are likely to be made with these parts. If you are choosing one of these devices, look carefully at the noise sideband performance: the higher frequency version of the RF2071 IC has noise sidebands a few dB lower than the lower frequency version.

WHAT NEXT?

The RF semiconductor industry is currently focused on mass-market applications such as mobile phones, WiFi and so on. The existing fractional-N synthesis parts are adequate for these systems and while there may be progressive increases in the scale of integration, there is little need for higher performance.

Development of fractional-N systems is within the range of the interested amateur, either by using the general-purpose parts on the market, or by developing their own using programmable logic array devices. A moderately-sized FPGA contains enough logic for a number of fractional-N synthesizers. For example, see the July/August 1998 *QEX* article by Ulrich L. Rohde, N1UL "A High-Performance Fractional-N Synthesizer" which describes a design covered by US patent 6509800 (2001).

A figure of merit for a fractional-N system is the maximum frequency at which the phase detector can operate. Higher frequencies allow the scrambled noise to be spread over a greater frequency range, making it easier to filter. The obvious approach is to develop faster and faster logic, but there is an alternative: Several fractional-N dividers with several separate phase detectors may have their outputs combined. The phases of the outputs from the separate dividers may be offset from each other by programming registers differently in each scrambler, and the reference signals to the phase detectors may be offset to match.

Several phase detectors can thus act sequentially over each detector's cycling period, making a system with an effective phase detector frequency several times that of a single phase detector. The effective phase detector frequency can even be higher than the output frequency. A further elaboration would be to seed the pseudo-random noise generators in each divider differently. In this way the noise components from each divider will not correlate, though the tuning components correcting the VCO frequency will correlate. This means that the tuning components add more strongly, as voltages, while the noise components add more weakly as power. Each doubling of the number of dividers has the potential for a 3 dB improvement in noise performance of the system. This multiple divider arrangement is currently covered by a patent, but individuals are free to read them, to experiment and to perhaps find a better way. Patents eventually expire and their technology enters the public domain. Each increase in the density of programmable logic makes it easier.

9.7.4 PLL Synthesizer Phase Noise

Differences in resonator Q usually make the phase-noise sidebands of a loop's reference oscillator much smaller than those of the VCO. Within its loop bandwidth, a PLL acts toward matching the phase-noise components of its VCO to those of the reference. There are several processes which get in the way of this actually happening, which are outlined here.

Dividing the reference oscillator signal f_{XO} to produce the signal f_{REF} which is applied to the phase detector also divides the deviation of the reference oscillator's phase-noise sidebands, translating to a 20 dB reduction in phase noise per decade of division. This models as a factor of –20 log (R) dB, where R is the reference divisor value, since f_{REF} is less than f_{XO}. We also know that within its loop bandwidth the PLL acts as a frequency multiplier and this multiplies the deviation of the phase noise sidebands present at the PFD, again by 20 dB per decade or equivalently by a factor of 20log(N) dB, where N is the loop divider's value. Between the reference oscillator and the PLL output, the sidebands on the reference signal are increased by 20 log (N/R) dB.

COUNTER AND PFD NOISE

Logic circuits have a noise characteristic that is extremely important to PLL design. Any circuit, when you really get down to it, is always an analog circuit. In this case the switching threshold of the logic circuits has a tiny amount of noise on it. This small amount of noise manifests itself in a very slight variation in when the logic circuit actually switches, even if the input clock is perfectly clean. We can think of this small timing jitter as a small shift in the output signal "zero crossing," which is directly equivalent to a phase modulation.

The amount of this timing jitter is constant, no matter the operating frequency. Thus, the amount of phase shift this represents depends on the operating frequency: 1 nanosecond of jitter at 1 kHz is very small, but represents 36 degrees at 100 MHz. As a result we get different measures of the noise floor from digital circuits that depend on the frequency at which they are operating. This digital noise floor interferes with the PLL action to match the VCO noise to the divided reference oscillator noise as measured at the PFD inputs.

VCO NOISE

The PLL can track only slowly moving noise, well within its bandwidth. Therefore VCO noise components that change slowly enough for the PLL to measure and track will be increasingly canceled successfully. Any VCO noise component that changes at a rate faster than the PLL bandwidth will not be changed at all. At offset frequencies beyond the PLL bandwidth the VCO noise is still present as if the PLL were not even there.

Does this imply that to get a low-noise synthesizer we are encouraged to make the PLL bandwidth very wide? Well, yes, to a certain degree. When we build PLL synthesizers we soon find that the logic noise from the prior section begins to get in the way if the loop bandwidth gets too wide. When this happens the total PLL output noise actually begins to increase as the bandwidth gets wider. There is a range of loop bandwidth values where the total PLL output noise has a minimum. This range is centered at the offset frequency where the logic noise floor, multiplied by 20 log (f_{OUT}/f_{REF}), has the same value as the VCO intrinsic phase noise.

Clearly, having a VCO design with minimum phase noise is very important to a good, low-noise PLL synthesizer. Much effort is spent on this area in industry. A summary of important results from these noise reduction efforts is presented in the section Improving VCO Noise Performance below.

FRACTIONAL DIVISION NOISE

From the brief discussion on fractional-N principles, we note that this whole idea is based on changing the feedback divider value in a semi-randomized way. This inherently jitters the output from the feedback divider, which is a source of phase noise into the PFD. This noise source is algorithmic instead of physical, but the noise is a big problem nonetheless.

OTHER NOISE SOURCES

Phase noise can be introduced into a PLL by other means. Any amplifier stages between the VCO and the circuits that follow it (such as the loop divider) will contribute some noise, as will microphonic effects in loop- and reference-filter components (such as those due to the piezoelectric properties of ceramic capacitors and the crystal filters sometimes used for reference-oscillator filtering). Noise on the power supply to the system's active components can modulate the loop. The fundamental and harmonics of the system's ac line supply can be coupled into the VCO directly or by means of ground loops.

9.7.5 Improving VCO Noise Performance

It is tempting to regard VCO design as a matter of coming up with a suitable oscillator topology with a variable capacitor, simply replacing the variable capacitor with a suitable varactor diode and applying a tuning voltage to the diode. Unfortunately, things are not this simple (as if even this is simple!). There is the matter of applying the tuning voltage to the diode without significantly disturbing the oscillator performance. There is also an issue of not introducing parasitic oscillation with the varactor circuit.

Next, as mentioned earlier, one would not like the tuning voltage to drop below the voltage swing in the oscillator tank. If this is allowed to occur, the tuning diodes go into conduction and the oscillator noise gets worse. A good first approach is to use varactor diodes back to back as shown in **Fig 9.49**. This allows the tank voltage swing to be developed across two diodes instead of one, as well as allow for a more balanced loading of the oscillator's tank. The semiconductor industry has realized this and there are a number of varactors available prepackaged in this configuration today.

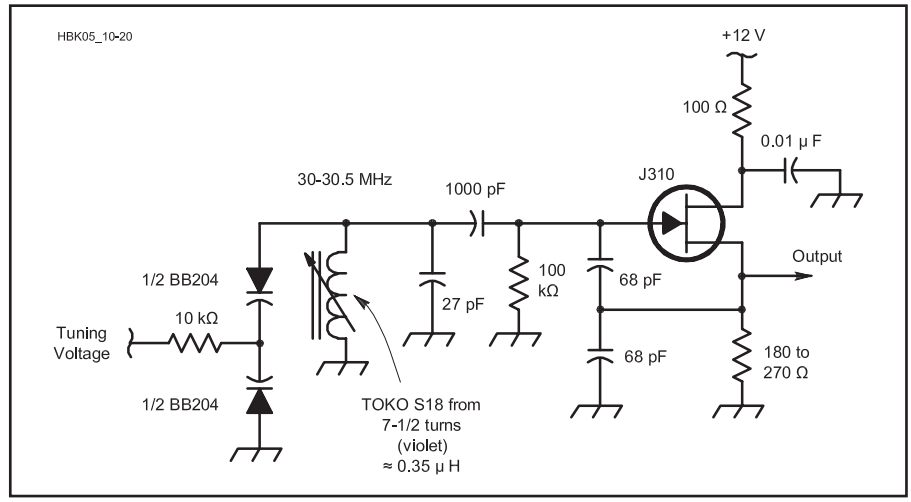


Fig 9.49 — A practical VCO. The tuning diodes are halves of a BB204 dual, common-cathode tuning diode (capacitance per section at 3 V, 39 pF) or equivalent. The ECG617, NTE617 and MV104 are suitable dual-diode substitutes, or use pairs of 1N5451s (39 pF at 4 V) or MV2109s (33 pF at 4 V).

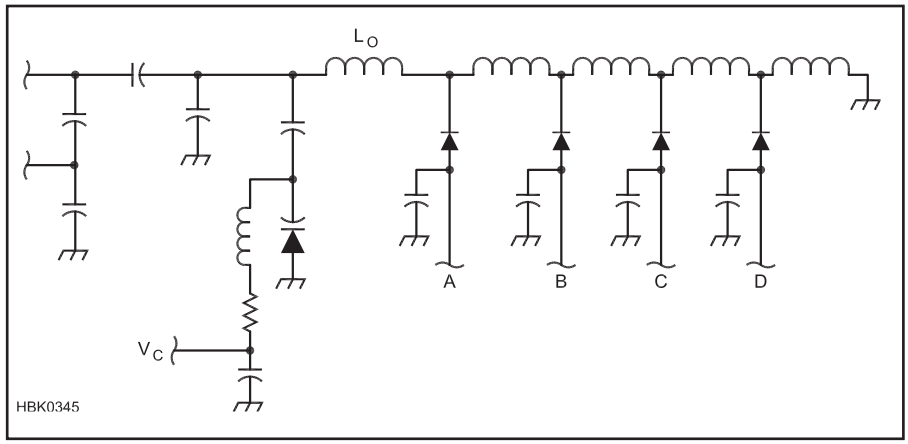


Fig 9.50 — The resonator portion of an inductor-switched segment-tuned VCO. A varactor diode provides tuning over a small range. Diode switches will alter the total inductance, changing the frequency in larger steps. Inductor-switched, capacitor-switched, and combinations are all used in VCO designs. (From Hayward, *Introduction to Radio Frequency Design*, Chapter 7. See references.)

IMPROVING VCO OPERATING Q

Often the Q of passive capacitors available for use in an oscillator tank exceeds the Q of available varactors. One way of reducing the influence of the varactor is to use only the amount of varactor capacitance required to tune the oscillator over its desired range. The balance of the capacitance is supplied to the tank in the form of a higher-Q fixed capacitor. This has the advantage of not requiring the varactor to supply all the capacitance needed to make the circuit function, and often allows for the use of a lower capacitance varactor.

Lower capacitance varactors typically exhibit higher Q values than their larger capacitance counterparts. This concept can be extended by splitting the oscillator tuning range, say 70 MHz to 98 MHz (for a typical lower-side up-converter receiver design popular for the last few decades), into multiple bands. For this example let us consider four oscillators, each with 7 MHz of tuning range. We desire the varactor Q effects to be swamped by high-Q fixed capacitors. This can be further improved through the use of a "segment-tuned VCO" discussed below. A secondary but important benefit of this is to reduce the effective tuning gain (MHz/volt, K_0) of the oscillators, making them less susceptible to other noise voltage sources in the synthesizer loop. These noise sources can come from a variety of places including, but not limited to, varactor leakage current, varactor tuning drive impedance and output noise of the driving operational amplifier or charge pump.

Segment-tuned VCOs provide the designer with additional benefits, but also with additional challenges. By segmented we mean that circuit elements, which could be both inductance and capacitance, are selected for each range that the VCO is expected to tune. **Fig 9.50** shows the frequency range-switching section of a typical VCO in which several diode switches are used to alter the total tank circuit inductance in small steps. These segments create a type of "coarse tuning" for the VCO, and the output of the PLL loop filter performs "fine tuning" with the varactor diode. Usually the component values are arranged in some sort of binary tree. In some integrated designs, 64 or even 128 sub-bands are available from the VCO.

Many times the segmented-VCO concept is applied to an oscillator design that is required to cover several octaves in frequency. For example, this would be the case with a single-IF radio with the IF at about 8 MHz. The VCO would be required to cover 8 MHz to 48 MHz for 100 kHz to 50 MHz coverage of a typical transceiver.

While segmentation allows one to build a multi-octave tunable oscillator, segmentation also imposes some additional constraints. Recalling the earlier section in this chapter on oscillators, the condition for oscillation is an oscillator loop gain of 1 at a phase angle of 0 degrees. Over several octaves, the gain of the oscillating device (typically a transistor) varies, decreasing as operating frequency increases. While conventional limiting in the oscillator circuit will deal with some of this, it is not good practice to let the normal limiting process handle the entire gain variation. This becomes the role of automatic gain control (AGC) in multi-octave oscillator designs. Application of AGC allows for the maintenance of the oscillation criteria, a uniform output and good starting characteristics, and lower noise across the operating bandwidth.

Finally, a properly designed segmented VCO can improve synthesizer switching speed. The segmentation allows the designer to "pre-steer" the PLL system and reduce the time required for the loop filter to slew the VCO to the desired frequency for lock. Frequency-locked loops (FLL) are often employed for this steering operation to be sure that it happens properly.

9.7.6 A PLL Design Example

As our design example, let us consider a synthesized local oscillator chain for a 10 GHz transverter. **Fig 9.51** is a simplified

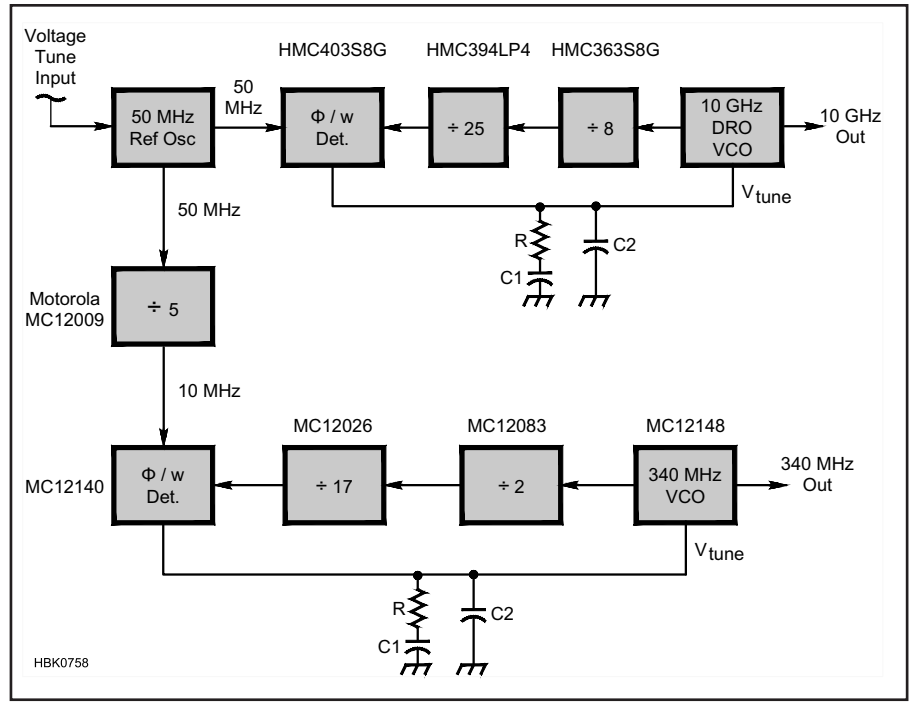


Fig 9.51 — A simplified block diagram of a PLL local oscillator for a 10 GHz converter.

block diagram of this 10 GHz converter. This example is chosen because it is a departure from the traditional multi-stage multiply-and-filter approach. It permits realization of the oscillator system with two simple loops and minimal RF hardware. It is also representative of what is achievable with current hardware, and can fit in a space of 2 to 3 square inches. This example is intended to be a vehicle to explore the loop design aspects and is not offered as a "construction project." The multiple design details required are beyond the scope of this chapter.

Two synthesized frequencies, 10 GHz and 340 MHz, are required. Since 10.368 GHz is one of the popular X-band traffic frequencies, we initially mix this with the 10 GHz LO to produce an IF of 368 MHz. The 368 MHz IF signal is subsequently mixed with the 340 MHz LO to produce a 28 MHz final IF, which can be fed into the 10 meter input of any amateur transceiver. We focus our attention on the design of the 10 GHz synthesizer only. Once this is done, the same principles are applied to the 340 MHz section. Our goal is to design a low-noise LO system (by adopting minimum division ratios) with a loop reference oscillator that is an integer multiple of 10 MHz. Using this technique allows the entire system to be locked at a later time to a 10 MHz standard for precise frequency control.

For the microwave synthesizer we consider using a line of microwave integrated circuits made by Hittite Microwave in gallium-arsenide (GaAs) material. These devices include a selection of prescalers operating to 12 GHz, a 5-bit counter that operates to 2.2 GHz and a phase/frequency detector that operates up to 1.3 GHz. If we use a crystal reference frequency f_{XO} of 100 MHz, and also apply that as f_{REF} into the PFD (therefore R = 1), then the feedback divider number needs to be N = 10,000/100 = 100. One way to realize this in hardware is to represent 100 = 4 × 25, starting with a divide-by-4 prescaler and finishing with the 5 bit counter programmed to divide by 25. The divide-by-4 prescaler output at lock will be 2500 MHz, which is too high for the 2200 MHz limited programmable counter. We need a design change.

The obvious solution is to select a divide-by-8 prescaler, providing a 1250 MHz output from the 10 GHz input. We cannot program the counter to half of 25, so we need to leave it programmed at 25. This makes the output from the feedback divider at 10,000/(8×25) = 50 MHz. We need to set R = 2.

Before even thinking about designing the loop filter, we need to know the VCO gain, VCO noise performance, divider noise performance, phase detector gain, phase detector noise performance and finally reference noise performance. For the 10 GHz VCO, we are always looking for parts that are easily available, useable and economical, so salvaging a dielectric resonator from a Ku band LNB is promising (see "SHF Super Regenerative Reception by Andre Jamet, F9HX, in Jan-Feb 2002 *QEX*). These high-Q oscillators can be fitted with a varactor and tuned over a limited range with good results. The tuning sensitivity of our dielectric resonator VCO is about 10 MHz per volt and the phase noise at 10 kHz offset is –87 dBc/Hz, and –107 dBc/Hz at 100 kHz.

The phase detector and divider information is available from the device data sheets. The HMC363 divide-by-8 operates up to 12 GHz and has a programmable charge pump that sets the phase detector gain K_d. It is usually good to keep this gain high, so we choose to use a 2 mA charge pump current, giving K_d = 0.32 mA/radian. The data sheet also says that this PFD has an output noise floor of –153 dBc/Hz measured at 100 kHz offset. The HMC394 programmable divider operated up to 2.2 GHz with the same output noise floor. The HMC984 PFD operated up to 350 MHz with a noise figure of merit (FOM) of –231 dBc/Hz/Hz-f_{REF}, so with f_{REF} = 50 MHz the PFD output noise floor is –231 + 10 log (50,000,000) = –154 dBc/Hz. Assuming the R divider is implemented in CMOS, the output noise floor from it is –163 + 10 log (50,000,000/125000) = – 137 dBc/Hz. This noise is much higher than the noise from the GaAs dividers, so it is actually better here to use a GaAs divide-by-2 for the R counter instead of using CMOS.

The logic noise floor for the entire PLL is the sum of the individual noises from each divider and the PFD. The result is –147 dBc/Hz. This is determined at the PFD. To calculate how this noise will measure at the PLL output we need to add 20LogN = 46 dB. Thus the output noise floor due to PLL logic devices is –101 dBc/Hz. This is close to the VCO phase noise at an offset of 100 kHz, so minimum noise design suggests that we select 100 kHz as our loop bandwidth.

An alternative is to eliminate the R counter and directly use a 50 MHz reference. An excellent choice for a low noise reference is the one described by John Stephensen on page 13 in Nov/Dec 1999 *QEX*. The noise performance of this VCXO is in the order of –160 dBc/Hz at 10 kHz offset at the fundamental frequency. Translating this to the output frequency means adding 20 log N, for a result of –114 dBc/Hz. Eliminating the R counter also lowers the logic noise floor to –104 dBc/Hz at the output. The translated reference oscillator noise is 10 dB below the noise floor from the logic devices, so the logic noise floor dominates.

Using this information we can now design the loop filter. Assuming that the VCO tuning voltage is between 0.5 and 4.5V we can directly use the charge pump included in this PFD and therefore select the passive third order loop filter from Fig 9.43. We use the equations in Fig 9.46 and calculate loop filter component values of R = 6977 ohms, C1 = 724 pF, and C2 = 80 pF. We therefore select 6.8k, 820 pF, and 82 pF for these component values respectively. The Bode plot of the theoretical and actual PLL dynamics is shown in **Fig 9.52**. It is nearly impossible to tell them apart!

If the VCO requires higher tuning voltages, you can insert a noninverting op-amp gain stage between the output of this loop filter and the VCO. Choose a low input current op-amp to minimize leakage from the loop filter capacitors. Be careful — the gain of this amplifier stage changes the effective VCO gain that the loop experiences. When designing the loop filter components the "design" VCO gain must be replaced by the product of the actual VCO gain and the amplifier gain. It is also essential to assure that the 1 dB bandwidth of the voltage amplifier

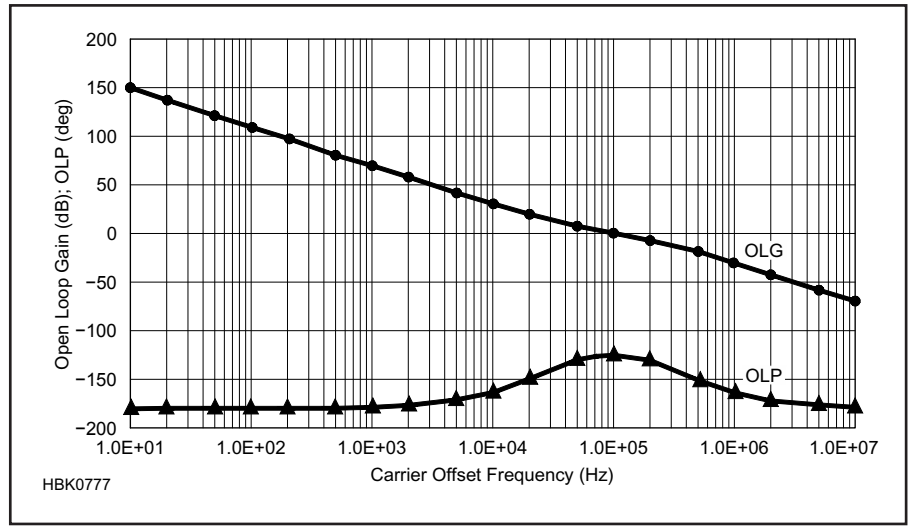


Fig 9.52 — Comparisons of the theoretical and actual PLL dynamics show extremely good correspondence.

greatly exceeds the loop bandwidth so that it does not degrade the PLL phase response and hence loop stability.

9.7.7 PLL Measurements and Troubleshooting

VCO GAIN

One of the first things we need to measure when designing a PLL is the VCO gain. The tools needed include a voltmeter, some kind of frequency measuring device like a receiver or frequency counter and a clean source of variable dc voltage. The circuit in **Fig 9.53** containing one or more 9 V batteries and a 10-turn, 10 kΩ pot does nicely. One simply varies the voltage some amount and then records the associated frequency of the VCO. The gain of the VCO is then the change in f divided by the change in voltage (Hz / V).

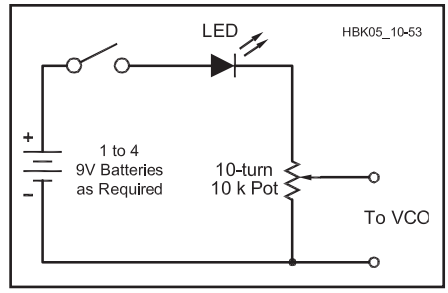


Fig 9.53 — Clean, variable dc voltage source used to measure VCO gain in a PLL design.

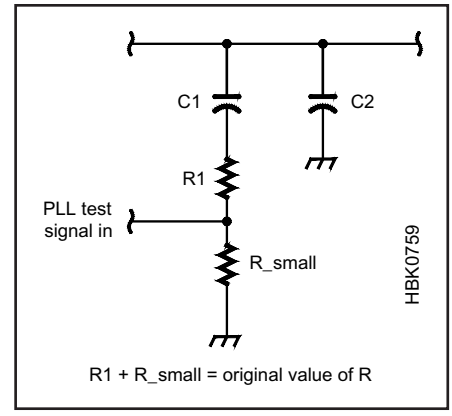


Fig 9.54 — A simple testing structure for PLL dynamics.

LOOP BANDWIDTH

Measuring the actual bandwidth of the PLL usually means measuring the entire gain and phase responses of the PLL. There is a much easier way that needs only a square-wave generator and an oscilloscope. This method uses the PLL testing structure of **Fig 9.54** developed by Glenn Ewart that injects a low-value square wave into the loop at a low impedance point so that impulse response can be observed directly. The test signal is also ground-referenced and is independent of the loop locking voltage.

Start by swapping the series RC components in the loop filter so the resistor is connected to ground and the capacitor attaches to the VCO tuning line. Then split the resistor into two resistances that together add up to the total resistance needed by the filter. The bottom resistor connected to ground is very small — 50 Ω is a nice choice when the total resistor value is much greater than 50 Ω. The top resistor is temporarily replaced by a potentiometer that can make up the desired remaining resistance. Across the bottom resistor we connect the square-wave generator and set it to a small amplitude (100 or 200 mV is common) at a frequency a few percent of the loop bandwidth, and operate the PLL. Looking at the VCO tuning line with an oscilloscope we see the impulse response of the PLL.

Now adjust the potentiometer way off-value to the low side. The impulse response will now show ringing. The frequency of this ringing is a good approximation of the PLL loop bandwidth.

SETTLING TIME

Having measured the loop bandwidth, readjust the potentiometer back to its nominal value. The impulse response should look *much* cleaner! It is tempting to look at the settling time of the impulse response and say that this is the settling time of the PLL. This unfortunately is not quite true.

The PLL is not fully settled until capacitor C1 is fully charged. This usually takes slightly longer than what the impulse response itself shows. Move the scope probe to the "ground" side of C1 and measure when this voltage reaches zero. This means there is no more current flowing through the filter resistors and the capacitor is fully charged.

TROUBLESHOOTING PLLS

Here are some frequently encountered problems in PLL designs:

- The outputs of the phase detector are inverted. This results in the loop slewing to one or the other power supply rails. The loop cannot possibly lock in this condition. Solution: Swap the phase detector outputs.
- The loop cannot comply with the tuning voltage requirements of the VCO. If the loop runs out of tuning voltage before the required voltage for a lock is reached, the locked condition is not possible. Solution: Re-center the VCO at a lower tuning voltage or increase the rail voltages on the op amp.

The loop is very noisy and the tuning voltage is very low. The tuning voltage on the varactor diodes in the VCO should not drop below the RF voltage swing in the oscillator tank circuit. Solution: Adjust the VCO so that the loop locks with a higher tuning voltage.

9.7.8 Commercial Synthesizer ICs

In this section, we explore using commercially available synthesizer chips and the role of DDS in more recent hybrid architectures. The following is not intended to be project oriented, but rather is designed to expose the reader to additional concepts that cannot be fully explored here. The reader, being made aware of these ideas, may wish to examine them in detail using references at the end of this chapter.

Many synthesizer chips have been introduced in recent years for cellular and Wi-Fi applications. One might reasonably ask if any of these devices are well suited to amateur applications. The short answer is — probably not. Applications using these chips strive for a minimum of external components, so they are usually not flexible in design. These chips conform to a strict applications profile in which the communication link is typically sending a few tens of megabits for distances of less than 3 miles (5 km). Some are even designated as "low noise" with respect to other chips of their ilk, but these noise levels are not really low with respect to most amateur requirements. The phase noise, while adequate for their intended application, is not good enough for many HF, VHF and UHF applications without additional measures being taken.

Despite all this, they do have some interesting properties and capabilities that can be exploited with additional design. Some properties that can be exploited are programmable charge pump current, a rich set of division options for creating multiple-loop synthesizers and typically low power consumption.

One of the easiest ways to improve the overall performance is to follow one of these chips with additional frequency division. Consider the following example: One of these chips could be used as a 500 to 550 MHz synthesizer, followed with two cascaded decade dividers for a total division of 100. This division would reduce the phase noise profile by 40 dB, making a reasonably quiet synthesizer for the 5 to 5.5 MHz range. The step size would also be reduced by a factor of 100, making the spacing required in the 500 to 550 MHz range equal to 1 kHz for a step size of 10 Hz at 5 MHz. This would make a good local oscillator for a simple traditional radio that covers 80 and 20 meters using both mixer products against a 9 MHz SSB generator.

There are also other techniques that can prove helpful. Decoupling the VCO from the chip will permit one to avoid much of the "on chip" noise that VCOs are susceptible to at the expense of some more complexity. If the VCO is implemented externally, there is an opportunity to design it with increased

operating Q, thereby improving the overall phase noise performance. An external VCO also opens other opportunities.

As mentioned earlier, these chips are designed for operation at a V_{CC} of 3 to 5 V, typically using an internal charge pump to generate the operating voltage. This limits the tuning voltage swing to V_{CC}. One must be able to fit the entire tuning range voltage and the ac voltage excursion in the VCO tank circuit within the V_{CC} range. As mentioned at the end of the earlier section Improving VCO Noise Performance, this problem can be overcome with the addition of voltage gain in an external operational amplifier, running at a higher voltage. This allows the signal-to-noise ratio of the oscillator to be improved by increasing the tank voltage swing and still having adequate voltage range to perform the tuning function. There are certainly more examples of how the performance of these devices could be improved for amateur applications.

The use of DDS (Direct Digital Synthesis) in an amateur transceiver goes back to at least 1987 when Bob Zavrel, W7SX, and the author used a unit from Digital RF Solutions as the VFO for an HF rig. Spurious performance of this DDS was below –75 dBc and it worked very well. More modern integrated DDS devices are improving rapidly and are capable of producing a good and economical medium performance transceiver; they are not as yet capable of "competition grade" performance. Using these chips still requires some sort of analog/digital hybrid to achieve this. (DSP and DDS are discussed in the **DSP and Software Radio Design** chapter.)

One method of incorporating DDS within a hybrid synthesizer system is to have the DDS supply the least significant digits of the frequency resolution and to sum that DDS output into a conventional divide-by-N loop that supplies the most significant digits. If desired, this signal can be passed through a sufficiently narrow filter to further attenuate any DDS spurious signals. This method is employed in a number of commercial signal generators as well as some of the more modern transceivers. Another widely used approach is to take advantage of the extremely small step size available from DDS devices and use this as the reference frequency into a conventional PLL synthesizer. The loop bandwidth of the PLL acts now as a tracking band-pass filter to reduce the DDS output spurious signals. Most modern FM broadcast transmitters use the latter technique when broadcasting CD-ROM and other digitized material.

9.8 Glossary of Oscillator and Synthesizer Terms

Buffer — A circuit that amplifies the output of a circuit while isolating it from the load.

Bypass — Create a low ac impedance to ground at a point in the circuit.

Cavity — A hollow structure used as an electrical resonator.

Closed-loop — Operation under the control of a feedback loop (see also **open-loop**).

Coupling — The transfer of energy between circuits or structures.

Damping (factor) — the characteristics of the decay in a system's response to an input signal. The **damping factor, ζ,** is a numeric value specifying the degree of damping. An **underdamped** system alternately overshoots and undershoots the eventual steady-state output. An **overdamped** system approaches the steady-state output gradually, without overshoot. A **critically-damped** system approaches the steady-state output as quickly as possible without overshoot.

dBc — Decibels with respect to a carrier level.

DC-FM — control of a signal generator's output frequency by a dc voltage.

Decouple — To provide isolation between circuits, usually by means of filtering.

Direct digital synthesis (DDS) — Generation of signals by using counters and accumulators to create an output waveform.

Distributed — Circuit elements that are inherent properties of an extended structure, such as a transmission line.

ESR — Equivalent series resistance.

Free-running — Oscillating without any form of external control.

Fundamental — Lowest frequency of natural vibration or oscillation.

Integrator — A low-pass filter whose output is approximately the integral of the input signal.

Intermodulation — Generation of distortion products from two signals interacting in a nonlinear medium, device, or connection.

Isolation — Preventing signal flow between two circuits or systems. **Reverse isolation** refers to signal flow against the desired signal path.

Jitter (phase jitter) — Random variations of a signal in time, usually refers to random variations in the transition time of digital signals between states.

Linearization — Creation of a linear amplification or frequency characteristic through corrections supplied by an external system.

Loop gain — The total gain applied to a signal traveling around a feedback control loop.

Lumped (element) — Circuit elements whose electrical functions are concentrated at one point in the form of an electronic component.

Match — Equal values of impedance.

Modulus — The number of states of a digital counter or divider.

Motional capacitance (inductance) — The electrical effect of a crystal's mechanical properties, modeled as a capacitance (inductance).

Natural frequency (ω_n) — Frequency at which a system oscillates without any external control.

Noise bandwidth — The width of an ideal rectangular filter that would pass the same noise power from white noise as the filter being compared (also called **equivalent noise bandwidth**).

Open-loop — Operation without controlling feedback.

Oscillation — Repetitive mechanical motion or electrical activity created by the application of positive feedback.

Overtones — Vibration or oscillation at frequencies above the **fundamental**, usually harmonically related to the fundamental.

Permeability tuning — Varying the permeability of the core of an inductor used to control an oscillator's frequency.

Phase-lock — Maintain two signals in a fixed phase relationship by means of a control system.

Phase noise — Random variations of a signal in time, expressed as variations in phase of a sinusoidal signal.

Phasor — Representation of a sinusoidal signal as an amplitude and phase, often drawn as a vector.

Power density — Amount of power per unit of frequency, usually specified as dBc/Hz or as RMS voltage/□Hz.

Prescaler — A frequency divider used to reduce the frequency of an input signal for processing by slower circuitry.

Preselector — Filters applied at a receiver's input to reject out-of-band signals.

Pull — Change the frequency at which a crystal oscillates by changing reactance of the circuit in which it is installed.

Quadrature — A 90° phase difference maintained between two signals.

Reciprocal mixing — Noise in a mixer's output due to the LO's noise sidebands mixing with those of the desired signal.

Relaxation oscillation — Oscillation produced by a cycle of gradual accumulation of energy followed by its sudden release.

Resonator — Circuit or structure whose resonance acts as a filter.

Simulation — Calculate a circuit's behavior based on mathematical models of the components.

Spurious (spur) — A signal at an undesired frequency, usually unrelated to the frequency of a desired frequency.

Squegg (squeeg) — Chaotic or random jumps in an oscillator's amplitude and/or frequency.

Static (synthesizer) — A synthesizer designed to output a signal whose frequency does not change or that is not changed frequently.

Synthesis (frequency) — The generation of variable-frequency signals by means of nonlinear combination and filtering (direct synthesis) or by using phase-lock or phase-control techniques (indirect synthesis).

TCXO — Temperature-compensated crystal oscillator. A **digitally temperature-compensated oscillator (DTCXO)** is controlled by a microcontroller or computer to maintain a constant frequency. **Oven-controlled crystal oscillators (OCXO)** are placed in a heated enclosure to maintain a constant temperature and frequency.

Temperature coefficient (tempco) — The amount of change in a component's value per degree of change in temperature.

Temperature compensation — Causing a circuit's behavior to change with temperature in such as way as to oppose and cancel the change with temperature of some temperature-sensitive component, such as a crystal.

Varactor (Varicap) — Reverse-biased diode used as a tunable capacitor.

VCO — Voltage-controlled oscillator (also called **voltage-tuned oscillator**).

VFO — Variable-frequency oscillator.

VXO — Variable crystal oscillator, whose frequency is adjustable around that of the crystal.

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