# A Programmable MBIST with Address and NPSF Pattern Generators

by

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**REPORT**

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The Report Committee for William Hugh O'Donnell
Certifies that this is the approved version of the following report:

# A Programmable MBIST with Address and NPSF Pattern Generators

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# A Programmable MBIST with Address and NPSF Pattern Generators

William Hugh O'Donnell, M.S.E.
The University of Texas at Austin, 2013

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The movement to smart mobile connected devices which consolidate functions of traditionally separate devices is driving innovation in System-on-chips (SoCs). One of the innovations helping to meet the current needs of SoCs is the integration of larger memory with the processor, and with this, comes the challenge of testing all the memory cells. The programmable memory BIST offers a flexible approach to designers and testers because it allows the memory test algorithms to be updated when new memory fault models are discovered. But this flexibility comes as a trade-off to area as the BIST circuitry needs to be integrated next to the memory array. This report proposes enhancements to an existing design that will improve flexibility by enhancing the address generation schemes while simultaneously eliminating the need for an auxiliary memory in cases where a Type-1 NPSF background will be used. A comparison of the base design to the proposed design shows the address and data generation improvements can be achieved with only 1.8% increase in area with an 8KB memory.

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Renee

Renee E. Babcock | Degree Plan Evaluator III | Graduate School | The University of Texas at Austin | (512) 232-3629

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