Tests for Resistive and Capacitive Defects in Address Decoders

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Abstract: *This paper presents a complete analysis, at the electrical level, of address decoder faults caused by resistive opens, and by capacitive-coupling between address lines. Several authors [3, 4, 12] have demonstrated the importance of this class of faults. New test conditions, and new march tests are derived to detect the resulting faults; and industrial results, applied to DRAMs, show the effectiveness of the new tests.*

Key words: *Defects, opens, address decoders, capacitive coupling, dynamic faults, test conditions*

1 Introduction

Memory technology has been used since a long time to push the state-of-the-art in the semiconductor industry. Because of the regular structure of memories, cell area optimization has a very high payoff. This implies that the dimensions of the transistors and the widths of, and distances between, wires have been minimized. The consequence is a high sensitivity to defects such as opens, shorts, and bridges within the memory cell array and in other parts of the memory. In addition, memories have another special property, different from logic: they have signals with a very high fan out. The lines carrying those signals run across the memory area and therefore have, in addition to a high load, also a high capacitance. This makes them very sensitive to delay type behavior, because of their capacitive coupling with other signal, power and ground lines. Examples of such lines are: bit lines, word lines and address decoder preselect lines.

The faults within a memory can be divided into faults in the memory cell array, in the address decoders, and in the read/write logic. Much has been published on fault models, and on tests for faults, in the memory cell array [2, 9, 10], because the memory cell array occupies about 80% of the area of a memory die. However, faults in the address decoders and address decoder paths, denoted as *Address decoder Faults (AFs)*, have only gotten limited attention.

This paper presents a complete analysis, at the electrical level, of AFs caused by resistive opens and by capacitive-coupling between address lines. Several authors have shown the importance of this class of AFs [3, 4, 12]. New test conditions, and new march tests, are derived to detect the resulting faults.

The paper is organized as follows. Section 2 describes the functional AFs, which historically have been considered the only class of AFs; together with conditions march tests have to satisfy in order to detect that class of AFs. Section 3 analyzes the effects electrical opens in the address decoders, and capacitive-coupling between address lines, have on the fault behavior of address decoders, and proposes conditions for detecting those faults. In Section 4 tests for the new AFs are derived. Section 5 describes industrial results, obtained from applying the new tests to a collection of DRAM chips, and Section 6 ends with conclusions.

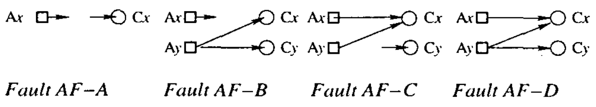
2 Functional address decoder faults

Functional address decoder faults have long been considered the only class of AFs [1, 2]. Because this paper builds on the notation and the detection conditions for this class of AFs, their notation and types will be described in Section 2.1, and their detection conditions in Section 2.2.

2.1 Notation and types of functional AFs

In this paper, the following notation will be used to describe functional AFs: An *address* is indicated with *uppercase italic alphabetic*, a *cell* with the corresponding *lowercase italic alphabetic*, and the symbol '-' means *no* address or *no* cell. E.g., $<Xy>$ means an AF whereby address *X* accesses cell *y*, $<-y>$ means that cell *y* is not accessible, because no address exists for accessing cell *y*; and $<Xx>$ denotes that address *X* accesses cell *x*, which is proper (i.e., no fault). The following types of AFs are considered to occur in address decoders (see Figure 1):

AF-A: $<X-,-x>$ An address does not access its cell, *AF-B:* $<X-,Yxy>$ An address uniquely accesses multiple cells, *AF-C:* $<Xx,Yx,-y>$ A cell is uniquely accessed by multiple addresses, and *AF-D:* $<Xx,Yxy>$ An address additionally accesses other cells.



Fault AF−A *Fault AF−B* *Fault AF−C* *Fault AF−D*

Figure 1. Functional address decoder faults

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2.2 Conditions for detecting functional AFs

As has been described in [1, 2] the above AFs will be detected by *any* march test, provided that that test satisfies certain conditions. Below we will first introduce the notation for march tests; thereafter, the detection conditions for AFs will be given.

A *march test* consists of a sequence of *march elements*. A *march element* consists of a sequence of operations applied to every cell (n = the # of cells in the memory), in either one of two address orders:

1. Increasing (⇑) address order; from cell 0 to cell n-1
2. Decreasing (⇓) address order; from cell n-1 to cell 0

Example: Test MATS+ {⇕(w0);⇑(r0,w1);⇓(r1,w0)}

- Test consists of 3 march elements: M0, M1 and M2.
- M0: ⇕(w0) means 'for i = 0 to n-1 do A[i]:=0'. The address order is irrelevant (Denoted by ⇕).
- M1: ⇑(r0,w1) means 'for i = 0 to n-1 do {read A[i]; A[i]:=1}'
- M2: ⇓(r1,w0) means 'for i = n-1 to 0 do {read A[i]; A[i]:=0}'

Condition AF: Any march test, which contains the following two march elements, will detect AF-A through AF-D.

1. ⇑(rx,...,w$\bar{x}$) Means either ⇑(r0,...,w1) or ⇑(r1,...,w0)
2. ⇓(r$\bar{x}$,...,wx) Note: '...' means any number of r or w operations; $\bar{x}$ means NOT x

The proof for Condition AF is as follows (see Figure 1):

AF-A: Ax does not access a cell. The result of a read produces a fixed value (either a 0 or a 1) such that this behaves as a SAF. The rx of Condition AF-1 will detect AF-A in case it behaves as a SA$\bar{x}$ fault, the r$\bar{x}$ of Condition AF-2 will detect AF-A in case it behaves as a SAx fault. Note: AF-A may also behave as a *stuck open fault (SOF)* [11]. In that case, the fault will be detected probabilistically, with an escape probability of 2^{-r} (where r represents the number of read operations applied to Address Ax).

AF-B: Ax does not access a cell. AF-B will be detected for the same reasons as AF-A.

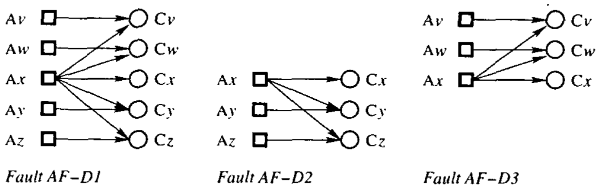
AF-C: The sub-fault $<Yx>$ will be detected as follows. If Ax < Ay (i.e., the address of cell x is lower than the address of cell y) then Condition AF-1 will detect the fault: the w$\bar{x}$, when applied to Ax, will write a $\bar{x}$ into Cx, next, the rx will be applied to Ay and detect the fault. Condition AF-2 will detect the fault if Ax > Ay.

AF-D: The sub-fault $<Yxy>$ will be detected. This fault causes more than one cell to be accessed simultaneously. A more general case of AF-D is shown in Figure 2, whereby Ax accesses multiple cells. For AF-D1 Av < Ax <Az; i.e., Ax accesses additional cells with addresses higher and lower than Ax. For AF-D2 Ax accesses additional cells with addresses higher than Ax, etc. When a read operation is applied to Ax, while accessing multiple cells, which do not contain the same value, the result of this read operation can be the following:

a. A *deterministic function* (the logical AND or OR) of the read values. Condition AF-1 detects AF-D1 and AF-D2, if x=0 (i.e., the march element of Condition AF-1 will be ⇑(r0,...,w1)) and when reading multiple cells results in the logical OR of the read values; and if x=1 and when reading multiple values results in the logical AND of the read values. Analogously, Condition AF-2 detects AF-D1 and AF-D3.

b. A *random result* (when the read cells contain different values)

1. Condition AF-1: ⇑(rx,...,w$\bar{x}$) detects AF-D1 and AF-D2. When Ax is written with $\bar{x}$, cells Cv...Cz of AF-D1, and cells Cx...Cz of AF-D2 are written with $\bar{x}$. This will be detected when Cy is read: reads $\bar{x}$ while expecting x.
2. Condition AF-2: ⇓(r$\bar{x}$,...,wx) detects AF-D1 and AF-D3. When Ax is written with x, cells Cv...Cz of AF-D1, and cells Cv...Cx of AF-D3 are written with x. This will be detected when Cw is read: reads x while expecting $\bar{x}$.



Fault AF-D1 *Fault AF-D2* *Fault AF-D3*

Figure 2. Generalized versions of fault AF-D

3 Resistive opens in address decoders and capacitive-coupling between address lines

Figure 3 depicts part of a CMOS address decoder, which is typical for many memory designs. The address bits A0, A1 and A2 have been predecoded into the signals A0, $\bar{A}$0, A1, $\bar{A}$1, A2 and $\bar{A}$2. The decoding of the *word lines* (WL0 - WL7), also referred to as *rows*, is done using 3-input CMOS NAND gates and 2-input NOR gates, together with a buffer circuit. WL0 is selected if {$\bar{A}$2,$\bar{A}$1,$\bar{A}$0}={1,1,1}; indicating that A0=0, A1=0 and A2=0. Column decoders, which select a pair of *Bit Lines (BLs)*, have a similar structure, and therefore will not be discussed. In decoders, defects can cause opens at the following locations (they will be discussed below, together with the AFs caused by capacitive-coupling between address lines):

1. Between logic gates (*inter-gate opens*). Figure 3 shows an inter-gate open in the line from $\bar{A}$1 to the NAND gate decoding $\overline{\text{WL0}}$.
2. Inside logic gates (*intra-gate opens*). Figure 4 shows an intra-gate open in the drain of the pull-up transistor of the NAND gate for input A2.

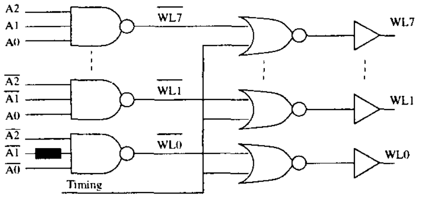


Figure 3. Inter-gate open defect

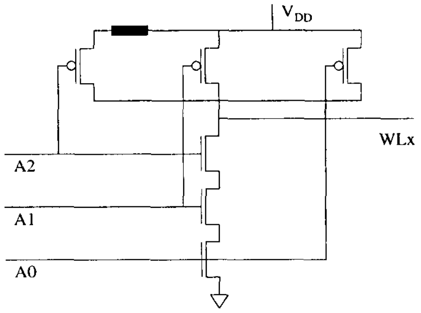


Figure 4. Intra-gate open defect

3.1 Inter-gate opens

Depending on the value of the inter-gate open defect, R_{def}, the following cases can be recognized:

R_{def} = very large: For sufficiently high values of R_{def}, the corresponding input of the NAND gate will behave as an open connection. Depending on the leakage current in the NAND gate of WL0, the following may occur:

a. The input will be pulled low, which means that WL0 will never be selected, causing the AF-A of Section 2.1. This will be detected by any march test which satisfies Condition AF.

b. The input will be pulled high, which means that WL0 will be selected, whenever $\{\bar{A}2,\bar{A}0\}=\{1,1\}$, independent of $\bar{A}1$; causing AF-D of Section 2.1. This will be detected by any march test which satisfies Condition AF.

R_{def} = intermediate: In this case, R_{def} will cause a *delay* on the signal $\bar{A}1$ of the CMOS NAND gate of WL0. The consequence is that the rise and fall times of WL0, during the *activation* and the *deactivation* (which means the *precharge*) phases of the memory cycle, will be delayed, causing *dynamic faults*.

a. *Activation (WL0 changes from 0 → 1)* The delay caused by R_{def} will become effective during activation of WL0, if this activation is caused by a 0 → 1 transition of $\bar{A}1$. In the example decoder of Figure 3, this will occur upon a switch from WL2 → WL0, from WL3 → WL0, from WL6 → WL0, and from WL7 → WL0. Due to the delayed activation of WL0 the first read or write operation intended for WL0 is still (partially) applied to the WL accessed prior to WL0. Note, this fault will not occur upon a switch from WL1 → WL0, from WL4 → WL0, and from WL5 → WL0. In general, if R_{def} is in input A_d ($\bar{A}_d$) of the CMOS NAND gate for WLq, then the 0 → 1 transition will occur upon any switch from any WLp to WLq, with A_d=0 ($\bar{A}_d$=0) for WLp. If R_{def} is in the input A_d ($\bar{A}_d$) of some CMOS NOR gate for WLq, then the 0 → 1 transition will occur upon a switch from any WLp with A_d=1 ($\bar{A}_d$=1) to WLq. This fault results in an AF-D, provided that the proper address sequence is applied; see Condition AF-Open below.

b. *Deactivation (WL0 changes from 1 → 0)* WL0 will be precharged if $\bar{A}0$ and/or $\bar{A}1$ and/or $\bar{A}2$ make a 1 → 0 transition; because that will cause WL0 to change form 1 → 0. A precharge which starts when *only* $\bar{A}1$ makes a 1 → 0 transition will incur a delay; hence causing a potential fault. This happens upon any of the following address changes: WL0 → WL2, WL0 → WL3, WL0 → WL6, and WL0 → WL7; this fault will not occur upon the following address changes: WL0 → WL1, WL0 → WL4, and WL0 → WL5. The consequence of this precharge delay will be that WL0 will still be active, while the next address (WL2, WL3, etc.) is also activated, potentially causing two WLs to be active simultaneously. This fault results in an AF-D, provided that the proper address sequence is applied; see Condition AF-Open below.

Condition AF-Open: In order to detect all faults caused by activation and deactivation (or precharge) delays, while the structure of the address decoder is not known, a test has to perform a rx or a wx operation to a WLp, followed by a r$\bar{x}$ operation to WLq. This sequence of two operations has to be applied to all address pairs {WLp,WLq} which have addresses with a *Hamming distance (H)* of 1 (*H*=1); which means that the two addresses differ in exactly one bit (Denoted by the addressing sequences $\Uparrow^i$ and $\Downarrow^i$). A test satisfies Condition AF-Open if it contains the two march elements of Case A (Case A.1, and Case A.2a or Case A.2b) or of Case B (Case B.1, and Case B.2a or Case B.2b):

A.1: $\Uparrow^i$(rx, ..., w$\bar{x}$)
A.2a: $\Downarrow^i$(rx, ..., w$\bar{x}$) A.2b: $\Downarrow^i$(r$\bar{x}$, ..., wx)
B.1: $\Uparrow^i$(rx, ..., w$\bar{x}$,r$\bar{x}$)
B.2a: $\Downarrow^i$(rx, ..., w$\bar{x}$,r$\bar{x}$) B.2b: $\Downarrow^i$(r$\bar{x}$, ..., wx,rx)

Considering the fact that memories contain separate row and column decoders, each test only has to be performed for a single row and a single column. The resulting test length is of order $\Theta(\sqrt{(n)} * log_2(n))$.

3.2 Intra-gate opens

Figure 4 shows a resistive intra-gate open defect in the pull-up path (the p-channel transistor) of a CMOS NAND gate. The test consequences for the case that R_{def} = *very large* (which causes the well-known CMOS Stuck-Open fault [13]) are a subset of the case when R_{def} = *intermediate*. In the latter case R_{def} will cause a delay in the 0 →

1 transition on the output of the NAND gate of Figure 4, if that transition is *only* caused by a 1 → 0 transition on A2. This will occur with the two-pattern sequence $\{1,1,1\}$ → $\{0,1,1\}$; i.e., the first pattern causes the pull-down path of the gate to conduct, while the second pattern causes the pull-up path to be activated only through the transistor with the R_{def} in its path. In general, for any open in the pull-up path, all two-pattern sequences with H=1 have to be applied. Tests satisfying Condition AF-Open will detect this fault.

If R_{def} is situated in the pull-down path, all 1 → 0 transitions will be delayed. This will happen for any two-pattern sequence $\{X,X,X\}$ → $\{1,1,1\}$; whereby at least one "X" has the value 0. A test, which satisfies Condition AF, will detect this fault.

3.3 Capacitive-coupling between address lines

A delayed activation can be caused by inter-gate and intra-gate opens, as shown in Section 3.1 and Section 3.2, respectively. However, with the modern high-speed logic decoders an additional source of inter-gate signal delays occurs due to capacitive coupling between signal lines; see Figure 5 [6]. Consider the AND gate with inputs A and B, and output R. Input A has a '1'; input B makes a 0 → 1 transition and is capacitively coupled to line C. Case 1 shows the delay when C=0, Case 2 when line C also makes a 0 → 1 transition simultaneously with line B, and Case 3 when C makes a 1 → 0 transition simultaneously with line B. From Case 3 it will be clear that the 0 → 1 transition on R will be delayed by the 1 → 0 transition on line C; while Case 2 accelerates the 0 → 1 transition on R. An analogous situation occurs when input B makes a 1 → 0 transition. These transition delays (accelerations) also occur between address lines, such as WLs, BLs, and/or predecoded lines. Then the activation (deactivation) of line Lq may be delayed (accelerated) when line Lp is deactivated (activated) simultaneously. The detection condition for the capacitive-coupled delay, for the case that the decoder structure and the layout of the address lines is not known, is: For any pair of lines {Lp,Lq}, Lp has to make a 0 → 1 (1 → 0) transition while Lq simultaneously makes a 1 → 0 (0 → 1) transition, for all address-line pairs Lp,Lq. If the layout of the address lines is not known, then only a test which checks all address pairs will detect all faults. However, the tests satisfying Condition AF-Open will detect most faults.

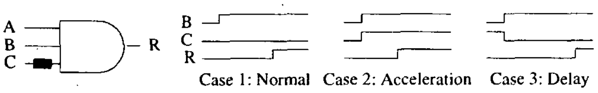


Figure 5. Influence of capacitive coupling

4 Tests for opens in decoders and for capacitive-coupling between address lines

This section derives tests for opens in address decoders and capacitive-coupling between address lines, for the cases that the structure of the address decoder is not known, and that the structure of the decoder is known.

Unknown decoder structure: The two tests below satisfy Condition AF-Open of Section 3.1. Test a is based on the detection of *Read-after-Write (RaW)* faults, while Test b is based on the detection of *Read-after-Read (RaR)* faults.

a. $\{\Updownarrow(\mathrm{w}x);\ {}_D\Uparrow^i(\mathrm{r}x, ..., \mathrm{w}\bar{x});\ {}_D\Downarrow^i(\mathrm{r}\bar{x}, ..., \mathrm{w}x)\}$

b. $\{\Updownarrow(\mathrm{w}x);\ {}_D\Uparrow^i(\mathrm{r}x, ..., \mathrm{w}\bar{x},\mathrm{r}\bar{x});\ {}_D\Uparrow^i(\mathrm{r}\bar{x}, ..., \mathrm{w}x,\mathrm{r}x)\}$

where: $x \in \{0,1\}$, and the march elements with addressing orders ${}_D\Uparrow^i$ and ${}_D\Downarrow^i$ have to be repeated with an address increment (decrement) of 2^i for a single row and column; i.e., $D \in \{R,C\}$, R = # of rows. For example for row-address bit 0 (R0), the address increment/decrement is: $2^0 = 1$, for R3 the increment/decrement is $2^3 = 8$, etc. Note that the address incrementing/decrementing operation has to use end-around carry to allow for all possible address; e.g., in case of a 3-bit row address and an increment of 2^2=4, the address after 110 is 001, etc. Both tests only have to be performed for one row and one column, this results in a test time to order $\Theta(\sqrt(n) * log_2(n))$. If the tests are performed for all rows and all columns the test time will be $\Theta(n * log_2(n))$.

Known decoder structure: If the structure of the address decoder is known, then only a *subset* of all possible address pairs within a row/column has to be generated. For example, suppose that in the decoder of Figure 3, input A2 ($\bar{A}2$) is the output of a predecoder with inputs A6, A5 and A4, then all address pairs with H=1 of lines A6, A5, A4, A2, A1, A0 of the following form have to be generated: {{0,0,0, A2, A1, A0}, {1,1,1, A2, A1, A0}} and {{1,1,1, A2, A1, A0}, {0,0,0, A2, A1, A0}}. This applies to inter-gate and intra-gate opens, as well as to capacitive-coupling between address lines.

Table 1. Empirical test results

#	Test	SCs	1	2	3	4	5	6
1	March C-	48	**234** **163**	144 70	149 124	131 90	50 26	62 30
2	PMOVI	48	144 70	**201** **144**	188 133	178 140	51 25	69 35
3	XMOVI	16	149 124	188 133	**256** **291**	187 192	52 27	73 37
4	YMOVI	16	131 90	178 140	187 192	**213** **217**	53 26	72 37
5	GALCOL	1	50 26	51 25	53 27	53 26	**53** **27**	50 27
6	GALROW	1	62 30	69 35	73 37	72 37	50 27	**96** **45**

5 Empirical evaluation of tests

This section covers industrial results of two experiments, whereby special emphasis is given to tests for the fault models discussed in this paper.

5.1 Industrial evaluation of DRAM tests

In this experiment [7, 8] a large set of tests has been applied to a selected set of DRAM chips. It has been performed at room and high temperature (at T=25 °C and T=75 °C, respectively). The number of chips tested was 1896 for T=25°C, whereby a total of 1140 chips passed; these were tested at high temperature thereafter.

For this study, the following tests are of interest:

1. March C-: {⇕(w0);⇑(r0,w1);⇑(r1,w0);⇓(r0,w1);⇓(r1,w0)}
2. PMOVI: {⇓(w0);⇑(r0,w1,r1);⇑(r1,w0,r0);⇓(r0,w1,r1);⇓(r1,w0,r0)}
3. XMOVI: {⇓(w0);⇑(r0,w1,r1);⇑(r1,w0,r0);⇓(r0,w1,r1);⇓(r1,w0,r0)}
4. YMOVI: {⇓(w0);⇑(r0,w1,r1);⇑(r1,w0,r0);⇓(r0,w1,r1);⇓(r1,w0,r0)}
5. GALCOL: See [2, 7]
6. GALROW: See [2, 7]

The PMOVI test is the MOVI test [2, 5], however, it is only performed using an address increment/decrement of 1. The XMOVI performs X-fast addressing (the row-address is incremented most frequently) with increments/decrements of 2^i for the row address; YMOVI is similar for the column address. The tests have been performed with several *stresses*, such as Voltage, Timing, Temperature, Data Background, etc. A combination of stresses is called a *Stress Combination (SC)*. The following stresses have been used, resulting in a maximum number of 3*4*2*2 = 48 SCs per test.

1. Addressing: X-fast, Y-fast, and Address Complement
2. Data backgrounds: Solid, Checkerboard, Row-strip and Column stripe
3. Voltage: V_{CC} = 4.5 V and V_{CC} = 5.5 V.
4. Timing: t_{RCD} (RAS to CAS delay) minimal, and maximal

Naturally the XMOVI test can only be performed with 16 SCs, because the Address stress has to be X-fast. The GALROW and GALCOL tests have been performed only for a single SC because of their long test times. Table 1 shows the results of the tests. The column "SCs" lists the number of SCs the test has been performed with. That means that March C- has been performed 48 times, each time with a different combination of the above-mentioned stresses. The column labeled "1" is the column for March C-; etc. The entries represent the intersections of the *fault coverages (FCs)* of the corresponding two tests; the top number applies to T=25°C, the bottom number to T=75°C. For example, the intersection of row "2" (PMOVI) with column "1" shows the number of faults PMOVI and March C- have in common; this is 144 for T=25°C. The intersection of row "2" with column "2" is the FC of PMOVI; this is 201 for T=25°C and 144 for T=75°C. The FC of March C- when all 48 SCs are applied is 234. When March C- is only applied with 16 SCs (using only the X-fast addressing stress) then the FC = 119, when only the Y-fast addressing stress is used, FC = 213; for T=25°C (not shown in Table 1). This allows for a more fair comparison with XMOVI and YMOVI, which only use X-fast and Y-fast addressing stress, respectively. From the table it can be seen that XMOVI and YMOVI have a higher FC than PMOVI. This may be caused by speed related faults and faults caused by opens in the address decoders; however, faults with other causes may also have contributed to this higher FC. The FC of March C- is 234, which is higher than PMOVI, XMOVI and YMOVI; however, the intersections of March C- with PMOVI, XMOVI and YMOVI are rather low (144, 149 and 131 respectively). This indicates that many of the faults detected by March C- are different from those of PMOVI and YMOVI. The FC of GALCOL and GALROW are rather low; the reason may be that they only have been performed with 1 SC. Table 1 shows the importance of tests with address increments/decrements of 2^i.

5.2 ProMOS test results

ProMOS Technologies Inc. is manufacturing SDRAM devices of current standard densities and organizations in its wafer plant, based in Hsinchu, Taiwan, using most recent processing technologies. The production test flow of these devices uses one test, which satisfies *Condition AF-Open*. This test shall be denoted as *decoder test (DT)*. Several march patterns in the test flow prior to the DT test satisfy *Condition AF*. The chips failing the DT therefore represent unique faults covered by Condition AF-Open, which pass Condition AF. They are referred to as *AF-Open chips*, whereas address decoder faults, failing also Condition AF in standard march tests, are referred to as *AF-chips*. AF-chips are not easily separated from the vast number of other faults detected by standard march tests. The following data is therefore limited to AF-Open chips.

Of all the chips rejected in the full test flow from wafer to component level, about 1 chip out of every 1500 is a unique AF-Open chip; this corresponds with 667 ppm. They were collected and analyzed in detail by non-destructive *Electrical Failure Analysis (EFA)*, to determine which of the defects discussed in Section 3 induced the faulty behavior. If the decoder structure is known, it is possible to distinguish between those defects, by correlating address pairs in the test pattern, which are inducing faults to the row or column addresses of the induced faults. Three different fault types could be distinguished among AF-Open chips. Group 1: 70% of the rejects have decoder faults specific to the architecture of tested chips. Group 2: 15% are chips with defects not related to any decoder. Group 3: 15% are chips with inter-gate opens in the decoder, with R_{def} = intermediate.

The Group 1 faults are not discussed in the theoretical part of this paper. DRAMs use fuses, which can be shot by laser or electrically, to replace defective areas of the memory after a prefuse test with non-defective "redundant" parts of the memory. The defects causing Group 1 faults are not located in the direct address decoder path, but in the decoder circuits, which evaluate the address information stored in fuses. Condition AF-Open is a sufficient condition to detect this fault. Detailed discussion of a fault outside the direct decoder path and specific to one DRAM-architecture is beyond the scope of this paper.

It is a frequent observation that a production test not only detects the faults for which it is originally designed, but also uncovers new faults or gives better coverage to other known faults. Group 2 rejects fall into this category. They are not due to any decoder problem, but therefore also not topic of this paper.

Group 3 rejects are of a type discussed in Section 3.1: Inter-gate opens with R_{def} = *intermediate* on the input address signal of one decoder NAND gate. The theoretically predicted behavior could be observed in the electrical analysis: After precharge of the defective NAND this fault induces AF-D with several simultaneously activated WLs (Columns). The same resistive defect also causes AF-A after the activation of the defective NAND gate, when the WL (Column) connected to this gate is not activated in time. The fault is only induced, if subsequent Activate-Precharge cycles use a subset of all possible address pairs with H=1, as required by Condition AF-Open.

The observed decoder faults occurred in the row- and in the column decoder with about the same likelihood. No intra-gate opens, and no faults due to capacitive coupling, were observed among AF-Open chips. This does not mean that they do not exist. Due to the limited sample size, on which detailed EFA was performed, it can only be concluded, that the likelihood for these defect types is at least one to two orders of magnitude smaller than for inter-gate opens in ProMOS SDRAM products. The likelihood of an open defect for a given signal line should increase with its length. The layout lengths of inter-gate signal lines have to be inevitably longer than those of intra-gate signal lines. This explains the higher likelihood of inter-gate opens. Capacitive coupling is an effect, which can be simulated during the design and layout phase of a chip. If this is done carefully, faults due to this effect should be minimized. Open defects on the other hand are due to random variations in the manufacturing process of a chip, which cannot easily be avoided. This could be an explanation, why inter-gate opens are more probable than capacitive coupling faults. The defect probability for intra- and inter-gate opens, as well as capacitive coupling faults will depend strongly on the design, layout and manufacturing process of a chip. The observed defect distribution for ProMOS SDRAMs may therefore not be representative for other products.

6 Conclusions

A complete analysis of opens in memory address decoder paths has been presented. The opens have been divided into inter-gate and intra-gate opens. In addition, delay faults caused by capacitive coupling between decoder lines have been shown to exist. The Condition AF-Open, which states the requirement a test has to satisfy in order to detect all open and delay faults in an address decoder, has been derived. Empirical results, based on a large set of tests, applied to DRAM chips, show the importance of tests for opens in the address decoder paths. Results from ProMOS shows that tests, specifically designed for detecting open faults in SDRAM chips, reduce the ppm level by about 670. In addition, they show that the major failure mode is that of inter-gate opens; intra-gate opens and dynamic faults were considered to be less likely by one to two orders of magnitude. When the relative area of the decoders i taken into consideration, the inter-gate opens have about the same likelihood for row- and column decoders.

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