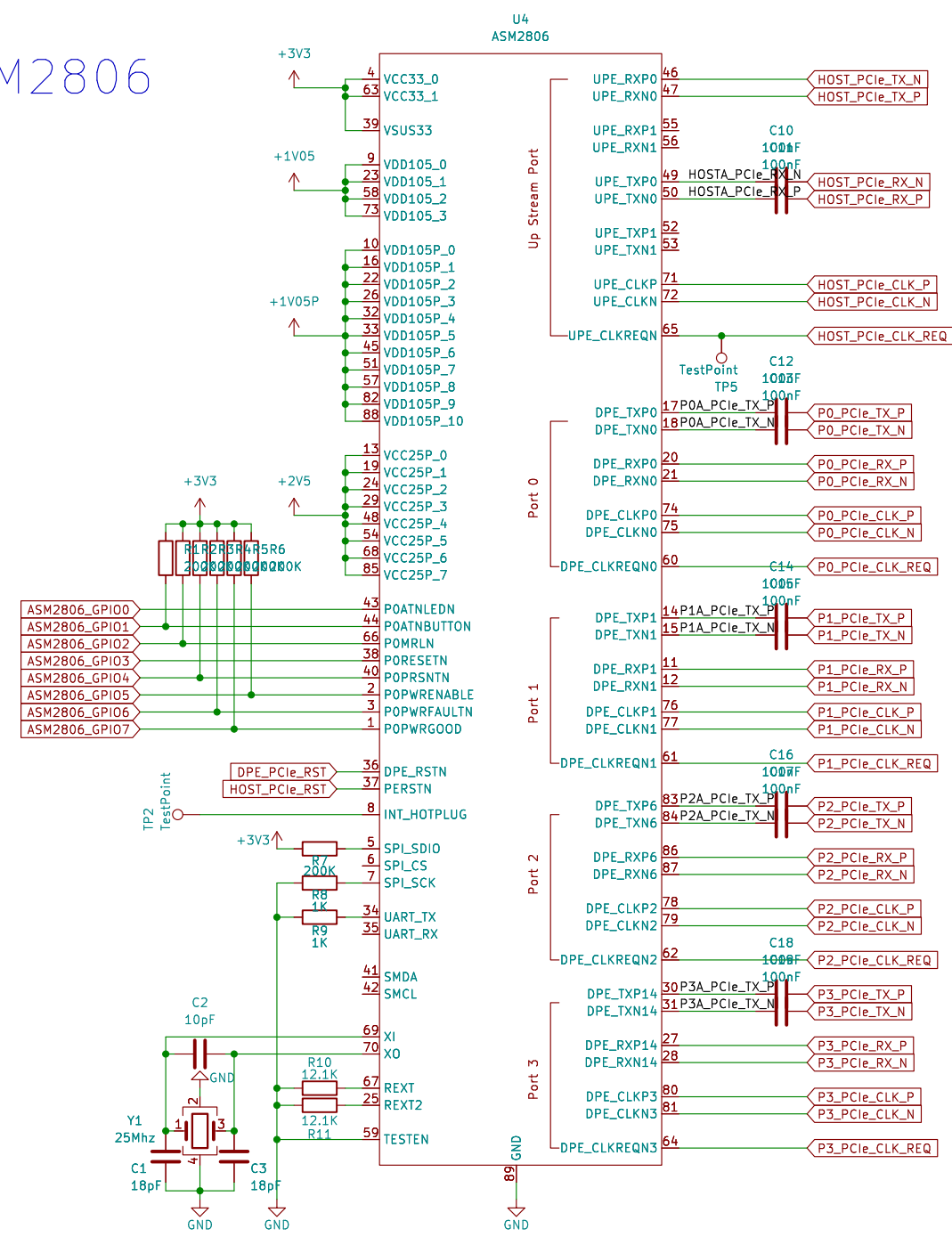
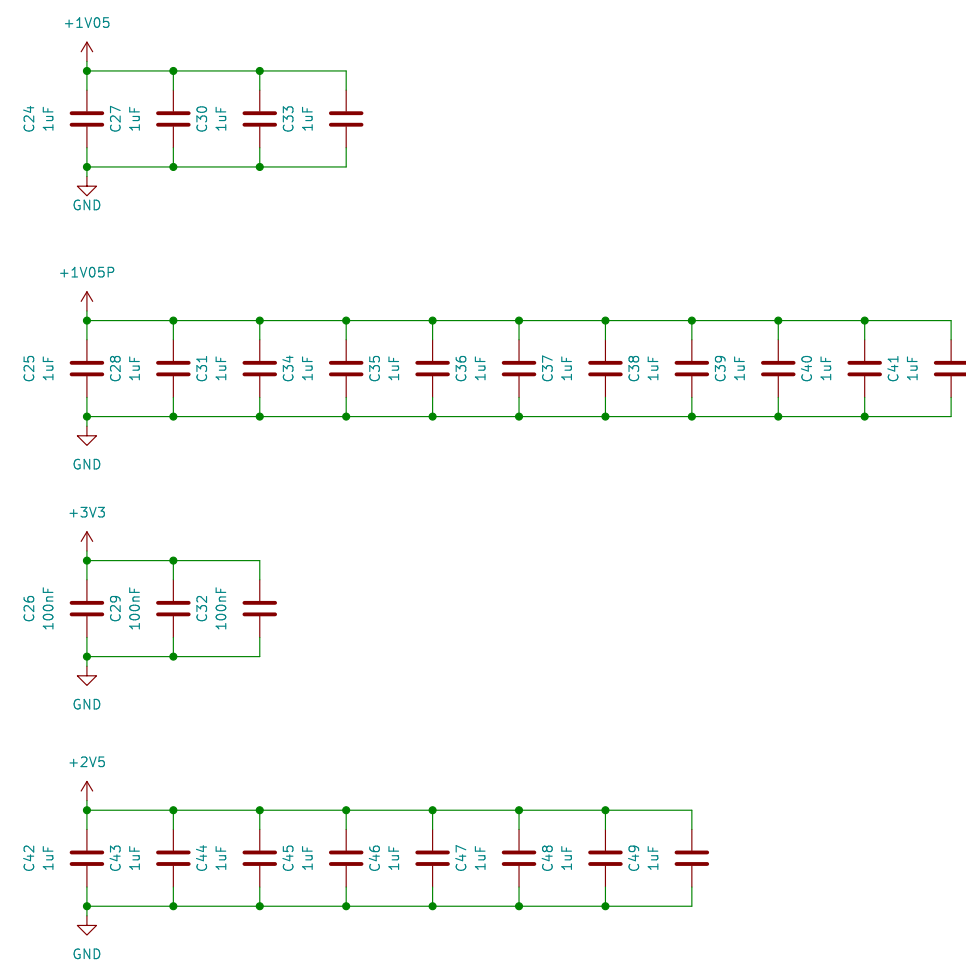


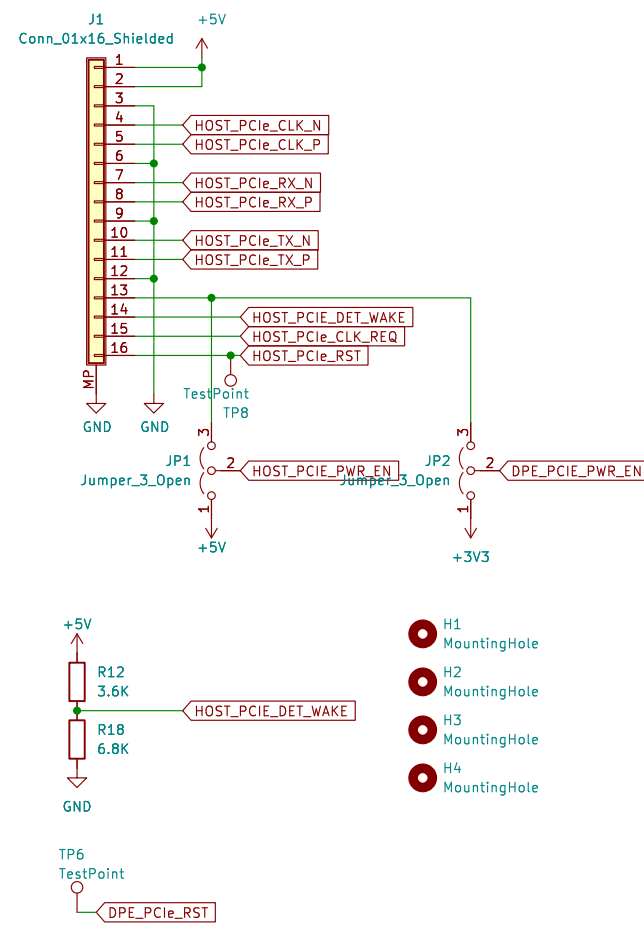
ASM2806



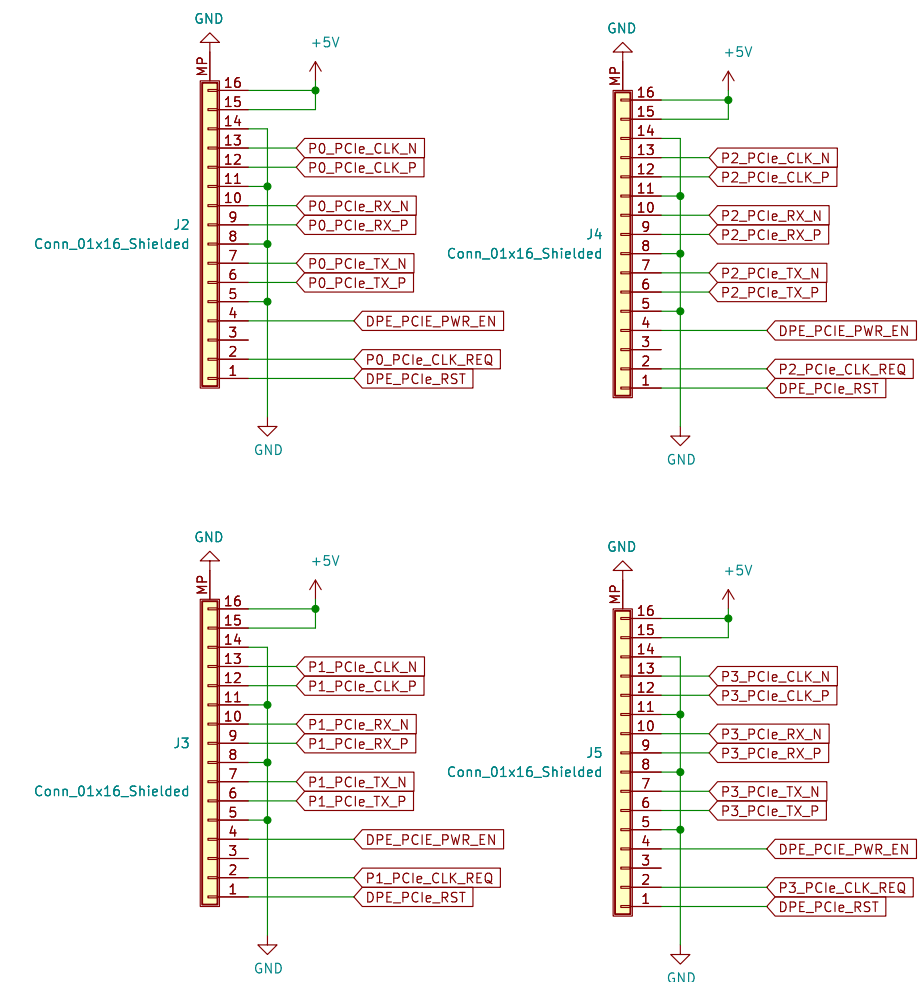
ASM2806 Decoupling Caps



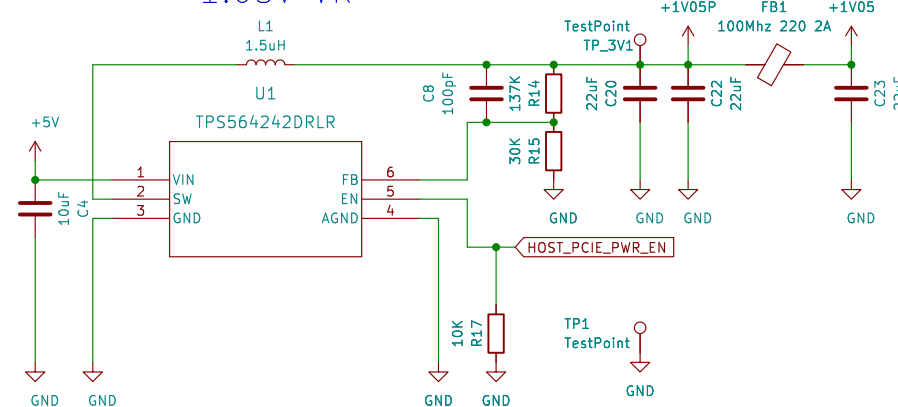
Upstream Port



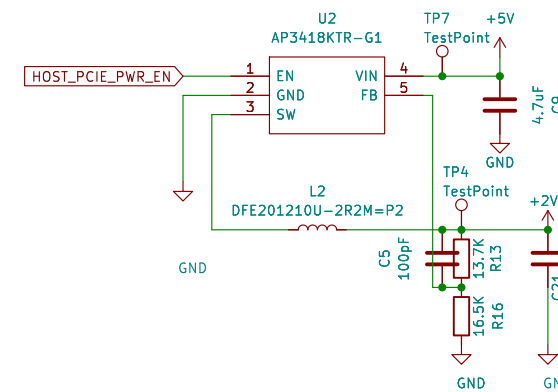
Downstream Ports



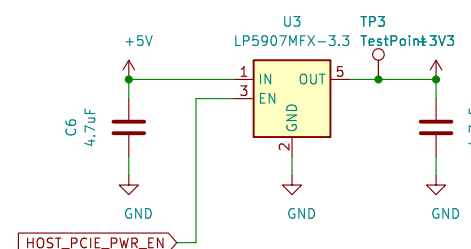
1.05V VR



2.5V VR



3.3V LDO



Designed by Will Whang

Sheet: /
File: ASM2806_Breakout.kicad_sch

Title: PCIE 3.0 Hub Testing boardf

Size: A2	Date: 2024-11-06	Rev: v1.0
KiCad E.D.A. 8.0.4		Id: 1/1