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ECE 177

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Lab 6 Prelab

Question 1:

Register 16 bit

Clock speed 100kHz

Prescaler 2,4,8

With each Prescaler how long would it take to fill.

With a prescale of one, it would be $(100kHz)^{-1} * (2^{16}-1)*1= 655.35ms$

Two: $(100kHz)^{-1} * (2^{16}-1)*2 = 1.31s$

Four: $(100kHz)^{-1} * (2^{16}-1)*4=2.62s$

Eight: $(100kHz)^{-1} * (2^{16}-1)*4=5.24s$

The maximum delay achievable would be with the Prescaler of 8 of 5.24s.

Question 2:

Register 8 bit

Clock speed 1MHz

Prescaler 2-256, 2,4,8,16,32,64,128,256

Delay 9.92ms

Max value: upper limit 2^8 -1=255, min 0

$(1MHz)^{-1}$*(max value)*Prescaler =9.92ms

(max value)*Prescaler=(9.92ms)/$((1MHz)^{-1})$

(max value)*Prescaler=9920

(max value)=9920/prescaler=9920/256 trying largest prescaler

Max value=38.75 can't do decimals

Max value = 9920/128=77.5 nope

Max value = 9920/64=155 that we can do (this one)

155 is less than 255 and greater than 0 so it works

checking below to make sure it isnt the only one

Max value = 9920/32=310 No can do its >255

So for a delay of 9.92ms on a 1Mhz clock with an 8bit register, the Prescaler needs to be 64 and the max value needs to be 155.

Question 3

Register 8 bits max of 255

Clock speed 10kHz

Desired total delay 382.5ms

No alteration to max value or Prescaler assuming max register and one for prescale.

$(10kHz)^{-1} * (2^8-1)*1=25.5ms$

25.5ms through one full cycle, how many cycles for 382.5ms

382.5ms/25.5ms = 15 cycles

15 cycles are needed for the setup to reach a net delay of 382.5ms.