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# MOSFET Gate Drive Circuit Design Considerations for Integrated High Switching Frequency Buck Converter


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***Abstract*—nowadays, manufacturers of power management integrated circuits (PMICs) are producing devices that integrate many of the functional blocks required in power supplies in single tiny chips. This paper highlights the design considerations for power MOSFET's gate drivers as a part of highly integrated, high switching frequency (few MHz range) PMICs optimized to be fabricated using CMOS fabrication technologies.**

**The paper is also focused on the effect of parasitic elements associated with integration of the driver and the power MOSFET gate parasitic elements on the performance of an integrated buck converter and its effect on the switching time and loss in power MOSFETs. Finally, a driver has been tested using spice simulations to validate the theory and the results have been presented.**



***Keywords— MOSFET; gate-drivers; switching; Integrated circuit; Miller; Shoot-through;***


## I. Introduction

Many of PMICs manufacturers are going to produce fully integrated power solutions to safe the area needed for the power solution. Integrating power solutions has a lot of limitations depending on the fabrication technology that limits the devices that can be used by the designer.

MOSFET gate driving is similar to driving a very high impedance capacitive network this is because of the fact that the gate is electrically isolated from the source by a silicon dioxide layer so ideally, no current flows into the gate when a dc voltage is applied. However, a very small leakage current flows to maintain the gate voltage and also during the switching periods to charge and discharge the device capacitances [1].

In this paper, MOSFET switching behavior will be analyzed so that an efficient gate driving circuit and the effect of the total gate parasitic elements on the MOSFET switching time can be investigated. After that, some consideration about placing the gate driver on the IC will be discussed and some switching problems - when using the driver as a part on a synchronous buck converter - have been highlighted.

## II. MOSFET Switching Behavior

Usually, power MOSFET is modeled using its terminal capacitances as shown in Fig.1. These non-linear and voltage dependent capacitances in addition to the gate–drive circuit output impedance determine the device switching speed.

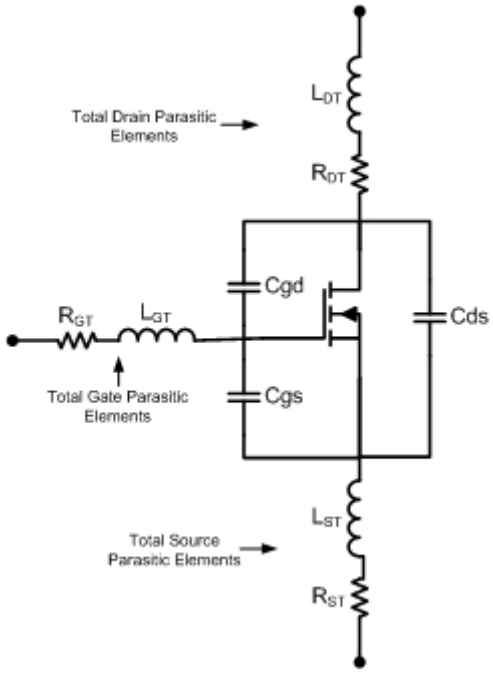


Figure.1: MOSFET's parasitic elements.

When MOSFET is considered with these additional parasitic elements shown in the above figure, it becomes increasingly difficult to derive equations that describe the switching behavior of the MOSFET. Ignoring the parasitic inductances, source and drain resistances; it is possible to come up with

formulas for the turn-on and turn-off time periods of MOSFET [2], [3], [4], [5].

*MOSFET turn on:*
MOSFET's turning on transition is consists of four basic periods as illustrated in Fig. 2.

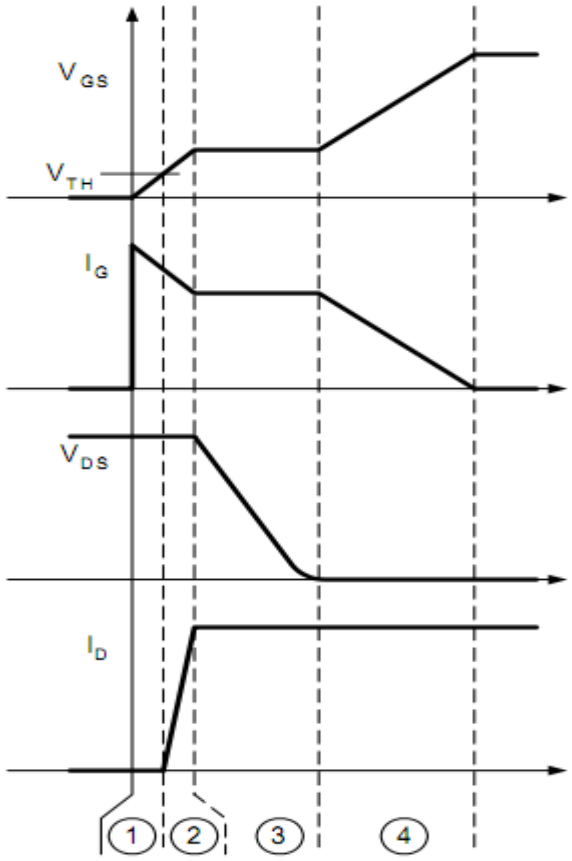


Figure.2: Simplified MOSFET turn on transition.

*Period 1 ($t_1$):*
In this period, MOSFET's gate to source voltage ($V_{gs}$) starts to increase to the threshold voltage ($V_{th}$) and no current flows from drain to source. During this period most of the gate current is charging $C_{gs}$ and a small current charging $C_{gd}$. Period time can be estimated using the following equation:

$$t_1 = R_G(C_{GS} + C_{GD}) \ln\left[\frac{1}{1-\frac{V_{th}}{V_{GS\_final}}}\right] \quad (1)$$

*Period 2 ($t_2$):*
In this period, the gate voltage goes from $V_{th}$ to miller voltage $V_{GP}$, the gate current continues charging the gate capacitances and drain current is rising to its final value. Period time can be estimated using the following equation:

$$t_2 = R_G(C_{GS} + C_{GD}) \ln\left[\frac{1}{1-\frac{V_{GP}}{V_{GS\_final}}}\right] \quad (2)$$

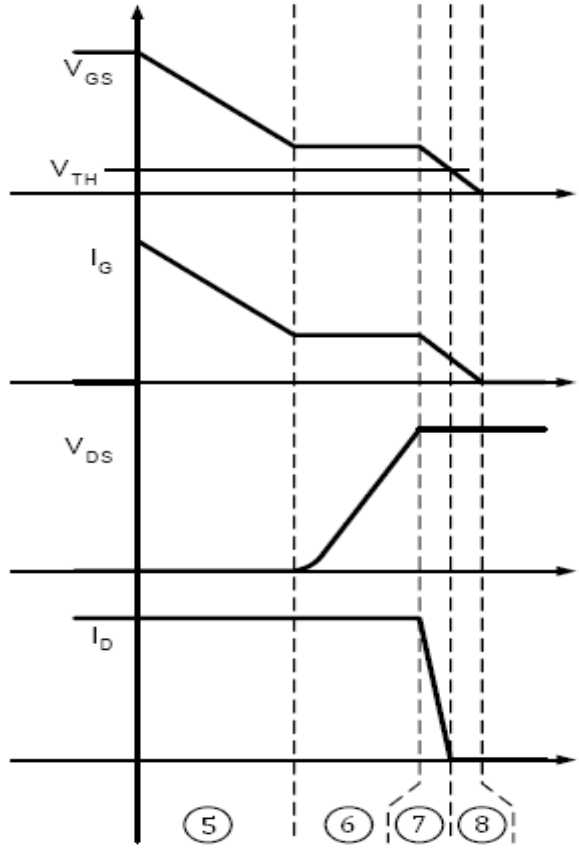


Figure.3: Simplified MOSFET turn off transition.

*Period 3 ($t_3$):*
This period is called "Miller period" as a sufficient current from the driver goes to discharge $C_{gd}$ to compensate the rapid change in the $V_{ds}$ voltage and $V_{gs}$ is almost constant and equals miller voltage $V_{GP}$. During this period, $V_{ds}$ goes to its final value $V_{ds}$(on). Period time can be estimated using the following equation:

$$t_3 = \frac{(V_{DS}-V_F)R_G C_{GD}}{V_{GS\_final}-V_{GP}} \quad (3)$$

Where: $V_F$ is darin to source voltage when MOSFET is 'ON'
$V_{DS}$ is drain to source voltage when MOSFET is 'OFF'

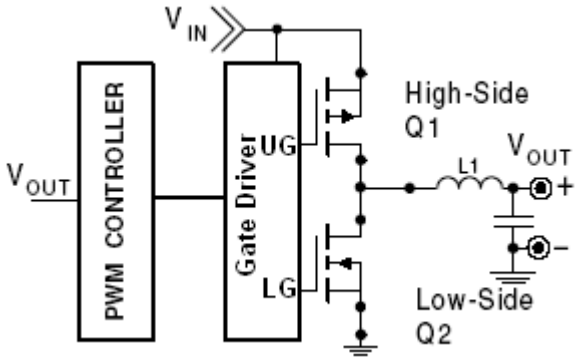


Figure.4: Synchronous buck converter

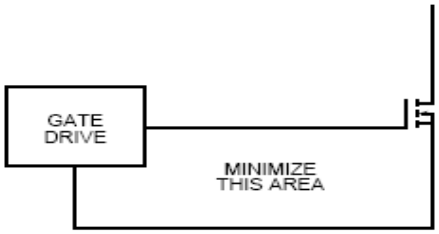


Figure.5: Minimizing gate driver impedance.

*Period 4 ($t_4$):*

During this period, gate to source voltage goes to its final value and the gate current is shared equally between $C_{gd}$ amd $C_{gs}$ and MOSFET is considered to be 'ON' but its $R_{ds}$ resistance reaches its final value at the end of this period.

*MOSFET turn off:*

Using the same principles of turn-on transitions, the turn off transition is also consists of four basic periods as illustrated in Fig. 3 and can be calculated using the following equations:

$$t_5 = R_G(C_{GS} + C_{GD})\ln\left[\frac{V_{GS\_APP}}{V_{GP}}\right] \quad (4)$$

$$t_6 = R_G C_{GD}\left[\frac{V_{DS}-V_F}{V_{GP}}\right] \quad (5)$$

$$t_7 = R_G(C_{GS} + C_{GD})\left[\frac{V_{GP}}{V_{th}}\right] \quad (6)$$

## III. Gate Drive Circuit for High Switching Frequency, Fully Integrated Buck converter

From the preceding discussion, simple gate driver must be able to charge and discharge the input capacitance of the MOSFET. Figure.4 shows a simple configuration of synchronous buck converter [6]. Digital logic circuits (TTL or CMOS) can easily be used to drive directly the gate of power MOSFET. Because CMOS has limited source current and sink current capabilities, the modest delay in rise time and fall time are expected due to the Miller effect. On the other hand, BJTs that can be implemented using CMOS fabrication technologies have poor characteristic and can only provide one type of BJTs [7].

To facilitate higher switching frequency operation and faster switching, the P and N channel complimentary pair MOSFET driver is usually used. MOSFET Totem Pole is inverting and offers voltage gain to improve on the pre driver rise and fall times. Unfortunately, CMOS driver suffers from shoot through current, caused by the threshold voltage overlap during on and off transitions. In order to gain the benefits from CMOS based driver, more circuits should be added to the gate driver.

Problems most often encountered with the gate drive circuit are voltage spikes large enough to breakdown the gate oxide, oscillation, ringing or false turn-on. Usually, these problems can be solved by a proper layout and the electrical design of the driver circuit. To minimize these problems, the following design rules and precautions should be followed when designing and laying out driver circuits [8].

## IV. Design Considerations for MOSFET Gate Drive Circuits

Usually the design process are expressed on the following capacitance; input, output, and reverse common source capacitances (*Ciss*; *Coss* , and *Crss* , respectively). All these capacitances are related according to the following:

$C_{iss} = C_{gs} + C_{gd}$ when $C_{ds}$ is shorted (7)

$C_{oss} = C_{ds} + C_{gd}$ when $C_{gs}$ is shorted (8)

$C_{rss} = C_{gd}$ (9)

The device switching speed depends largely on $C_{rss}$ and the total gate driver output impedance seen from the MOSFET's gate, so the designer should make the gate drive circuit very near to the MOSFET to minimize the parasitic elements cased by wiring inside the chip. This concept is illustrated in Fig. 5. The interconnection from the gate driver to the MOSFET can be modeled with a lumped inductance and can be calculated using the rectangular conductor inductance formula; also the resistance can be calculated by using the rectangular conductor resistance formula.

The designer should make the driving circuit to be under-damped RLC circuit with a predetermined overshoot to achieve high switching speeds.

***Shoot-through problem***

Shoot-through is defined as the condition when both MOSFETs are either fully or partially turned on, providing a path for current to "shoot-through" from the input voltage to the ground [9], [10]. Shoot-through can be minimized by means of inserting dead time between switching signals applied on the gate of buck converter's MOSFETs to make sure

that the two switches will never go 'ON' together and leads to shorting the input voltage source. Usually the insertion of dead time is made using a break before make switching circuit as shown in Fig. 6.

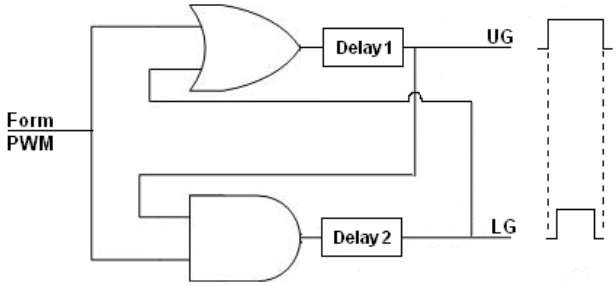


Figure.6: Dead time generator

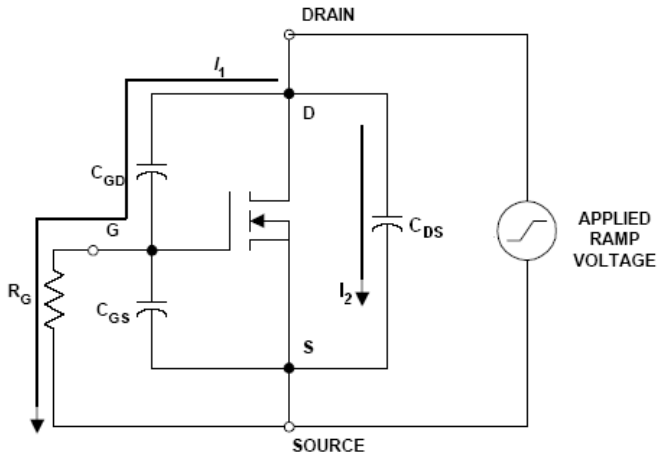


Figure.7: Shoot-trough problem on the low side MOSFET

Another type of shoot-through occurs when the high-side MOSFET is turning on and a high *dv/dt* on the drain of the low side MOSFET couples charge through $C_{GD}$ and make it to turn on. This phenomenon is illustrated in Fig. 7. It is clearly noticeable that the faster the high-side MOSFET is turned on, the more susceptible the low-side synchronous MOSFET becomes to *dv/dt*-induced turn-on [5].

## V. The Effect of Gate Parasitic Elements On Switching Behavior - Spice Simulations -

A CMOS based gate drive circuit has been simulated using SPICE program for 5MHz synchronous buck converter. The circuit has input voltage of 2.5V, output voltage of 1.2V and 10A of load.

The methodology that used to investigate the effect of the total equivalent gate resistance ($R_{GT}$) and the total gate equivalent inductance ($L_{GT}$) on the switching behavior of integrated buck depended on testing three circuits; the first circuit is to test the CMOS based gate driver without adding any gate parasitic elements, the second circuit includes only $R_{GT}$. Finally, in the third circuit the effect of $L_{GT}$ and $R_{GT}$ has been considered.

Switching waveforms is shown in Figs. 8-11; Figs. 8, 9 show the effect of parasitic on high side MOSFET (P-Channel MOSFET) turn-on and turn-off respectively. Similarly Figs. 10, 11 show the effect of parasitic on low side MOSFET (N-Channel MOSFET) turn-on and turn-off respectively.

Simulation results shows that, gate equivalent parasitic resistance increases switching time specially miller period which increases switching loss of the MOSFET specially when the switch is turning-off, so it is recommended to reduce the gate resistance as minimum as possible.

Adding the equivalent gate inductance – which has been omitted in the previous circuits for purpose of simulation only – can improve the switching behavior of the MOSFET. But the designer should take care of the overshoot on the source-to gate voltage. Excess overshoot can cause an unexpected operation on the switch.

Another investigation has been made by simulating the buck converter using 50% of the used gate parasitic elements to illustrate the improvement in converter losses. Table.1 summarizes all the results obtained from the simulated circuits. In this case, adding $L_{GT}$ to the circuit increases the overshoot and causes a false turn-on of the low side MOSFET (shoot-through) as shown in Fig. 12.

| Gate Parasitic | | Efficiency | Switching Loss | |
|---|---|---|---|---|
| | | | High Side | Low Side |
| Parasitic-free | | 88.3% | 204 mW | 74 mW |
| 100% | $R_{GT}$ | 81.8% | 1241 mW | 164 mW |
| | $R_{GT}$ + $L_{GT}$ | 82.5% | 1121 mW | 146 mW |
| 50% | $R_{GT}$ | 86.5% | 501 mW | 90 mW |
| | $R_{GT}$ + $L_{GT}$ | 86.7% | 446 mW | 100 mW |

Table.1: Simulation results for synchronous buck

## VI. Conclusion

Successful design of a MOSFET gate driver not only depends on the selection of a low impedance driver circuit topology but also is strongly dependent on the IC layout. If a low impedance driver circuit is employed and the gate parasitic elements are properly taken into account, higher switching frequencies could be used.

The designer of gate drivers for integrated synchronous buck converter should take care of the following rules:

1- Providing dead time (break before make switching) to cancel shorting the input voltage source.
2- The driver must be able to drive the capacitive gate of power MOSFETs.

3- Make the gate drive circuit as close as possible to the power MOSFET to minimize the total gate parasitic elements.

Also the designer should optimize the high-side MOSFET switch to avoid the shoot-through problems due to high *dv/dt* on the low side MOSFET.

## VII. Acknowledgement

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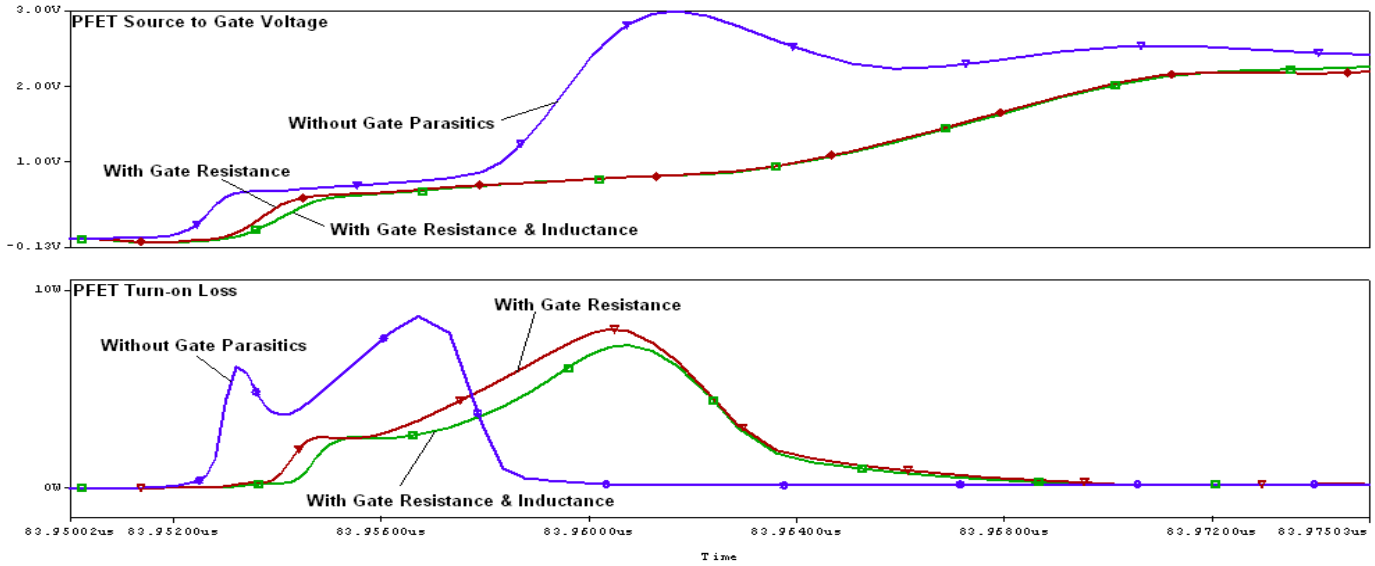


Figure.8: High Side MOSFET Turn-on Period

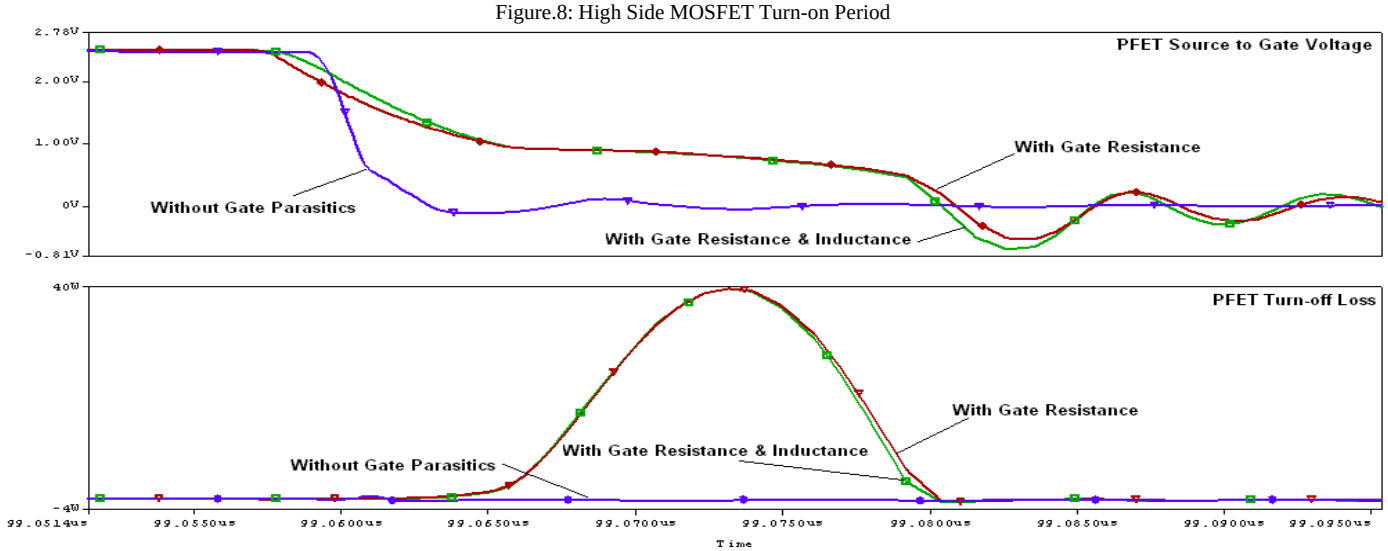


Figure.9: High Side MOSFET Turn-off Period

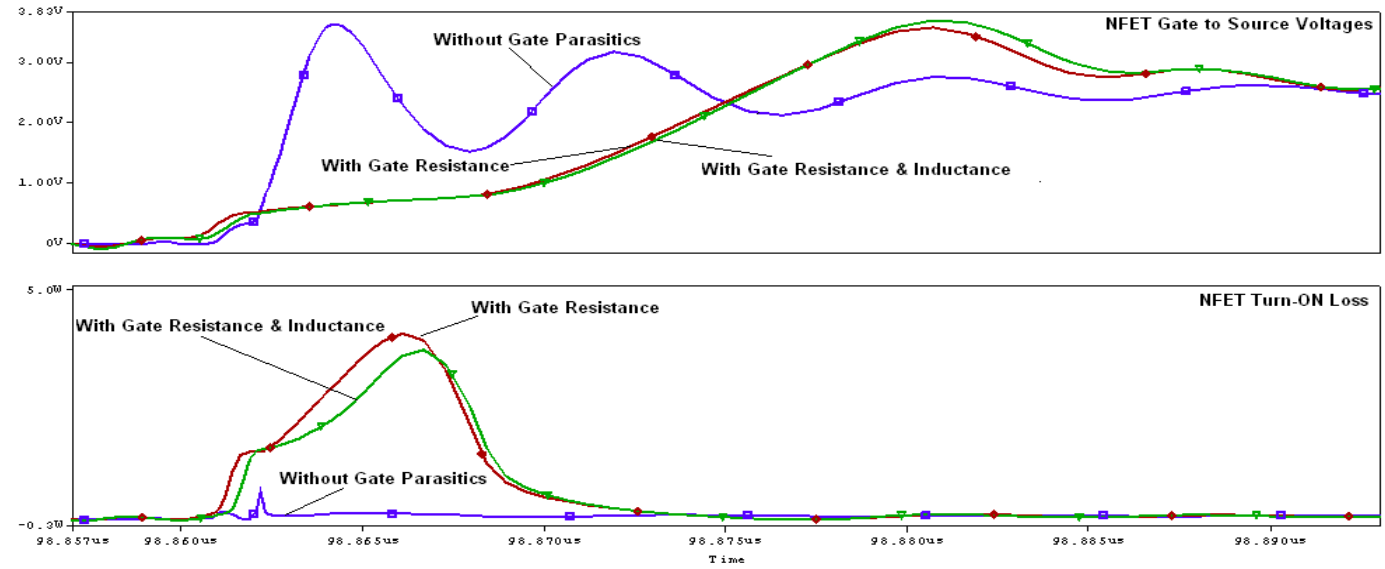


Figure.10: Low Side MOSFET Turn-on Period

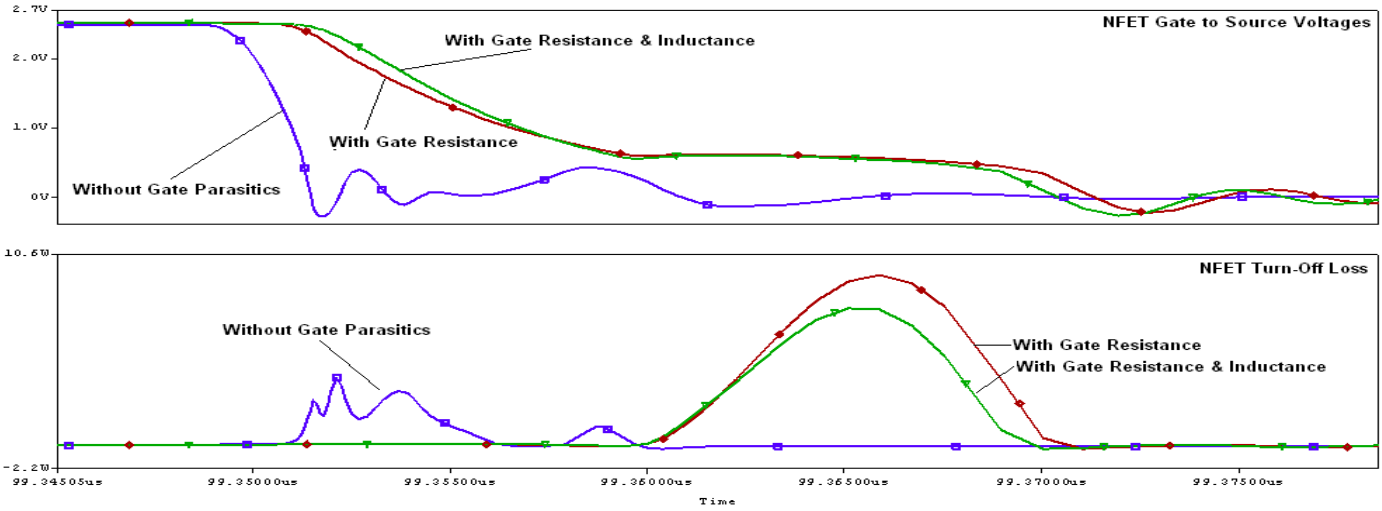


Figure.11: Low Side MOSFET Turn-off Period.

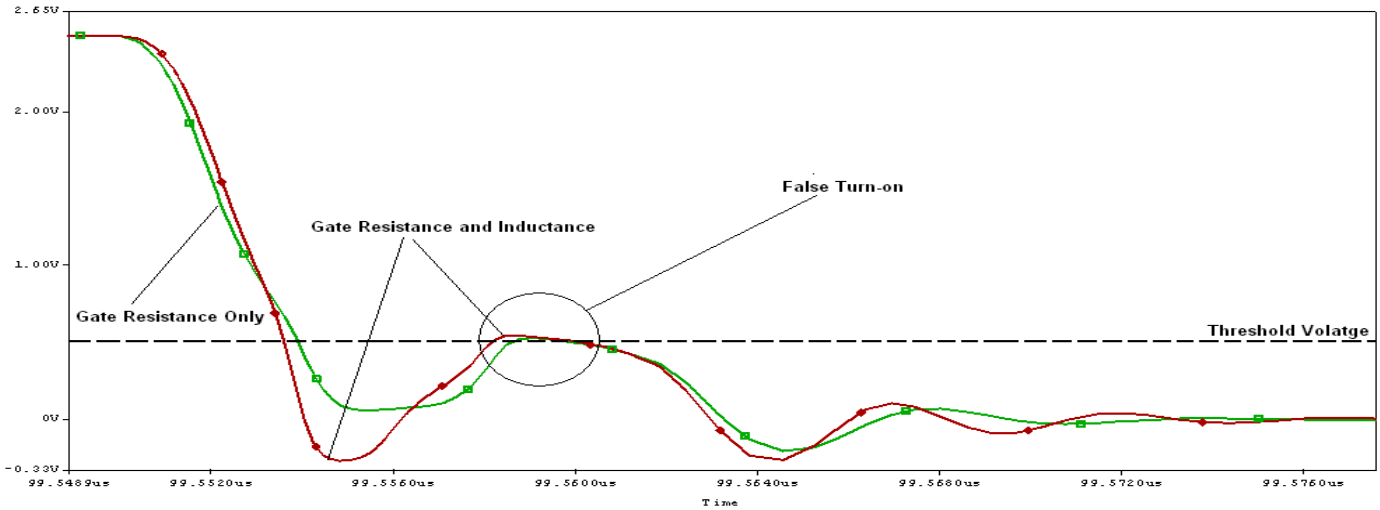


Figure 12: False Turn-on on low side MOSFET caused by gate-source voltage Oscillation.