RISC-V Processor Design

Fascicle 8: Yosys/Icestorm/Arachnepnr/Nextpnr tools

(15 minutes)
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UNIVERSITY OF CAMBRIDGE

University of Cambridge
Department of Engineering

Physical Computation Laboratory

Intended Learning Outcomes for Today

By the end of today's session, you will be able to:

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❸ Use Yosys to check whether certain signal values are possible in your design

❹ Use Yosys to visualize your at the RTL, gate, and Verilog block levels

```
module e4Encoder_8bitData_1bitControl(dataIn, worstCaseDeviationCode, encoderOut);
        input           [7:0]   dataIn;
        input           [0:0]   worstCaseDeviationCode;
        output reg      [7:0]   encoderOut;

        reg             [7:0]   M1encoderOut;

        reg             [7:0]   M1dataIn;



        always @ (*)
        begin
                case (worstCaseDeviationCode)
                        1'b0:
                        begin
                                M1dataIn = 8'h00;
                        end

                        1'b1:
                        begin
                                M1dataIn = dataIn;
                        end
                endcase



                /*
                 *      M1dataIn => worst-case deviation is '10'
                 */
                case (M1dataIn)
                        8'h00,8'h01,8'h02,8'h03,
                        8'h04,8'h05,8'h06,8'h07,
                        8'h08,8'h09,8'h0A       : M1encoderOut = 8'h00;
                        8'h0B                   : M1encoderOut = 8'h01;
                        8'h0C,8'h0D             : M1encoderOut = 8'h03;
                        8'h0E,8'h10,8'h11       : M1encoderOut = 8'h07;
                        8'h0F,8'h12,8'h13,8'h14,
                        8'h15,8'h16,8'h17,8'h18,

    ...
                        8'hF5,8'hF6,8'hF7,8'hF8,
                        8'hF9,8'hFA,8'hFB,8'hFC,
                        8'hFD,8'hFE,8'hFF        : M1encoderOut = 8'hFF;
                        default                  : M1encoderOut = 8'h00;
                endcase /* M1dataIn */



                /*
                 *      Select the final output from amongst the sub-encoder blocks.
                 */
                case (worstCaseDeviationCode)
                        1'b0: encoderOut = dataIn;
                        1'b1: encoderOut = M1encoderOut;
                        default : encoderOut = dataIn;
                endcase
        end /* always @ (*) */
endmodule /* e4Encoder_8bitData_1bitControl */
```

Use Yosys to Apply an Input to Combinational Logic


```
$ yosys -p "hierarchy -check; proc; opt; fsm; opt; memory; opt; eval -set
dataIn 8'h33 -set worstCaseDeviationCode 1'b1 -show M1dataIn -show M1encoder
-show encoderOut" e4Encoder_8bitData_1bitControl.v
```

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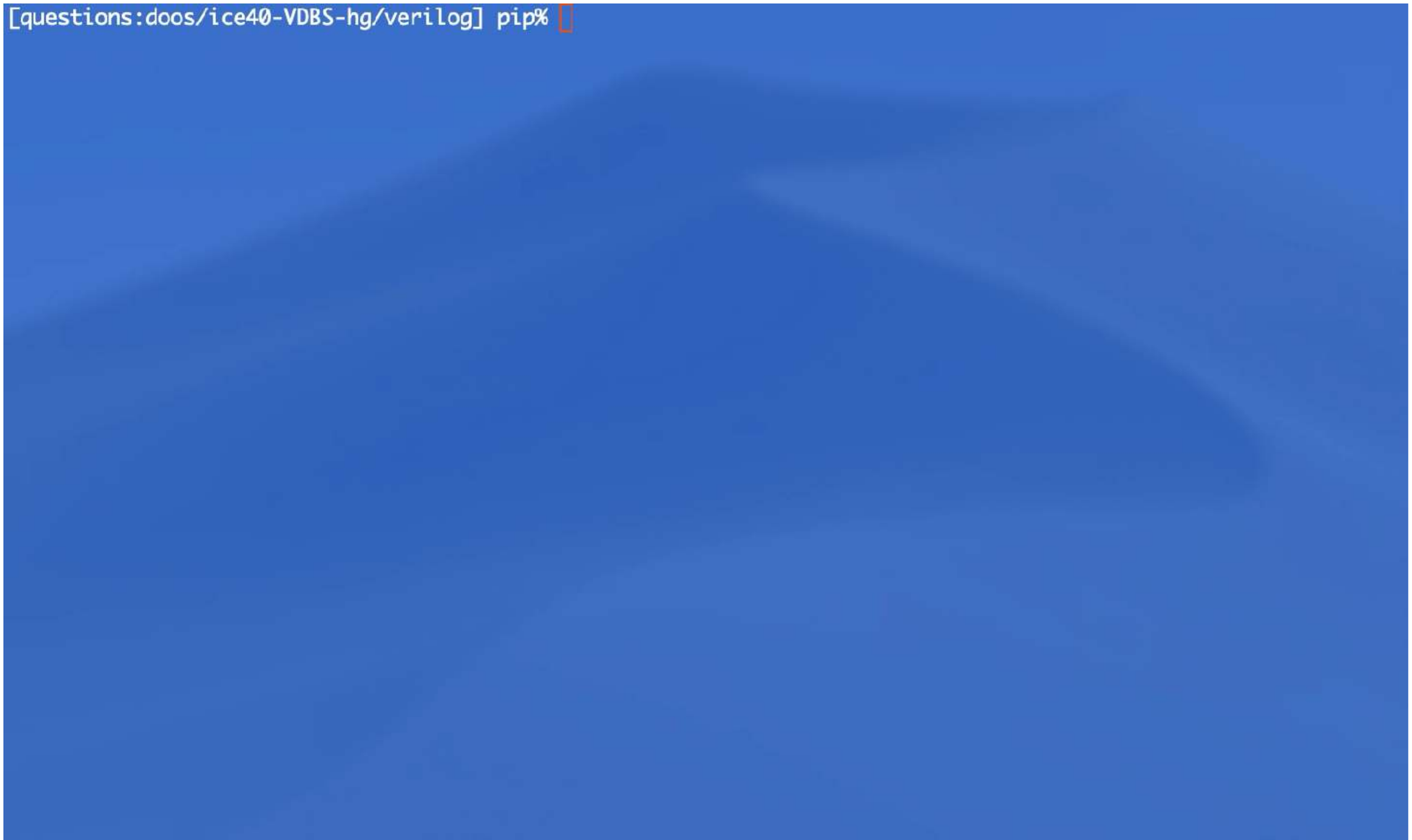
dataIn 8'h33 -set worstCaseDeviationCode 1'b1 -show M1dataIn -show M1encoder
-show encoderOut" e4Encoder_8bitData_1bitControl.v
```

Use Yosys to Evaluate a Truth Table for a Combinational Block

```
$ yosys -p "hierarchy -check; proc; opt; fsm; opt; memory; opt; eval -table
worstCaseDeviationCode,dataIn" e4Encoder_8bitData_1bitControl.v
```



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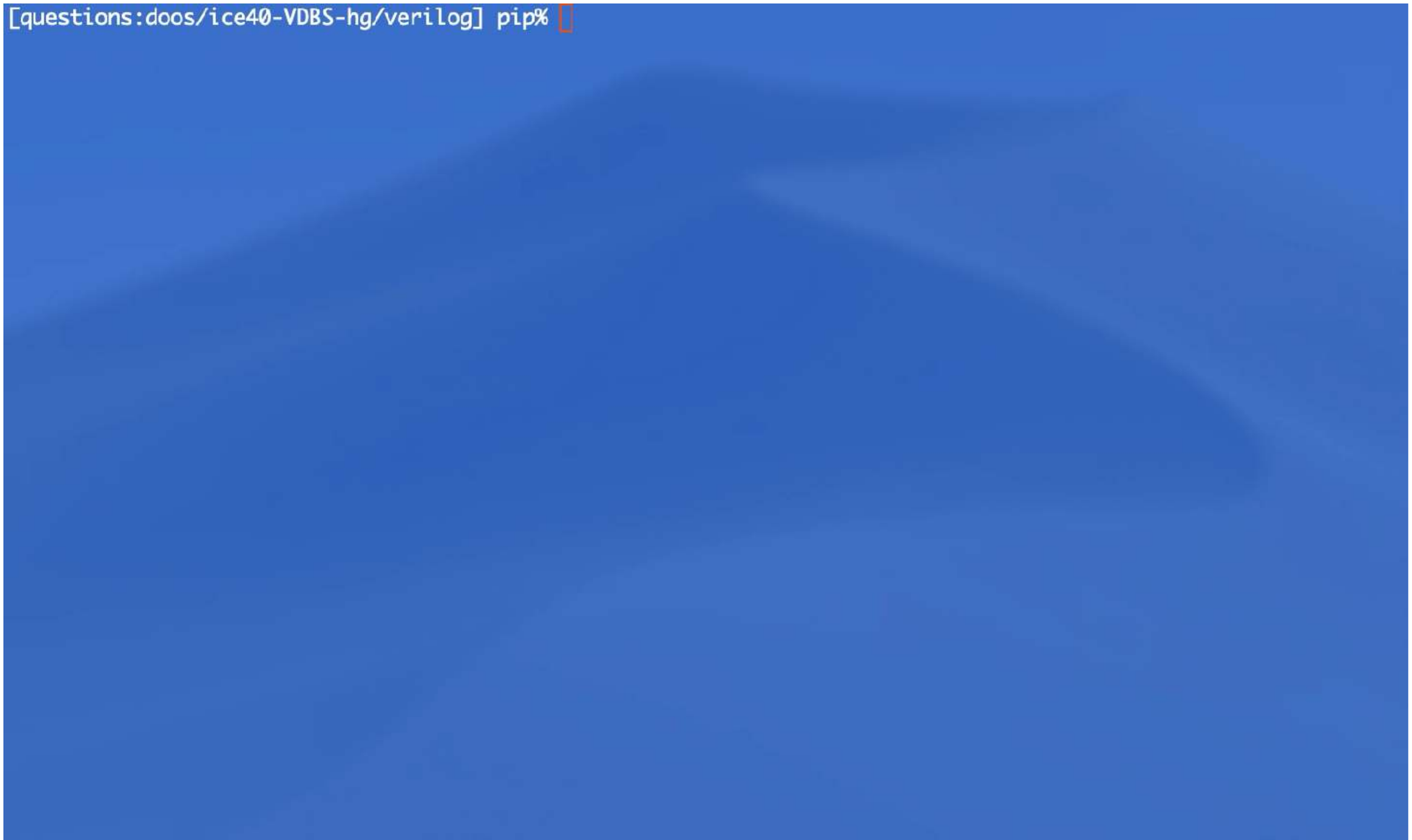

Use Yosys to Check Satisfiability for a Set of Conditions

```
$ yosys -p "hierarchy -check; proc; opt; fsm; opt; memory; opt; sat -set
encoderOut 8'b01111111" e4Encoder_8bitData_1bitControl.v
```

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encoderOut 8'b01111111" e4Encoder_8bitData_1bitControl.v
```
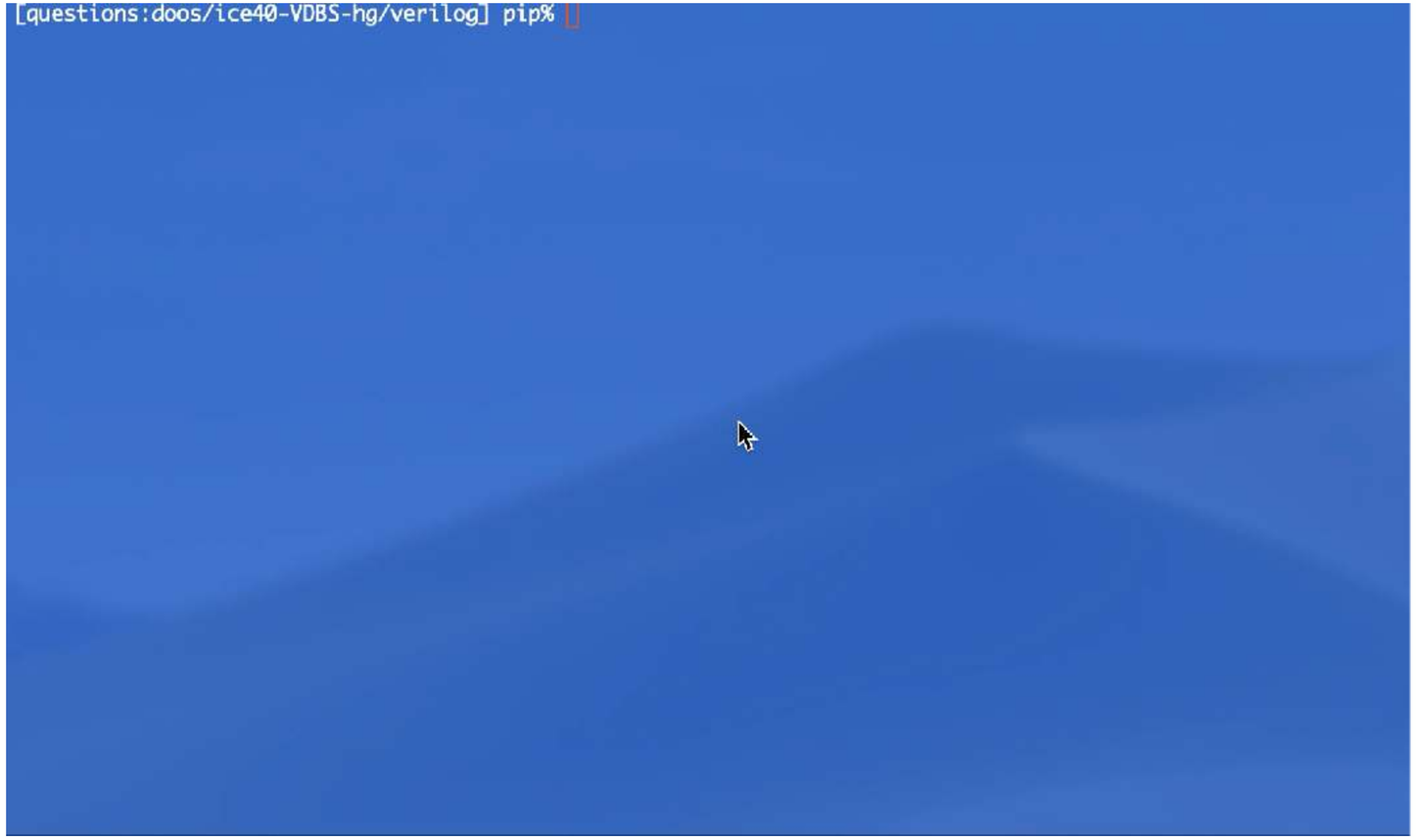

Use Yosys to Visualize Design at the Logic Gate Level

```
$ yosys -p 'hierarchy -check; proc; opt; fsm; opt; memory; opt; techmap; opt;
splitnets -ports; show -lib ./simlib.v -format pdf -prefix
e4Encoder_8bitData_1bitControl-cmos -colors 33 -width -stretch'
e4Encoder_8bitData_1bitControl.v
```



Next, view the generated file `e4Encoder_8bitData_1bitControl-rtl.pdf` using a PDF viewer

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e4Encoder_8bitData_1bitControl.v
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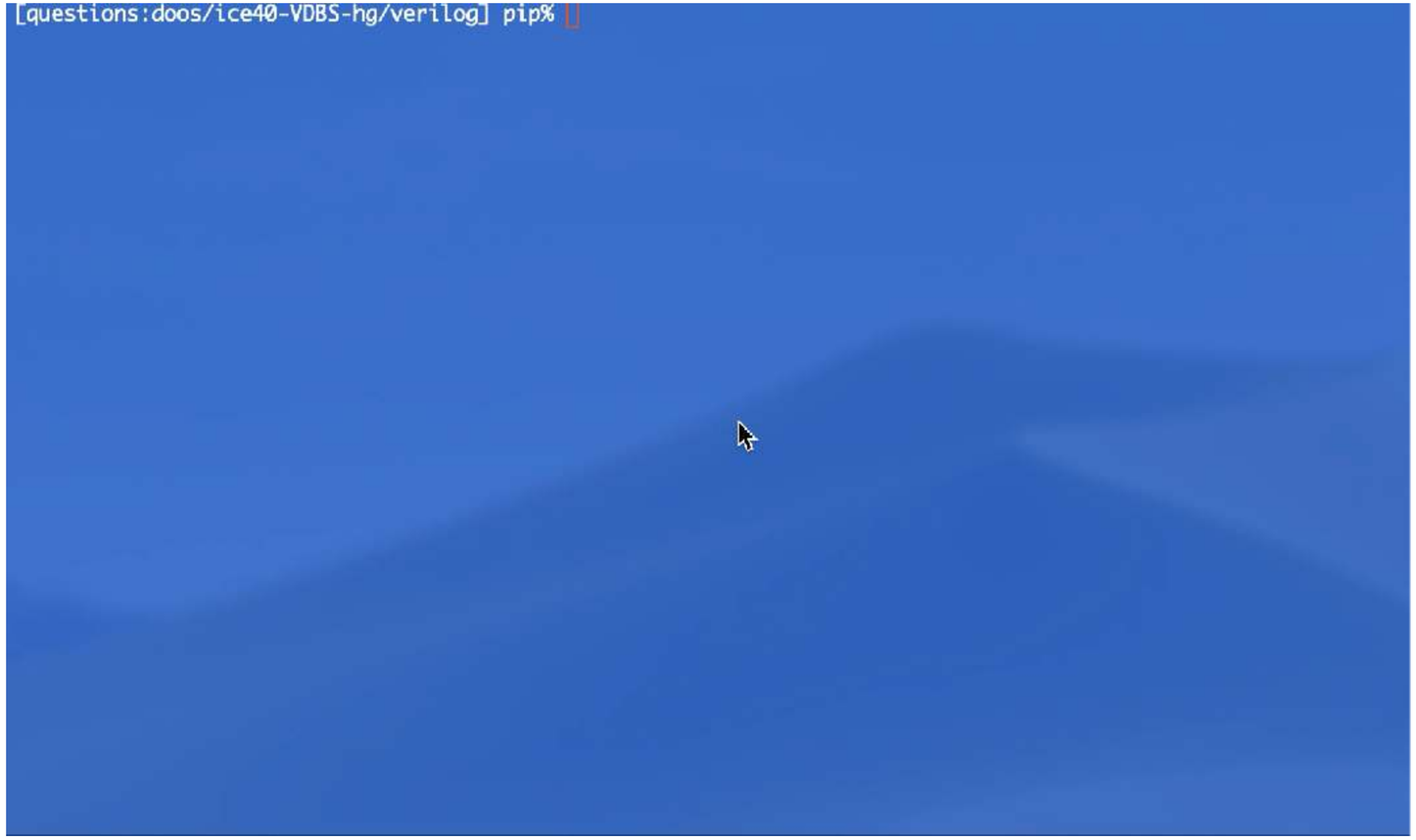

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Use Yosys to Visualize Design at the RTL-Block Level


```
$ yosys -p 'hierarchy -check; proc; opt; fsm; opt; memory; opt; show -format
pdf -prefix e4Encoder_8bitData_1bitControl-rtl -colors 33 -width -stretch'
e4Encoder_8bitData_1bitControl.v
```

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e4Encoder_8bitData_1bitControl.v
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Things to Do

❶ Drop off a **“muddiest point” sheet when you can**

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