VLSI Part 1 Submission – Group 5

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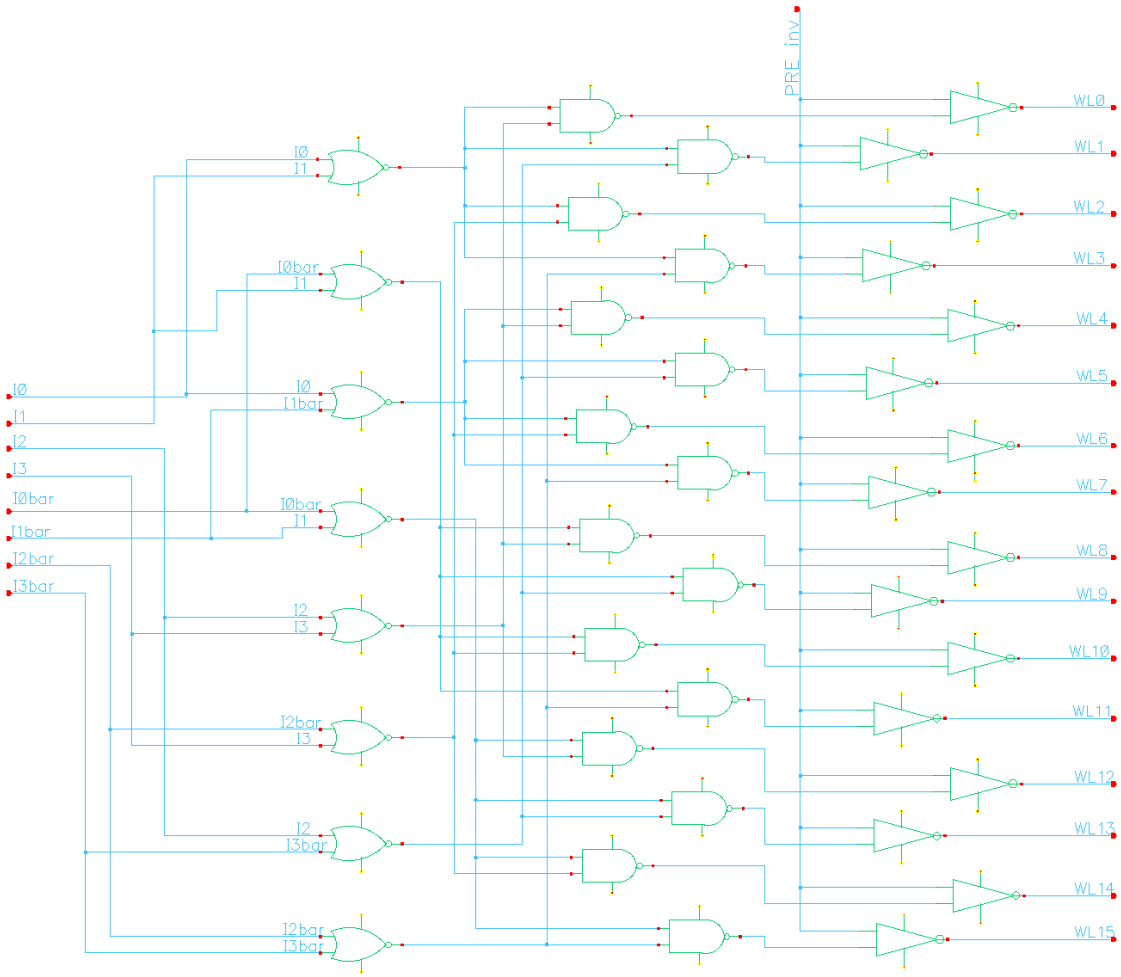
Table of Abbreviations

CLK	Clock
RE	Read Enable
WE	Write Enable
WL	Word Line
BL	Bit Line
BL_BAR	Bit Line Bar
PRE	Precharge
SA	Sense Amplifier
SAE	Sense Amplifier Enable
D	Data (Input of flip-flop)

Problem 1 – Decoder Logic

Top Level Schematic of Decoder



The top level decoder is shown above. Here, I0 to I3 and I0bar to I3bar are inputs the decoder will receive from the address register. WL0 to WL15 are the [WL] outputs which are synced with [PRE] signal, i.e. WL will not get low at the falling edge of [CLK]. But it will go low after approximately 200ps (50% of CLK). This is done so that we get more time in later part of the memory system. This allows us to reduce the size of SRAM cells because we will have more time margin for read and write operations (charging of [BL] & [BLbar] lines).

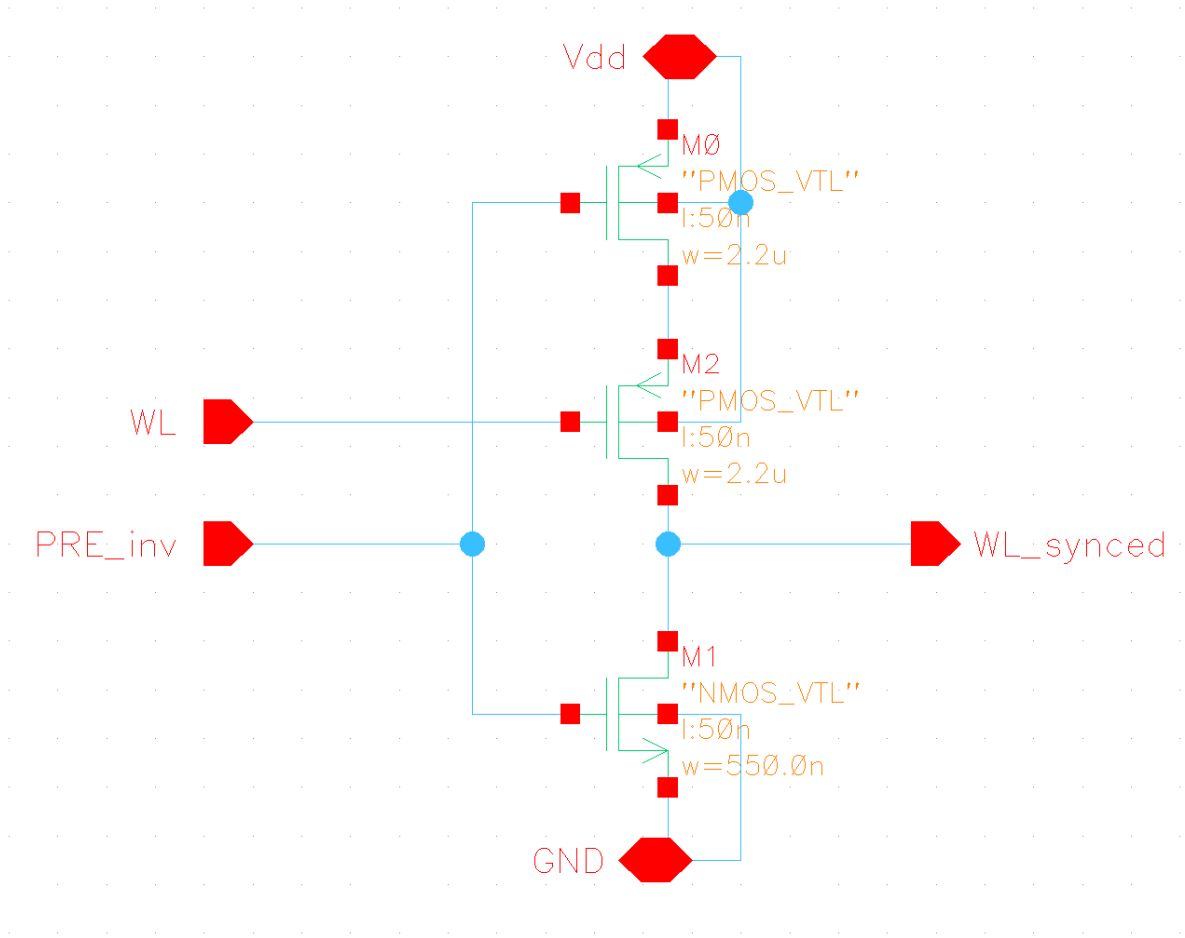
The logic that is implemented here is of CMOS predecoder. The inputs which are common between Word lines are merged and processed together, so as to remove the redundant logic gates and reduce the delay in critical path. Another main benefit of predecoder is that it reduces the fan-in of [WL] from 4 conventionally, to 2 in this case. This helps in optimizing the delay.

Here, static CMOS is used because it consumes lowest power and is the most robust.

In static CMOS also, NAND-NOR implementation (NAND in predecode stage & NOR in WL stage) is more easier as it does not need inversion at the output and gives correct functionality (i.e. turns WL ON when logic satisfies). But NOR is not good at pulling up, as it has transistors in series in Pull up network.

So, we have used the NOR-NAND implementation here. It gives 0 at the WL output when logic satisfies, but we want the [WL] to be 1 when the logic satisfies. So we have also used inverter at the end.

However, the inverter is not a regular inverter. It is a dynamic inverter that uses Pull Up Network to implement the logic. The reason for doing this is that dynamic logic has floating conditions. But we want [WL] to be 0 in all conditions except when logic satisfies. So in order to remove the floating condition, we use the below dynamic circuit.



What this circuit does is that it basically reverses the conventional dynamic logic implementation. When [PRE_inv] (inverted PRE signal) is 1, i.e. when [PRE] = 0, it does not

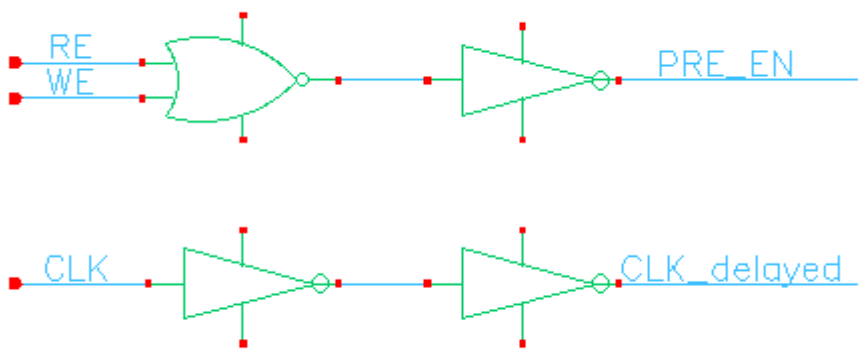
evaluate, rather it pulls the output node to 0. And when [PRE_inv] is 0, it evaluates the logic. The NOR-NAND logic which we have implemented here, gives 0 when logic satisfies. So when WL=0 gets coupled with PRE_inv=0, we get inverted WL, i.e. we get output 1 at the WL_synced pin.

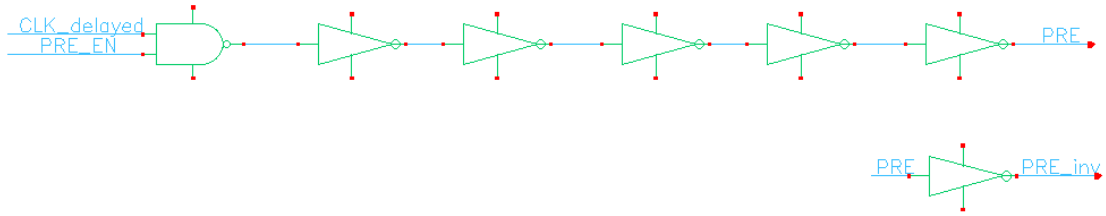
Apart from the resolved floating conditions of the this dynamic inverter, the added advantage of using this technique is that it ANDs the [PRE] signal with [WL] signal at low area cost.

Schematic of WL Logic

[WL] logic is implemented by ANDing the [PRE] signal with [WL] decoder output. The [PRE] signal itself is generated from the [CLK] by delaying the [CLK]. This delay is approximately equal to the Flipflop delay + decoder delay. So that in this time, the [PRE] is 0 which allows charging of the BL & BLbar.

Also, the [PRE] signal is only generated when either [RE] or [WE] are ON. Because when we are not doing any read or write operation, we don't want any [WL] to turn ON. This is done by keeping [PRE] to 0 when none of the [RE] or [WE] are high. It is implemented by the logic below.



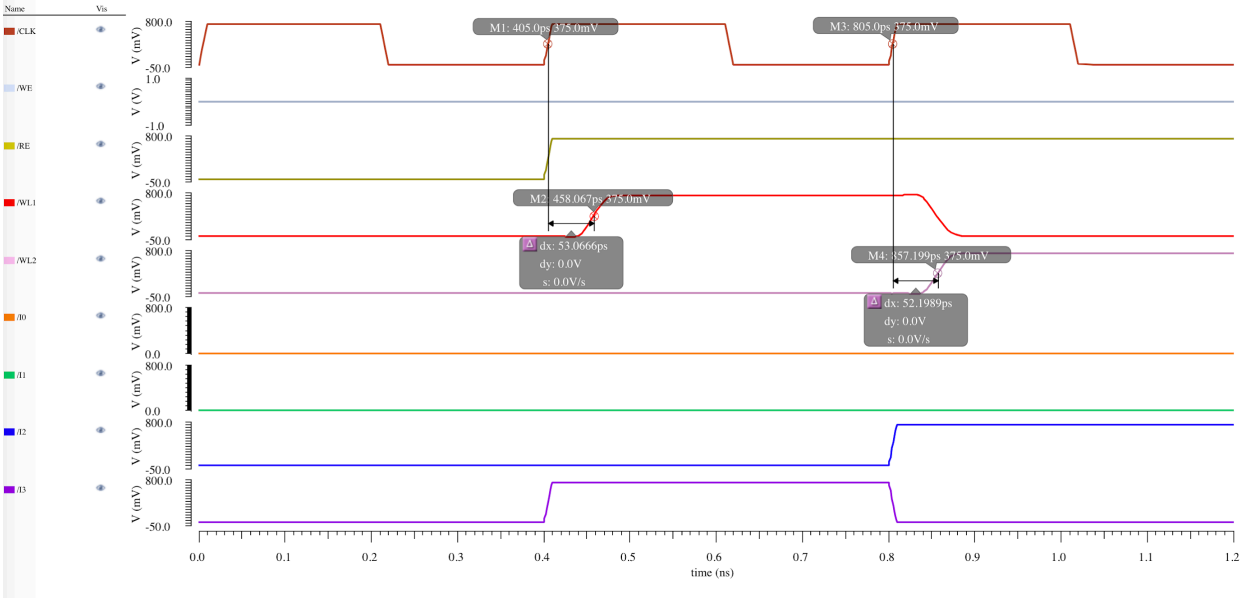


The CLK_delayed signal is generated here to match the delay of [RE]+[WE] with the [CLK] with which we AND, in order to get the output of [PRE].

Waveforms of Operation

Timing and Power

Delay from rising edge of the [CLK] to the rising edge of [WL] = 53.0666ps



Delay from falling edge of the [CLK] to the falling edge of [WL] = 113.193ps
Average Power dissipation = 41 microwatt

Problem 2 – Address and Data Register

Schematic of Single Flip-Flop

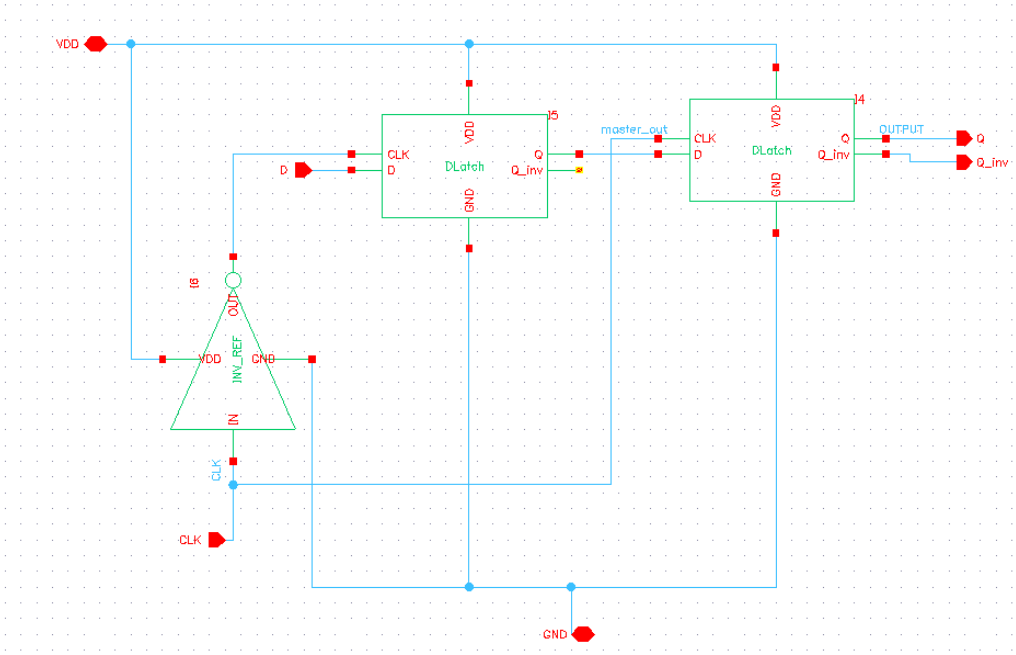


Figure (2.1): Single Flip-Flop

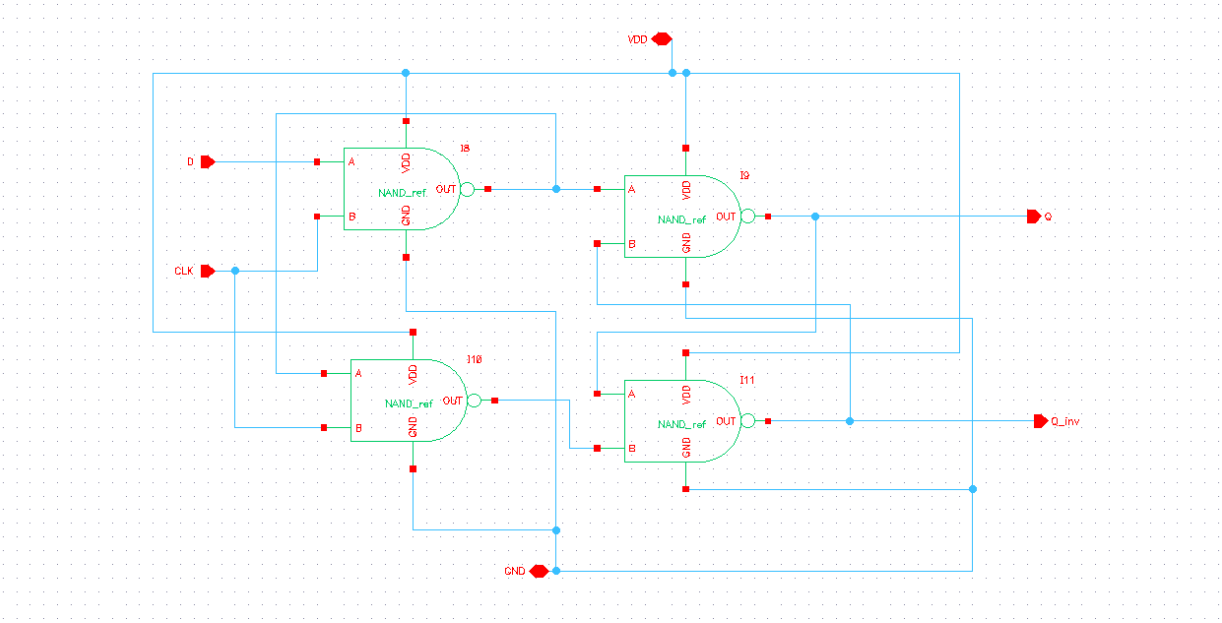


Figure (2.2): Single D-Latch

* See appendix B for NAND2 gate circuit parameters.

Description of Design Style

For the flip-flop, we utilized Master-slave flip-flop. We a little upsized the NAND Gate in D-Latch to drive the connected write circuit, which is connected to a very large output capacitor. We also tried smaller size of flip-flop, but it led to unsmooth output of the flip-flop. This is because the write circuit is heavier than the flip-flop.

In out flip-flop, we got the follow properties.

1. C-Q Delay : 27.014 ps [Refer Figure (2.7)]
2. SetUp Time: 10 ps [Refer Figure (2.8)]
3. Hold Time: 0 ps
4. Power Dissipation: 64.33E-6 (single flip-flop)

Waveforms of Operation

In Figure (2.4), the output data [Out] of flip-flop followed the input data [Data] when the clock is rising [Clk]. Then [Out] held the signal when [Clk] is not on positive edge.

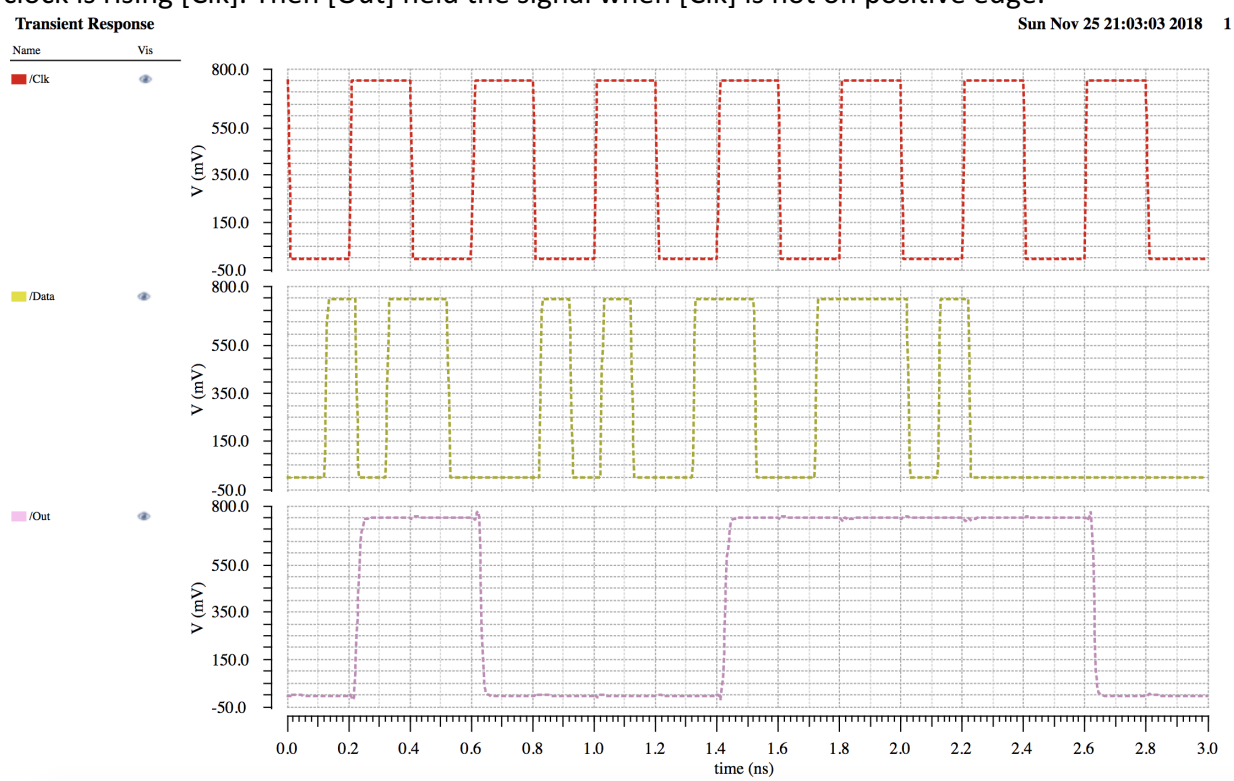


Figure (2.4): Output of single flip-flop

In Figure (2.5) and Figure (2.6), the two different [Out] signals are shown. In FIgure (2.5), [Data] arrived right violating the setup time. Therefore, [Out] at 2.2ns went low. On the other hand, in Figure (2.6), [Data] arrived satisfying setup time, so [Out] at 2.2ns went back to high voltage.

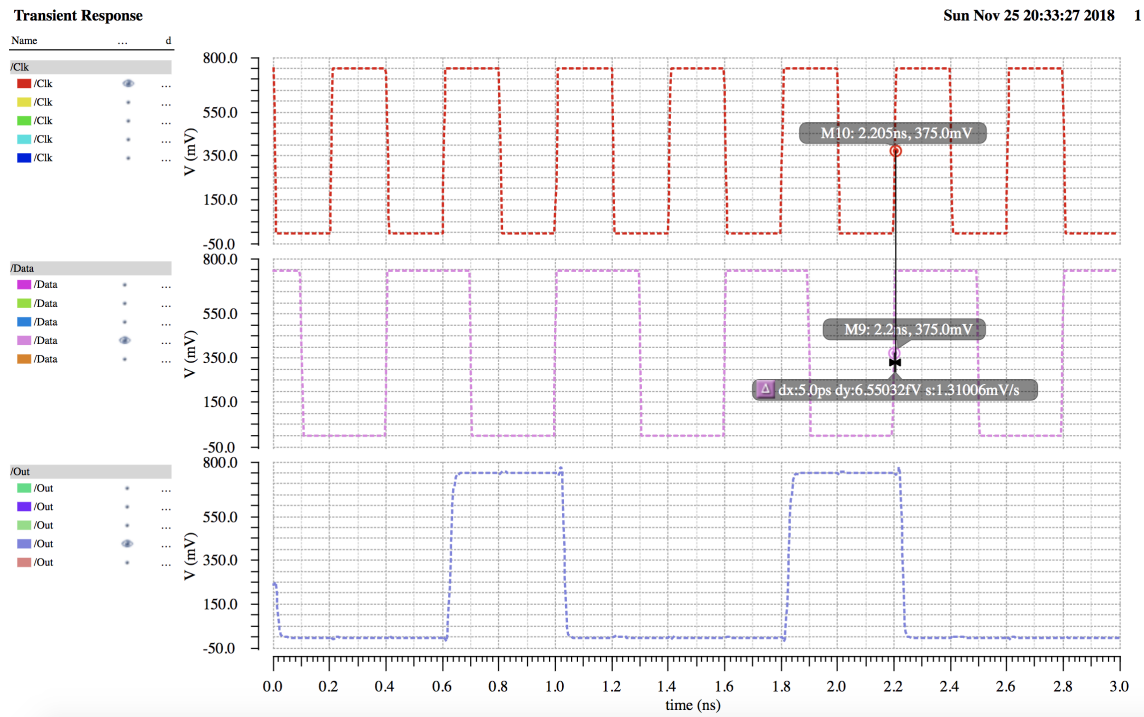


Figure (2.5): Test on input right just violating the setup requirement

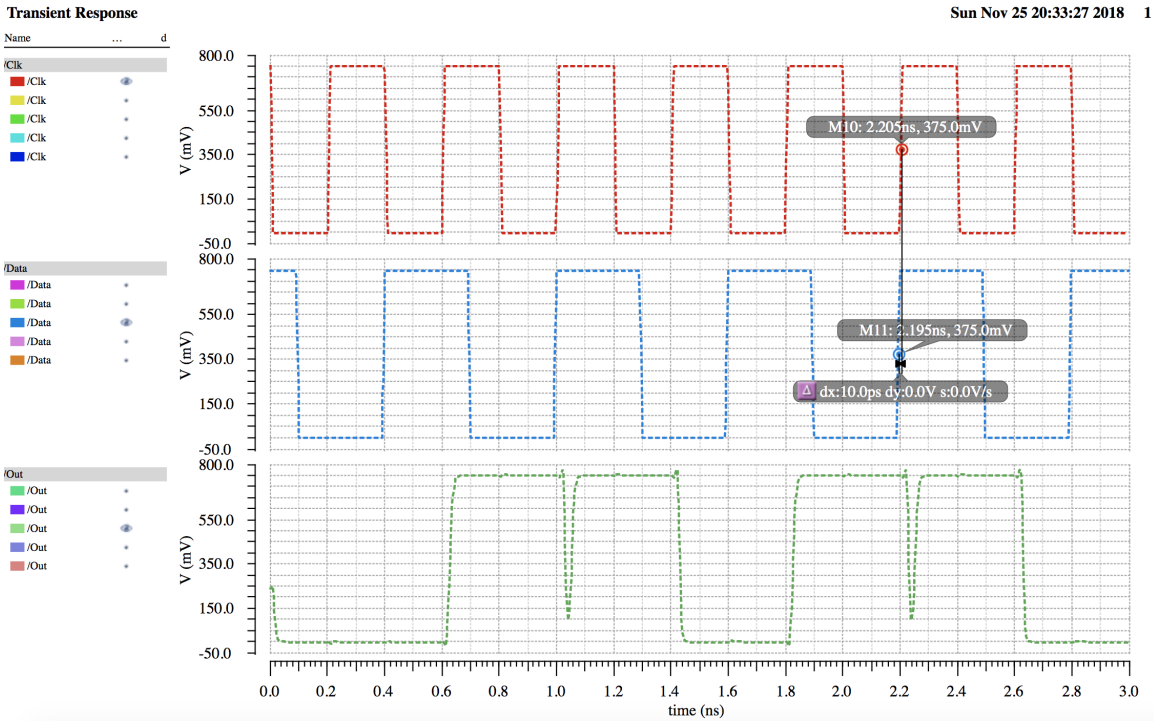


Figure (2.6): Testing on input just satisfying setup requirement

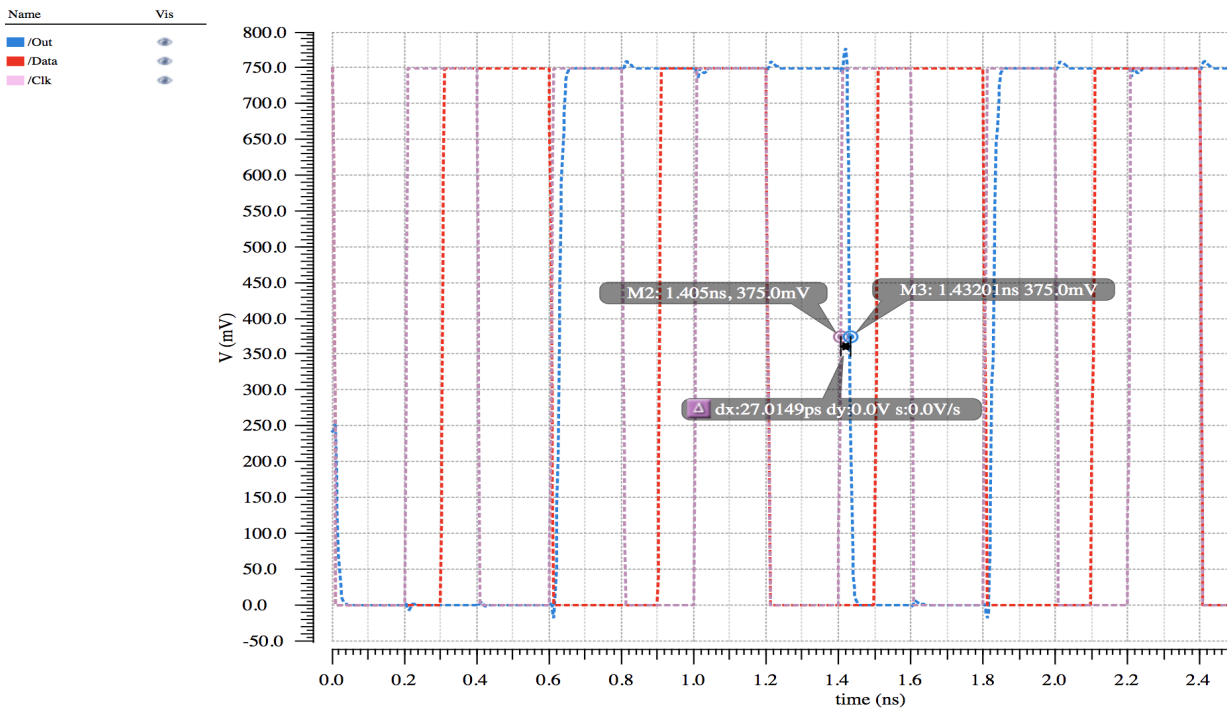


Figure (2.7): CLK-Q Delay for single flip-flop

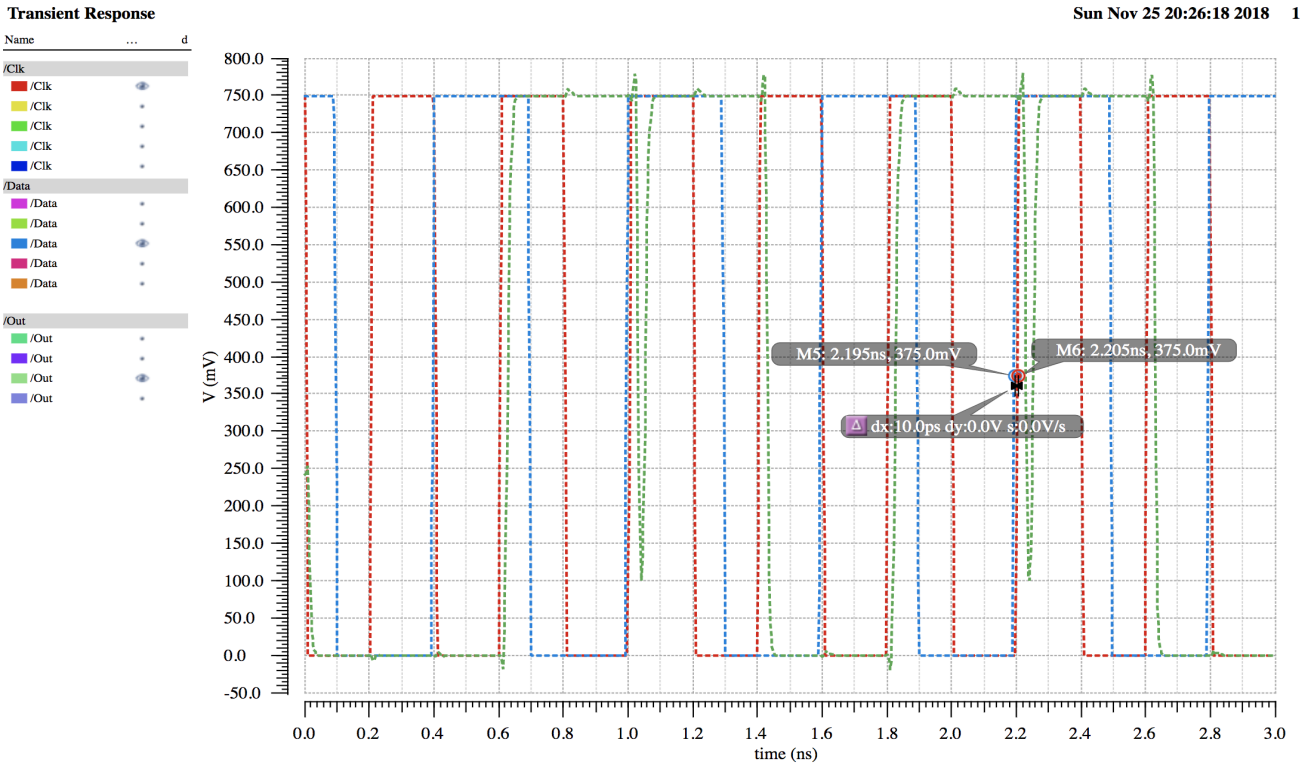


Figure (2.8): Setup time for single flip-flop

Problem 3 – Write Circuitry

Schematic

We connected one write circuit unit to output of our data register (as Figure (3.1)) to test our write circuit.

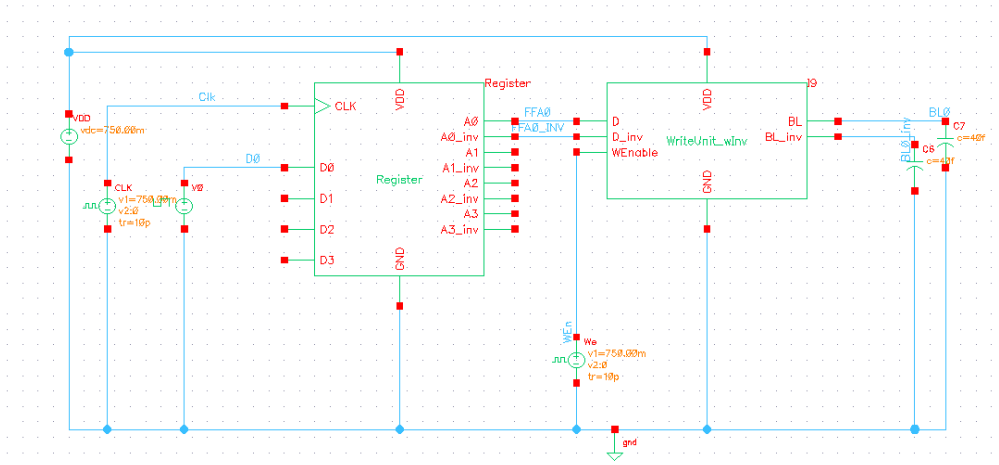


Figure (3.1): Testing Circuit

In our write circuit, we put an inverter chain (N = 2, u = 7.3441) before our transmission gate. This is because the bitline capacitance is very large (40 fC). We firstly put the inverter chain after the transmission gate. If so, we can make the transmission gate smaller. However, the inverter chain would keep pushing to the bit line even [WE] was off, which made the read circuit did not work correctly. To solve this problem, we put inverter chain before transmission gate and upsized the transmission gate.

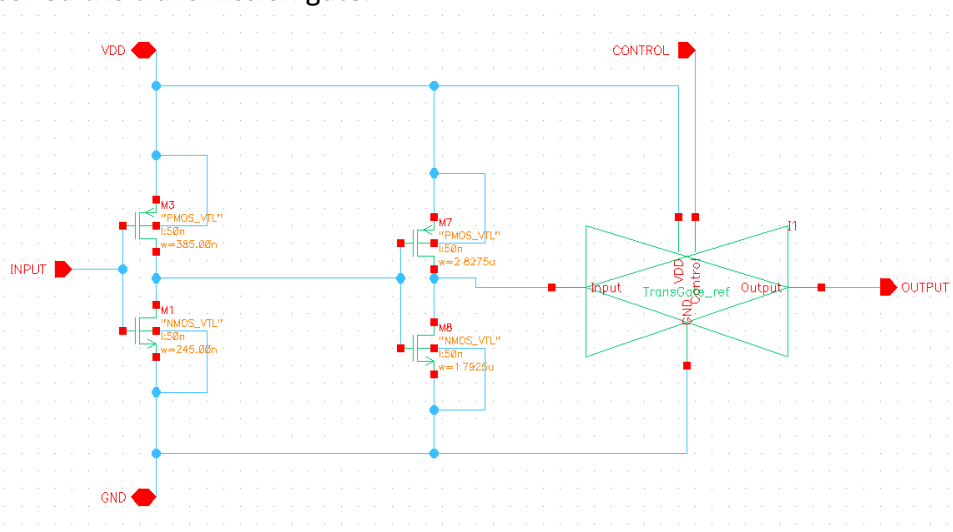


Figure (3.2): Write Circuit (In WriteUnit_wInv)

* See appendix C for write enable transmission gate parameters.

Testing Strategy

As the waveform below (Figure (3.4)), we can see:

1. When the [WE] signal is off, [BL] signal holds in the previous signal. [1.0ns - 1.4ns]
2. When the [WE] signal is on.
    a. When [D0] signal is high, the [BL0] signal goes high. [0.6ns]
    b. When [D0] signal is low, the [BL0] signal goes low. [1.4ns]
3. The [BL0_Inv] signal is always the inverted [BL0] signal.

Waveforms

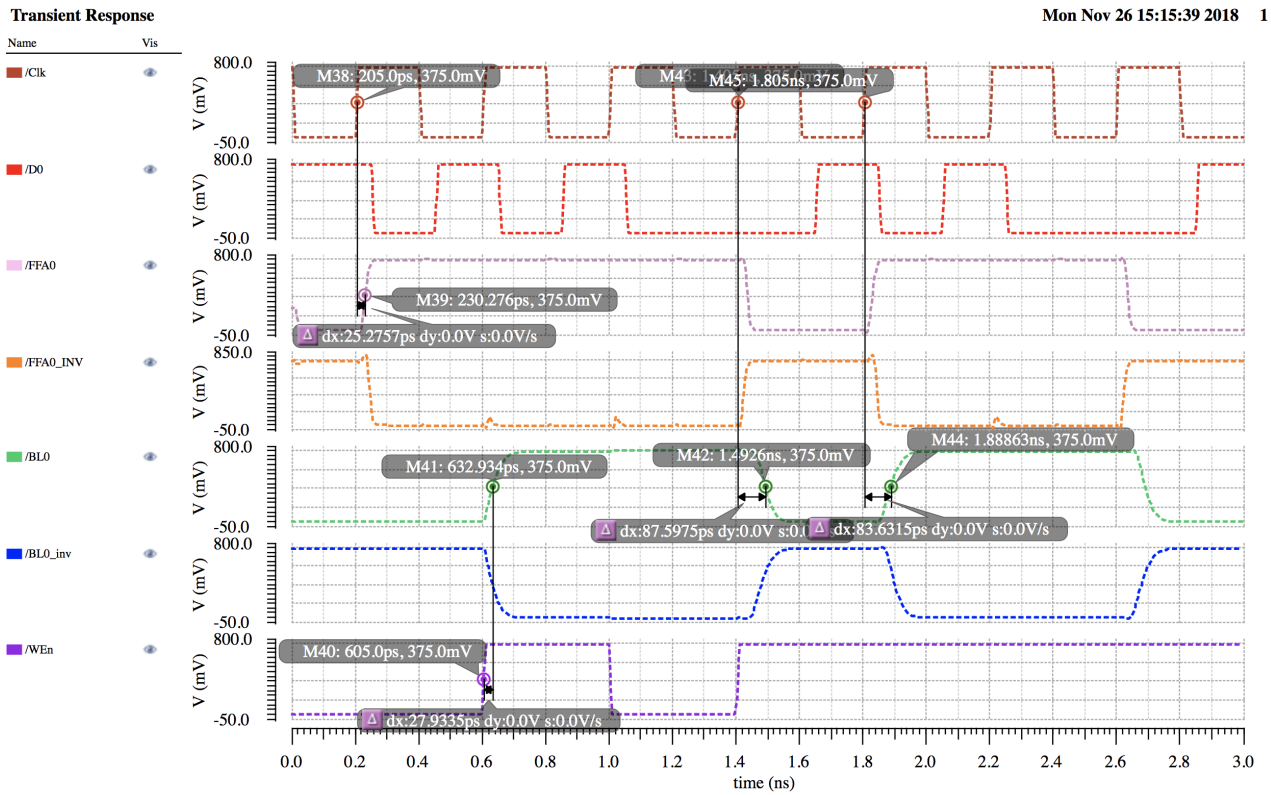


Figure (3.4): Waveform of the testing circuit (Figure (3.1)).

Timing

- Pre-charge is not related to write circuit.
- [D] signal has to arrive before setup time.
- Delay between positive edge [CLK] signal to [BL] signal is 83.632ps(low-to-high) and 87.596ps(high-to-low).
  *Shown in Figure (3.4) between 1.4ns and 1.9ns
    - This means the [WL] signal has to arrive after around 88ps of the start of the period. *This will be discussed more in problem 5.
- If the data register is already holding the signal which we want to write to the cell, then the delay is 27.9335ps. [Shown in Figure (3.4) at 0.6ns]

Problem 4 – Read Circuitry

Operation

The read circuit first uses an active low signal Precharge [PRE] to charge both BL and BL_bar to VDD. The PRE signal goes high once the bit lines have been charged to VDD, and cuts off the bit lines from the voltage supply.

The bit lines will slowly discharge since the charge is held in the bit line capacitances (assumed to be 40 fF). When the word line signal [WL] goes high, the access transistors connect the bit lines to the SRAM cell. One bit line will begin discharging quickly, denoting that it is connected to the node holding logic 0, and the opposite line was connected to the node holding logic 1.

A sense amplifier is then used to amplify the differential voltage between the two bit lines, and a latch then gives a steady output of VDD or 0 depending on which bit line was discharged. The output of the latch is the data that was stored in the SRAM cell.

Schematic

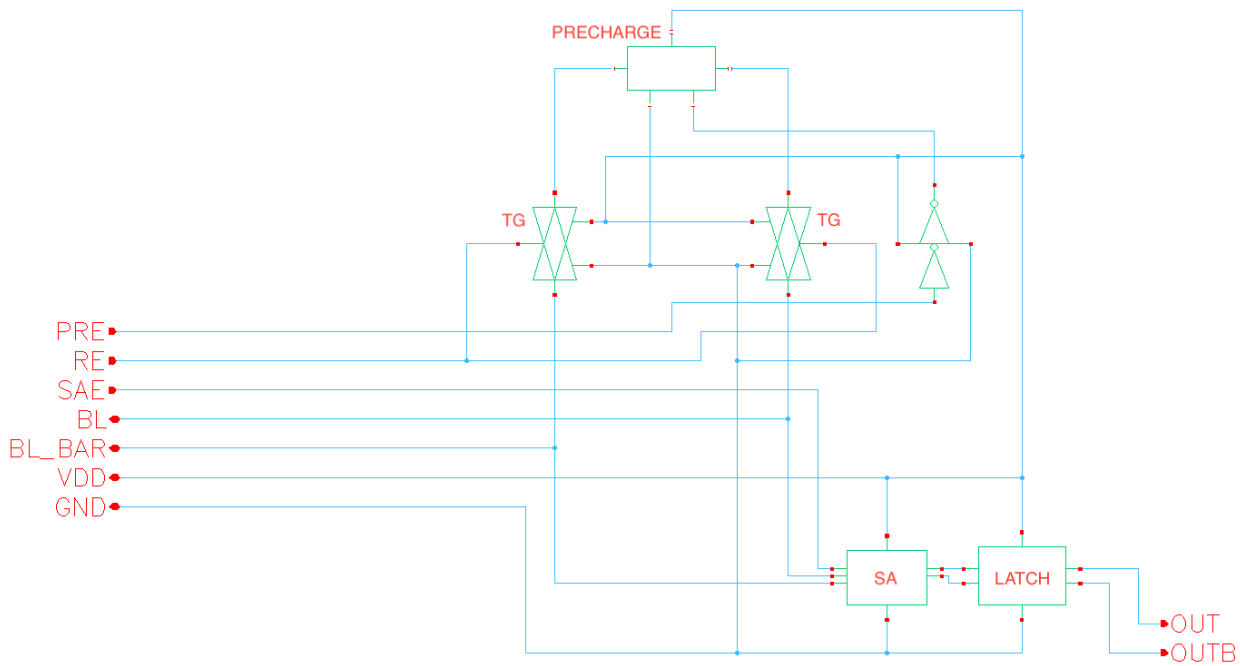


Figure (4.1): Read Circuitry Cadence Schematic

* See appendix D for precharge, sense amplifier, latch, transmission gate, and inverter chain circuit parameters.

Testing Strategy

<u>Precharge</u>

_____We test the precharge circuit by simply ensuring that the bit lines charge to VDD while [PRE] is low, and stop charging when the signal goes high.

Reading

To test whether the read circuit has the correct functionality, we can set waveforms for BL and BL_bar such that one signal discharges while the other remains constant. We turn on the sense amplifier using the [SAE] signal at some time after the discharging begins. The output at the latch should be VDD if BL_bar discharges, and 0 if BL discharges.

Figure (4.2) shows the output we expect to see if the read circuit is functioning properly.

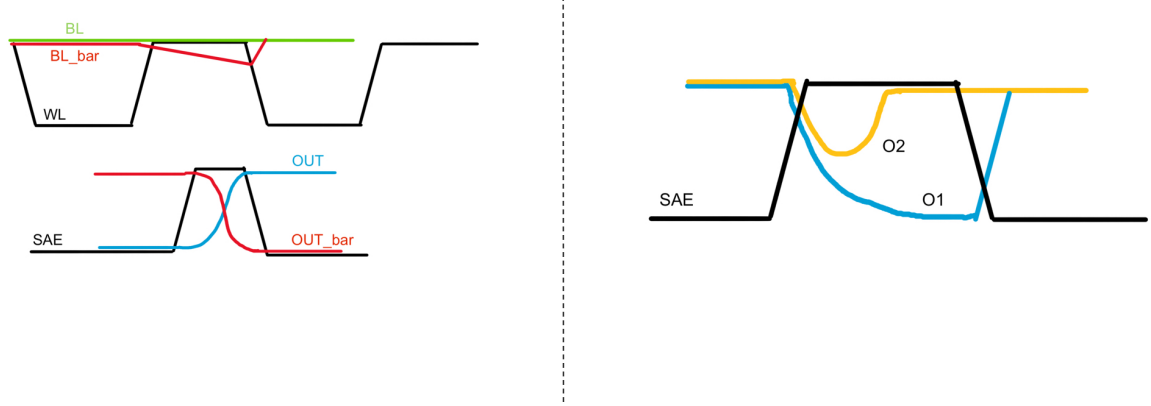


Figure (4.2): Expected Waveforms for Read Circuit

Important Signal Considerations

- The [PRE] signal should low until both bit lines are charged. The pulse width of [PRE] should be synced with [WL] since the bit lines should only be connected to the SRAM cell once both lines are charged.
- The [SAE] should only go high after [WL] and [PRE] have both gone high. Since the bit lines need to have discharged to some value before the sense amplifier can properly detect a voltage differential. [SAE] should also fall in sync with [WL] and [PRE] to ensure the sensing is complete by the time both bit lines begin to charge again.
- [SAE] should be only for as little time as possible and should only be high during a read cycle to conserve power.

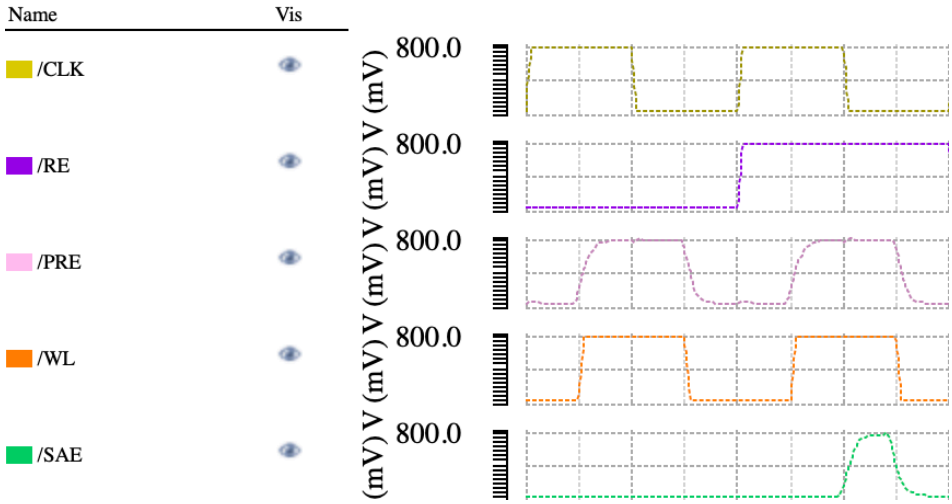


Figure (4.3): Global Synchronization for Read Circuit

The timing waveforms shown in Figure (4.3) show the global synchronization implemented to ensure the functionality of the read operation. The Precharge [PRE] and Sense Amplifier Enable [SAE] signals are generated from Clock [CLK] and Read Enable [RE]. Note that the Word Line [WL] signal has not been generated yet and has been simulated using an ideal pulse.

<u>Cadence Simulation of Read Operation</u>

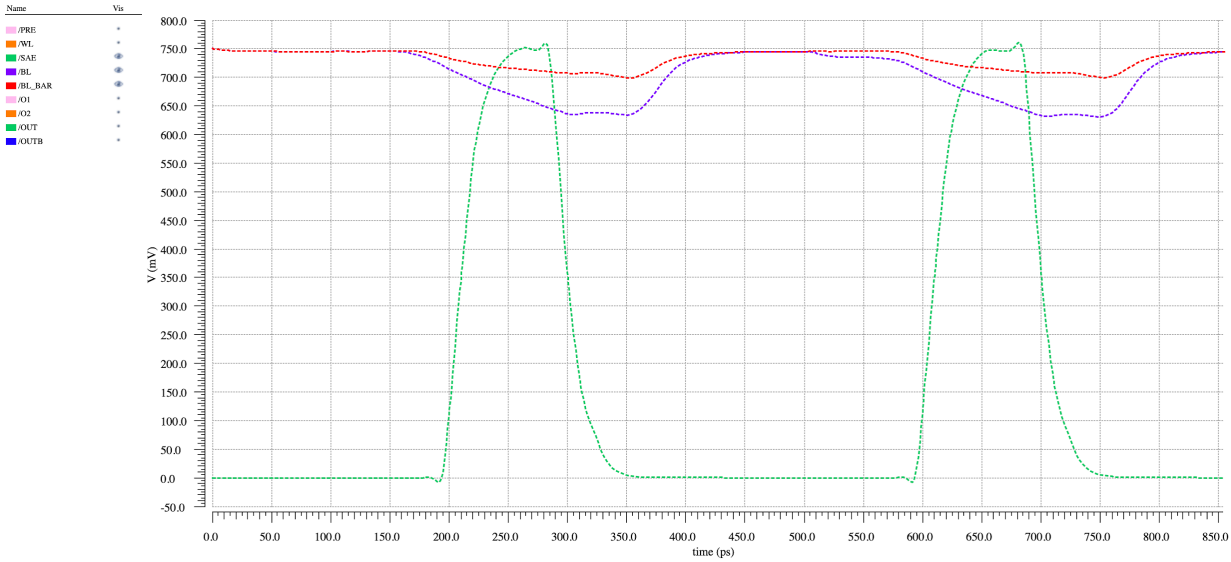


Figure (4.4): Bit Line & Behavior During Read

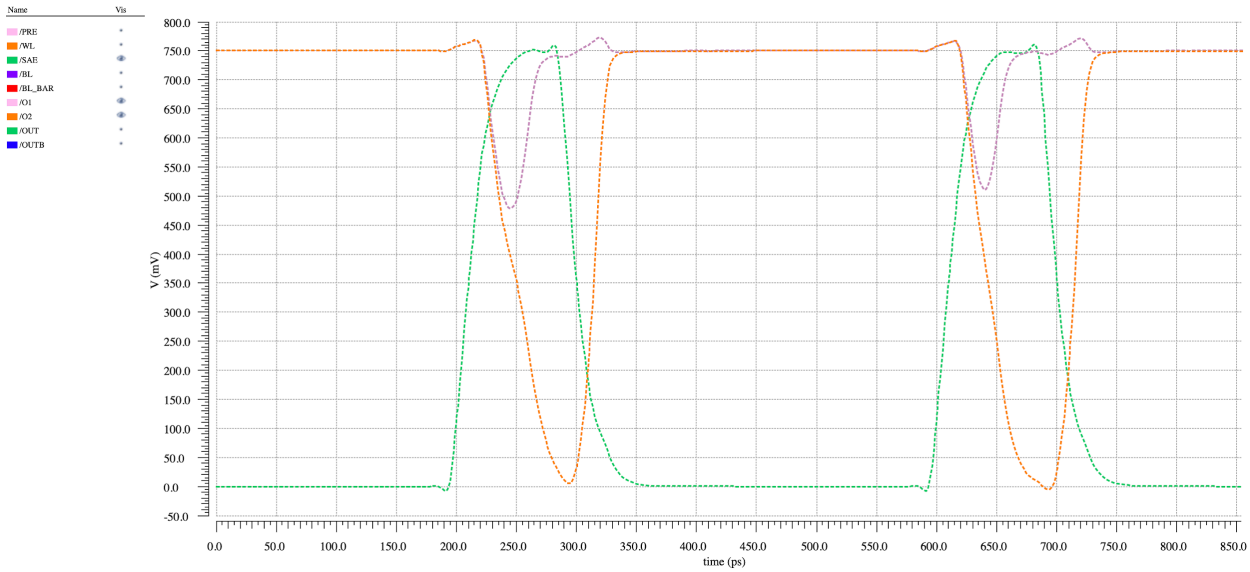


Figure (4.5): Output of Sense Amplifier During Read

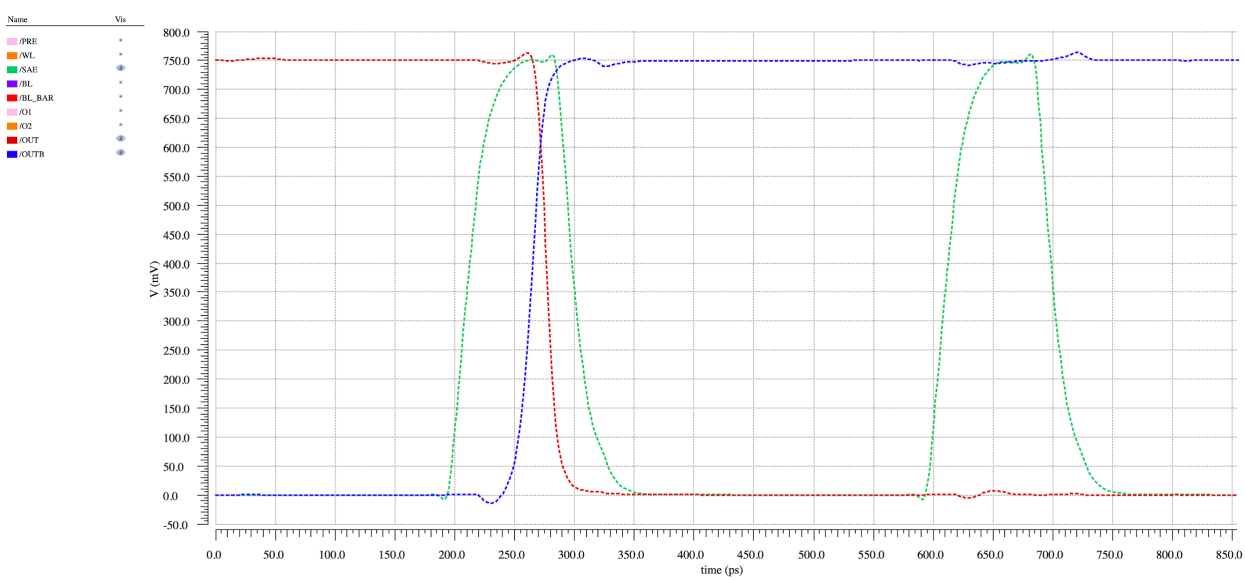


Figure (4.6): Output at Latch During Read

Figures (4.4), (4.5) and (4.6) reflect the behavior shown in Figure (4.2) and thus agree with our theoretical expectations for these waveforms.

<u>Timing of the Read Circuit</u>

- The delay from the rising edge of the SAE to the rising/falling edge of OUT and OUTB of the sense amplifier latch is the sense amplifier delay. This is the amount of time that the sense amplifier takes to detect a differential and give a stable output result. The delay of the sense amplifier as designed is 66.36ps.
- The delay from the rising clock edge of a read cycle to when either O1 or O2 decay to VDD/2 (Consider the longer of the two delays) is the delay that characterizes the read

circuit since it is the total time from the start of a read cycle to when the data appears at the output of the sense amplifier latch. The delay of the read circuit is 277.34ps.

Problem 5 – Complete Peripheral

Block Level Schematic

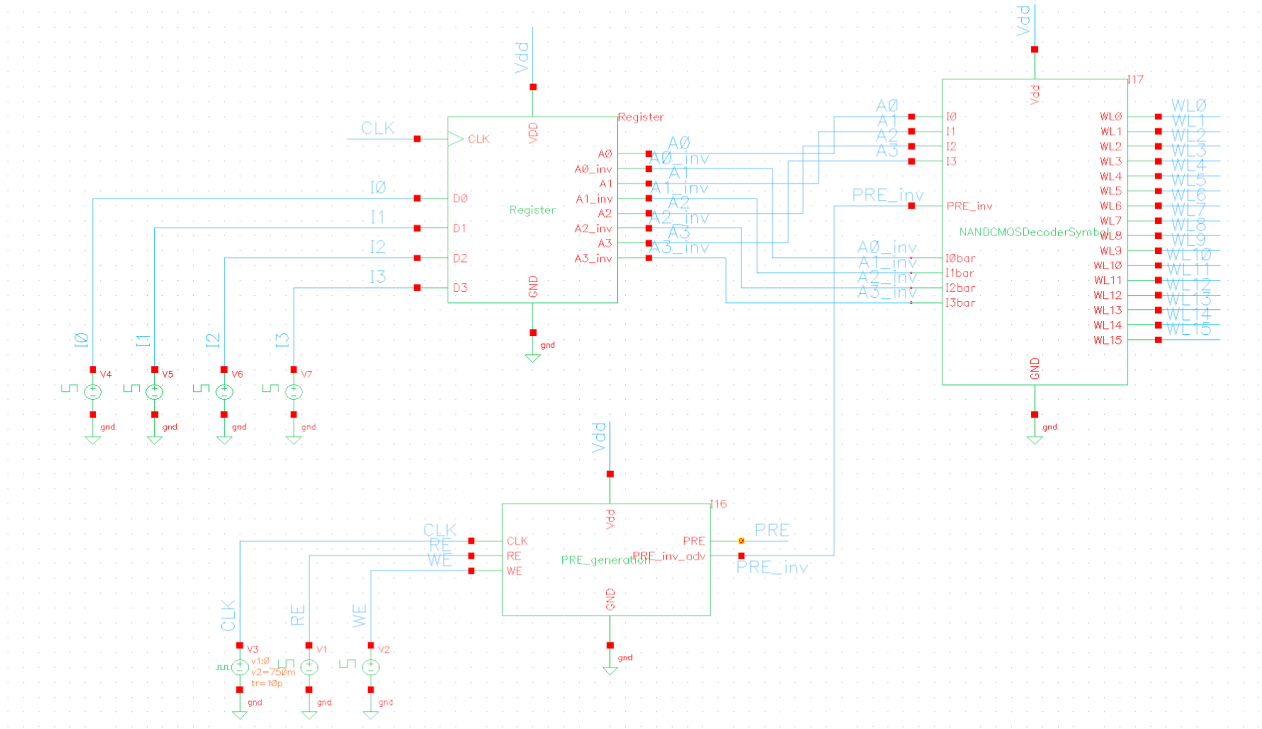


Figure (5.1): Full Peripheral - Row Circuit Cadence Schematic

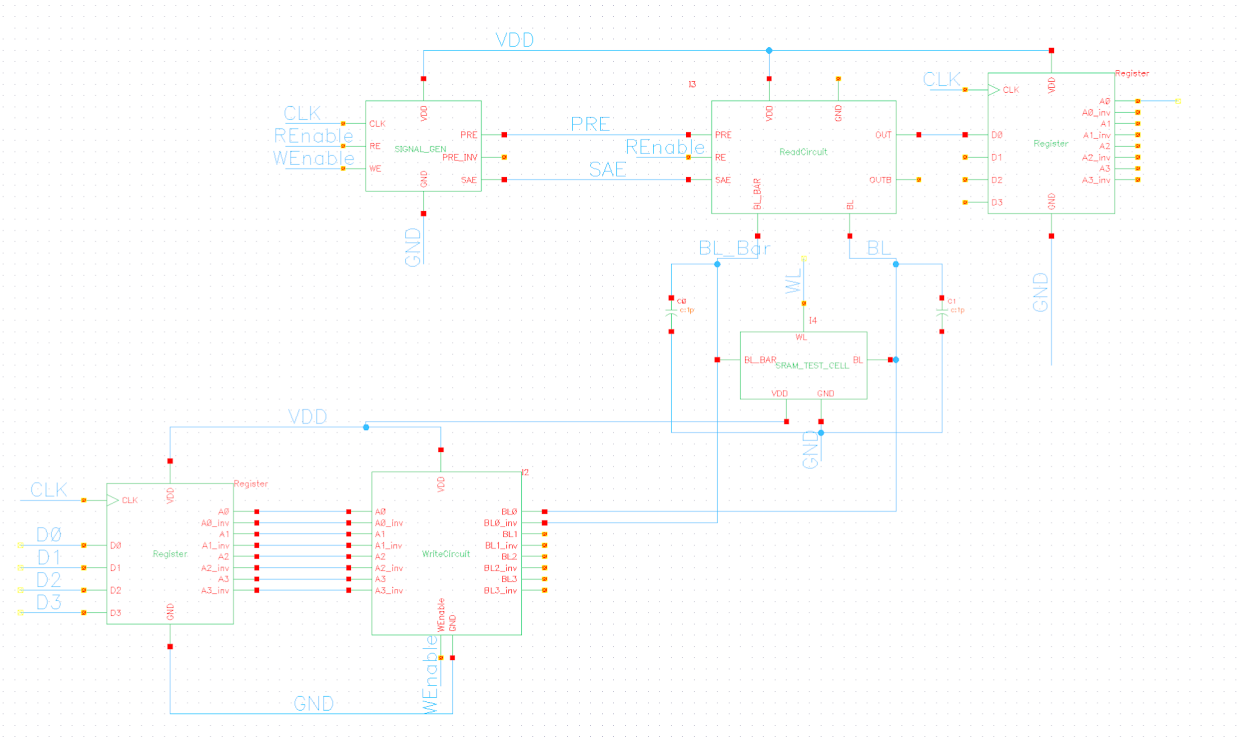


Figure (5.2) Full Peripheral - Column Circuit Cadence Schematic

Row Decoding Circuit

Figure (5.3) shows the waveforms for row address propagation to the WL.

<< Fig 5.3 comes here >>

Read Circuit

Figure (5.3) shows the waveforms for the read circuit operation. Considering the time slot between 0.4 - 0.6 ns, [RE] signal is high in this period. [SAE] goes to high approximately around 0.6 ns. At this point of time, [BL] is maintained to VDD, while [BL_BAR] is at (VDD – Δ). The falling [BR_BAR] signal triggers the sense amplifier and [O1] and [O2] start to fall. Since [BL_BAR] is falling and [BL] is maintained at VDD, [O1] falls faster than [O2], and prevents [O2] from falling further. The values of [O1] and [O2] are latched in the sense amplifier latch and the output can be seen in the [OUT] signal. Since initially the [BL] signal was maintained at VDD, the [OUT] signal going high represents that the correct value is latched by the sense amplifier at the output.

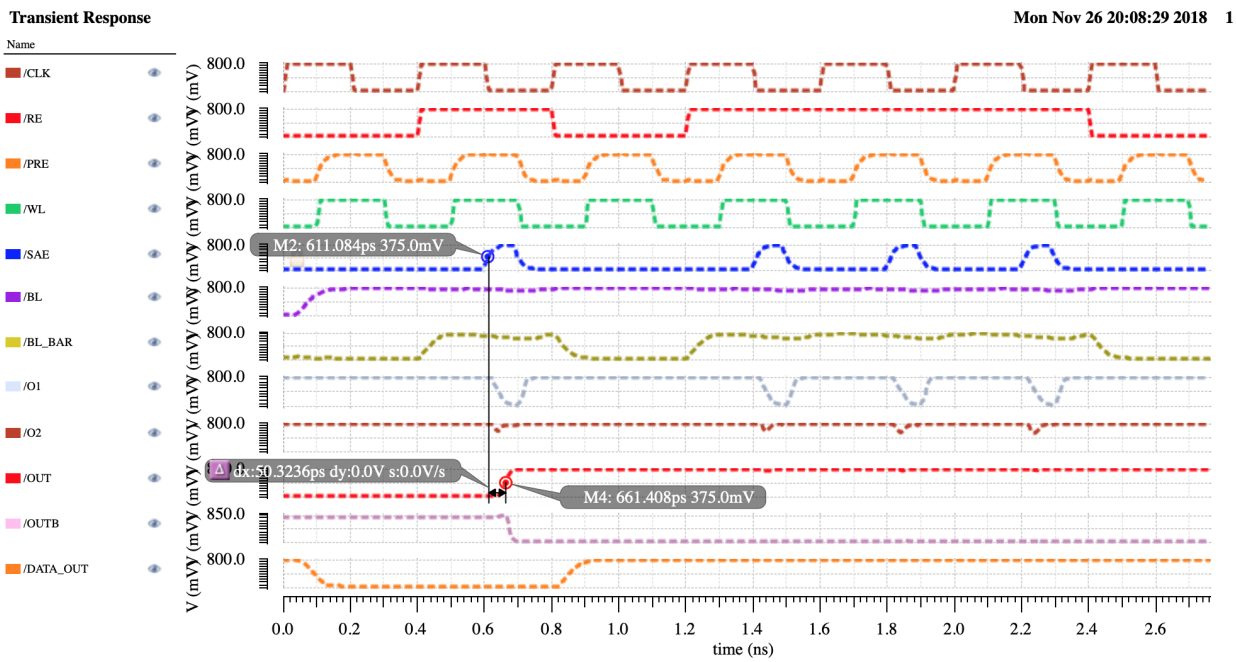


Figure (5.3): Read Circuit Waveform

Write Circuit

In time 2.5ns - 3.25ns, input of data register [D] is 1, and the output of data register [DATA_IN] follows [D] when [CLK] is rising. Since write enable signal [WE] is also on in this period, this data is written to bitline [BL]. Finally, this data is written to SRAM cell [SRAM_Cell].

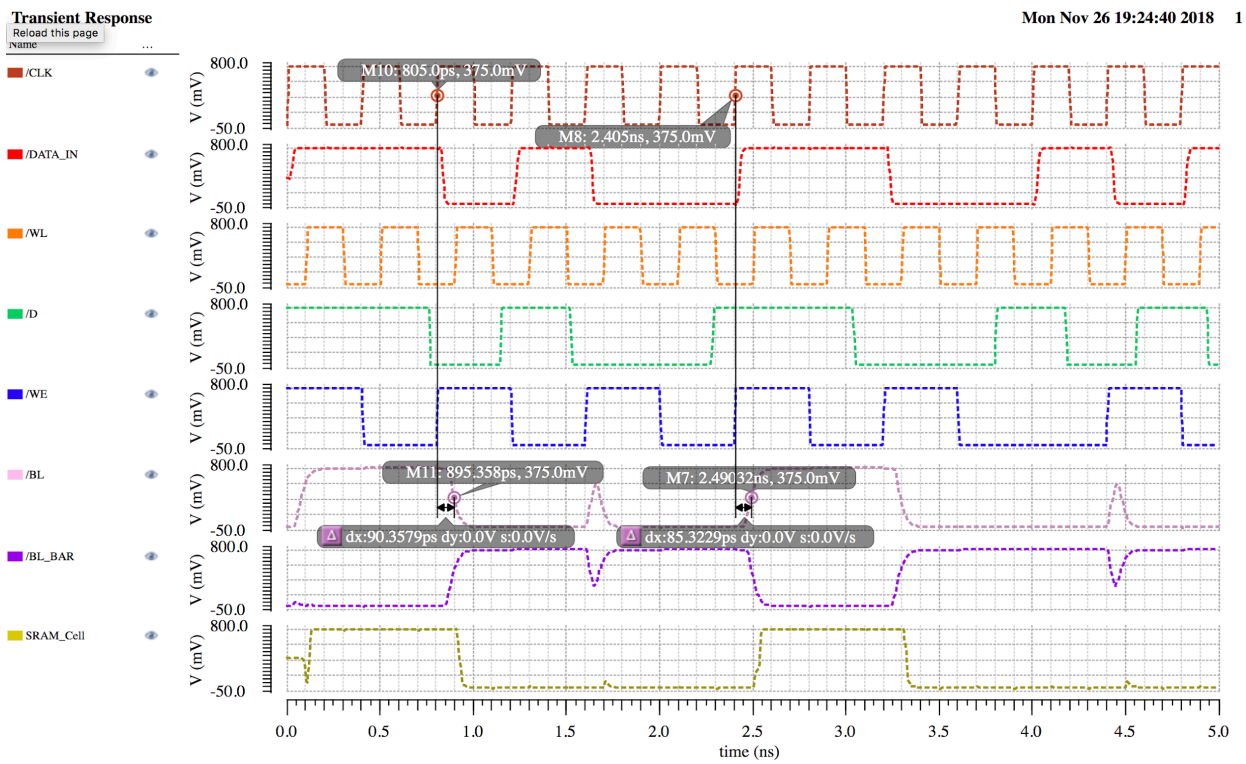


Figure (5.4): Write Circuit Waveform

Timing

Delay for Timing Path (1)

The timing delay from positive [CLK] edge to positive [WL] edge is 109.684ps.

Delay from the rising edge of [PRE] to the rising edge of [WL] is 34.19

Delay for Timing Path (2) – Read

As per Figure (5.2), the timing delay in the read circuit from the positive edge at [SAE] to the data arrival at the latch output is 50.3236ps.

Delay for Timing Path (2) – Write

As Figure (5.4) shows, the timing delay from positive edge of [CLK] to the bitline charging/ discharging are given below:

- Low-to-High : 85.32ps
- High-to-Low : 90.375ps

APPENDIX

A. Decoder Component Schematics

1. NOR2 Gate in Decoder

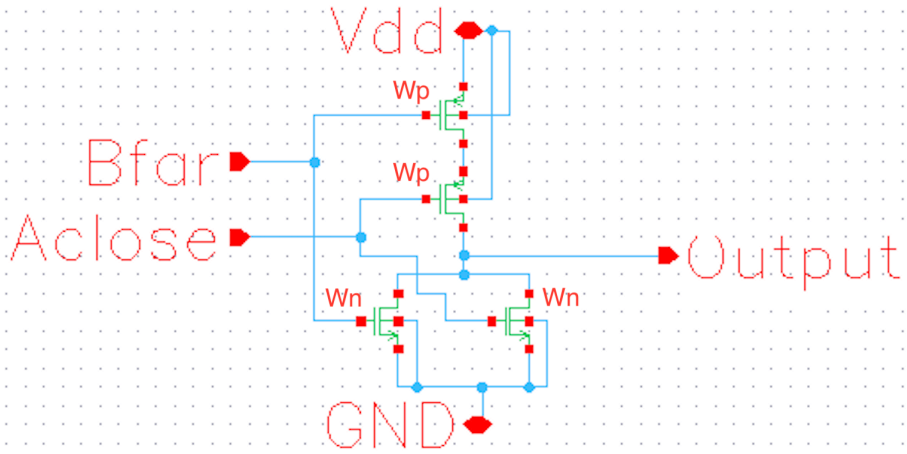


Figure (A-1): Decoder NOR2 Gate Cadence Schematic

Device	Parameter	Value
Pull Up Network PMOS	Wp (Typical for 2)	560 nm
Pull Down Network NMOS	Wn (Typical for 2)	140 nm

2. NOR2 Gate in Decoder

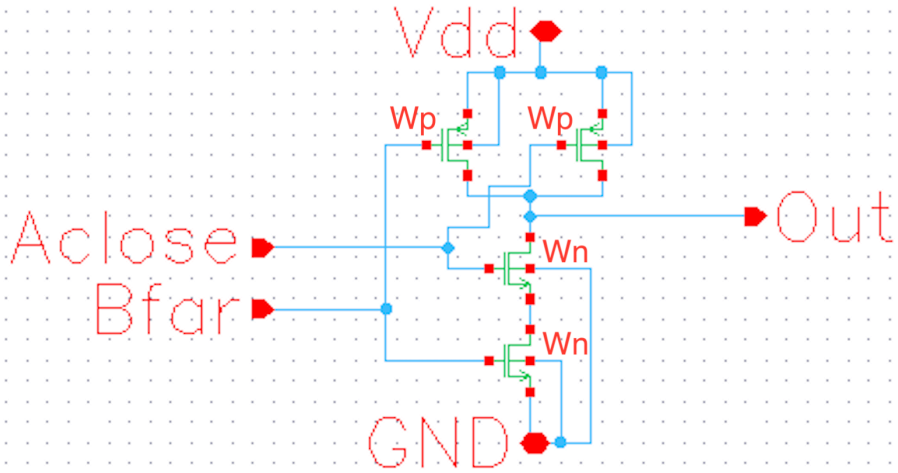


Figure (A-2): Decoder NAND2 Gate Cadence Schematic

Device	Parameter	Value
Pull Up Network PMOS	Wp (Typical for 2)	240 nm

Pull Down Network NMOS	Wn (Typical for 2)	240 nm

B. Register Component Schematics

1. <u>NAND2 Gate in D-Latch</u>

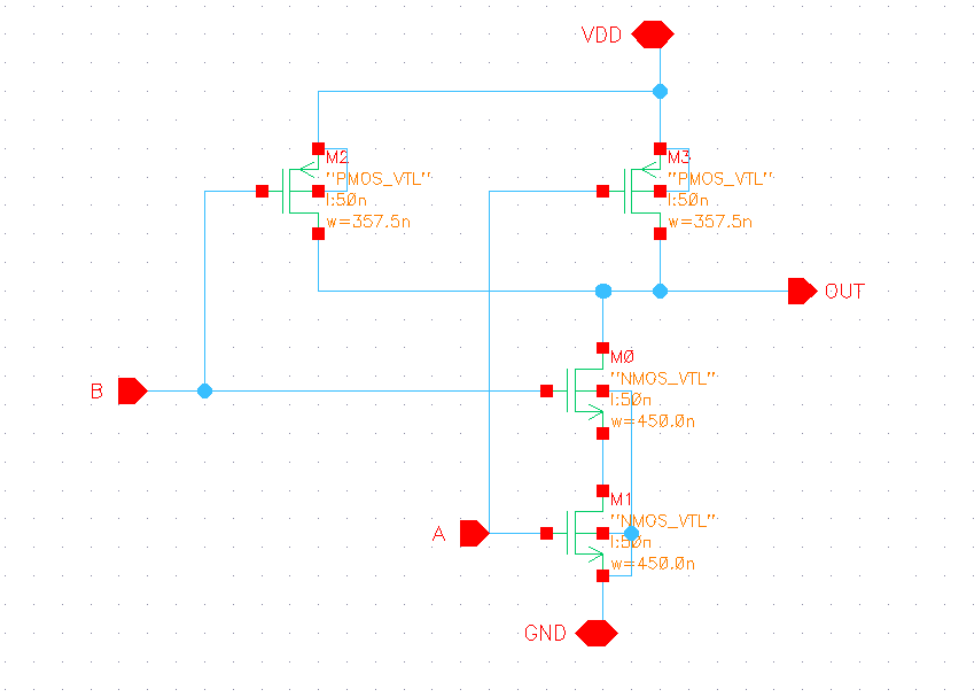


Figure (B-1): NAND2 Gate in D-Latch Cadence Schematic

Device	**Width**
PMOS (Typical for 2)	357.5 nm
NMOS (Typical for 2)	450 nm

C. Write Circuit Component Schematics

1. <u>Write Circuit Inverter Chain</u>

Device	**Width**
1st Stage Inverter PMOS	385 nm
1st Stage Inverter NMOS	245 nm

2nd Stage Inverter PMOS	2.8275 um
2nd Stage Inverter NMOS	1.7925 um

2. <u>Transmission Gate</u>

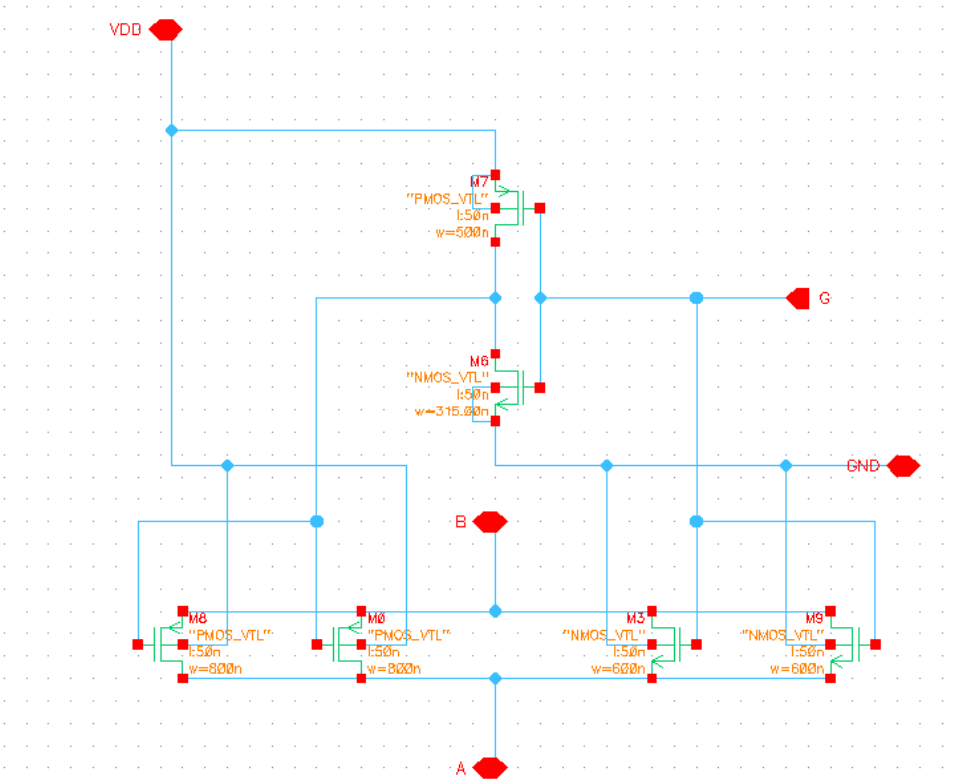


Figure (C-1): Write Enable Transmission Gate Cadence Schematic

Device	**Width**
Inverter PMOS	500 nm
Inverter NMOS	315 nm
Transmission Gate PMOS (Typical for 2)	800 nm
Transmission Gate NMOS (Typical for 2)	600 nm

D. Read Circuit Component Schematics

1. <u>Precharge Circuit</u>

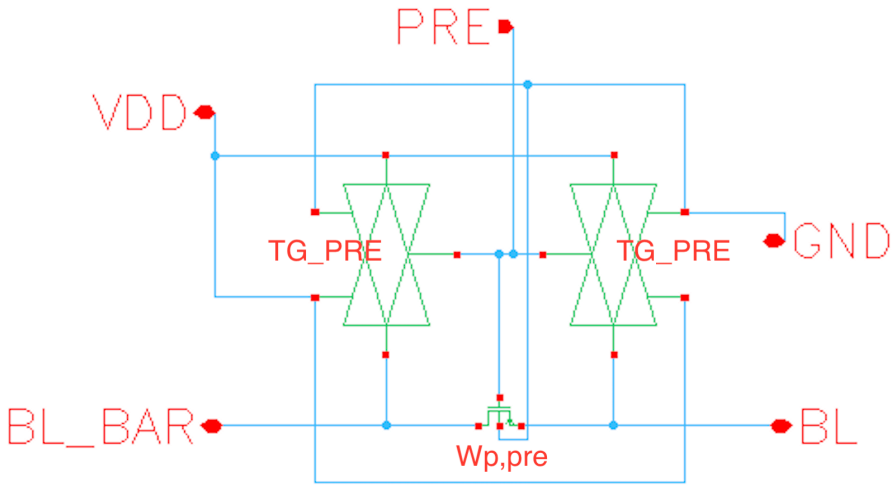


Figure (D-1): Precharge Circuit Cadence Schematic

Device	Parameter	Value
Precharge PMOS	Wp,pre	90 nm

*See appendix D-2 for precharge transmission gate parameters.

Description: The precharge circuit is designed to allow current to flow only when the [PRE] signal is low. While conducting, the transmission gates (active low) will allow both bit lines to charge to VDD.

2. <u>Precharge Transmission Gate</u>

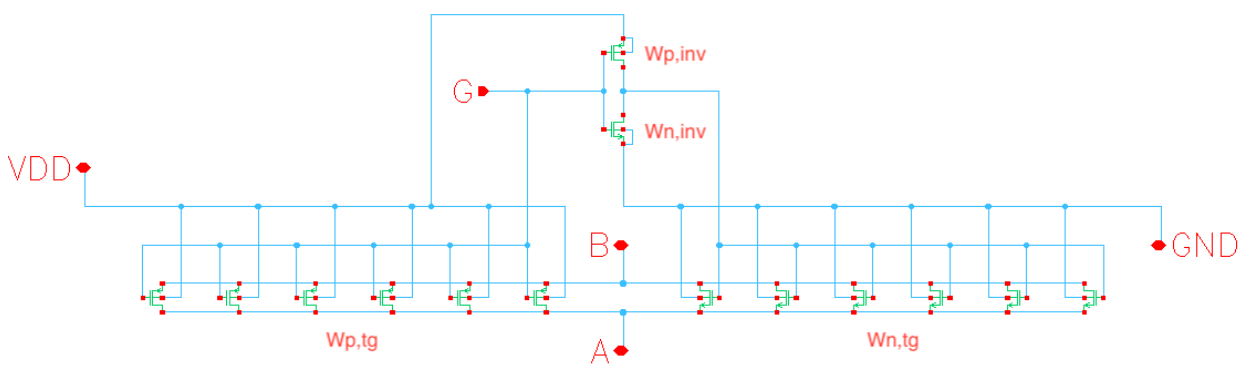


Figure (D-2): Precharge Transmission Gate Cadence Schematic

Device	Parameter	Value
Inverter PMOS	Wp,inv	570 nm
Inverter NMOS	Wn,inv	360 nm

Transmission Gate PMOS	Wp,tg (Typical for 6)	600 nm
Transmission Gate NMOS	Wn,tg (Typical for 6)	600 nm

Description: The precharge transmission gate is designed to ensure that the two bit lines (with assumed 40 fF capacitive loading) are able to charge to VDD within approximately 100ps.

3. <u>Read Enable Transmission Gate</u>

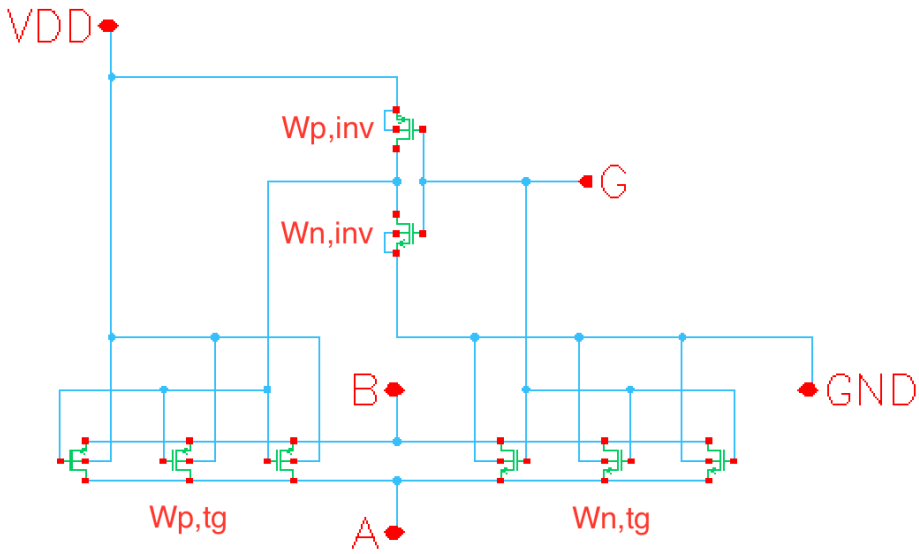


Figure (D-2): Read Circuit Transmission Gate Cadence Schematic

Device	**Parameter**	**Value**
Inverter PMOS	Wp,inv	570 nm
Inverter NMOS	Wn,inv	200 nm
Transmission Gate PMOS	Wp,tg (Typical for 3)	900 nm
Transmission Gate NMOS	Wn,tg (Typical for 3)	600 nm

Description: The read circuit transmission gate is designed to allow the [RE] signal (applied to G) to control the current flow from the precharge circuit (shown in appendix D-1) into the bit lines.

4. <u>Sense Amplifier</u>

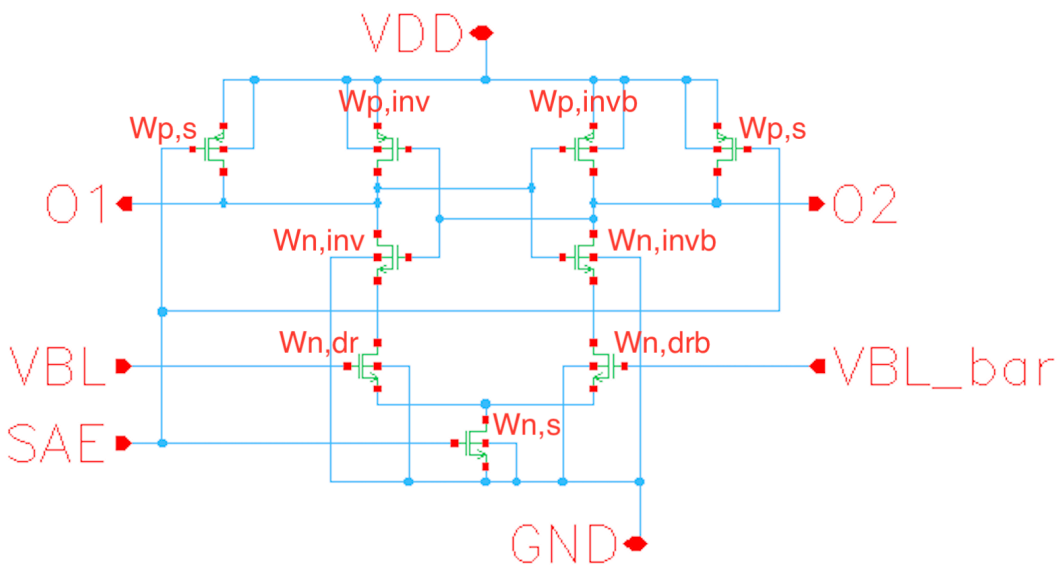


Figure (D-3): Sense Amplifier Cadence Schematic

Device	**Parameter**	**Value**
Inverter PMOS	Wp,inv & Wp,invb	570 nm
Inverter NMOS	Wn,inv & Wn,invb	360 nm
Bit Line NMOS	Wn,drb	520 nm
Bit Line Bar NMOS	Wn,dr	570 nm
Sense Amplifier Enable PMOS	Wp,s (Typical for 2)	570 nm
Sense Amplifier Enable NMOS	Wn,s	360 nm

Description: The sense amplifier is designed such that the voltage difference between VBL and VBL_bar is amplified and passed to O1 and O2. When the [SAE] signal is low, both O1 and O2 are charged to VDD. Once the signal goes high, both the Bit Line NMOS and Bit Line Bar NMOS will discharge. The transistor with the larger voltage at the gate will discharge faster, preventing the opposite from discharging any further. Thus, O1 and O2 will both stabilize at either logic '1' or logic '0' depending on the logic of each bit line.

5. <u>Sense Amplifier Latch</u>

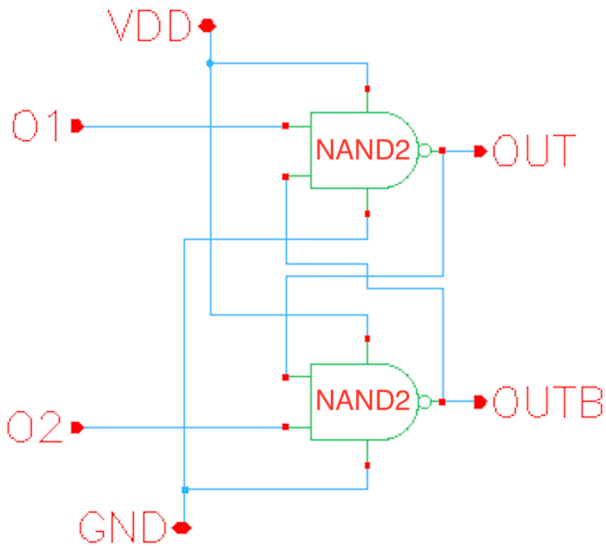


Figure (D-4): Sense Amplifier Latch

* See Figure (B-1) in appendix B for NAND2 gate parameters.

Description: This design of the sense amplifier latch will give and output of 0 or VDD matching the logic of O2. Its purpose is to provide OUT and OUTB as rail voltages based on the outputs O1 and O2 of the sense amplifier shown in Figure (D-3).