EL GY 6473
FALL 2018
Course Project: 64bit Memory System Design

Three part submission

Assistant Professor Shaloo Rakheja

Electrical and Computer Engineering, NYU

Grade distribution

- **Homework + project = 40%**
- **Homework = 16%**
- **Project = 24%**

Design of 64-bit SRAM + layout of SRAM array

Project will be done in groups of 4 each. Please choose your project partners.

Project components

Project Part	Due Date*
Part-1 Address decoder, address/data registers, read+write peripherals	**Nov. 25 (heavy deliverable)**
Part-2 SRAM cell + layout	**Dec. 08**
Part-3 SRAM array + layout = full report	**Dec. 21 (after final exam)**

In addition to these deliverables, we will have one more homework.

*All due dates are 11:55 PM on the date specified.

Project grading (i)

- Project deliverables are distributed in **three parts** with specific deadlines.
- Each submission is 8% of the total project weight (24%).
- In each submission, **2% goes toward meeting the deadline and 6% goes toward technical contents**: (i) style of presentation, (ii) clever design styles, (iii) meeting the specifications.
- You will receive a letter grade with each submission instead of points.
- At the end of the final report, I will collect your letter grades from all the submissions and average them out.

Project grading (ii)

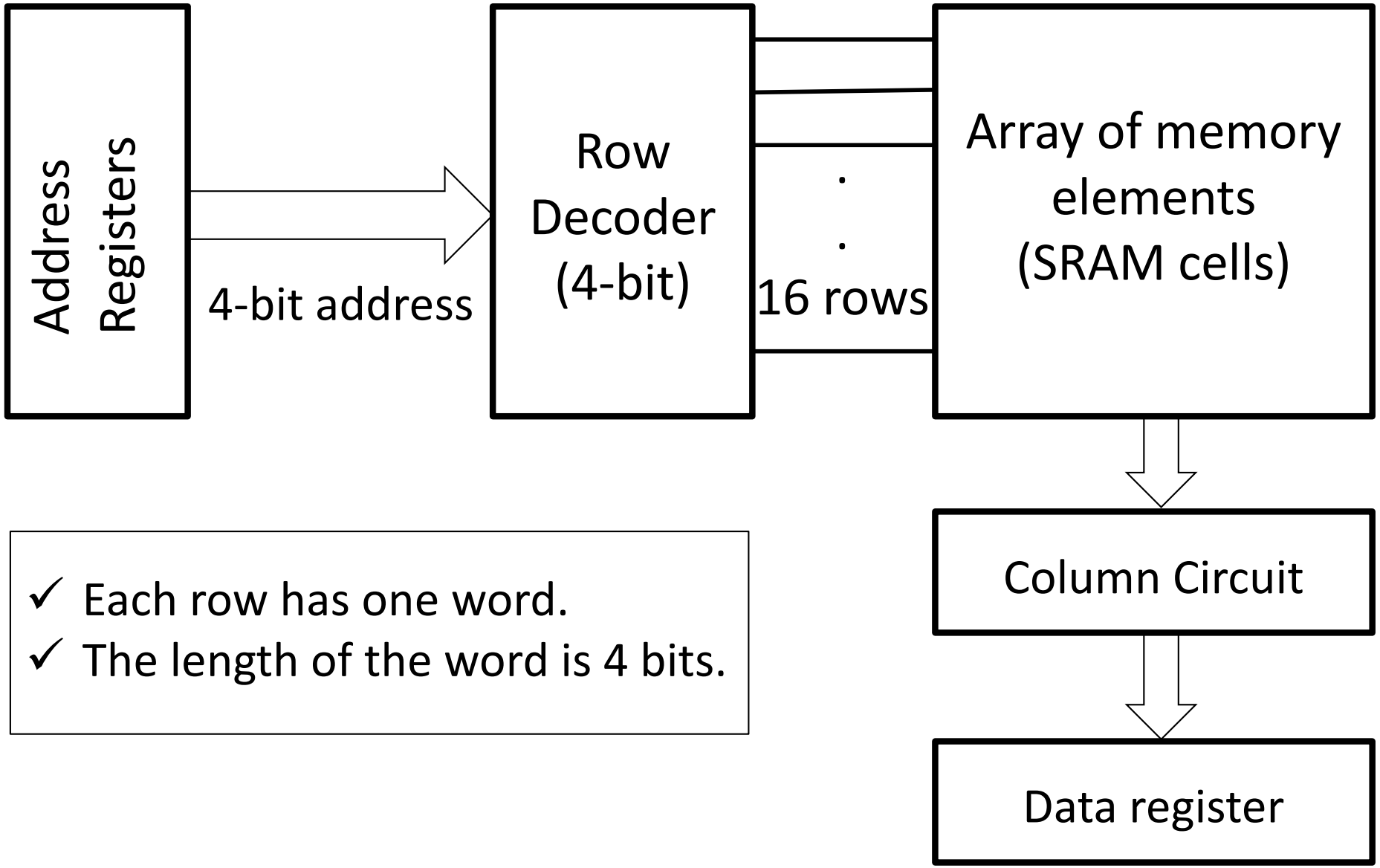
- With each submission, make sure you submit ALL of your CADENCE schematics on white background. All simulation results must be submitted on white background. A good option is to transfer the data from Cadence into a plotting tool for better readability.

- Show clear calculations for power dissipation, timing, functionality (wherever applicable.)

- Write as coherently as possible. I should be able to follow your design from the submitted report.

ONLY ONE REPORT PER PROJECT GROUP.
CLEARLY STATE ON THE COVER PAGE EACH TEAM MEMBER's CONTRIBUTION.

Memory (SRAM) System



- ✓ Each row has one word.
- ✓ The length of the word is 4 bits.

Configurations

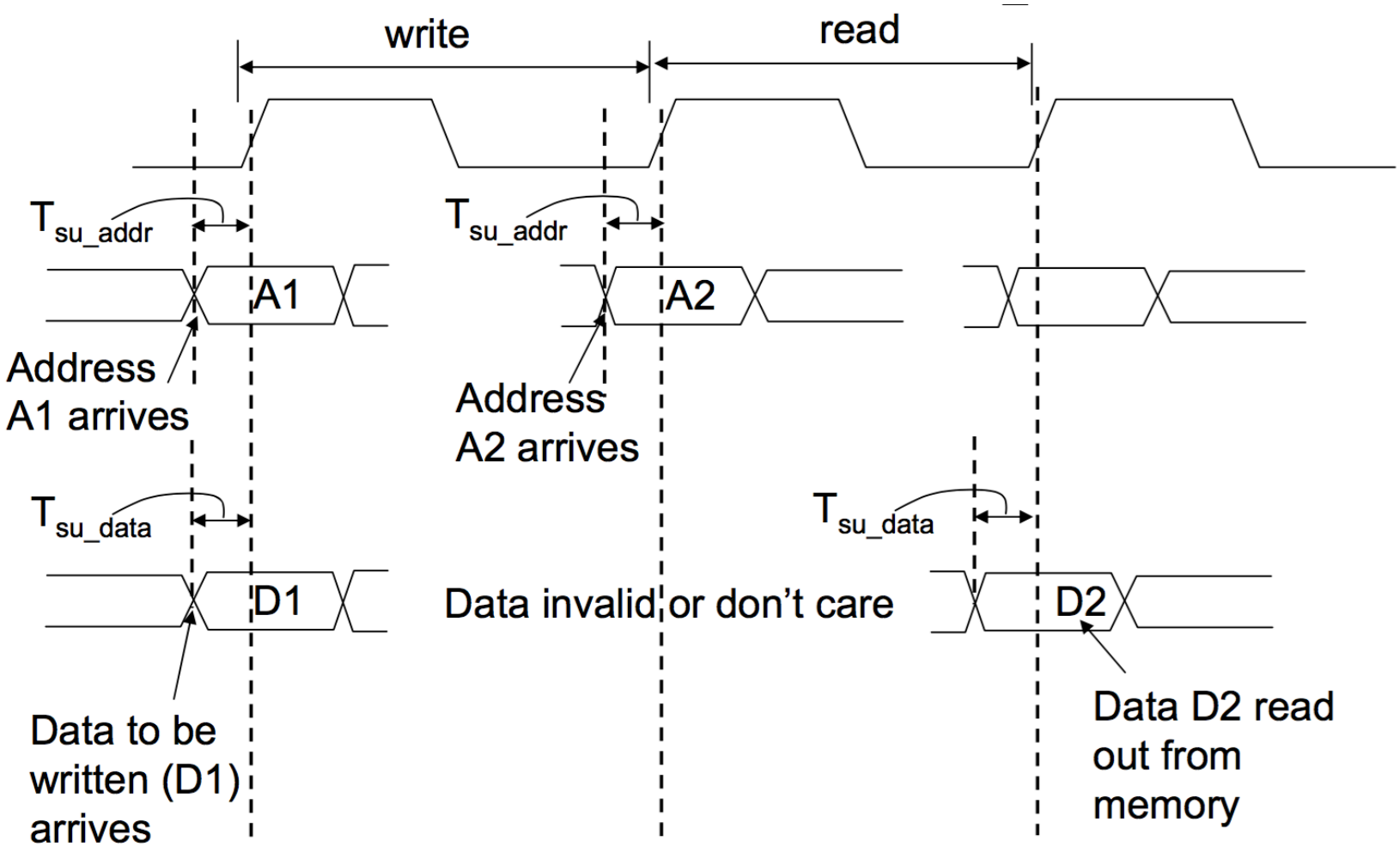
- Address: 4 bit
  - Stored in 4-bit register (4 Master-Slave Flip Flops)
- Data: 4 bit
  - Stored in 4-bit register (4 Master-Slave Flip Flops)
- SRAM array: 64 bit
  - 16 rows, 1 column (data width = 4 bits)
  - 4 bit row decoding
- Column circuits
  - Read and write circuits

Specifications

- Technology: FreePDK45 CMOS
  - Min. length = 50 nm, min. width = 90 nm
- Supply voltage: **0.75V**
- Target clock frequency: **2.5 GHz**
- SRAM cell area **< 0.8 µm^2**

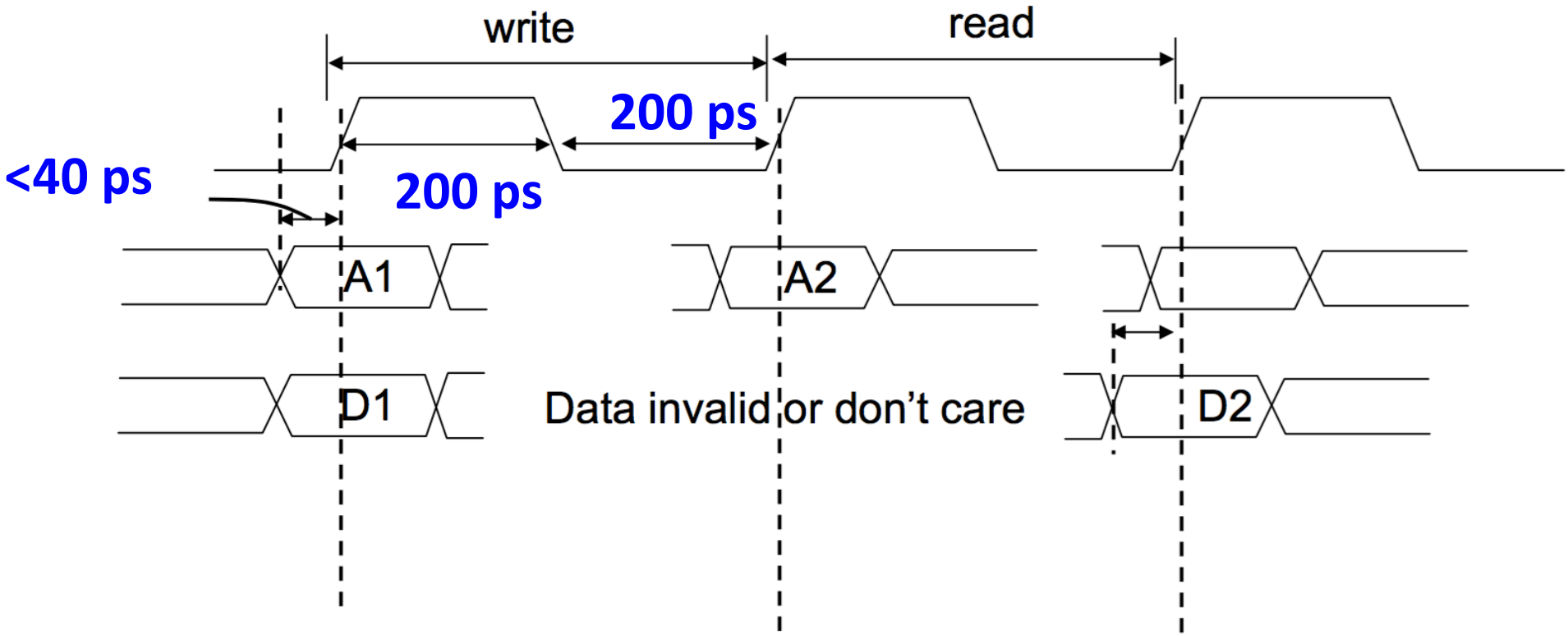
- *Connect body of PMOS to V_{DD} and the body of NMOS to ground always. This is important for Transmission Gate Design Styles.*

Functionality



- Functional testing: We will keep A1=A2 and see whether design gives D1=D2

Timing



- We will test whether the array functions correctly (i.e. you write and read data correctly) at a frequency of 2.5GHz at 0.75V?

Project Plan

Part-I:

- Decoder Logic and WL generation and address regs.
- Peripherals (R/W circuitry)
  - Schematic level design by **Nov. 25**

Part-II:

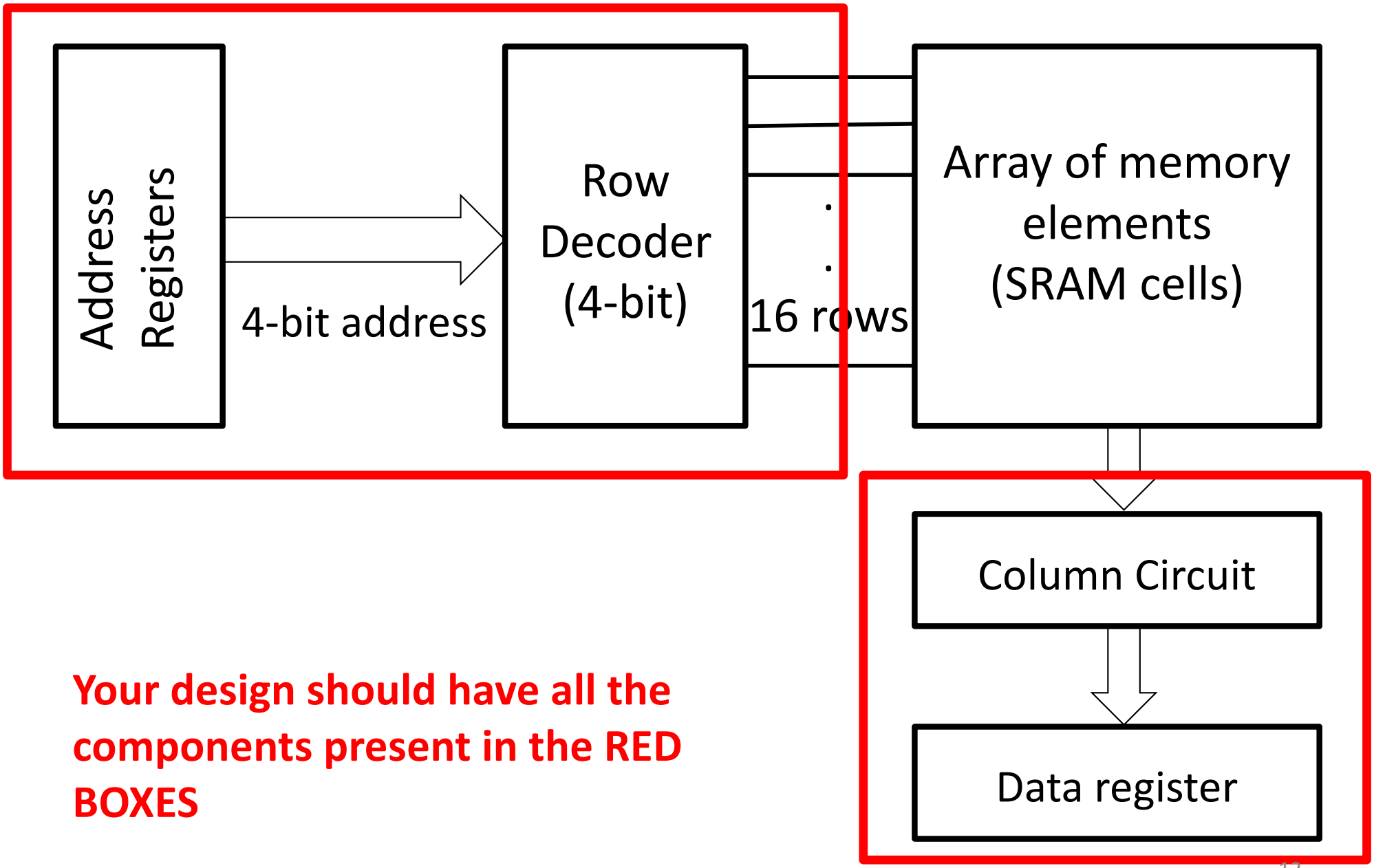
- Design and layout of the SRAM cell
  - Schematic level design and cell layout **Dec. 08**

Part-III:

- Layout of the array (DRC and LVS clean)+ all Cadence files **(Dec. 21)**
- Project report **(Dec. 21)**

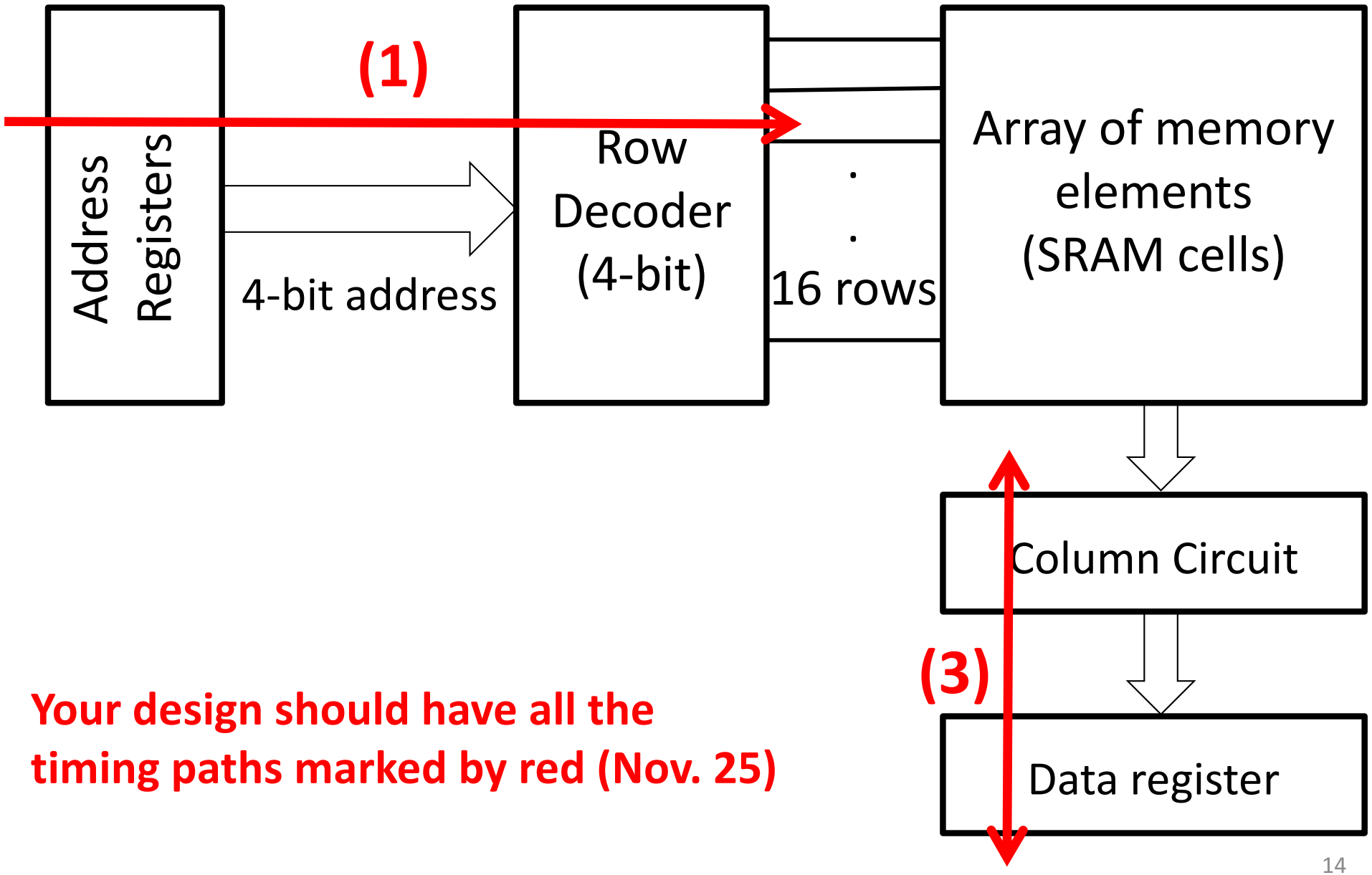
PART I SUBMISSION: PERIPHERAL CIRCUITS

November 25 deliverable



Your design should have all the components present in the RED BOXES

Problem 4: Timing path completed Peripheral



Your design should have all the timing paths marked by red (Nov. 25)

PART I Submission NOV. 25

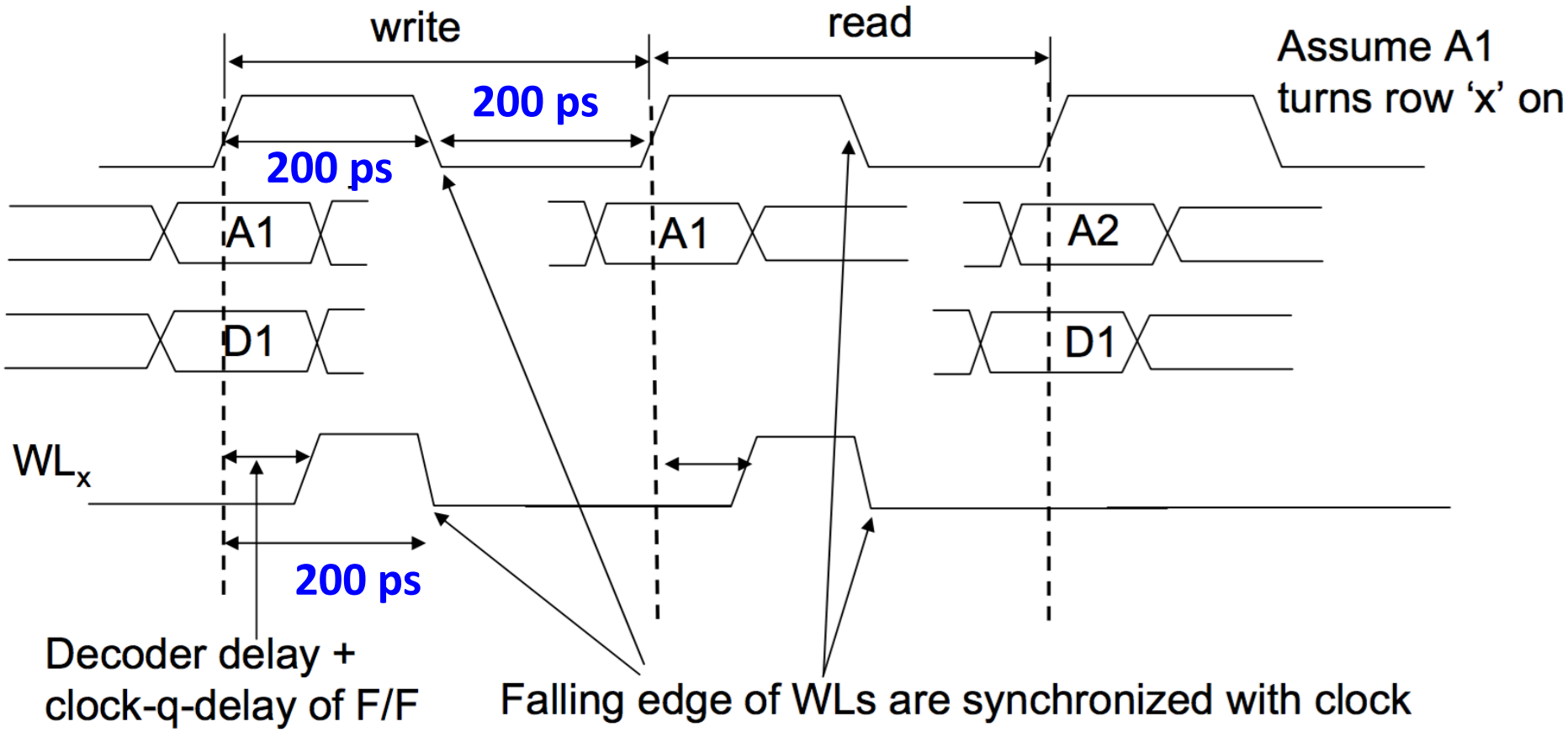
Part-I submission	Nov. 25
Problem 1	Row Decoder
Problem 2	Address and data registers
Problem 3	Write circuitry
Problem 4	Read circuitry
Problem 5	Full peripheral

PROBLEM 1: ROW DECODER

Problem-1: Decoder logic

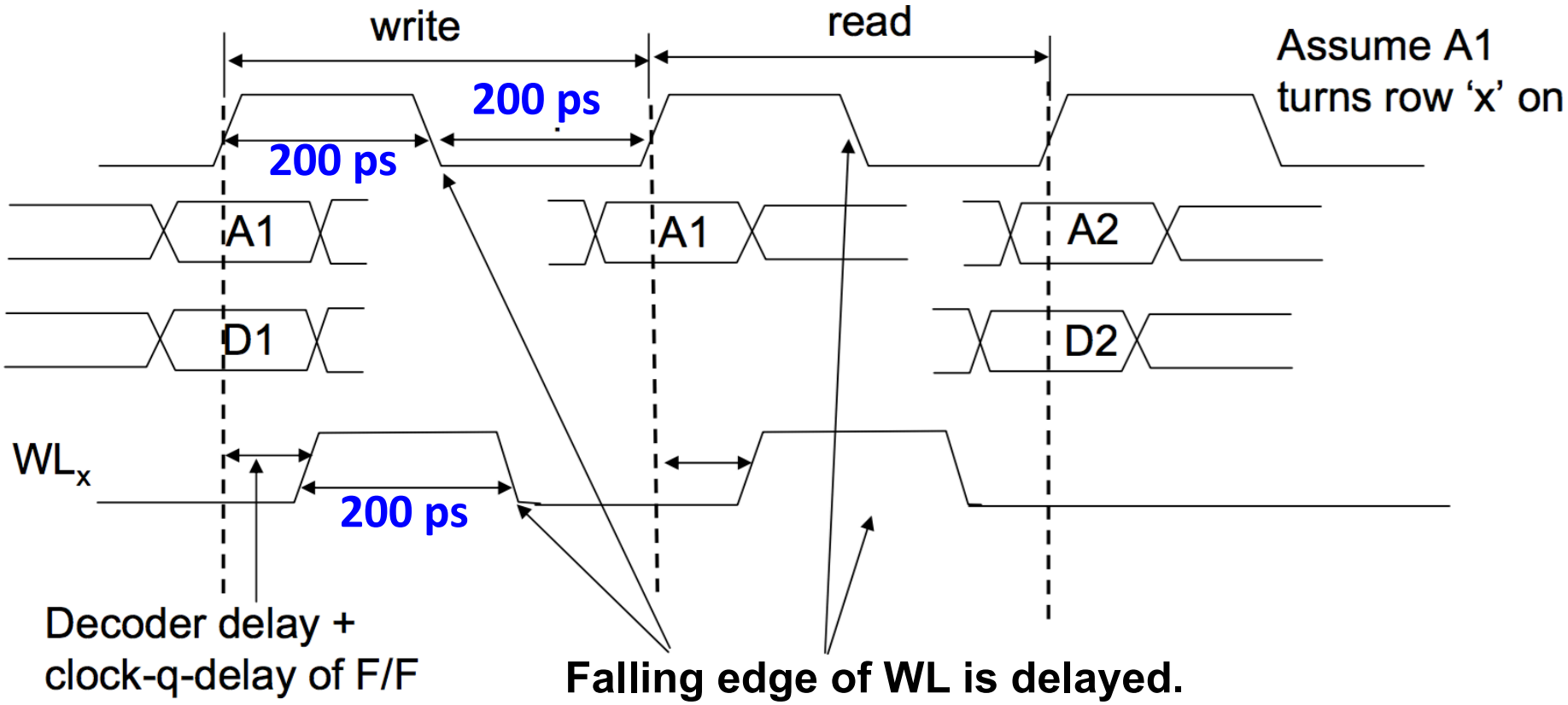
- **At the rising edge of the CLK, the address will be assigned to the Decoders.**
- **Row decoder:**
  - **Decode 4 bits (A_0, , A_3).**
  - **All the WL will be initially low.**
  - **The WL corresponding to the decoded address will make a low-to-high transition only after the decoding is complete.**
  - **The selected WL will make a high-to-low transition:**
    - either at the falling edge of CLK (i.e. CLK high-time = WL turn on time + decoder delay)
    - or after a time interval equal (from the rising edge of WL) to the 50% of clock period (i.e. CLK high-time = WL turn on time)

Timing details: Option 1



- **You may decide to synchronize the falling edge of the WL with falling edge of the CLK**
  - **Pros: Simple logic for WL generation**
  - **Cons: Tighter timing for SRAM cell**

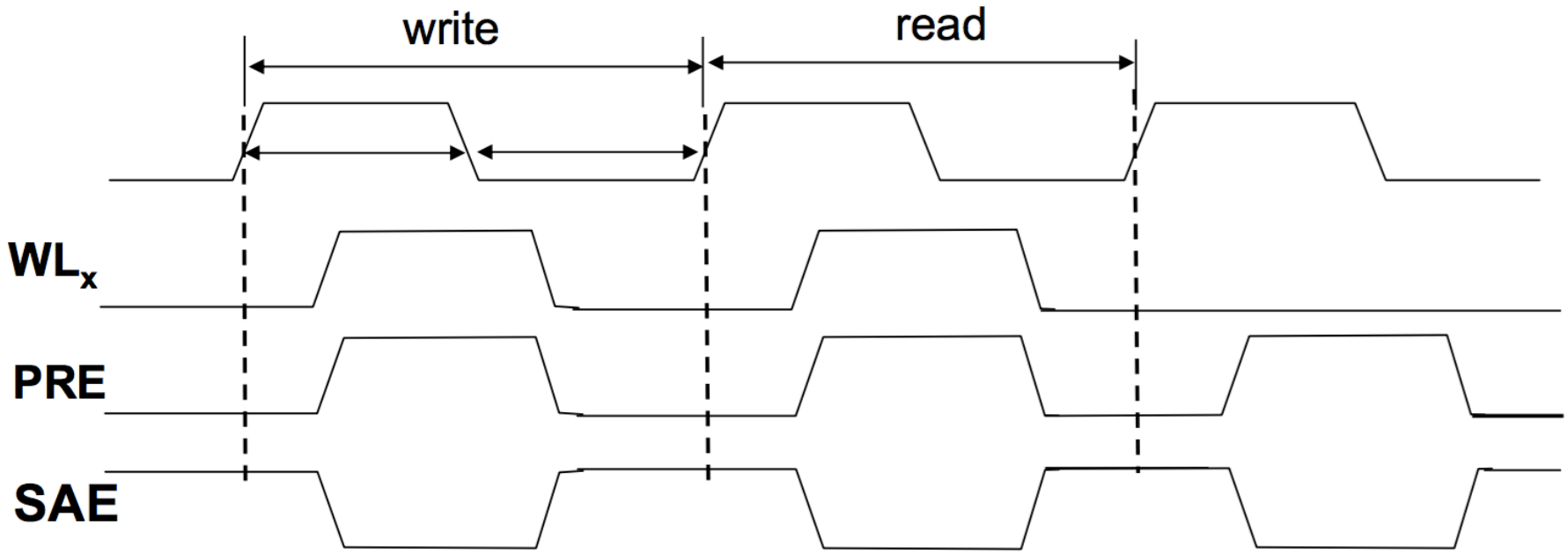
Timing details: Option 2



- **You may decide to delay the falling edge of the WL so that WL turn on time is same as the CLK high time**
  - **Pros : Less stringent timing for SRAM cell**
  - **Cons: Little more complex logic for WL generation**

You are free to choose any options

Other timing details

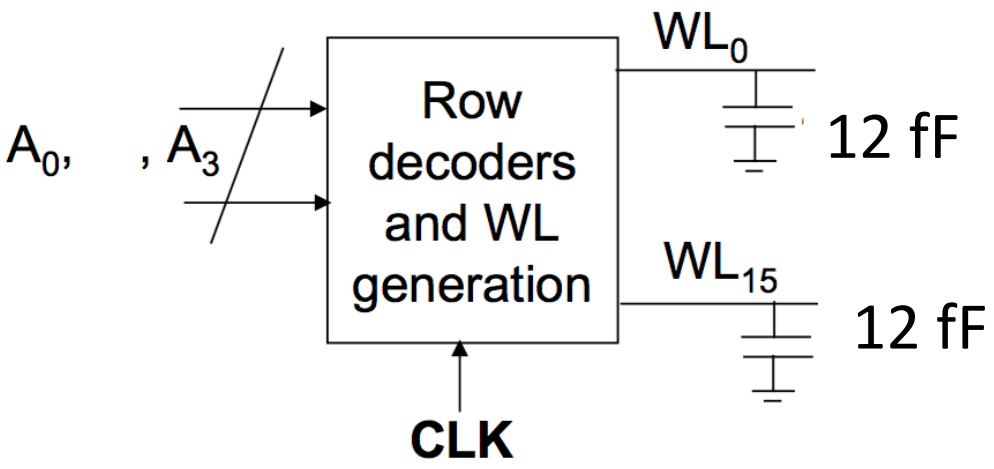


- Pre-charge (PRE) is synchronized with WL.
- Remember there are 16 WL signals but one pre-charge signals.
- You need to generate pre-charge signal from CLK and synchronize with all WL signals.
- SAE also needs to be generated from CLK and synchronized with PRE.
- If you use option (1), you can synchronize SAE and PRE with CLK as falling edge of the WL is synchronized with CLK.

Problem-1: Tasks

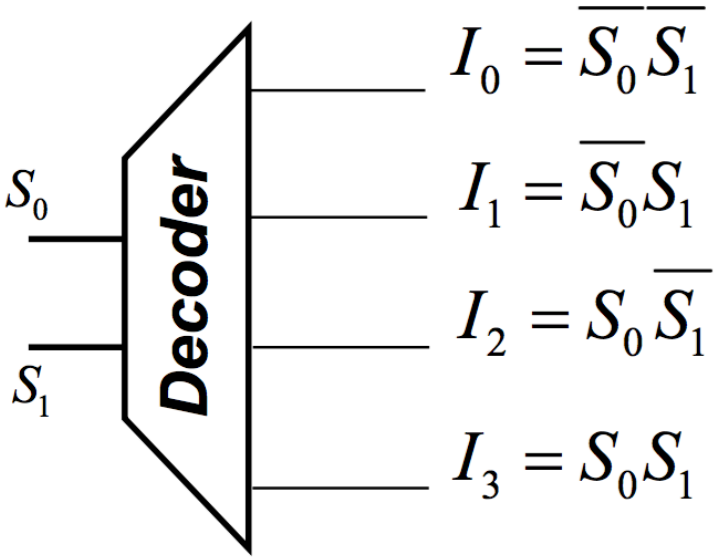
- Design the row decoder
  - Row decoder delay should be less than 25%-35% of CLK high time
- Ensure the logical functionality and timing of the WL signal for the chosen option.

Problem 1: Tasks



- Since we have not done the layout we do not know the exact capacitance of the WLs.
- For this part we will assume a 12 fF (possibly overestimation) capacitive load at each WL.

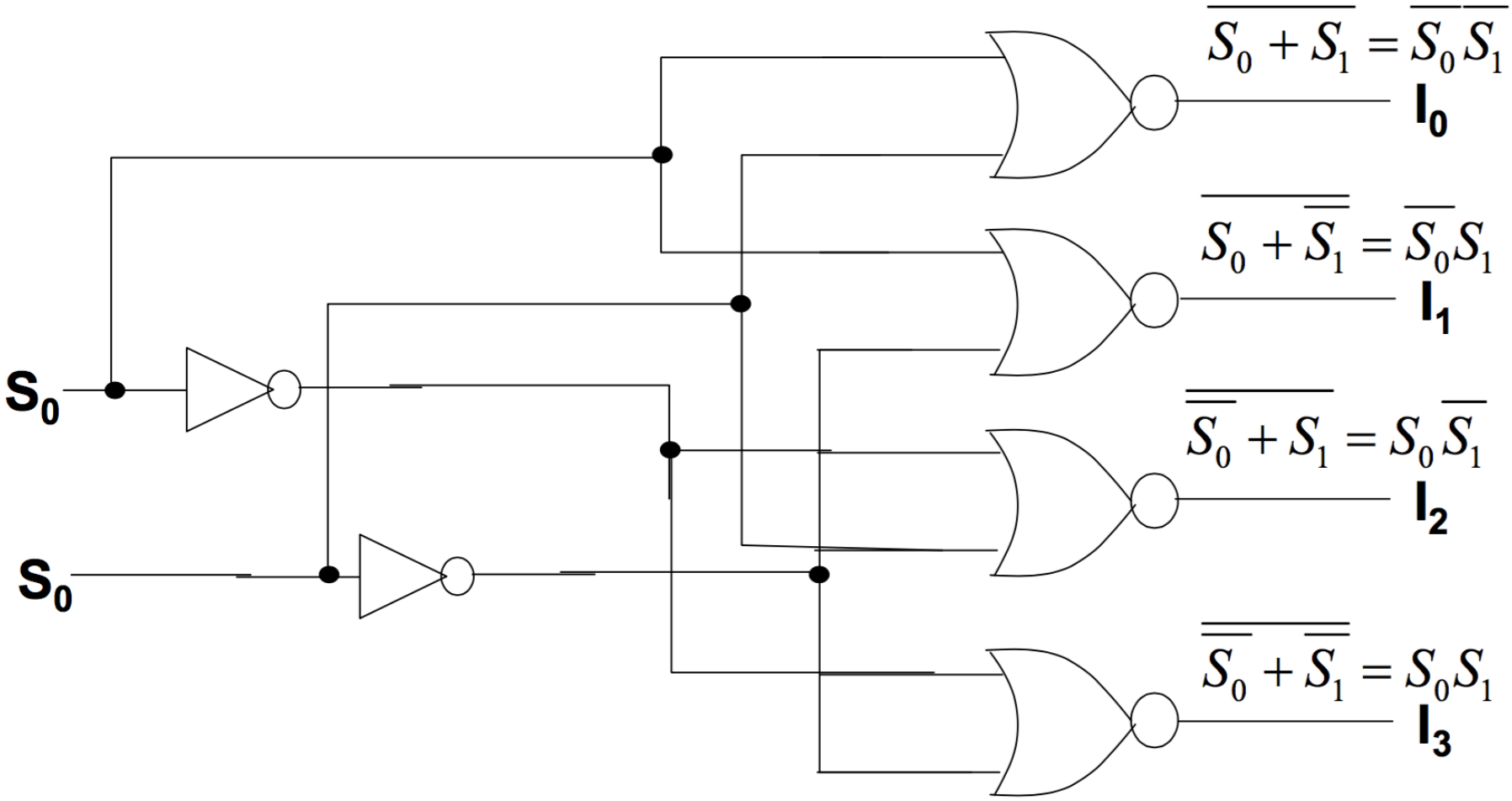
Example: 2-4 Decoder



S0	S1	I0	I1	I2	I3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- **Depending on the input conditions only 'one' output will be high and others will be low .**
- **You can also have only one output low and others high.**
- **Bottom line: only one output should be at a different state than the others.**

Example: 2-4 Decoder STATIC LOGIC STYLE



What to submit with homework on Nov. 25

- **A printout of the top-level schematic of the decoder from cadence**
- **A printout of the schematic which implements the WL logic**
- **A printout of the waveform of operation**
  - Consider two successive CLK cycles (400 ps to 800ps) and (800ps to 1200ps). Assume CLK is zero from 0 – 400 ps
  - Show waveform of WLs corresponding to a) A0 A1 A2 A3 = [0 0 0 0] and b) A0 A1 A2 A3 = [0 1 0 0]
  - Waveform should show the correct operation for the option you have chosen
- **Report:**
  - Delay from rising edge of the CLK to the rising edge of WL
  - Delay from falling edge of the CLK to the falling edge of the WL
  - Average Power dissipation

PROBLEM 2: ADDRESS AND DATA REGISTERS

Problem 2: Registers

- Design the 4 bit registers (you need to first design single flip-flop and then connect 4 of the flip-flops in parallel). Ensure that the design satisfies the following constraints
  - Target CLK period = 400ps
  - Setup time < 15% of CLK period
  - CLK-Q delay < 10% of CLK period
- Do not unnecessarily upsize devices as it will increase power dissipation

Problem 2: What to submit with homework on Nov. 25

- **Cadence schematic of the single flip/flop**
- **Describe the design style you have used**
- **Show waveform of operation for a single flip/flop**
  - Apply data to D and show it changes state in Q
  - Point the CLK-Q-Delay in the waveform
  - Show two cases one just satisfying setup requirement and one just violating the setup requirement
  - Report the setup time in your waveform and in your written solution
  - What is the hold time for your flip flop design?
  - What is the average power dissipation of the address register?

PROBLEM 3: WRITE CIRCUITRY

Problem 3: Write circuitry

- Design the Write circuit to apply the data to the bit-lines (you will need an additional input signal that tells whether a memory access operation is read or write)
  - Design the data drivers
  - Connect the write circuit to the column and implement the read/write control
  - Ensure that data driver will be connected to the columns if and only if write operation is selected
  - Assume that the bitlines have a capacitive load of 40 fF
- Connect the one bit of the data register to the write circuitry

What to submit with the homework on Nov. 25

- Cadence schematic
- Testing strategy
  - How will you verify the circuit? Draw the waveform that shows the circuit is working correctly.
  - Which delay(s) are important to ensure proper write operation?
  - Describe the global synchronization requirement for the entire system to ensure write operation
    - Remember you want the write data to arrive at the bitline before the WL signal goes high.
    - What should be the expected timing for Pre-charge, Column select arrival, data arrival at bitline, and WL arrival?
- Cadence waveform
- Report the delays that characterize the write circuit.

PROBLEM 4: READ CIRCUITRY

Problem 4: Read circuitry

- Describe the read circuit
  - Sense amplifiers
    - Ensure the sense-amplifier delay < 15%-20% of the CLK period (Assume 10 fF capacitance at the output)
    - Assume 10% worst-case mismatch in the width of sense-amplifier devices and find out the minimum bit-differential that can be correctly sensed.
- Ensure during read operation, write path is disconnected.
- Consider the global timing and synchronization requirements.

What to submit with HW on Nov. 25

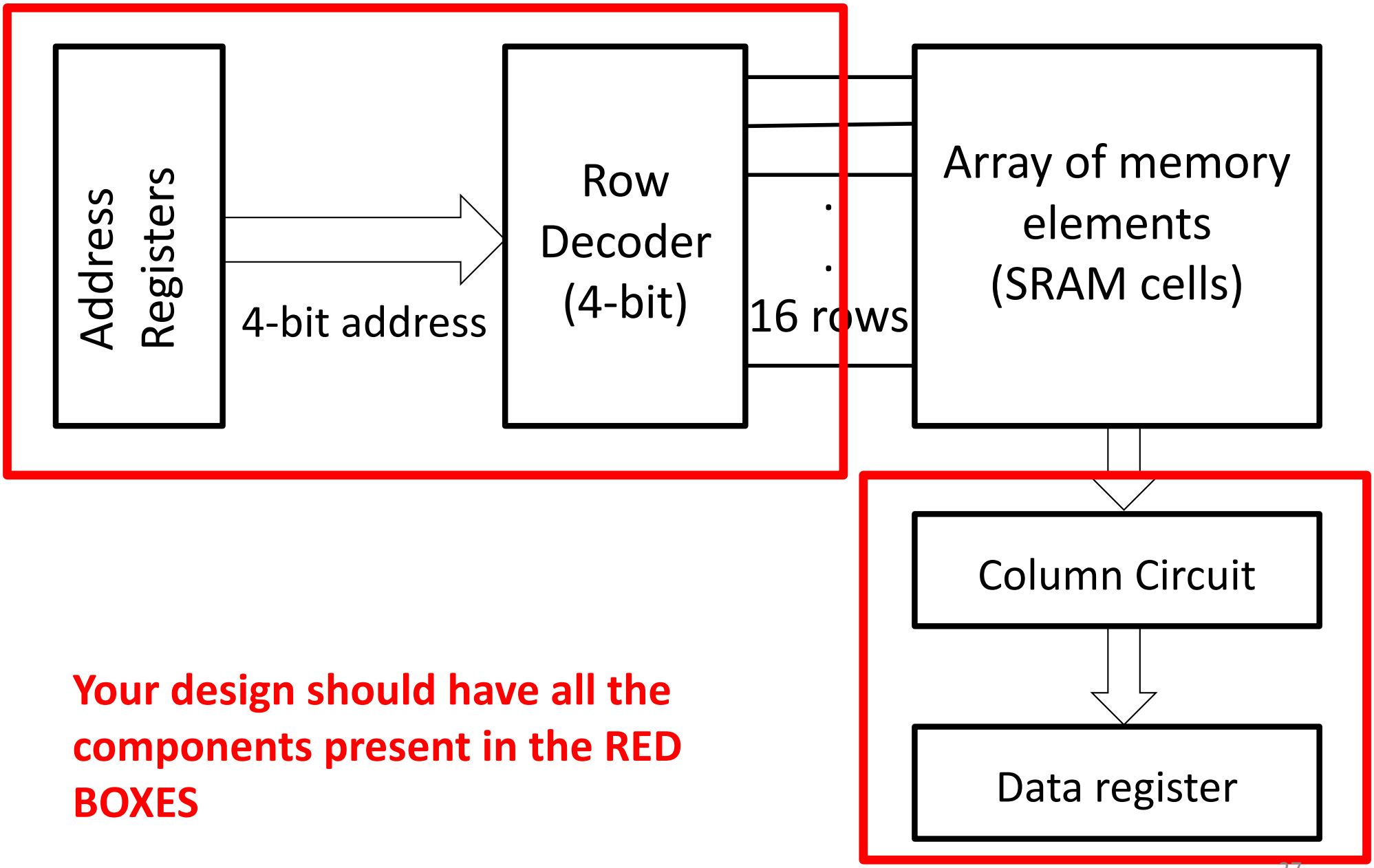
- Cadence schematic
- Testing strategy
  - How will you verify the circuit? Draw the waveforms that will tell you the circuit is functioning correctly.
  - Which delay(s) in the sense amplifier are important to ensure proper read operations?
  - Describe the global synchronization/timing requirement for the entire system to ensure read operation (draw simple waveform to explain this)
  - What happens to bitlines after WL goes high ?
  - What happens to the bitlines when sense-amplifier (SAE) gets enabled?
  - When the sensed data arrives at the output and gets latched at the data register?
- Show the waveform from CADENCE
- Report the delay that characterizes the read circuit.

PROBLEM 5: COMPLETE PERIPHERAL

Problem 5: Complete peripheral

- **Complete the row circuits**
  - Connect the 4- bit row address registers to Row decoders (with WL generation logic).
- **Complete the column circuits**
  - Assume 16 bitlines (bl and !bl) each with a cap. of 40fF
  - Connect the output of the bitlines to the read/write circuitry

Problem 5: Peripheral



Your design should have all the components present in the RED BOXES

What to submit with homework on Nov. 25

- **Block level Cadence schematic**
- **Waveform**
  - **Operation of Path (1): i.e. show row addr. gets propagated to the WL**
  - **Show waveforms verifying operation of Timing Path (3)**
    - **Read : Assume that VBL = VDD and !VBL = VDD - Δ for the column and show that if read operation is selected the sense-amp output latches the correct value**
    - **Write: Assume d = 1 and !d = 0 and show the bitlines for the column gets proper value**

What to submit with homework on Nov. 25

- **Report total delay for**
  - **Timing path (1): Positive CLK edge to positive WL edge**
  - **Timing path (2) – read: Positive edge at SAE to data arrival at the latch output**
  - **Timing path (2) – write: Positive edge at CLK to the change in the bitlines voltages (assume before the positive edge arrives all the bitlines are pre- charged to VDD)**

PART II SUBMISSION: SRAM CELL AND ARRAY (DEC. 08)

Problem 1

- **Create the schematic of SRAM cell with precharge transistors and 40fF bitline capacitances in Cadence**
  - ✓ Assume $W_p = W_{min}$, $W_{access} = 1.5W_p$, $W_{pd} = 2W_p$.
- **Simulate the cell to perform read and write operations**
  - ✓ Connect the cell to one WL (with 40fF cap) output of the row decoder circuits
  - ✓ Connect the column circuits to the cell.
  - ✓ Use worst-case Δ_{BIT} obtained previously for sense-amplifier firing. If you did not solve it use Δ_{BIT} = 100mV.

Problem 1

- SRAM cell design
- Do not worry about cell access delay at this point
  - let it be whatever it is for the assumed sizing.
  - At this point aim is to set-up schematic and simulation setup.
- Include the waveform showing the operations

Problem 2

- **SRAM cell design: size the different transistors of the SRAM cell to achieve the following cell parameters**

  - ✓ Read margin > 25% of V_{DD}
  - ✓ Write margin > 35% of V_{DD}
  - ✓ Cell access time (assuming 40fF bit line capacitances) is such that, total time required to obtain a bit-differential of Δ_{BIT} from the rising edge of the CLK < 200ps (i.e. CLK-q-delay of latch + row decoder + cell access time).
  - ✓ Cell area < 0.8 μm^2

Problem 2

- Use the methods described in lecture notes for **read margin and write margin measurements**.
- For **access time estimation** you can use either a simple read current based method or full transient simulation
- You can develop a simple formula for computing cell area from device widths (assuming L = 50 nm for all devices).
- Show the intermediate read margin, write margin, and cell access time values for different sizes you tried.
    - For read and write margins, give plots with respect to beta ratios (width ratio for you) as discussed in class.
    - For access time, plot the values as a function of device widths directly.

Problem 3 (solve concurrently with Problem 2)

- Draw the layout of the optimized cell from problem 2 in Cadence and estimate the total area.

- Perform DRC and LVS and include your DRC/LVS reports in your submission. Your design must be DRC?LVS clean to receive credit.

  - Remember you need to include the substrate and N-well contact even for the single cell to pass DRC.
  - Include it now, but later when you will create the SRAM array, you will delete them and create contacts at the higher level.

Problem 4

- Solve Problem-1 again with the optimized cell designed in Problem-2.
- Report the final “schematic-level” timing:
  - (a) CLK to WL
  - (b) cell access time
  - (c) sense-amplifier
  - (d) latch
- Show the maximum frequency at which you can read your array (schematic level).

Problem 5

- Create the schematic for the 16x4 array and connect it to the full-decoder and column circuits.
- This should complete the entire schematic level design of the entire memory system.
- Include the top level block diagram with your submission.

PART III SUBMISSION: ARRAY LAYOUT + FINAL REPORT (DEC. 21)

Array layout

- Make the layout of the full 16x4 SRAM array
- You need to add the pre-charge transistors to each column
  - Think about where you will place them
- Do not forget to include the substrate and the n0well contact
- Attach the power supply grid to the array
- Make it DRC and LVS clean
  - Remember to run LVS with 16x4 cell, pre-charge devices

Final Report

- Make the layout of the full 16x4 SRAM array
- You need to add the pre-charge transistors to each column
  - Think about where you will place them
- Do not forget to include the substrate and the n0well contact
- Attach the power supply grid to the array
- Make it DRC and LVS clean
  - Remember to run LVS with 16x4 cell, pre-charge devices

Final Report

- **IEEE Double-Column Format**
- **One report per group**
- **Present a block-diagram of the system and identify the critical components in the delay path**
- **Discuss the key design concept that you have used to design each components and interconnect them**
  - The key concepts only: Do not include the width of every transistors
  - If you have used any interesting technique this is the place to clearly mention it
  - Circuits are better understood from figures (not cadence printouts) – so figures to explain your trick
- **Present the schematic (with width of different transistors clearly readable - width numbers in Cadence printouts are normally not readable) and layout of the single SRAM cell**
  - **Include the layout as a figure in the word-file**

Final Report

- **Make a Table where you present the value of key properties of different components of your design**
  - Latch -> setup time and CLK-Q delay
  - Decoder -> row-decoder delay and column decoder delay (mention delay before array layout and after)
  - SRAM cell -> Read margin, write margin, area, and cell access time
  - Sense-amplifier -> worst-case delay and offset voltage
  - Write-circuit -> Delay to discharge a bitline from V_{dd} to 0
- **Show waeform (include only CLK, WL, cell nodes, bitlines, and final read-outs) of read and write operation**
  - Make sure the waveforms are readable
  - You will be given credit if you include the waveform as a figure in your report (not as a separate printout) – use the print-to-file option to create a picture, annotate it properly to indicate different signals

Final Report

- Report your total read access delay (CLK-edge to read-out signal) and write delay (CLK-edge to cell node)
- Report the maximum clock frequency till which you could run the system
- The maximum length (shorter the better) of the report is

4 pages

Additional pages will not only increase your effort it will also reduce your marks

4 page is a lot of space if you only report the important stuff - the top design conferences allow only 2-pages to explain a microprocessor design