The Universal NAND Gate

Required Reading: Sections 3-4 and 5-3 of <u>Digital Fundamentals</u> by Floyd

Objectives:

• To understand to logical properties of NAND gates.

- To learn the pin connections of the 74XX00 DIP integrated circuit.
- To connect inputs and outputs and test the operation of the NAND gate.
- To describe the operation of each of the NAND gates.
- To construct combinational logic circuits using only NAND gates
- To test the operation and complete a truth table of each circuit.

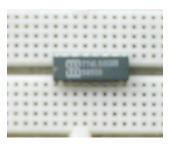
Materials: Lab kit for EL-204 and connecting wire

Equipment: Digital trainer

Procedure:

Part A: The 74XX00 Quad 2-input NAND DIP IC

- 1. Select the 74XX00 DIP IC from the components in the lab kit. Where XX my vary depending on the logic family included in the lab kit. Leave the trainer off until step 6.
- 2. Carefully insert the IC so it straddles the notch in the middle of the breadboarding socket and pin 1 is in the lower left as shown below.



- 3. Connect Vcc (pin 14) to the +5V power supply and GND (pin 7) to GND of the power supply.
- 4. Connect one of the two inputs to the first NAND gate on the package to Data Switch SW1 and the other to Data Switch SW2.
- 5. Connect the output of the first NAND (pin 3) to Logic Indicator L1.

The Data switches should put out an logical 1 when in the up position and a logical 0 when in the down position.

6. Apply power to the trainer and test the operation of the NAND by switching SW1 and SW2 to each condition in the truth table below and record the result.

| SW1 | SW2 | L1 |
|-----|-----|----|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

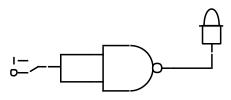
| SW1 | SW2 | L1 |
|-----|-----|----|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

7. Test the operation of the other three gates in the same fashion. Record any adverse results.

Part B: Other Logic Functions from NAND logic

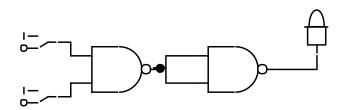
Construct each of the following logic circuits, complete the truth table, and identify the function being performed.

1.

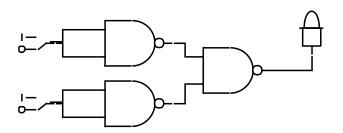


| SW1 | L1 |
|-----|----|
| 0 | |
| 1 | |
| L. | |

2.

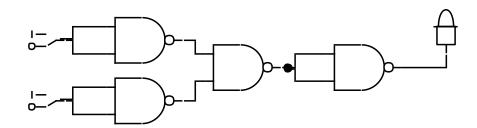


| SW1 | SW2 | L1 |
|-----|-----|----|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

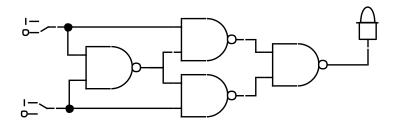


| SW1 | SW2 | L1 |
|-----|-----|----|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

4.



| SW1 | SW2 | L1 |
|-----|-----|----|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

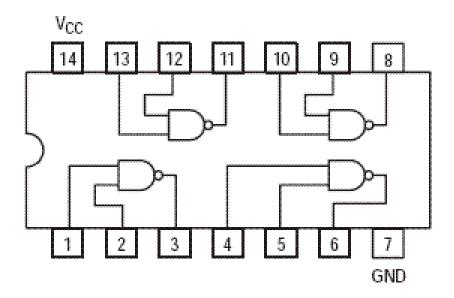


| SW1 | SW2 | L1 |
|-----|-----|----|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

Part C. Logic Design

Design, build, and test the operation of a logic circuit using only the 74XX00 that will perform the following function.

| A | В | С | |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |



7400 pin diagram