ENGR2420: Final Project

Designing a Rail-to-Rail CMOS Differential Amplifier
with a Constant-g_m Rail-to-Rail Input Stage

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1 Simple Rail to Rail Differential Amplifier

With shrinking supply voltages, rail-to-rail differential amplifiers are increasingly important in analog circuit design. To achieve this, the input stage of the differential amplifier can be designed with an N-channel and P-channel differential pair in parallel.

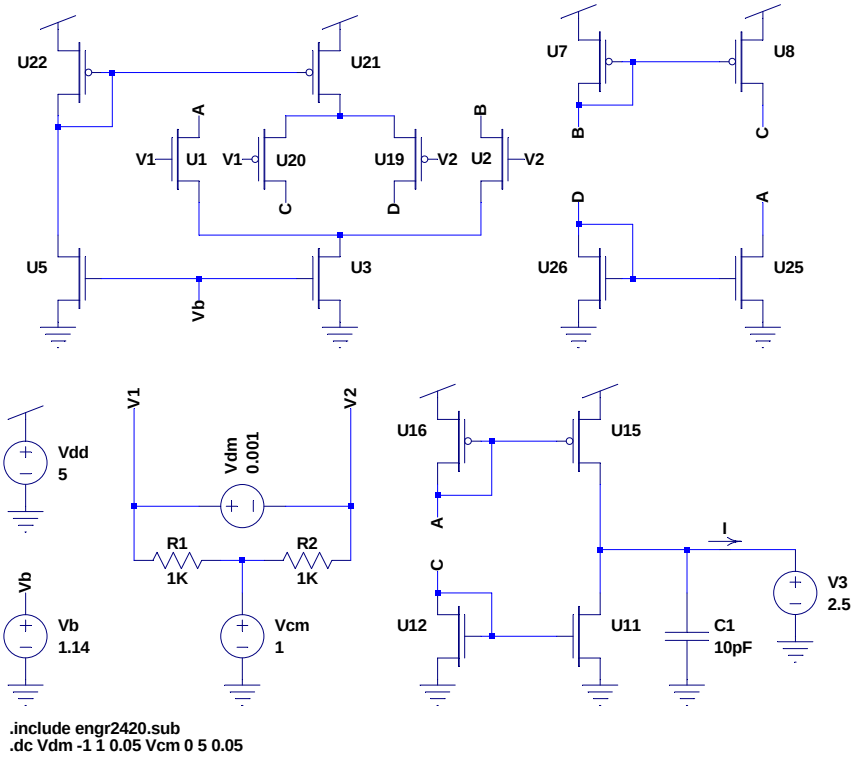

Figure 1: Schematic for a simple rail-to-rail differential amplifier connected as a unity-gain follower with a large load capacitor simulated in LTSpice.

When the common mode voltage (V_{cm}) is near the ground rail, only the P-channel differential pair operates, and near the V_{DD} rail, only the N-channel differential pair operates. However, in between the rails, both differential pairs are operating, which changes the transconductance (g_m) of the input stage, making it twice of that when only one differential pair is operating, as shown in Figure 2 on the following page.

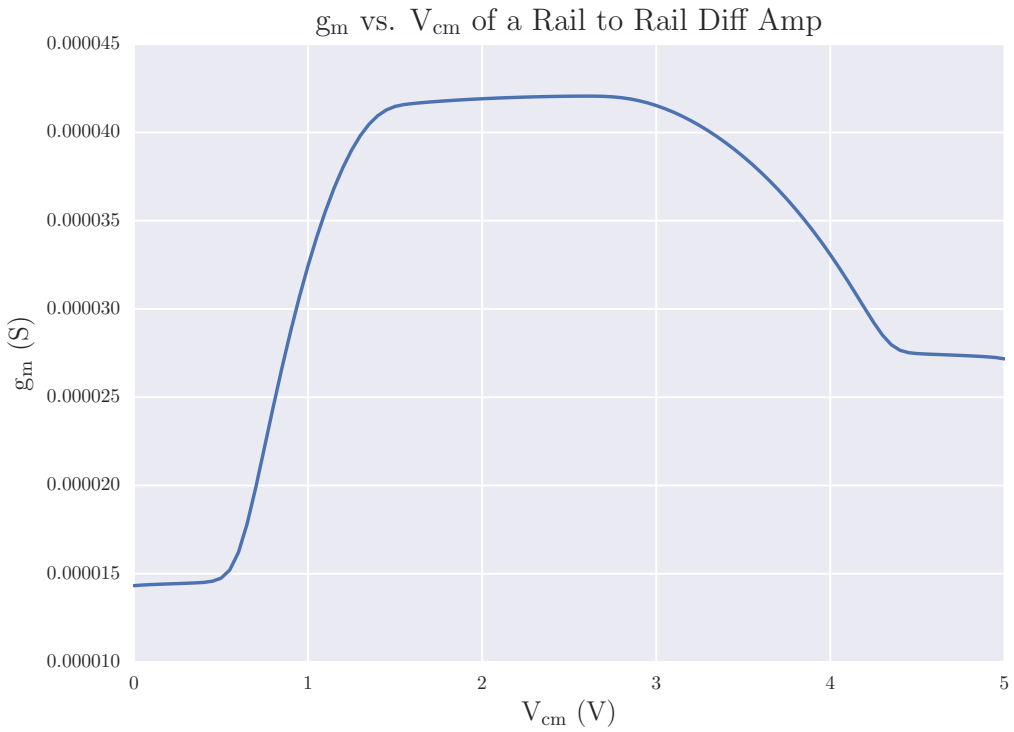

Figure 2: Transconductance of the rail-to-rail differential amplifier shown in Figure 1 on the preceding page versus the common mode voltage (V_{cm}).

2 Constant-g_m Rail to Rail Differential Amplifier

While there are many possible approaches to create a constant-g_m input stage to a rail-to-rail differential amplifier, a simple way to achieve constant-g_m is shown in Figure 3 on the next page.

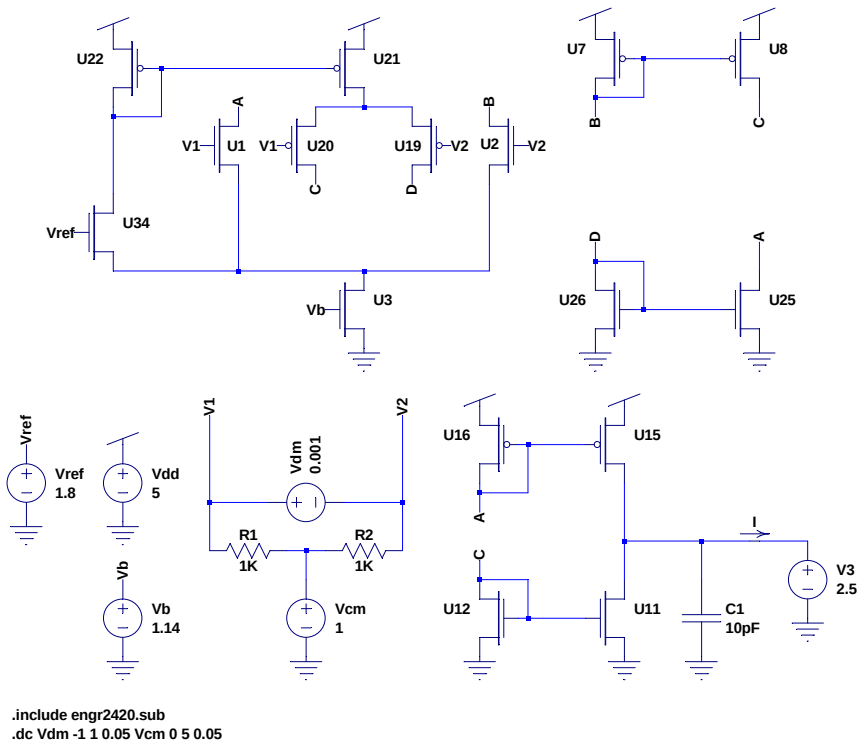

Figure 3: Schematic for a constant g_m rail-to-rail differential amplifier connected as a unity gain follower with a large load capacitor simulated in LTSpice.

In the rail-to-rail differential amplifier shown in Figure 1 on page 1, U5 mirrors the bias current (I_b) flowing through the nMOS bias transistor, U3, because both U5 and U3 are matched and have the same bias voltage (V_b). U22 and U21, which are also matched, form a pMOS current mirror, and because U22 is diode connected, the bias voltage for U21 will cause U21 to have the same I_b as U3.

Unfortunately, as V_{cm} leaves the rails, both the N-channel and P-channel differential pairs are active and their transconductances add, as shown in Figure 2 on the previous page. The problem is that the main factor controlling whether or not the N-channel and P-channel differential pairs are active is V_{cm}.

The rail-to-rail differential amplifier shown in Figure 3 mitigates the problem of a non-constant g_m. The only change is to disconnect the gate and source of U5 (now shown as U34) and reconnect them to V_{ref} and the node of the drain of U3, respectively. This allows us to tune V_{ref} and control when the N-channel and P-channel differential pairs are active.

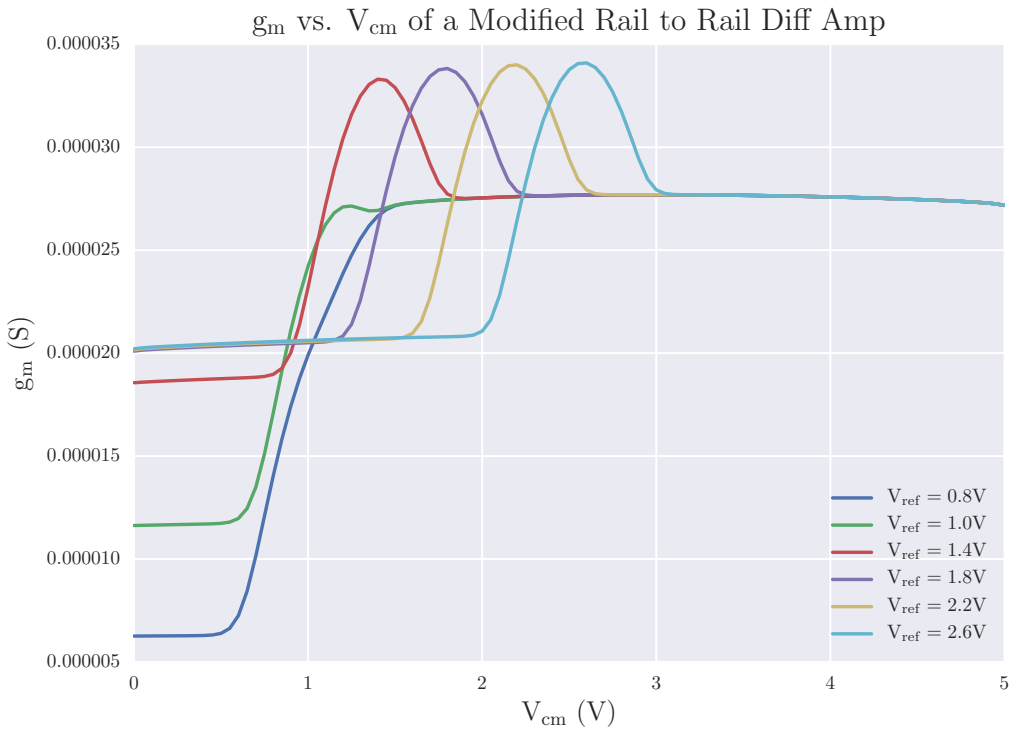

Figure 4: Transconductance of the constant g_m rail-to-rail differential amplifier shown in Figure 3 on the preceding page versus the common mode voltage (V_{cm}).

As V_{cm} drops from V_{DD}, the N-channel differential pair will eventually leave saturation. When that happens, current will begin flowing through U34, and the P-channel differential pair will begin to turn on. The current flowing through the P-channel differential pair will experience a proportional increase as the N-channel differential pair drops further and further out of saturation and U3 sources more and more current from U34. The opposite of this process happens when V_{cm} rises from the ground rail.

As a result, if V_{ref} is an appropriate value, U34 delays when the initially non-active differential pair turns on, and will only turn on the initially non-active differential pair as the initially active differential pair drops out of saturation. This results in a much flatter g_m curve from rail to rail, as shown in Figure 4.

When $V_{cm} = V_{ref}$, the current flowing through U34, U1, and U2 will all be about $\frac{1}{3}I_b$. This is the transition point when one differential pair becomes "more active" than the other differential pair. Because there is still a transition point where both differential pairs are active, g_m of this circuit is not completely flat, as shown by Figure 4. The peak of the spike in g_m corresponds to V_{ref} and where both differential amplifiers are contributing most to the overall transconductance of the circuit. It is, however, possible to tune V_{ref} to reduce or eliminate the spike in g_m at the cost of some bandwidth. For this simulated circuit, that is at about $1.04V$.

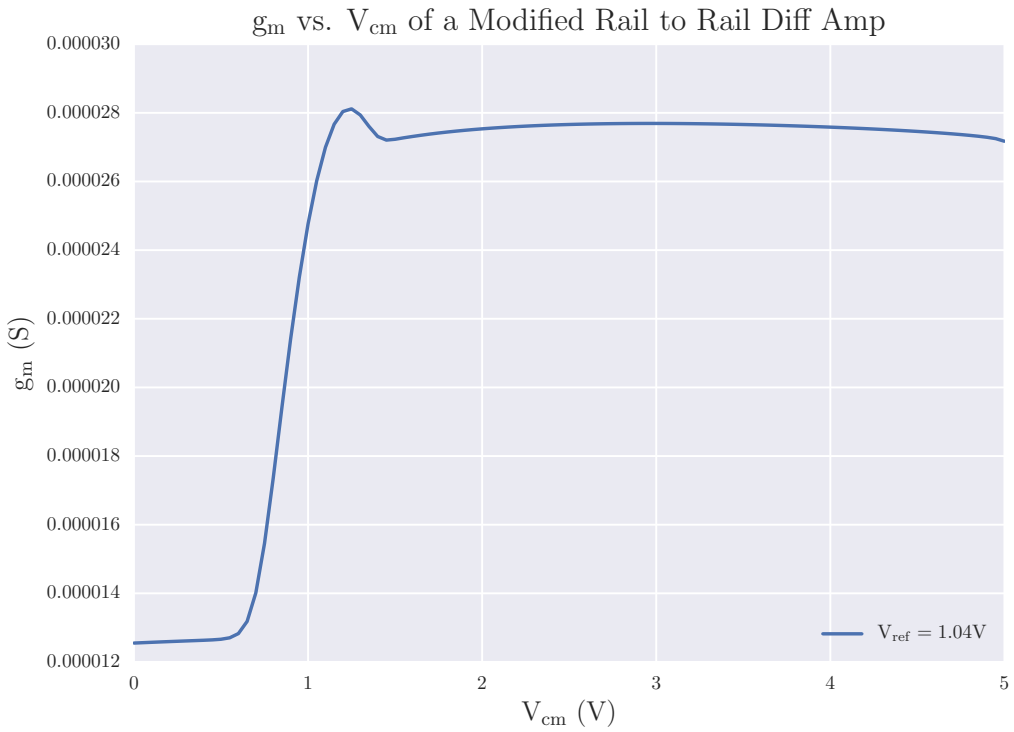

Figure 5: Transconductance of the constant g_m rail-to-rail differential amplifier shown in Figure 3 on page 3 versus the common mode voltage (V_{cm}) when V_{ref} is set to 1.04 V.

Another reason why the g_m characteristic for this circuit is not completely flat is due to electron/-hole mobility in nMOS and pMOS transistors. Because holes are less mobile than electrons, the pMOS transistors in this simulated circuit have a smaller transconductance gain than the nMOS transistors. This is why the g_m drops as V_{cm} approaches ground.

2.1 Below Threshold

When the bias transistor is below threshold, the spike in g_m is much smaller, as shown in Figure 6 on the next page.

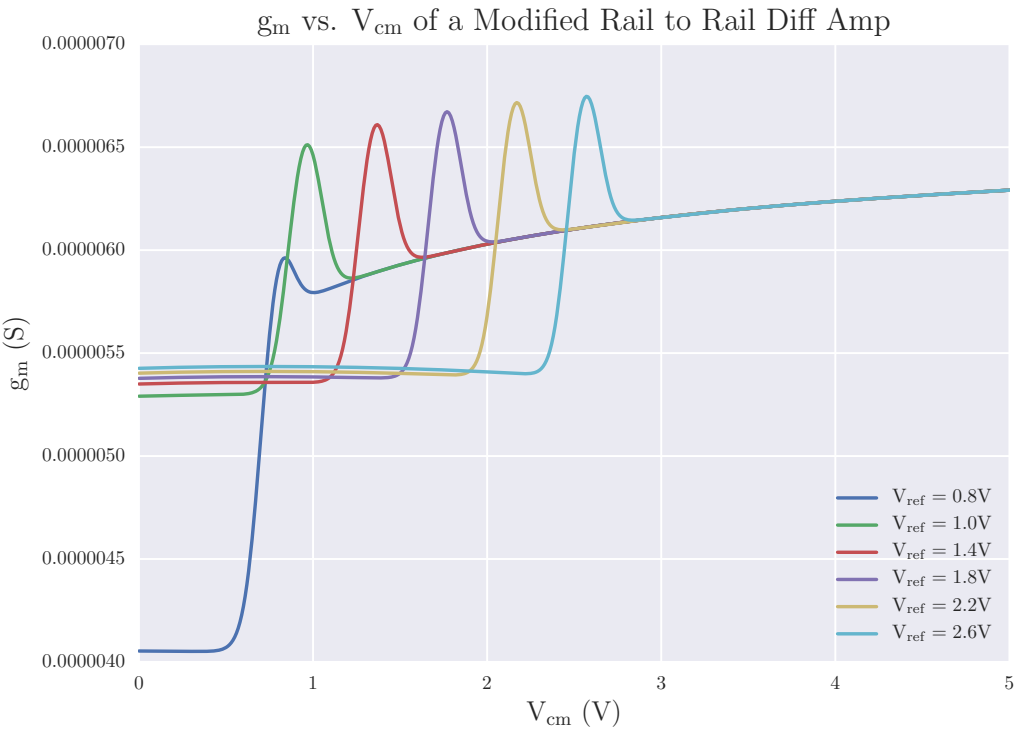

Figure 6: Transconductance of the constant g_m rail-to-rail differential amplifier shown in Figure 3 on page 3 versus the common mode voltage (V_{cm}) when the bias transistor is below threshold.

3 Appendix

To access the spice files and code for this project, go to my GitHub repository: `https://github.com/williamalu/CircuitsProject`

References

[1] Lu, Yan and Yao, Ruo He *Low-voltage constant-g_m rail-to-rail CMOS operational amplifier input stage*. Solid State Electronics, Elsevier, 2008.

[2] Minch, Bradley A. *A Low-Voltage MOS Cascode Bias Circuit For All Input Levels*. Cornell University, 2002.