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|  |  | Lab 2 Report |
|  |  | Logo, company name  Description automatically generated |
| William Beach  CDA3203 – Online Section  10/30/2022  Z23194964 |  |  |
|  |  |  |
|  |  | In lab 2, I’ve created a 1-bit half adder, 1-bit full adder, 4-bit full adder, 8-bit full adder, and 16-bit full adder circuit using only NAND gates. I’ve also utilized vector array notation and created a package of my components in order to abstract my VHDL code. This report includes the project settings, vector waveform files, VHDL code, and circuit drawings with only NAND gates (drawn using <https://app.diagrams.net/>) for each circuit. |

Graphical user interface, text, application

Description automatically generated**1-Bit Half Adder Circuit**

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| --- | --- | --- |
| Sum of Products  (Sum) :  F = AB’ + A’B  (Carry) :  F = AB |  | Scatter chart  Description automatically generated with medium confidenceGraphical user interface, table  Description automatically generated  Lab 2 Project settings 1-Bit Half Adder |
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A picture containing diagram

Description automatically generated

Vector Waveform Timing Diagram for 1- Bit Half Adder

Diagram

Description automatically generated

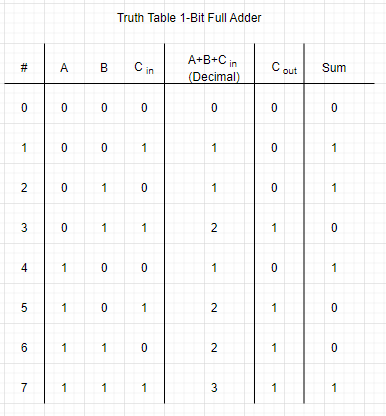
Graphical user interface

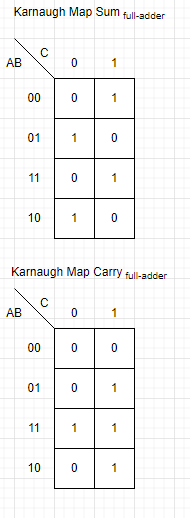
Description automatically generated with medium confidence**1-Bit Full Adder Circuit**

Sum of Products  
(Sum):

F = A’B’Cin + A’BC’in + AB’Cin’ + ABCin

(Carry):

F = BCin + AB + ACin

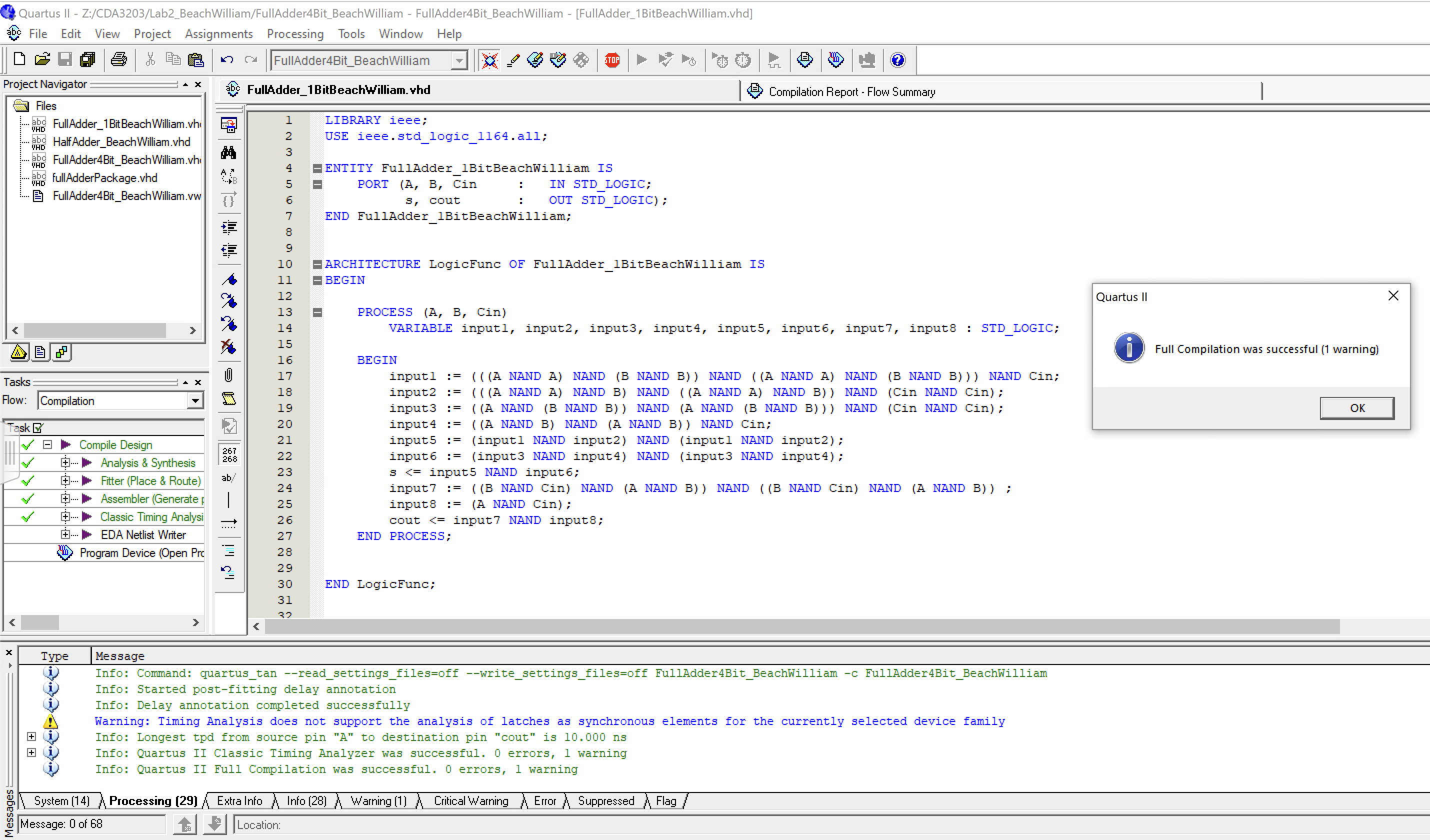


Graphical user interface, text, application, email

Description automatically generated

FullAdder Package that contains 1-Bit, 4-Bit, and 8-Bit Components

Lab 1 Project settings 1-Bit Full Adder



VHDL Code for 1-Bit Full Adder

A picture containing diagram

Description automatically generated

Vector Waveform Timing Diagram for 1-Bit Full Adder

Diagram

Description automatically generated

Graphical user interface, table

Description automatically generated

**4-Bit Full Adder Circuit**

Graphical user interface, text, application, email

Description automatically generated

VHDL Code utilizing package I made to contain full adder component

Lab 1 Project settings 4-Bit Full Adder

Graphical user interface

Description automatically generated

Vector Waveform Timing Diagram for 4-Bit Full Adder

Diagram, engineering drawing

Description automatically generated



**8-Bit Full Adder Circuit**

Lab 1 Project settings 8-Bit Full Adder

Table

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Graphical user interface, text, application

Description automatically generated

VHDL 8-Bit Full Adder using 2 4-Bit Components synthesized in fullAdder package

Graphical user interface, application, table

Description automatically generated

Diagram, schematic

Description automatically generatedTable

Description automatically generated with medium confidence**16-Bit Full Adder Circuit**

Vector Waveform Timing Diagram for 8-Bit Full Adder

Project settings 16-Bit Full Adder

Table

Description automatically generated with medium confidence

Graphical user interface, text, application

Description automatically generated

Graphical user interface, application

Description automatically generated with medium confidence

Vector Waveform Timing Diagram for 16-Bit Full Adder

VHDL 16-Bit Full Adder

Diagram

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