

# Lab 3 Report

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In lab 3, I've implemented data flip-flops to design and build memory. I utilize behavior architecture in lieu of design architecture to abstract the process. 1-Bit register, 16-Bit register, RAM, and program counter are designed and simulated. This report includes the project settings, vector waveform files, VHDL code, and circuit drawings with only NAND gates (drawn using <https://app.diagrams.net/>) for each circuit.

## Data Flip Flop (DFF)

### New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:

Z:/CDA3203/Lab3\_BeachWilliam/

Project name: DFF\_BeachWilliam

Top-level design entity: DFF\_BeachWilliam

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3064ATC100-4

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-85 °C

DFF (Data Flip Flop) Project settings

< Back

Next >

Finish

Cancel

The screenshot displays the Quartus II IDE interface. The top window shows the 'New Project Wizard: Summary' dialog, which lists the project settings for 'DFF\_BeachWilliam'. The settings include the project directory, name, top-level design entity, device assignments (MAX3000A, EPM3064ATC100-4), and EDA tools (all set to <None>). The operating conditions are also specified. Below the settings, a button labeled 'DFF (Data Flip Flop) Project settings' is visible. The bottom window shows the VHDL code for the DFF, which is a behavioral structure model. The code includes a library declaration, an entity declaration, and an architecture body. The architecture body contains a process that updates the output 'Q' on the rising edge of the clock 'clock'. The process is named 'PROCESS(clock)' and is enclosed in a 'BEGIN' block. The process body contains an 'IF' statement that checks if the clock is rising, and if so, it assigns the value of 'D' to 'Q'. The process ends with 'END PROCESS;' and the architecture ends with 'END Behavior;'. The bottom window also shows the 'Compilation Report - Flow Summary' and a message box indicating that the full compilation was successful with 2 warnings. The message box text is: 'Full Compilation was successful (2 warnings)'. The bottom window also shows the 'Messages' pane, which displays the compilation results, including warnings and errors.

Quartus II - Z:/CDA3203/Lab3\_BeachWilliam/DFF\_BeachWilliam - DFF\_BeachWilliam.vhd

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity	Macrocells	Pins
MAX3000A: EPM3064ATC100-4		
DFF_BeachWilliam	1	7

Tasks

Flow: Compilation

Task	Time
Compile Design	00:00:14
Analysis & Synthesis	00:00:06
Fitter (Place & Route)	00:00:02
Assembler (Generate programming files)	00:00:03
Classic Timing Analysis	00:00:03
EDA Netlist Writer	
Program Device (Open Programmer)	

Compilation Report - Flow Summary

```
1  -- Data Flip Flop Positive-Edge Triggered
2  -- Behavioral Structure VHDL Model
3  LIBRARY ieee;
4  USE ieee.std_logic_1164.all;
5
6  ENTITY DFF_BeachWilliam IS
7  PORT (D, clock: IN STD_LOGIC;
8        Q : OUT STD_LOGIC);
9  END DFF_BeachWilliam;
10
11 ARCHITECTURE Behavior OF DFF_BeachWilliam IS
12 BEGIN
13   --update on the rising edge of the clock
14   PROCESS(clock)
15   BEGIN
16     IF(RISING_EDGE(clock)) THEN
17       Q <= D;
18     END IF;
19   END PROCESS;
20 END Behavior;
```

Quartus II

Full Compilation was successful (2 warnings)

OK

Messages

Warning: Found pins functioning as undefined clocks and/or memory enables

Info: No valid register-to-register data paths exist for clock "clock"

Info: tsu for register "Q-reg0" (data pin = "D", clock pin = "clock") is 2.800 ns

Info: tco from clock "clock" to destination pin "Q" through register "Q-reg0" is 3.100 ns

Info: th for register "Q-reg0" (data pin = "D", clock pin = "clock") is -0.900 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings

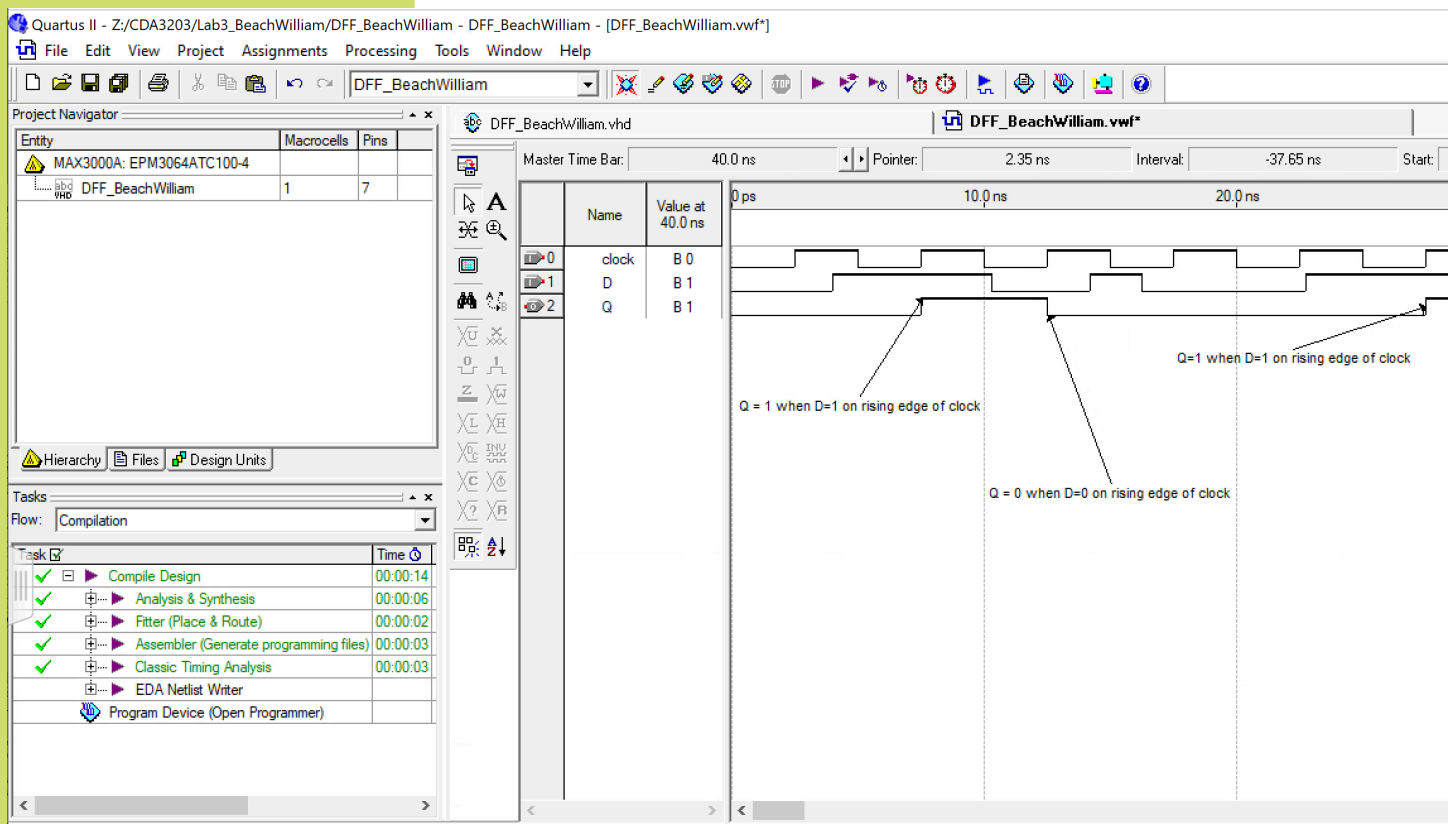
Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings

System (6) Processing (31) Extra Info Info (29) Warning (2) CriticalWarning Error Suppressed Flag

Message: 0 of 91

Location

Ln 8, Col 35 Idle NUM



Vector Waveform Timing Diagram for DFF

## 1-Bit Register

### New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:

C:/Users/public1/Lab3-BeachWilliam/

Project name: Register\_1Bit\_BeachWilliam

Top-level design entity: Register\_1Bit\_BeachWilliam

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3064ALC44-7

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-85 °C

Project settings 1-Bit Register

< Back

Next >

Finish

Cancel

Quartus II - C:/Users/public1/Lab3-BeachWilliam/Register\_1Bit\_BeachWilliam - Register\_1Bit\_BeachWilliam.vhd

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

MAX3000A: EPM3128AT1100-10

Register\_1Bit\_BeachWilliam

Register\_1Bit\_BeachWilliam.vhd

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ENTITY Register_1Bit_BeachWilliam IS
4  PORT (D, LOAD, CLOCK: IN STD_LOGIC;
5        Q: OUT STD_LOGIC);
6  END Register_1Bit_BeachWilliam;
7
8  ARCHITECTURE Behavior OF Register_1Bit_BeachWilliam IS
9  BEGIN
10     PROCESS (CLOCK)
11     BEGIN
12         IF RISING_EDGE (CLOCK) THEN
13             IF LOAD = '1' THEN
14                 Q <= D;
15             END IF;
16         END IF;
17     END PROCESS;
18 END Behavior;
```

Quartus II

Full Compilation was successful (2 warnings)

OK

VHDL Code for 1-Bit Register

Messages

Type Message

Warning: Found pins functioning as undefined clocks and/or memory enables

Info: No valid register-to-register data paths exist for clock "CLOCK"

Info: tsu for register "Q-reg0" (data pin = "D", clock pin = "CLOCK") is 6.600 ns

Info: tco from clock "CLOCK" to destination pin "Q" through register "Q-reg0" is 6.600 ns

Info: th for register "Q-reg0" (data pin = "LOAD", clock pin = "CLOCK") is -0.600 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings

Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings

System (185) Processing (31) Extra Info Info (29) Warning (2) CriticalWarning Error Suppressed Flag

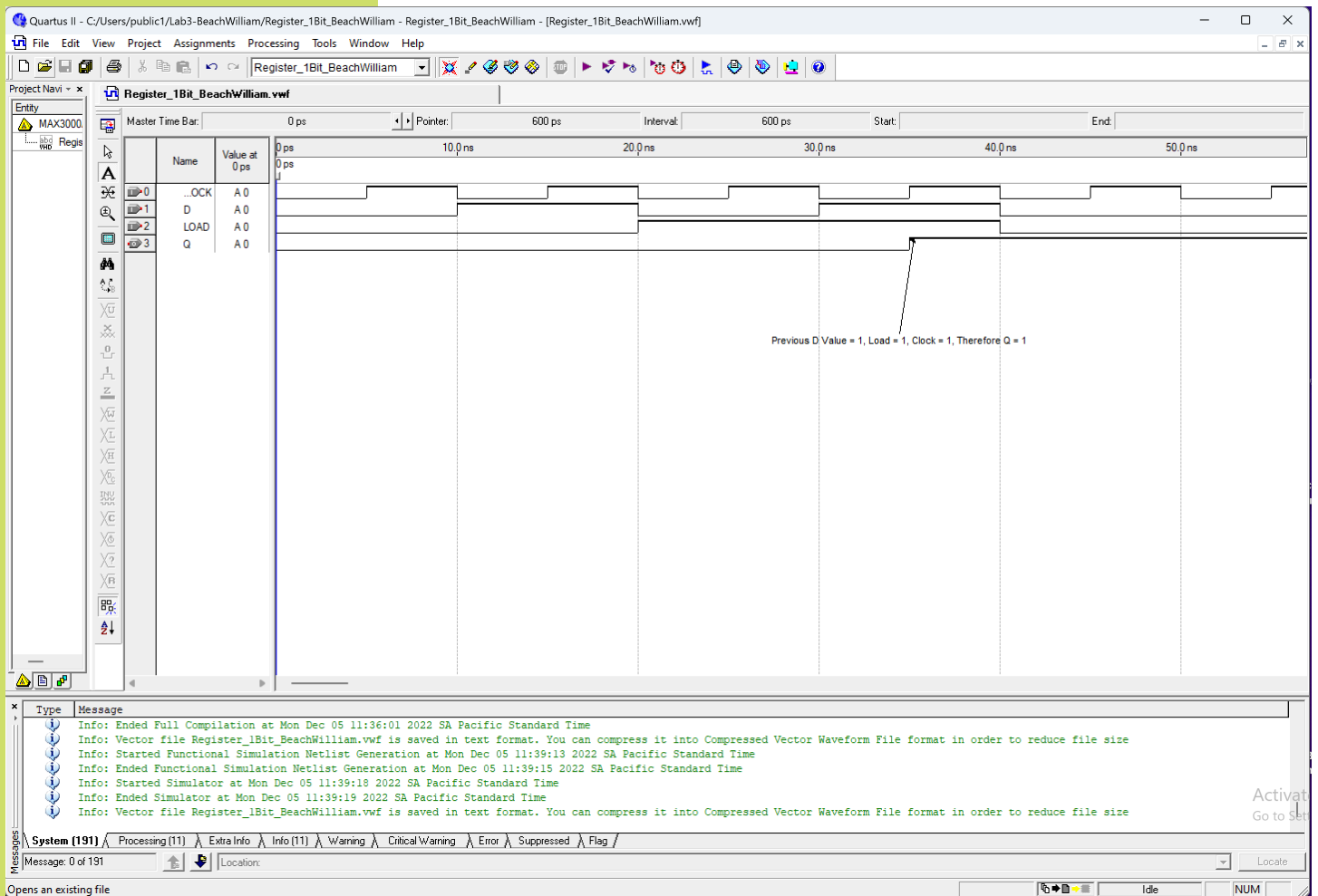
Message: 0 of 91

Location:

Ln 19, Col 10

Idle

NUM



Vector Waveform Timing Diagram for 1-Bit Register

## 16-Bit Register

### New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:

C:/Users/public1/Lab3-BeachWilliam/

Project name: Register\_16Bit\_BeachWilliam

Top-level design entity: Register\_16Bit\_BeachWilliam

Number of files added: 1

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3128AT1100-10

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-105 °C

< Back

Next >

Finish

Cancel

Project settings 16-Bit Register

Quartus II - C:/Users/public1/Lab3-BeachWilliam/Registered\_16Bit\_BeachWilliam - Register\_16Bit\_BeachWilliam.vhd

File Edit View Project Assignments Processing Tools Window Help

Project Navigator: Entity, MAX3000, Regis

Register\_16Bit\_BeachWilliam.vhd

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ENTITY Register_16Bit_BeachWilliam IS
4  PORT (LOAD, CLOCK: IN STD_LOGIC;
5        D      : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
6        Q      : OUT STD_LOGIC_VECTOR(15 DOWNTO 0));
7  END Register_16Bit_BeachWilliam;
8
9  ARCHITECTURE Behavior OF Register_16Bit_BeachWilliam IS
10 BEGIN
11   PROCESS (CLOCK)
12   BEGIN
13     IF RISING_EDGE(CLOCK) THEN
14       IF LOAD = '1' THEN
15         Q <= D;
16       END IF;
17     END IF;
18   END PROCESS;
19 END Behavior;
```

Compilation Report - Flow Summary

Quartus II

Full Compilation was successful (2 warnings)

OK

VHDL Code 16-Bit Register

Messages

Type Message

Warning: Found pins functioning as undefined clocks and/or memory enables

Info: No valid register-to-register data paths exist for clock "CLOCK"

Info: tsu for register "Q[15]-reg0" (data pin = "D[15]", clock pin = "CLOCK") is 6.600 ns

Info: tco from clock "CLOCK" to destination pin "Q[15]" through register "Q[15]-reg0" is 6.600 ns

Info: th for register "Q[0]-reg0" (data pin = "LOAD", clock pin = "CLOCK") is -0.700 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings

Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings

System (6) Processing (32) Extra Info Info (30) Warning (2) Critical Warning Error Suppressed Flag

Message: 0 of 94

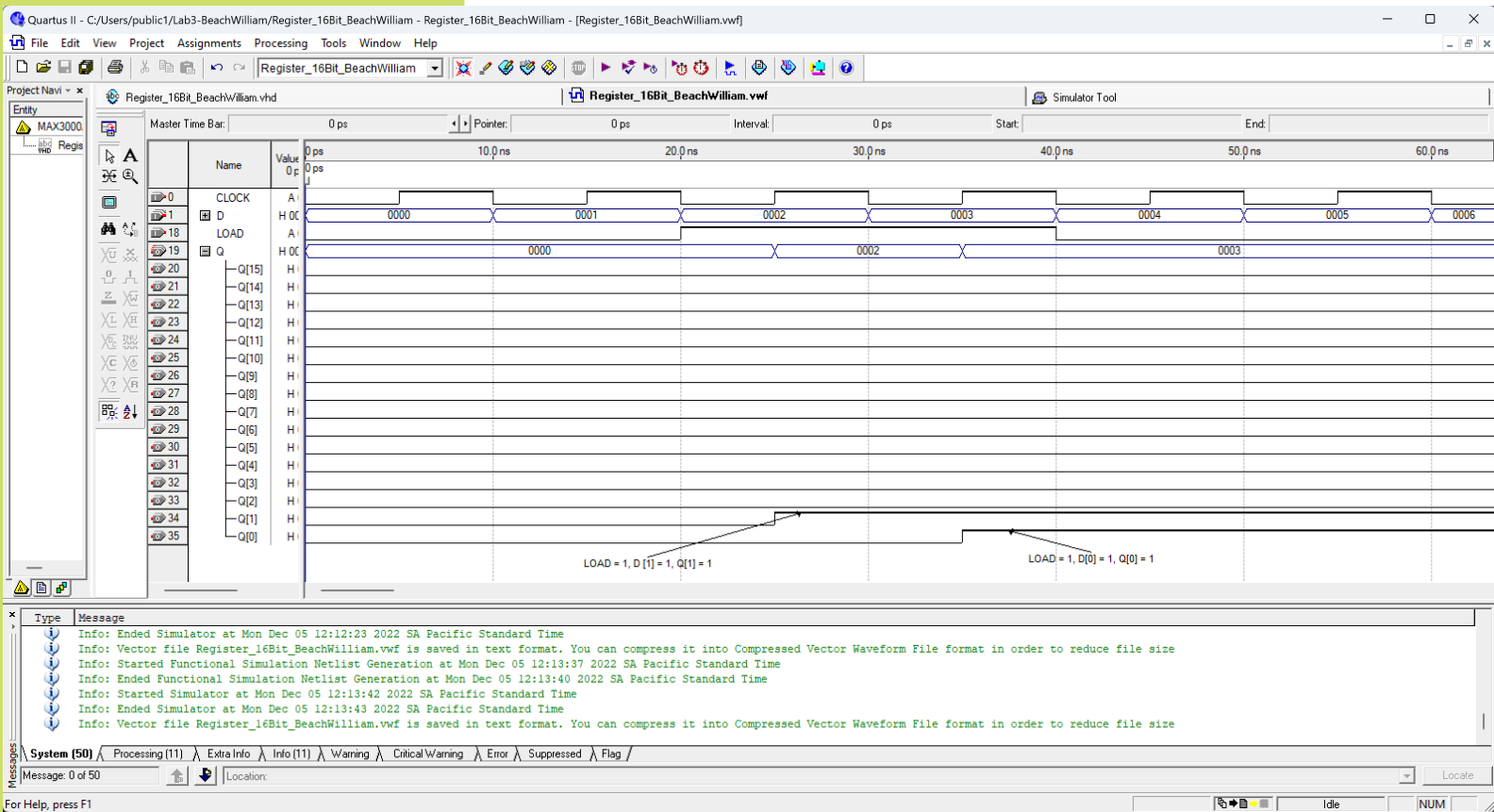
Location

For Help, press F1

Ln 18, Col 17

Idle

NUM



Vector Waveform Timing Diagram for 16-Bit Register

## Program Counter Register

New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:  
C:/Users/public1/Lab3-BeachWilliam/

Project name: PC\_Register\_BeachWilliam  
Top-level design entity: PC\_Register\_BeachWilliam  
Number of files added: 2  
Number of user libraries added: 0

Device assignments:  
Family name: MAX3000A  
Device: EPM3128AT1100-10

EDA tools:  
Design entry/synthesis: <None>  
Simulation: <None>  
Timing analysis: <None>

Operating conditions:  
Core voltage: 3.3V  
Junction temperature range: 0-105 °C

< Back Next > Finish Cancel

## Project settings Program Counter Register

Quartus II - C:/Users/public1/Lab3-BeachWilliam/PC\_Register\_BeachWilliam - PC\_Register\_BeachWilliam.vhd

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Files

- Register\_16Bit\_BeachWilliam.v
- Register\_1Bit\_BeachWilliam.v
- PC\_Register\_BeachWilliam.vf
- PC\_Register\_BeachWilliam.vv

PC\_Register\_BeachWilliam.vhd

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3 USE ieee.numeric_std.all;
4 ENTITY PC_Register_BeachWilliam IS
5     PORT (LOAD, INC, RESET, CLOCK: IN STD_LOGIC;
6           D: IN STD_LOGIC_VECTOR(15 DOWNTO 0);
7           Q: BUFFER STD_LOGIC_VECTOR(15 DOWNTO 0));
8 END PC_Register_BeachWilliam;
9
10 ARCHITECTURE Behavior OF PC_Register_BeachWilliam IS
11 BEGIN
12     PROCESS (CLOCK)
13     BEGIN
14         IF RISING_EDGE (CLOCK) THEN
15             IF RESET = '1' THEN
16                 Q <= "0000000000000000";
17             ELSIF LOAD = '1' THEN
18                 Q <= D;
19             ELSIF INC = '1' THEN
20                 Q <= STD_LOGIC_VECTOR(UNSIGNED(Q) + 1);
21             ELSE
22                 Q <= Q;
23             END IF;
24         END IF;
25     END PROCESS;
26 END Behavior;
```

Waveform1.vwf

Compilation Report - Flow Summary

Quartus II

Full Compilation was successful (2 warnings)

OK

Warning: Found pins functioning as undefined clocks and/or memory enables

Info: Clock "CLOCK" has Internal fmax of 97.09 MHz between source register "lpm\_counter:Q\_rtl\_0[dffs[0]]" and destination register "lpm\_counter:Q\_rtl\_0[dffs[0]]" (period= 10.3 ns)

Info: tsu for register "lpm\_counter:Q\_rtl\_0[dffs[0]]" (data pin = "INC", clock pin = "CLOCK") is 6.700 ns

Info: tco from clock "CLOCK" to destination pin "Q[15]" through register "lpm\_counter:Q\_rtl\_0[dffs[15]]" is 6.600 ns

Info: th for register "lpm\_counter:Q\_rtl\_0[dffs[15]]" (data pin = "D[15]", clock pin = "CLOCK") is -2.400 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings

Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings

System (103) Processing (46) Extra Info Info (44) Warning (2) Critical Warning Error Suppressed Flag

Message: 0 of 131

Location:

For Help, press F1

Ln 7, Col 29

Activate Windows

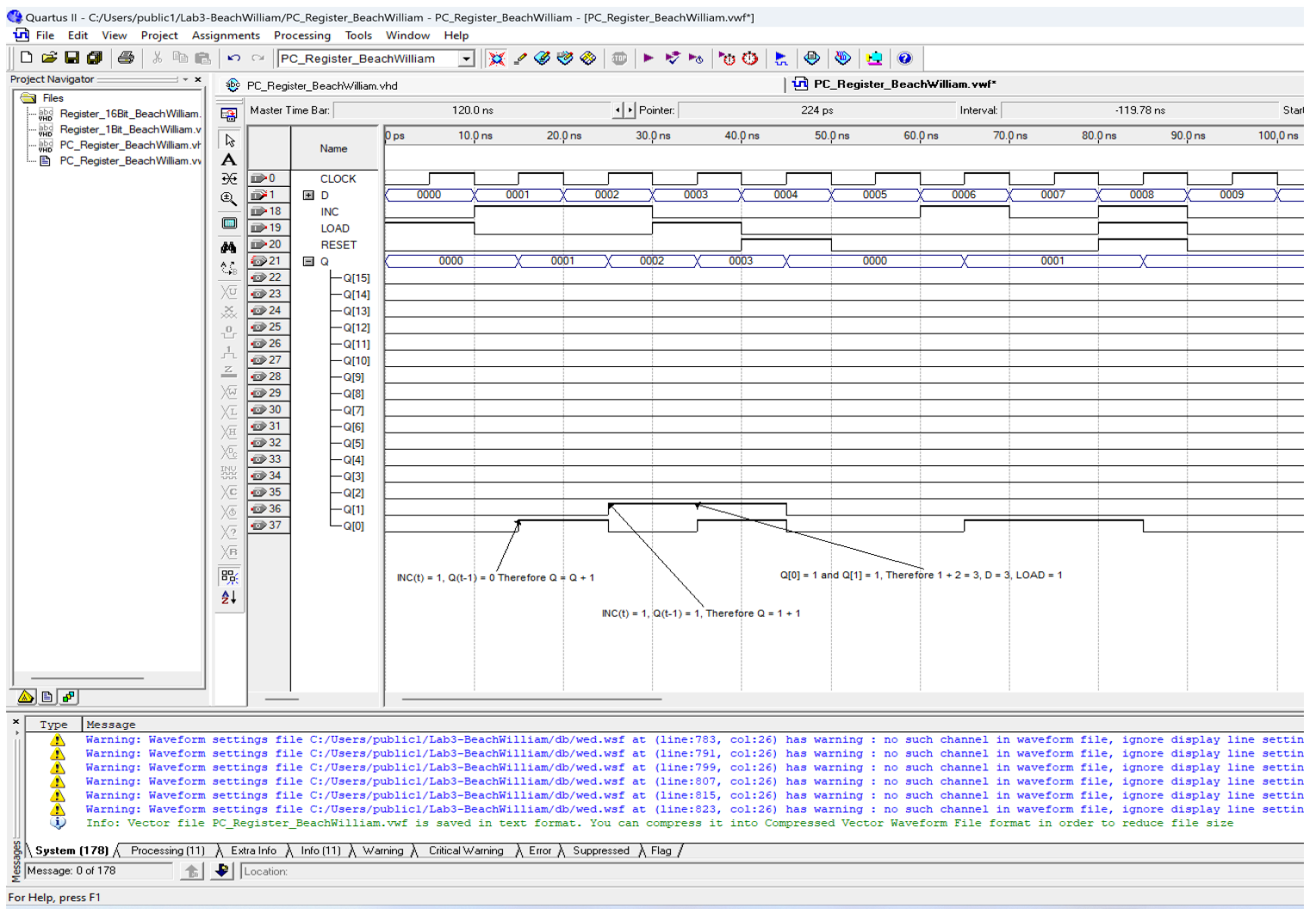
Go to Settings to activate Windows.

Locate

NUM

## Program Counter Register VHDL





Vector Waveform Timing Diagram PC Register

## 8 Register RAM

New Project Wizard: Summary [page 5 of 5] X

When you click Finish, the project will be created with the following settings:

Project directory:  
C:/Users/public1/Lab3-Beach/William/

Project name: RAM\_8\_Beach/William  
Top-level design entity: RAM\_8\_Beach/William  
Number of files added: 3  
Number of user libraries added: 0

Device assignments:  
Family name: MAX3000A  
Device: EPM3128AT1100-10

EDA tools:  
Design entry/synthesis: <None>  
Simulation: <None>  
Timing analysis: <None>

Operating conditions:  
Core voltage: 3.3V  
Junction temperature range: 0-105 °C

< Back Next > Finish Cancel

Project settings 8 Register RAM

Quartus II - C:/Users/public1/Lab3-BeachWilliam/RAM\_8\_BeachWilliam - RAM\_8\_BeachWilliam - [RAM\_8\_BeachWilliam.vhd]

File Edit View Project Assignments Processing Tools Window Help

RAM\_8\_BeachWilliam

RAM\_8\_BeachWilliam.vwf

Compilation Report - Flow Summary

Entity

MAX3000A

RAM

1

LIBRARY ieee;

2

USE ieee.std\_logic\_1164.all;

3

USE ieee.numeric\_std.all;

4

ENTITY RAM\_8\_BeachWilliam IS

5

PORT (LOAD, CLOCK: IN STD\_LOGIC;

6

ADDRESS : IN STD\_LOGIC\_VECTOR (2 DOWNTO 0);

7

D : IN STD\_LOGIC\_VECTOR (15 DOWNTO 0);

8

Q : OUT STD\_LOGIC\_VECTOR (15 DOWNTO 0));

9

END RAM\_8\_BeachWilliam;

10

11

ARCHITECTURE Behavior OF RAM\_8\_BeachWilliam IS

12

TYPE RAM\_ARRAY IS ARRAY (7 DOWNTO 0) OF STD\_LOGIC\_VECTOR (15 DOWNTO 0);

13

SIGNAL RAM\_SELECTION: RAM\_ARRAY;

14

BEGIN

15

PROCESS (CLOCK)

16

BEGIN

17

IF RISING\_EDGE (CLOCK) THEN

18

IF LOAD = '1' THEN

19

RAM\_SELECTION (to\_integer (unsigned (ADDRESS))) <= D;

20

END IF;

21

END IF;

22

END PROCESS;

23

Q <= RAM\_SELECTION (to\_integer (unsigned (ADDRESS)));

24

END Behavior;

Quartus II

Full Compilation was successful (2 warnings)

OK

Type

Message

Info: Clock "CLOCK" has Internal fmax of 125.0 MHz between source register "RAM\_SELECTION-21" and destination register "RAM\_SELECTION-21" (period= 8.0 ns)

Info: tsu for register "RAM\_SELECTION-20" (data pin = "ADDRESS[2]", clock pin = "CLOCK") is 6.100 ns

Info: tco from clock "CLOCK" to destination pin "Q[14]" through register "RAM\_SELECTION-34" is 10.800 ns

Info: Longest tpd from source pin "ADDRESS[0]" to destination pin "Q[15]" is 8.900 ns

Info: th for register "RAM\_SELECTION-35" (data pin = "D[15]", clock pin = "CLOCK") is -2.200 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings

Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings

System (73)

Processing (36)

Extra Info

Info (34)

Warning (2)

Critical Warning

Error

Suppressed

Flag

Message: 0 of 147

Location:

For Help, press F1

Ln 4, Col 29

Idle

NUM

VHDL 8 Register RAM

The figure is a Vector Waveform Timing Diagram for an 8 Register RAM. It displays the timing of several signals over a period of 240.0 ns. The signals are: CLOCK, ADDRESS (A[2]), D (D[15]), LOAD, and the 16-bit output Q (Q[15] through Q[0]).

The diagram shows the following sequence of events:

- Initial State:** LOAD = 0, D = 8, ADDRESS = 0, Q = 0.
- Event 1:** At approximately 20 ns, LOAD becomes 1, D becomes 2, and ADDRESS becomes 2. The output Q[2] changes to 2.
- Event 2:** At approximately 80 ns, LOAD becomes 0, D becomes 10, and ADDRESS becomes 2. The output Q[2] changes to 10.
- Event 3:** At approximately 140 ns, LOAD becomes 1, D becomes 12, and ADDRESS becomes 4. The output Q[4] changes to 12.

The output Q is shown as a 16-bit vector, with each bit Q[15] through Q[0] having its own signal trace. The diagram also shows the ADDRESS signal as a 3-bit vector (A[2] through A[0]) and the D signal as a 16-bit vector (D[15] through D[0]).

Vector Waveform Timing Diagram for 8 Register RAM