Lab 3 Report

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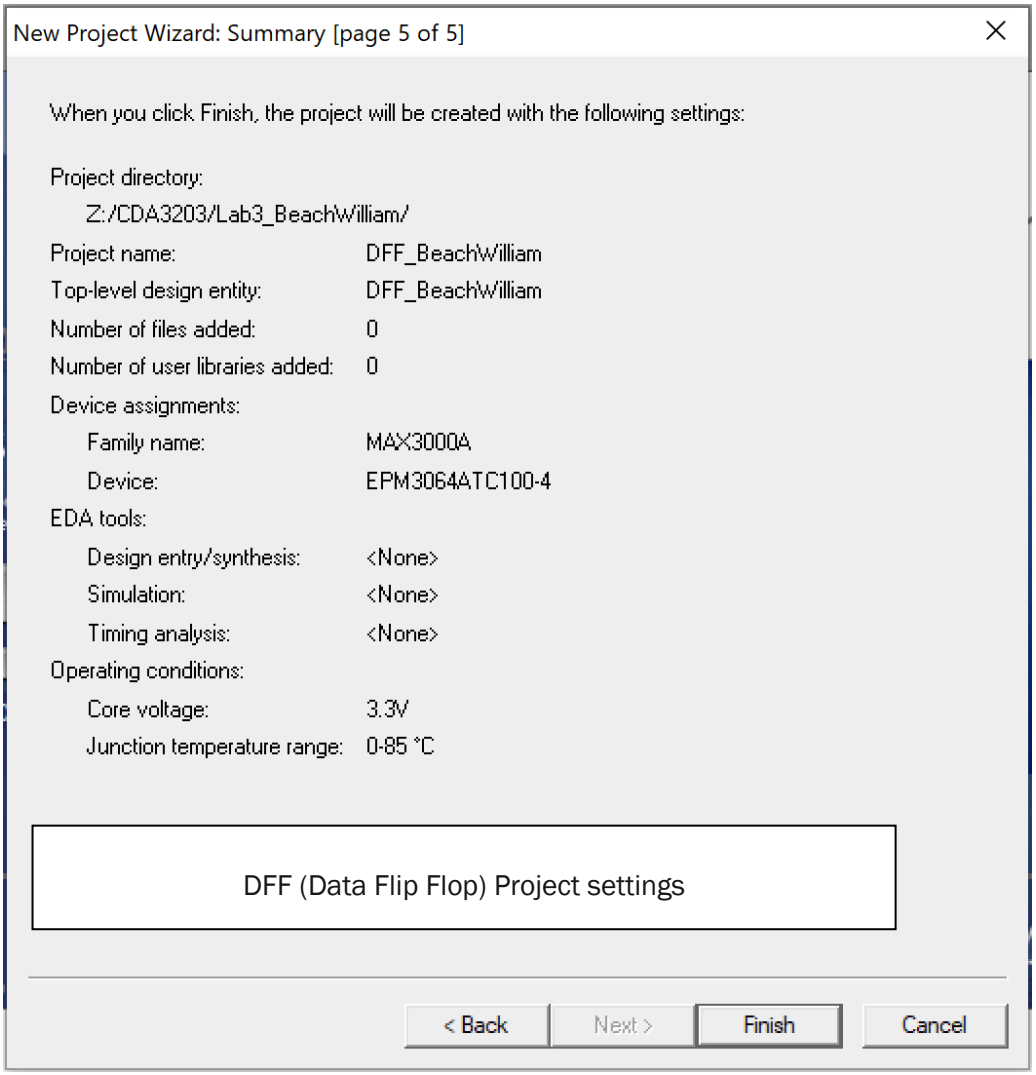
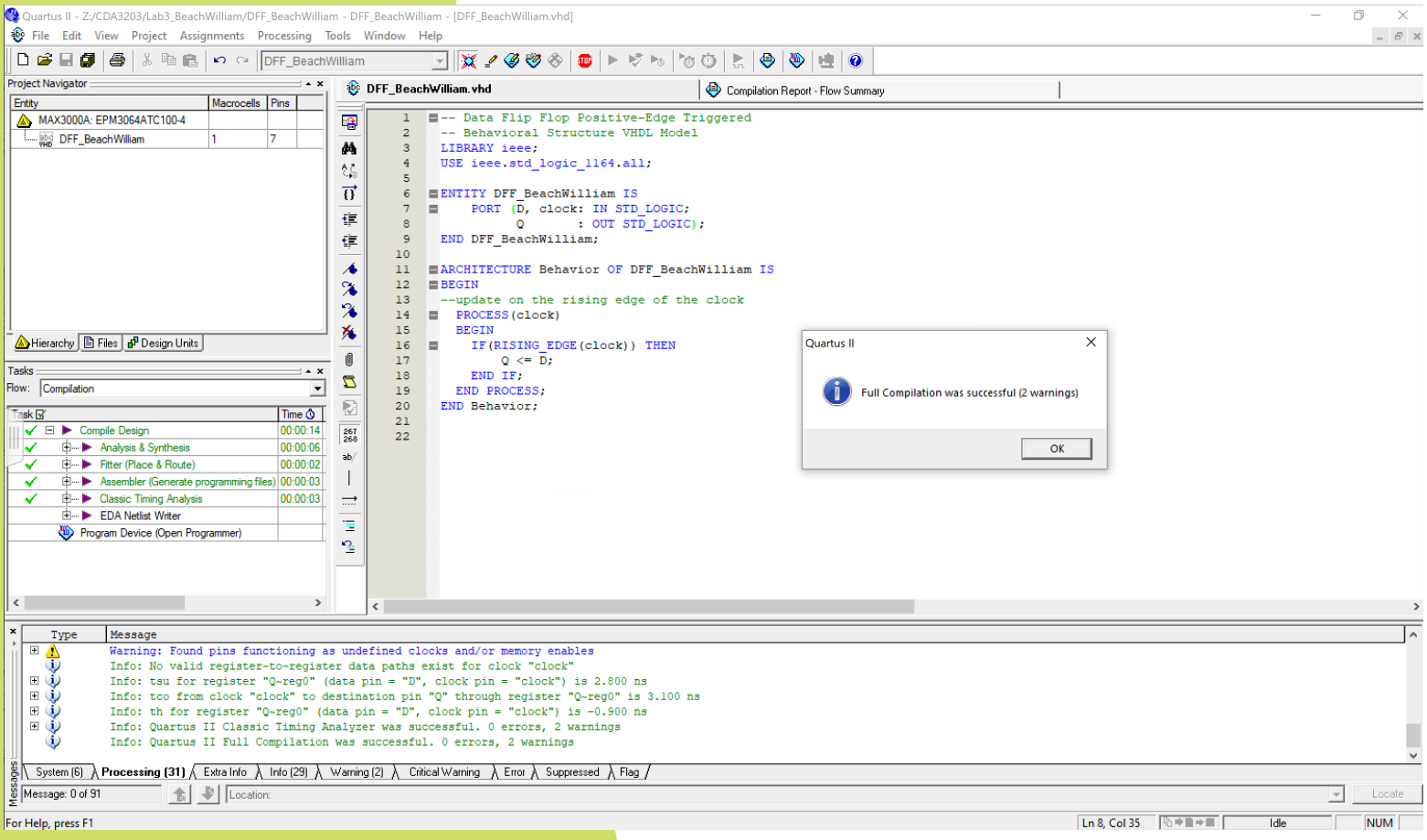
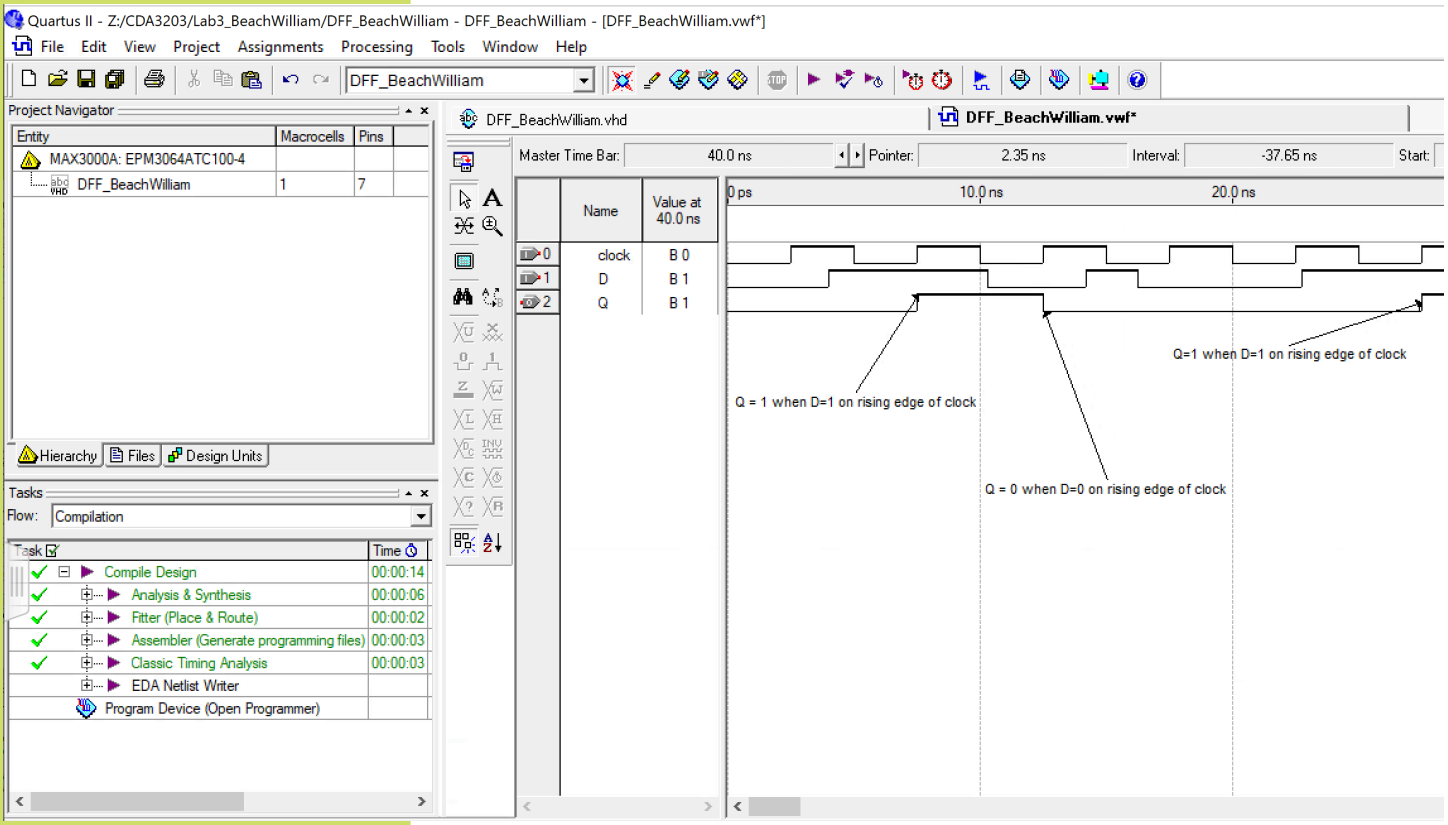
In lab 3, I've implemented data flip-flops to design and build memory. I utilize behavior architecture in lieu of design architecture to abstract the process. 1-Bit register, 16-Bit register, RAM, and program counter are designed and simulated. This report includes the project settings, vector waveform files, VHDL code, and circuit drawings with only NAND gates (drawn using https://app.diagrams.net/) for each circuit.

Data Flip Flop (DFF)



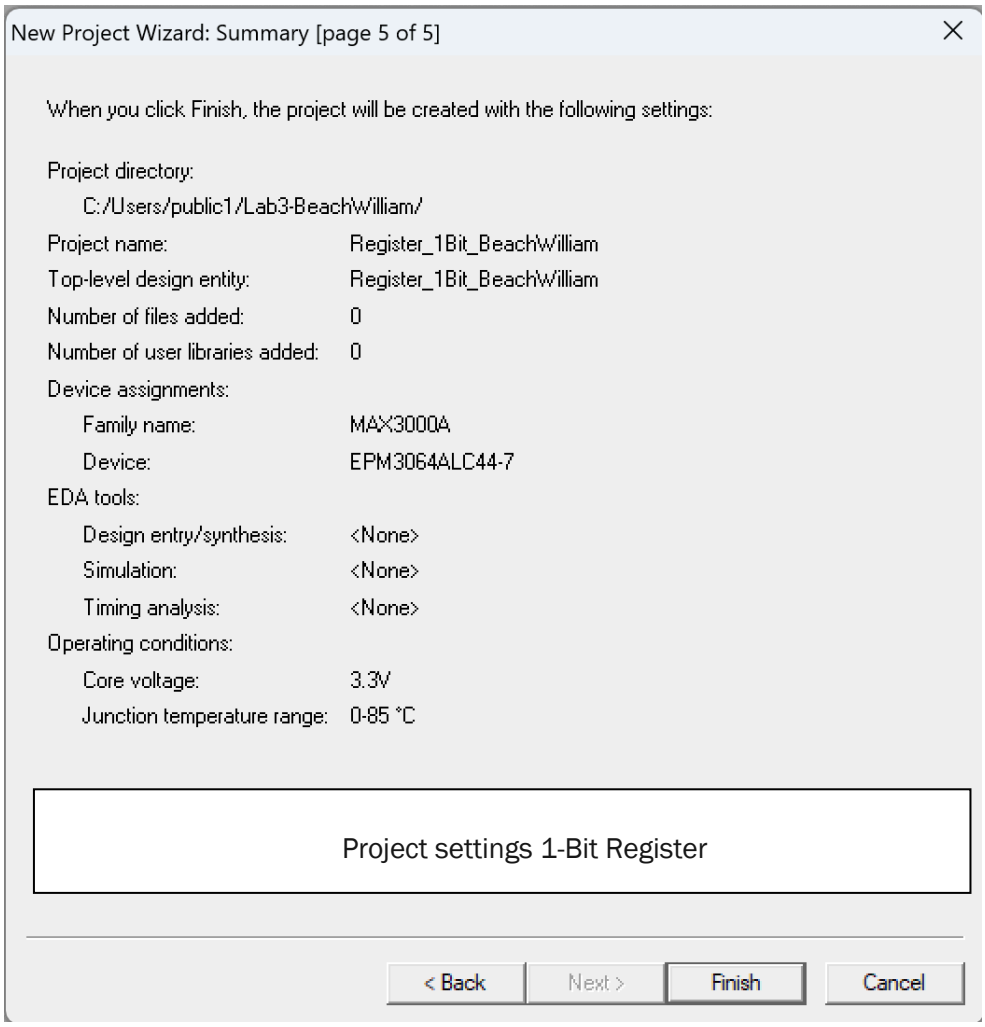
DFF (Data Flip Flop) Project settings



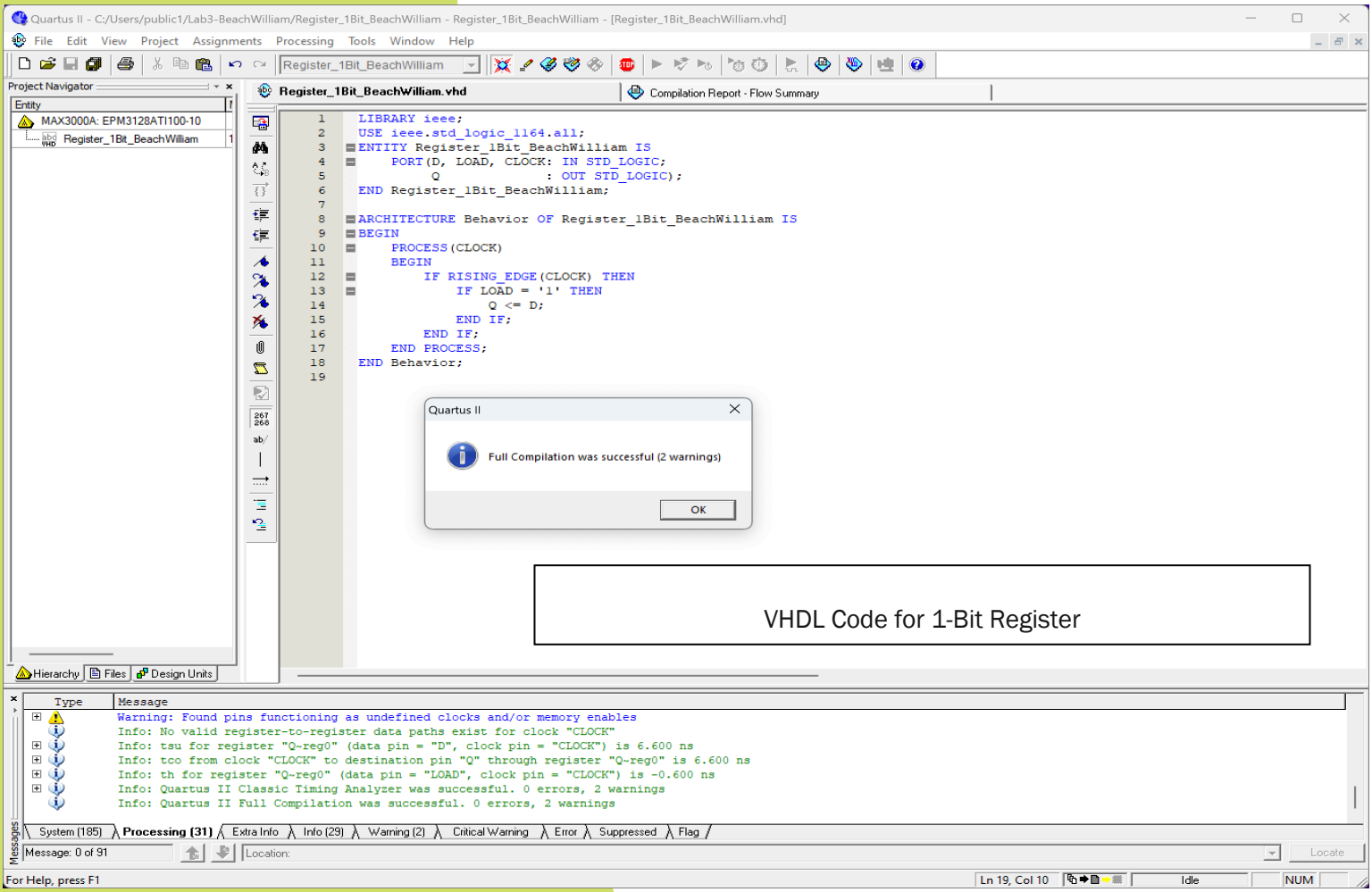


Vector Waveform Timing Diagram for DFF

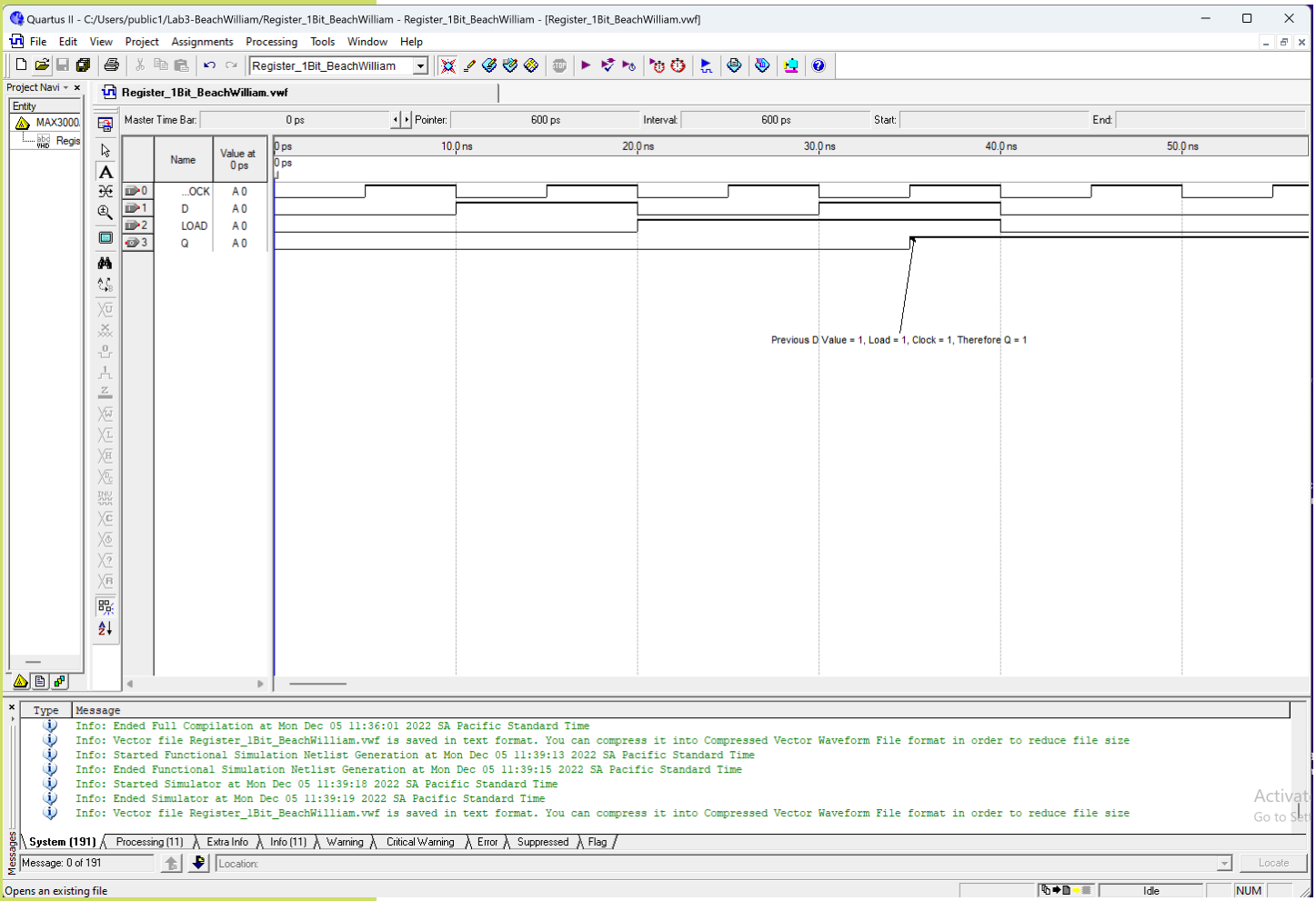
1-Bit Register



Project settings 1-Bit Register

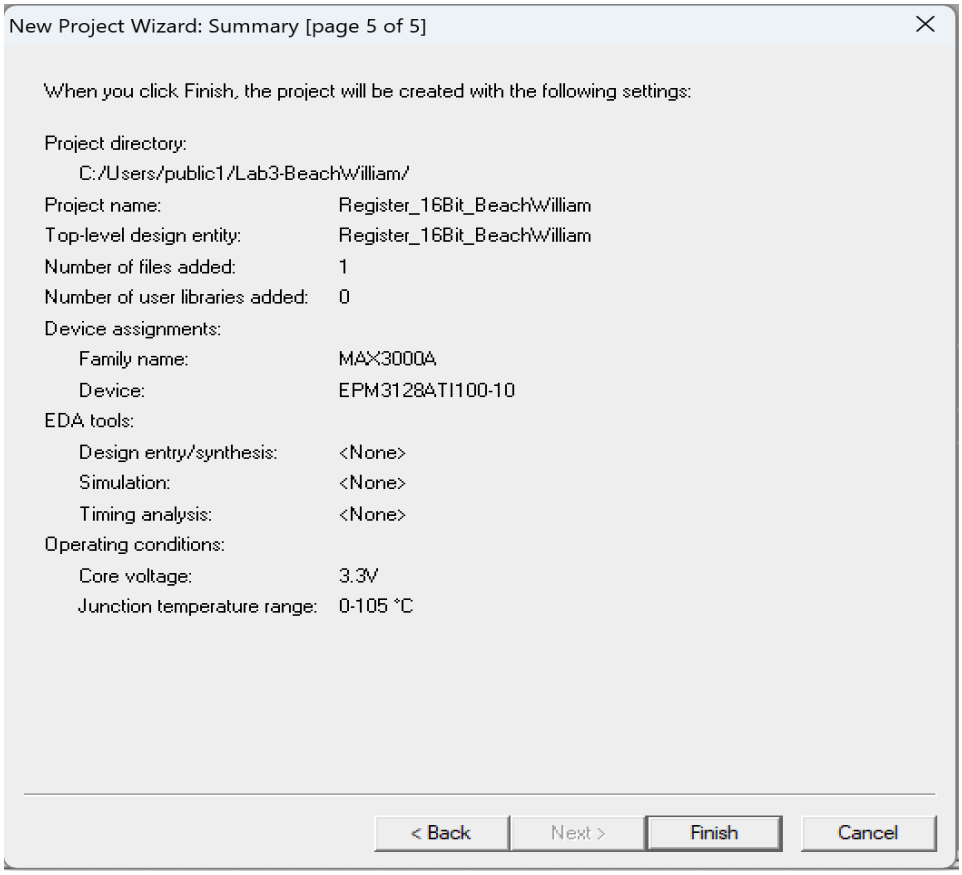


VHDL Code for 1-Bit Register

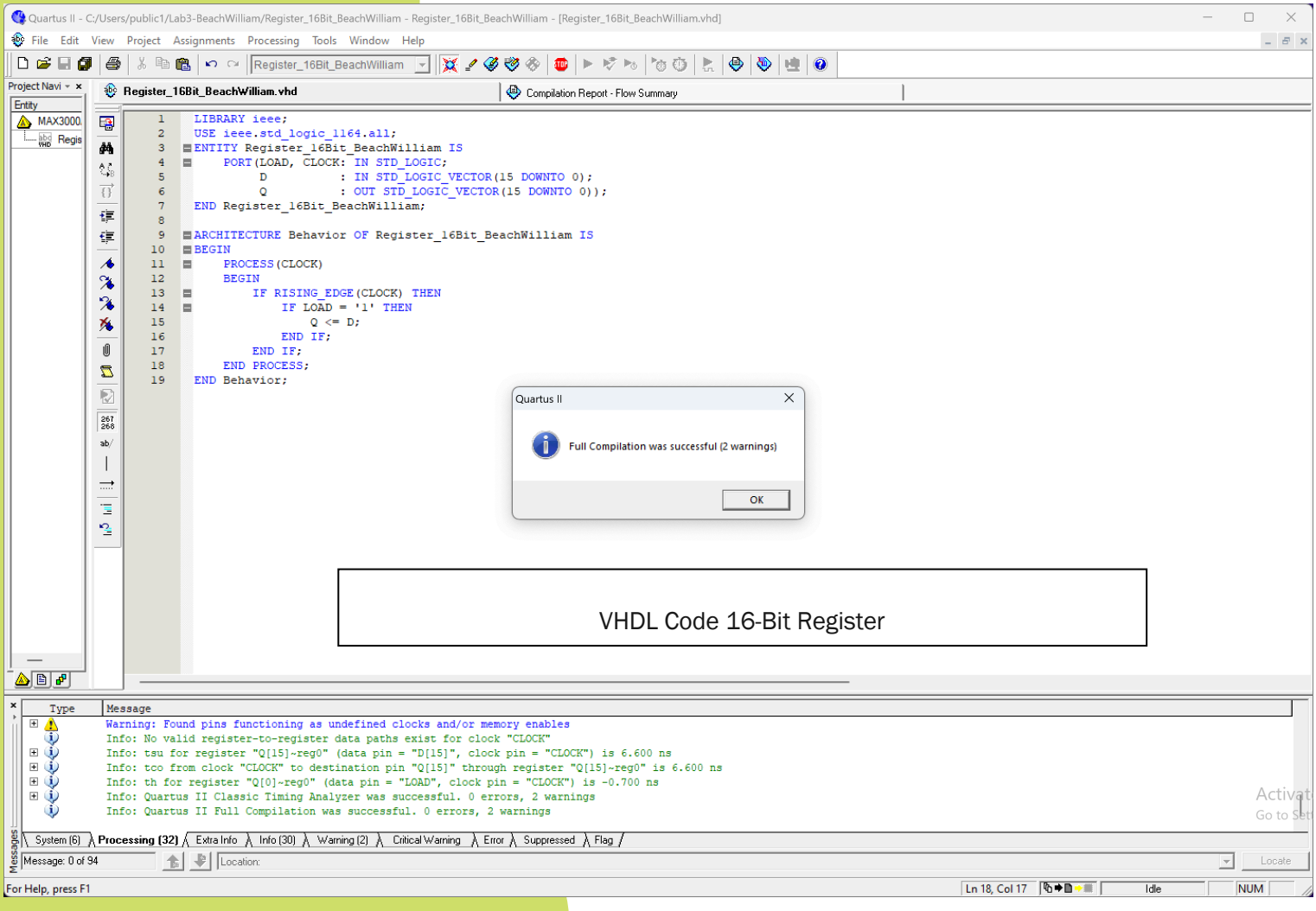


Vector Waveform Timing Diagram for 1-Bit Register

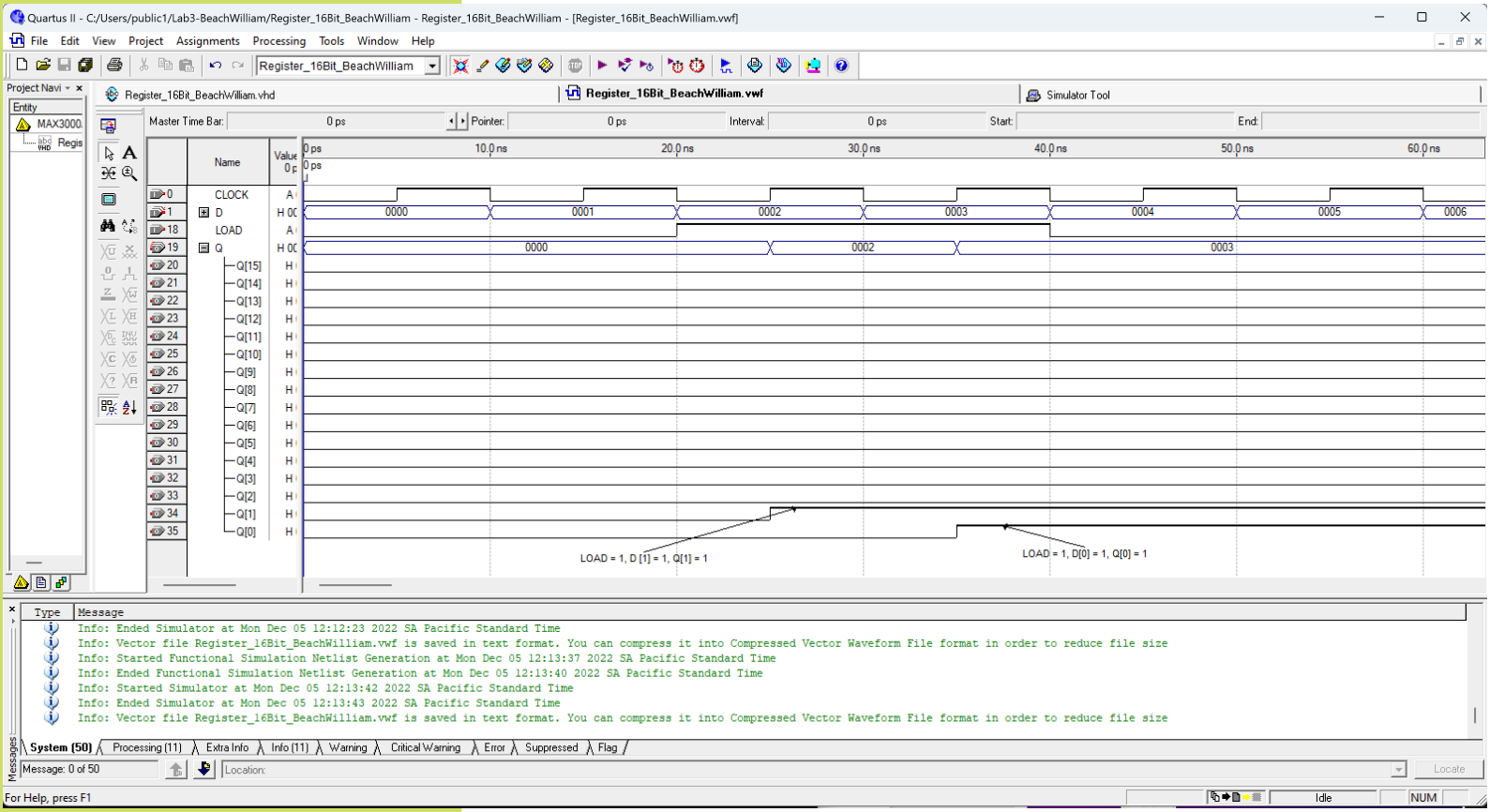
16-Bit Register



Project settings 16-Bit Register

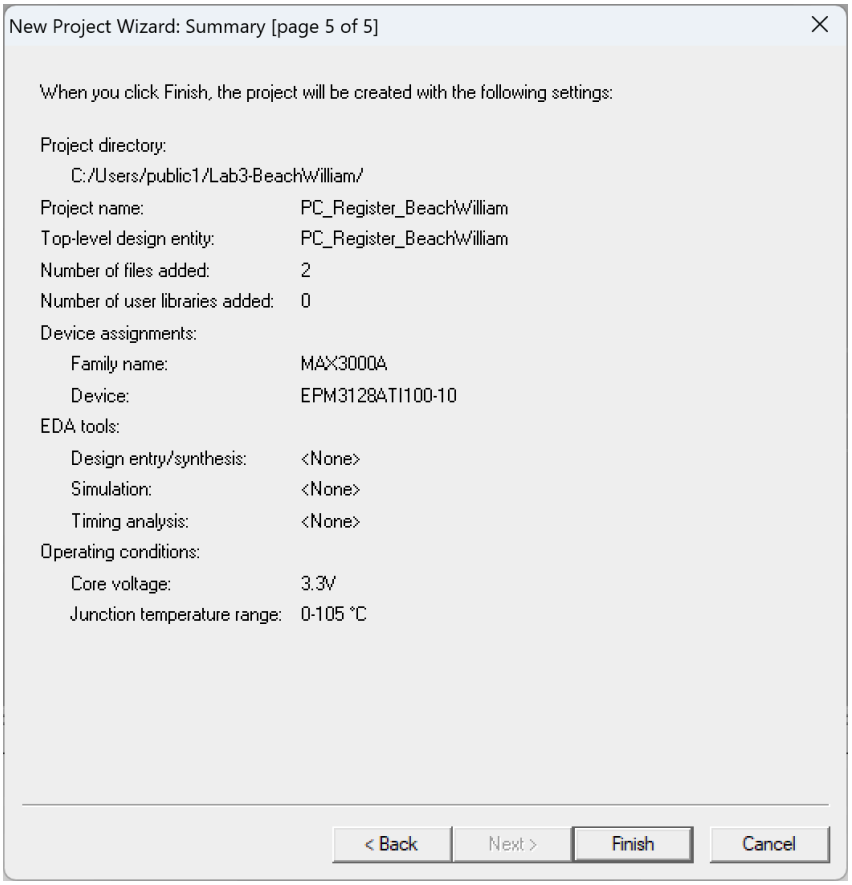


VHDL Code 16-Bit Register

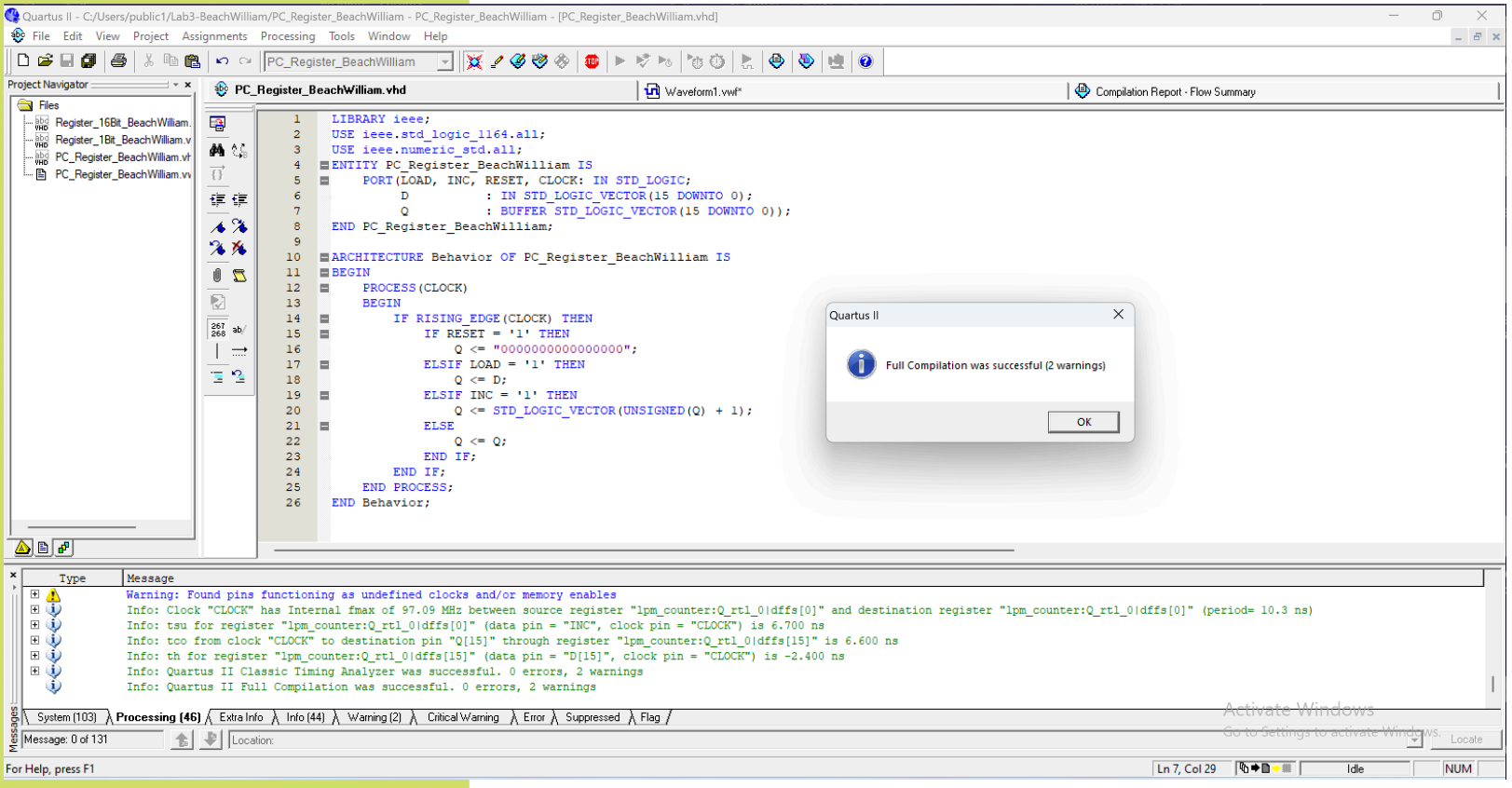


Vector Waveform Timing Diagram for 16-Bit Register

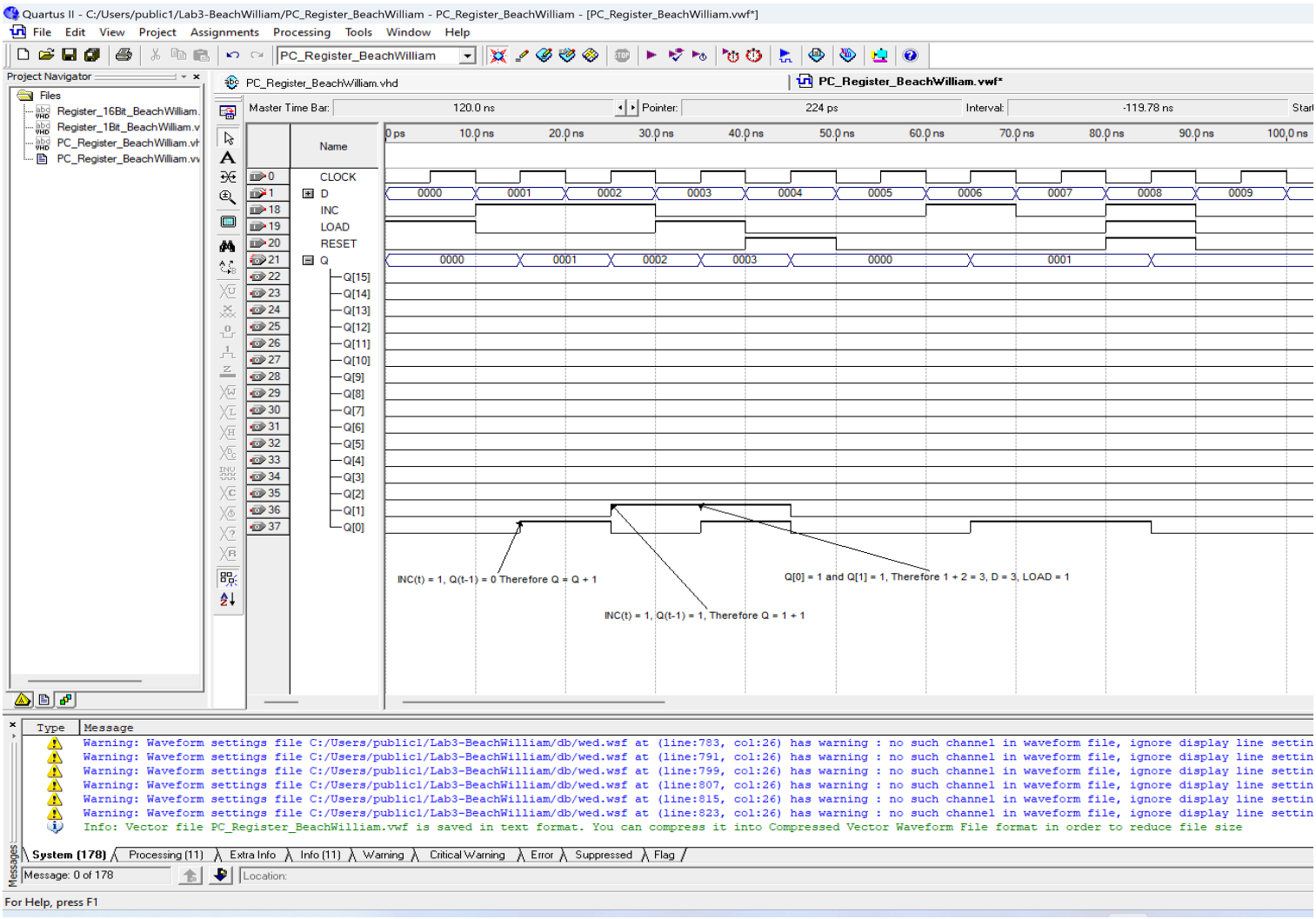
Program Counter Register



Project settings Program Counter Register

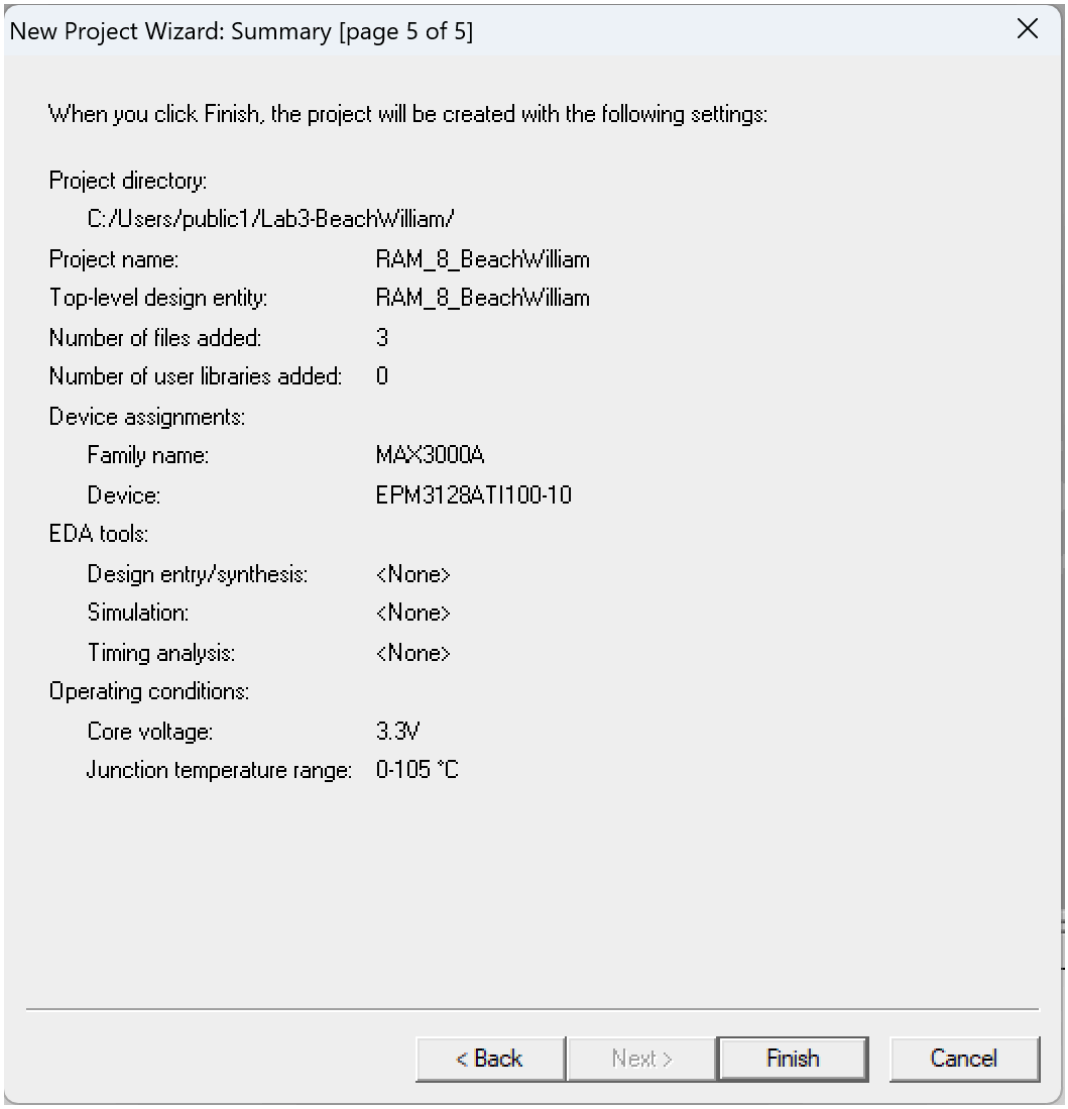


Program Counter Register VHDL

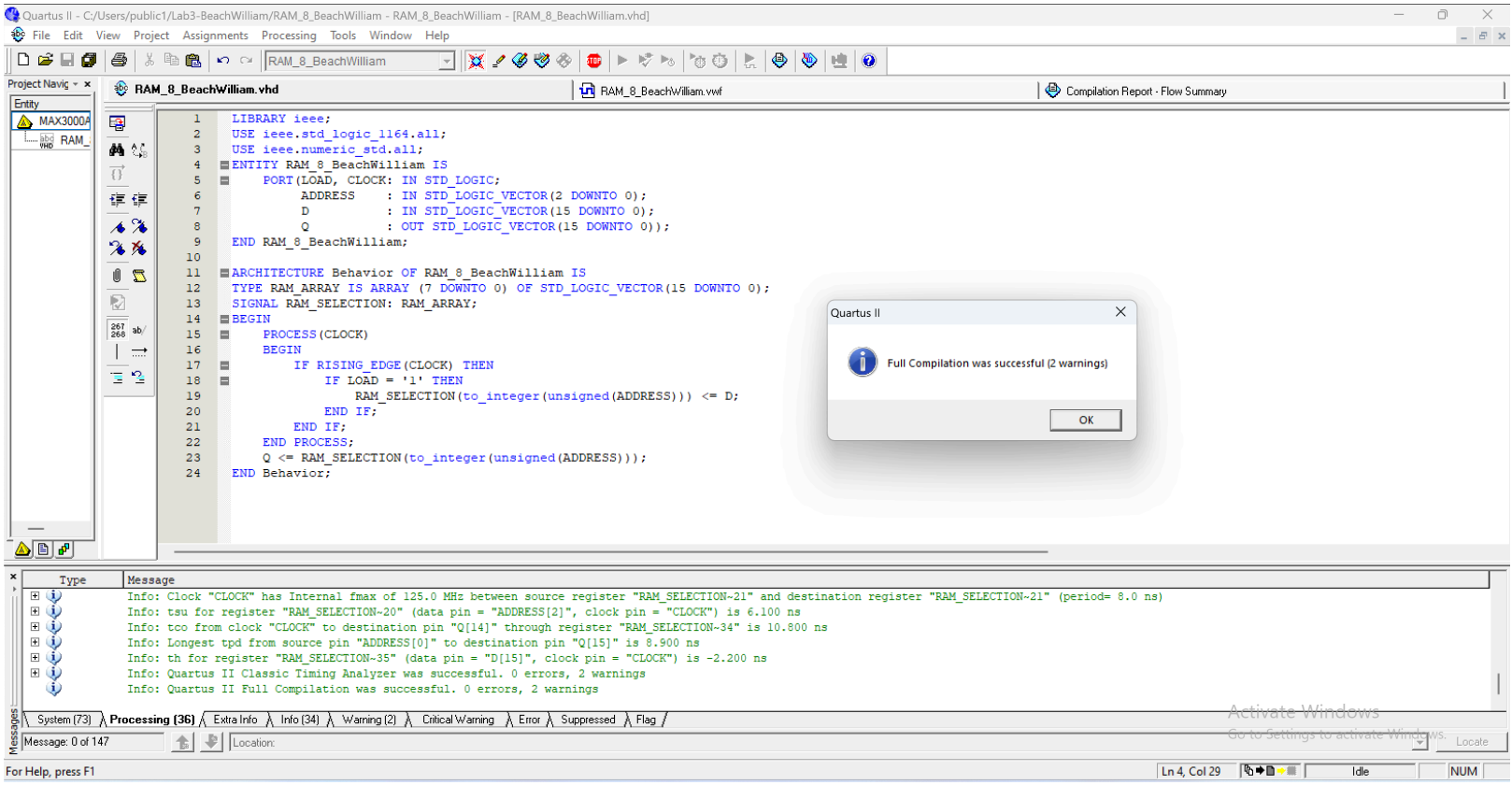


Vector Waveform Timing Diagram PC Register

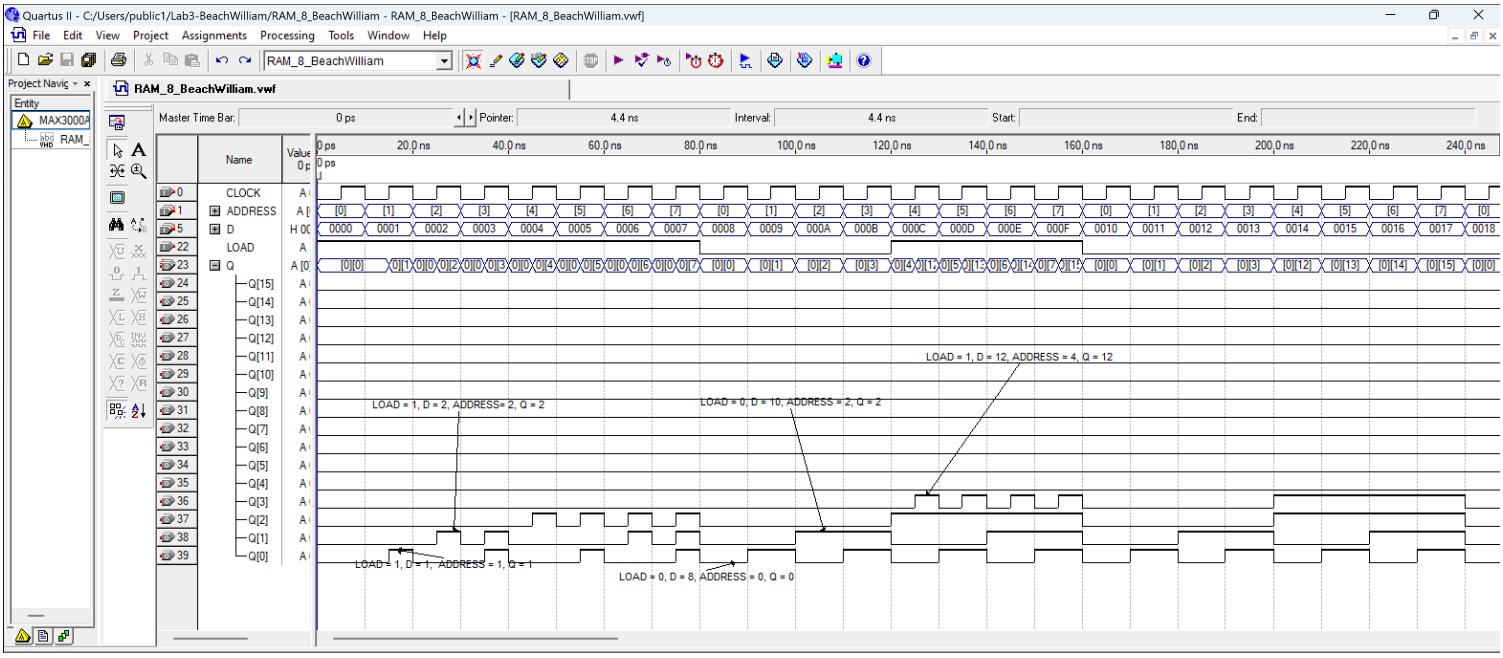
8 Register RAM



Project settings 8 Register RAM



VHDL 8 Register RAM



Vector Waveform Timing Diagram for 8 Register RAM