Lab 1 Report

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10/18/2022
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In lab 1, I've recreated 2 to 1, 4 to 1, 8 to 1 , and 16 to 1 multiplexers. The 2 to 1 multiplexer circuit was initially designed with AND-OR-NOT gates but for speed and cost, I converted all the gates to NAND gates. The following consecutive circuits are all built using the 2 to 1, 4 to 1, and 8 to 1 recycled multiplexer components. This report includes the project settings, vector waveform files, VHDL code, and circuit drawings with only NAND gates (drawn using https://app.diagrams.net/) for each multiplexer.

2 to 1 NAND Multiplexer

Original Equation: F = (X1 && S') + (X2 && S)

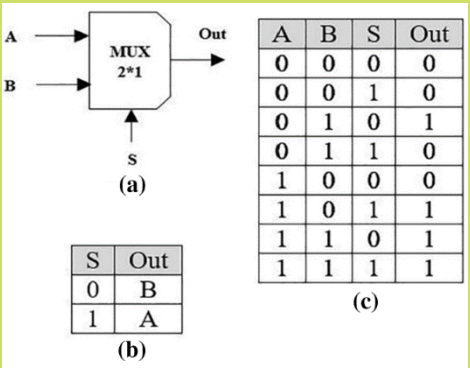
1. Two 2-input AND Gates
2. One 2-input OR Gate
3. One inverter

Converted to only NAND Gates:

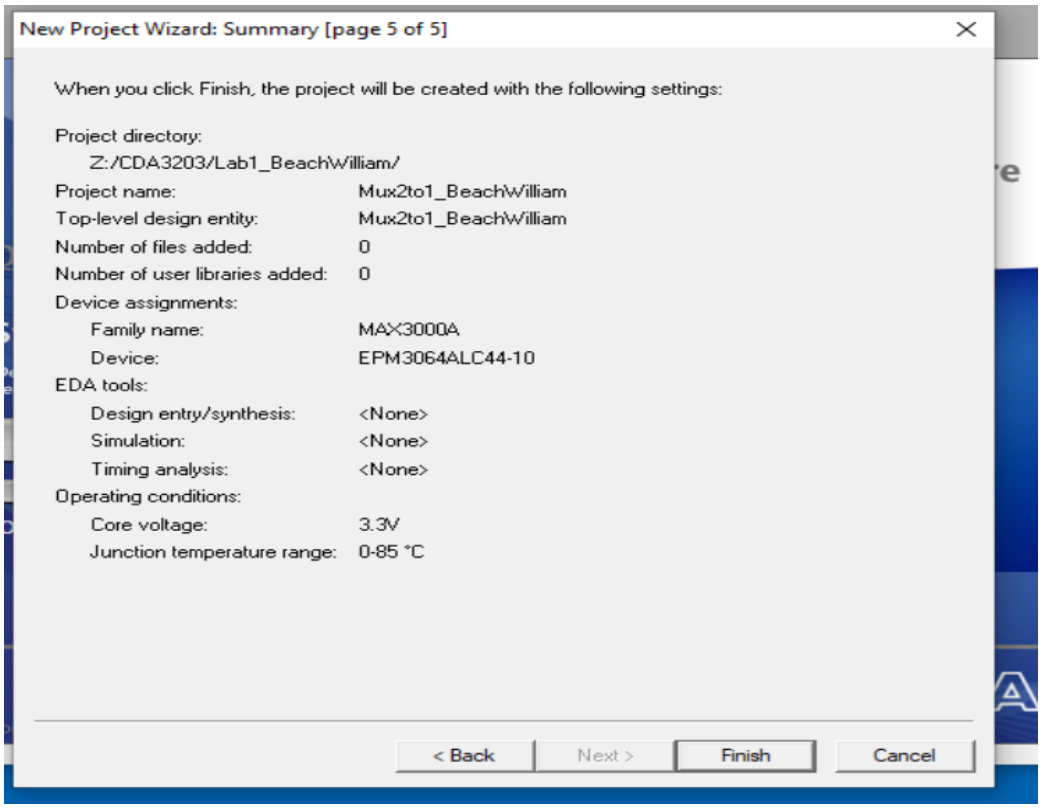
F = ((S NAND S) NAND X1) NAND (S NAND X2)

1. One inverter NAND gate
2. Three double input NAND gates

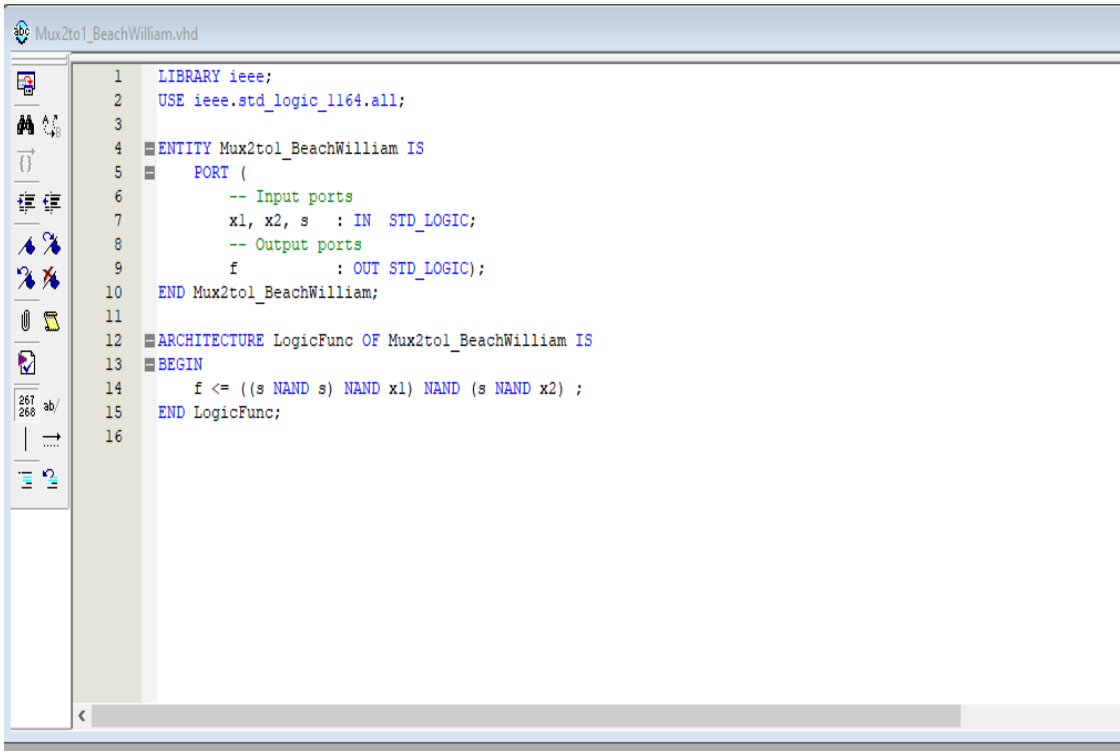
Truth Table for 2 to 1 Multiplexer



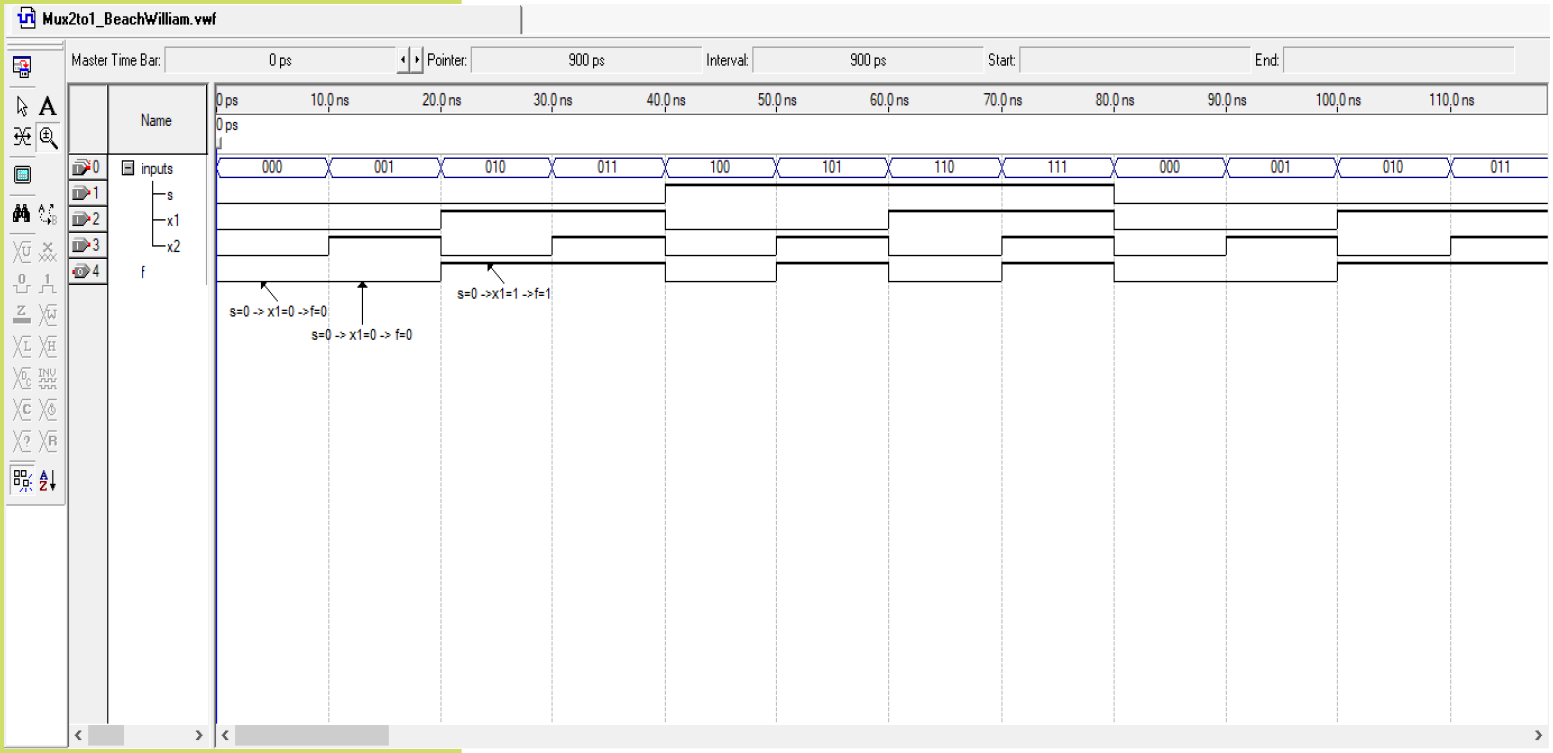
https://www.researchgate.net/figure/a-Multiplexer-schematic-structure-b-truth-table-of-the-mux-based-on-inputs-c-truth_fig14_340612297



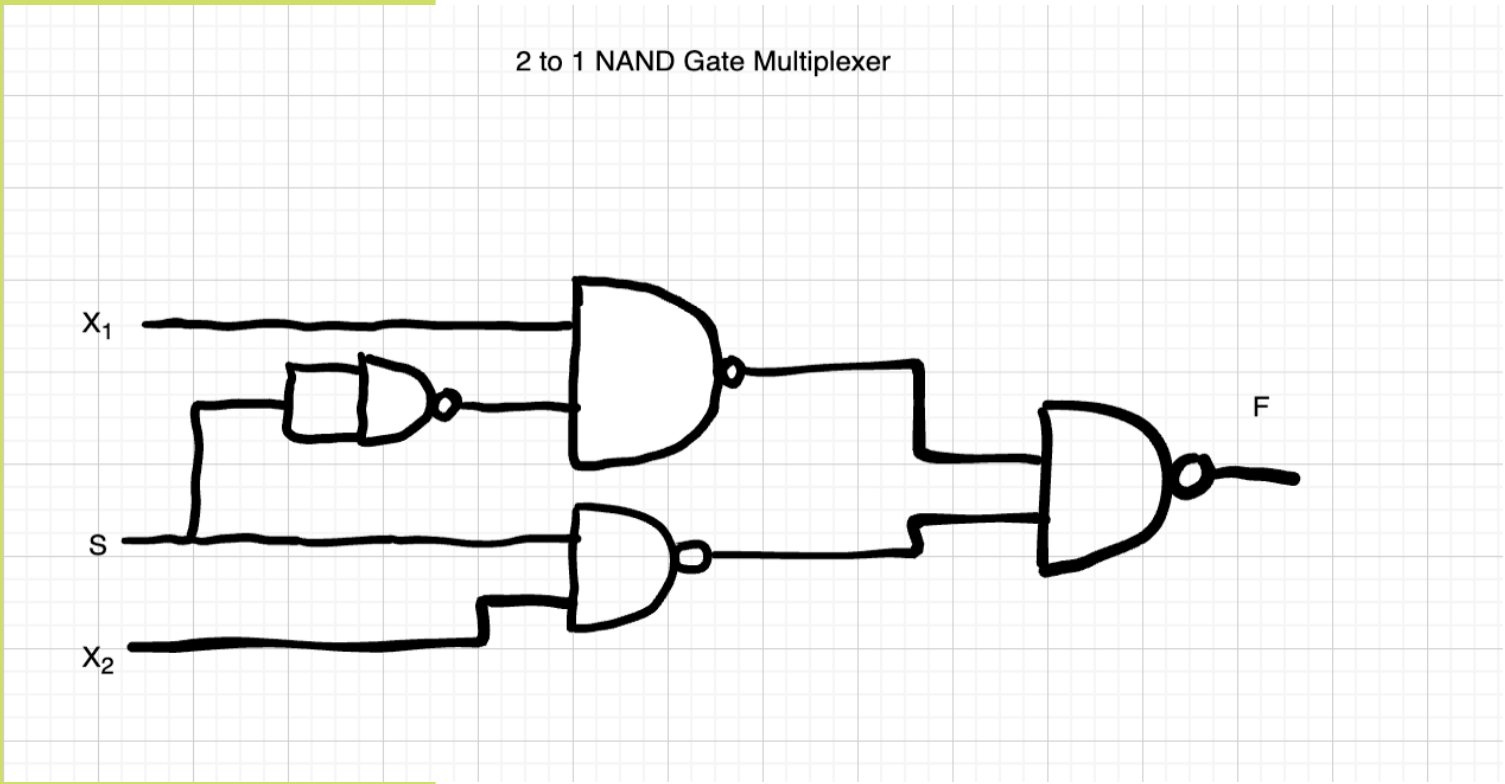
Lab 1 Project settings Mux2to1 in Altera Quartus



VHDL Code for 2 to 1 Multiplexer in Altera Quartus

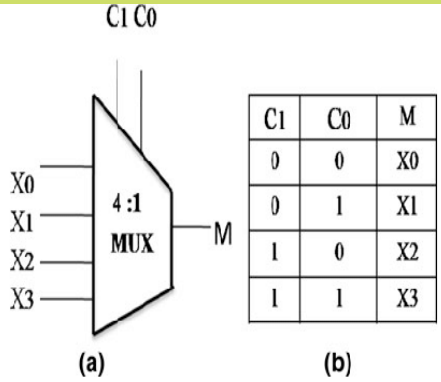


Vector Waveform Timing Diagram for 2 to 1 Multiplexer in Altera Quartus



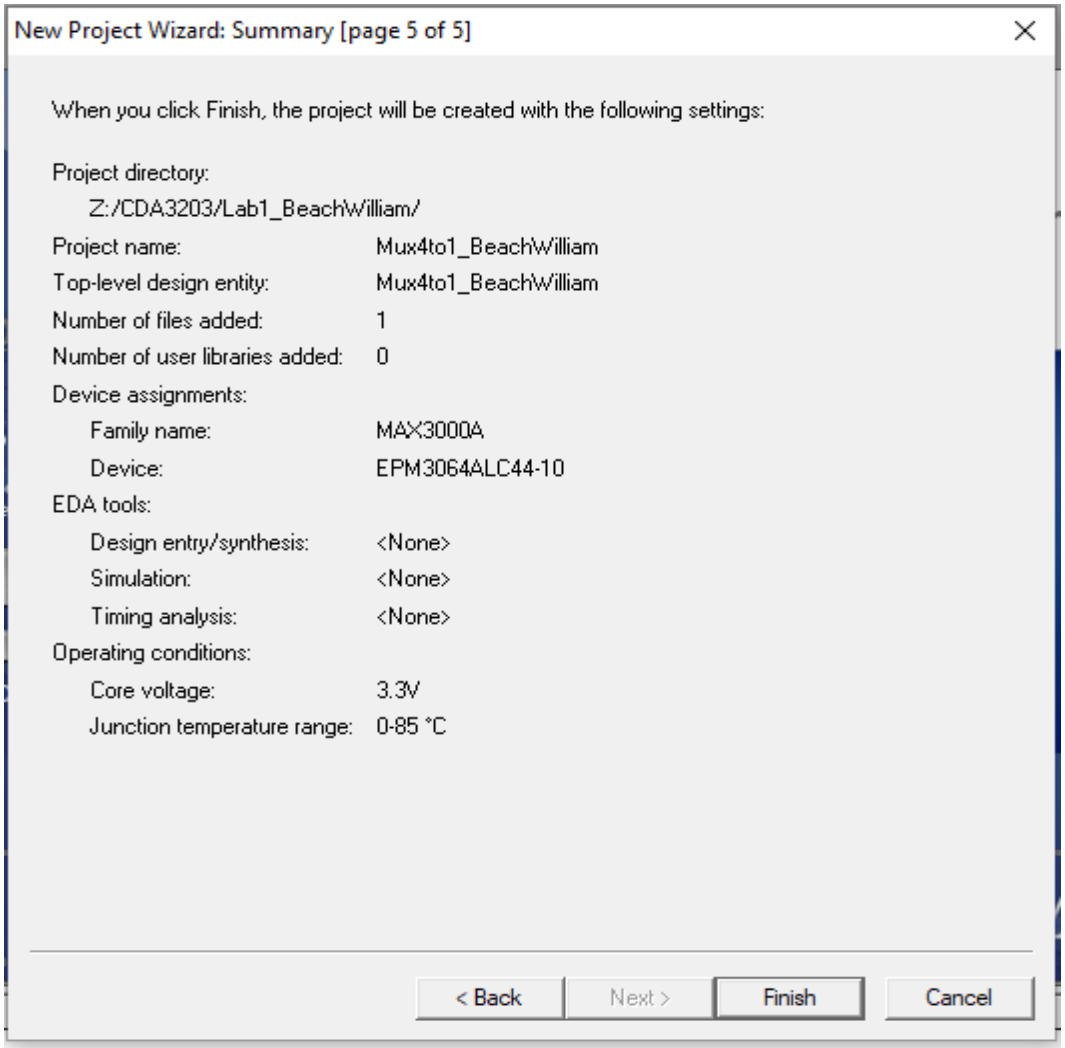
4 to 1 NAND Multiplexer

Truth Table for 2 to 1 Multiplexer

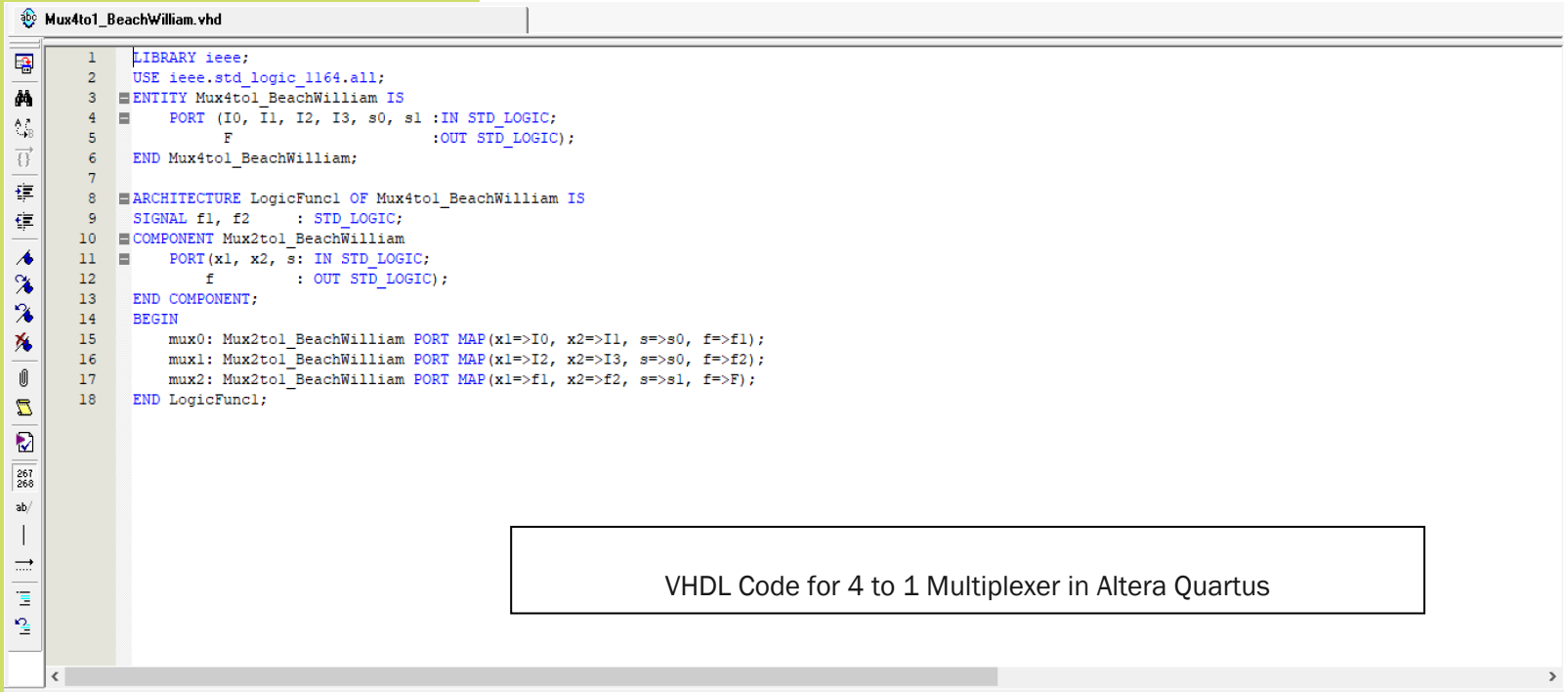


C1	C0	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

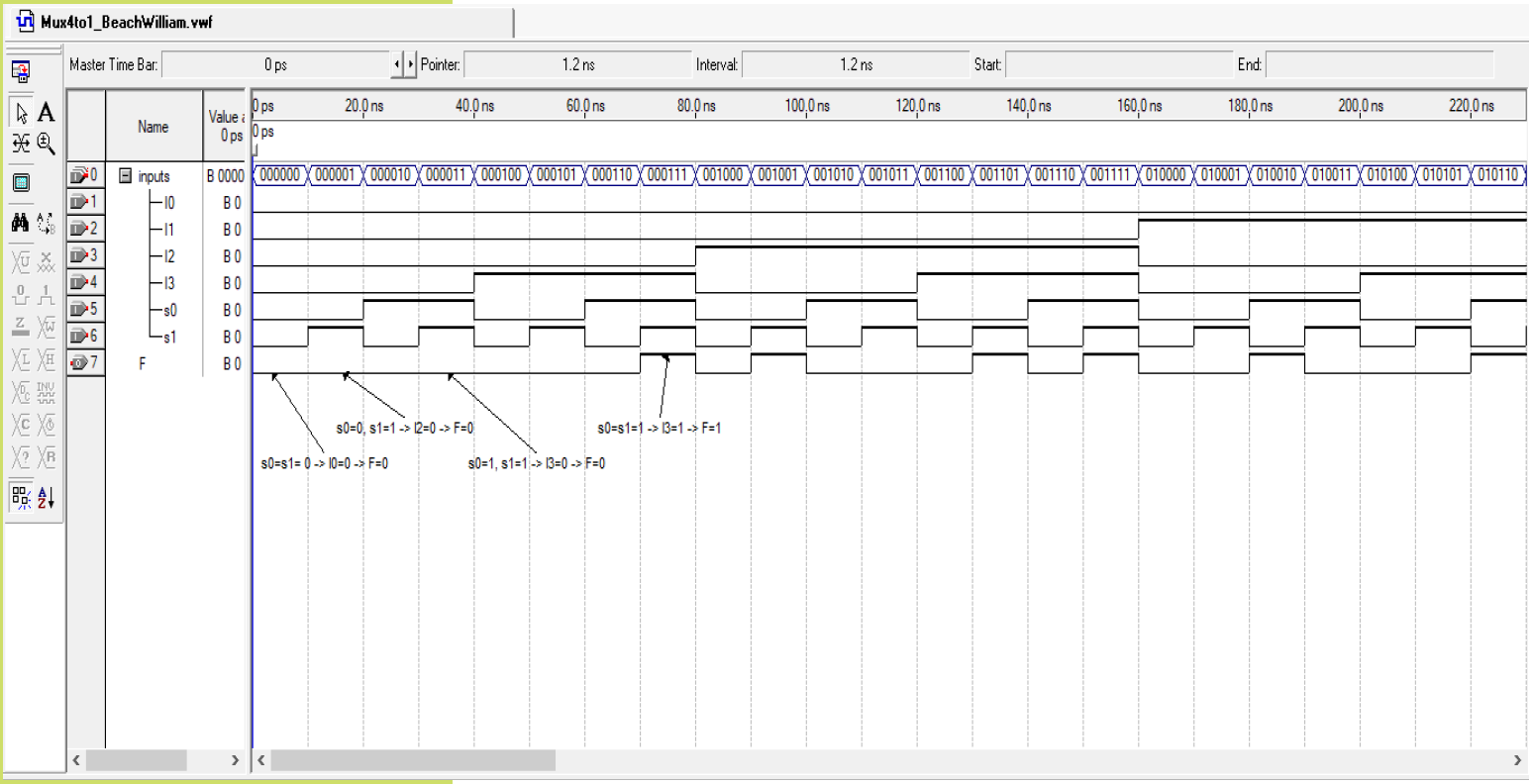
https://www.researchgate.net/figure/MUX-graphical-symbol-a-truth-table-b_fig1_257799438



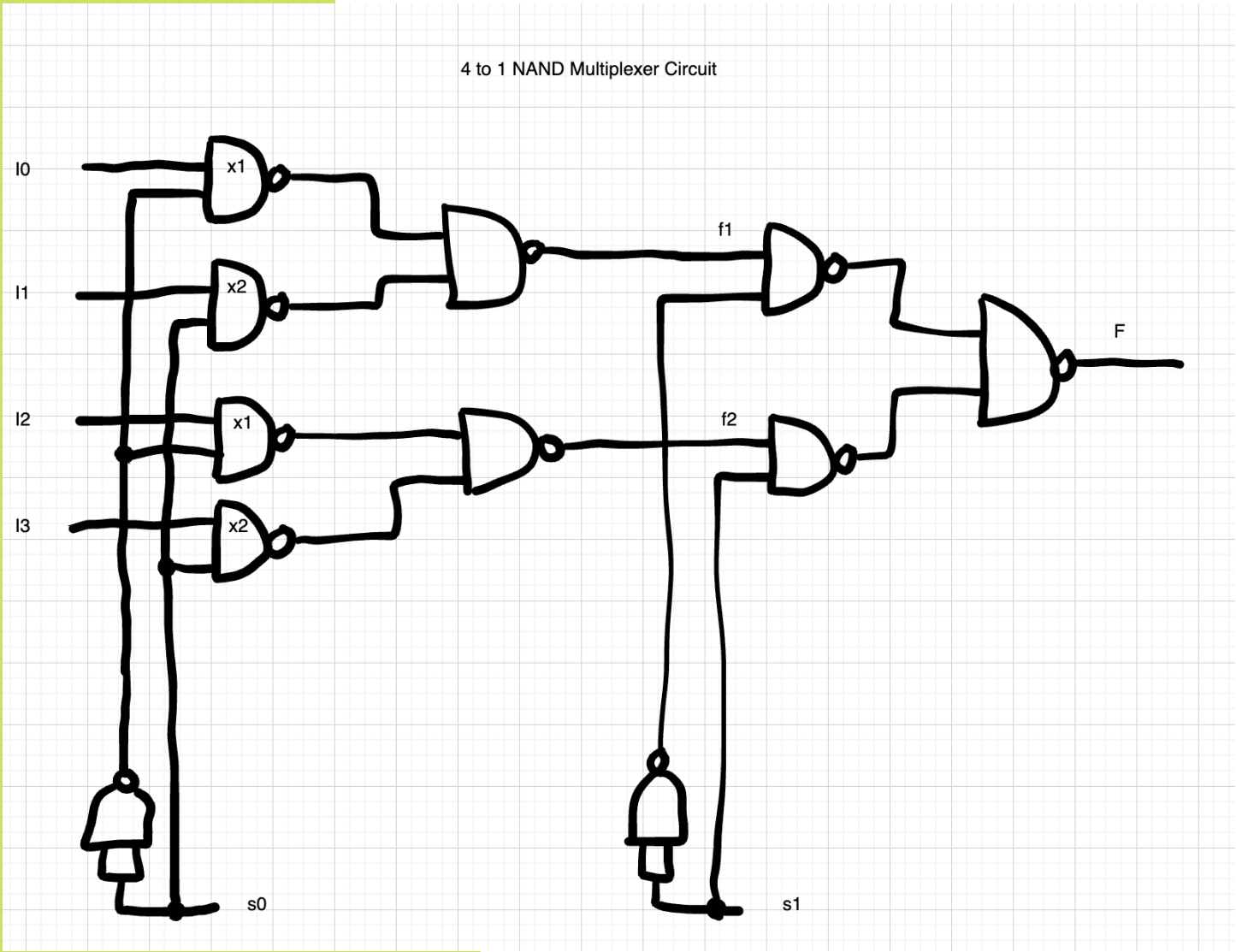
Lab 1 Project settings Mux4to1 in Altera Quartus



VHDL Code for 4 to 1 Multiplexer in Altera Quartus



Vector Waveform Timing Diagram for 4 to 1 Multiplexer in Altera Quartus

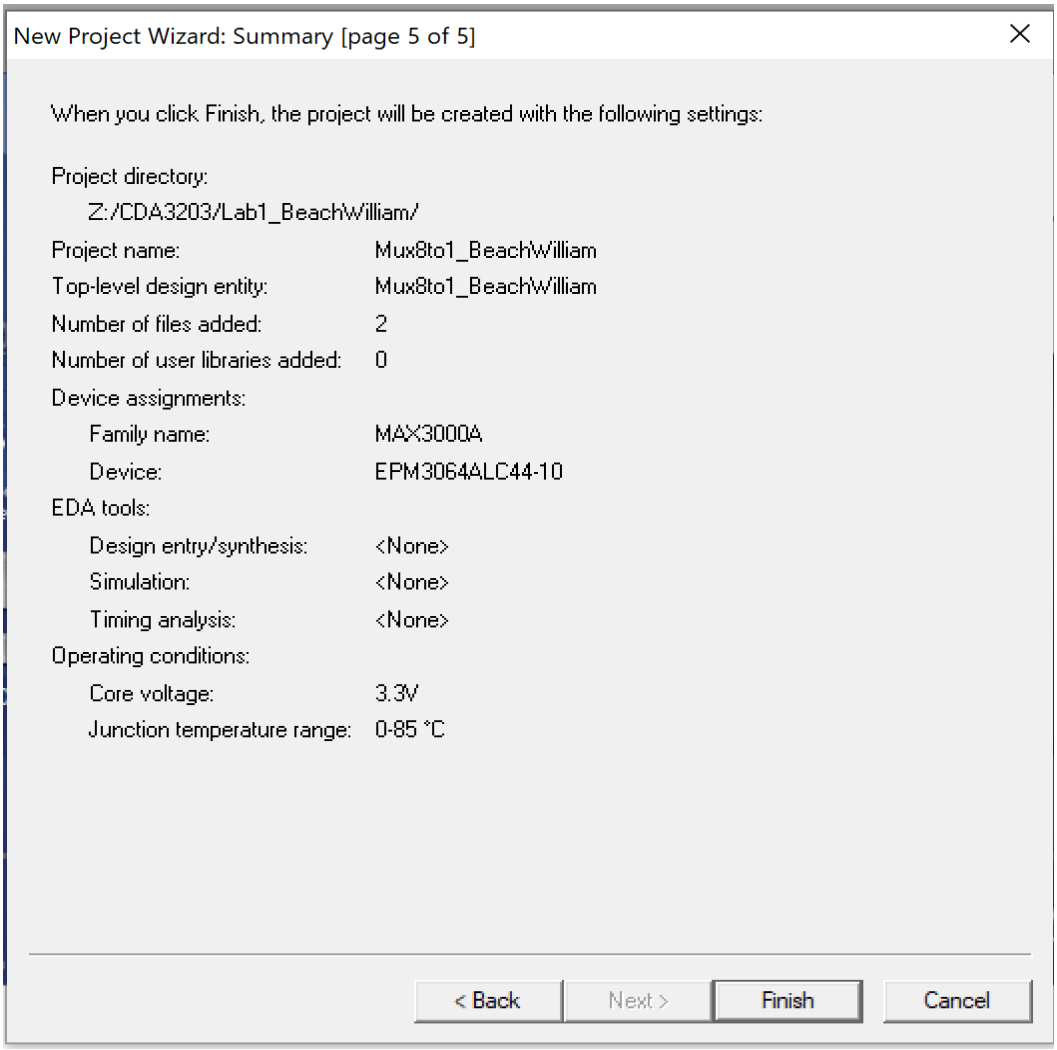


8 to 1 NAND Multiplexer

Truth Table for 8 to 1 Multiplexer

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

https://www.javatpoint.com/multiplexer-digital-electronics

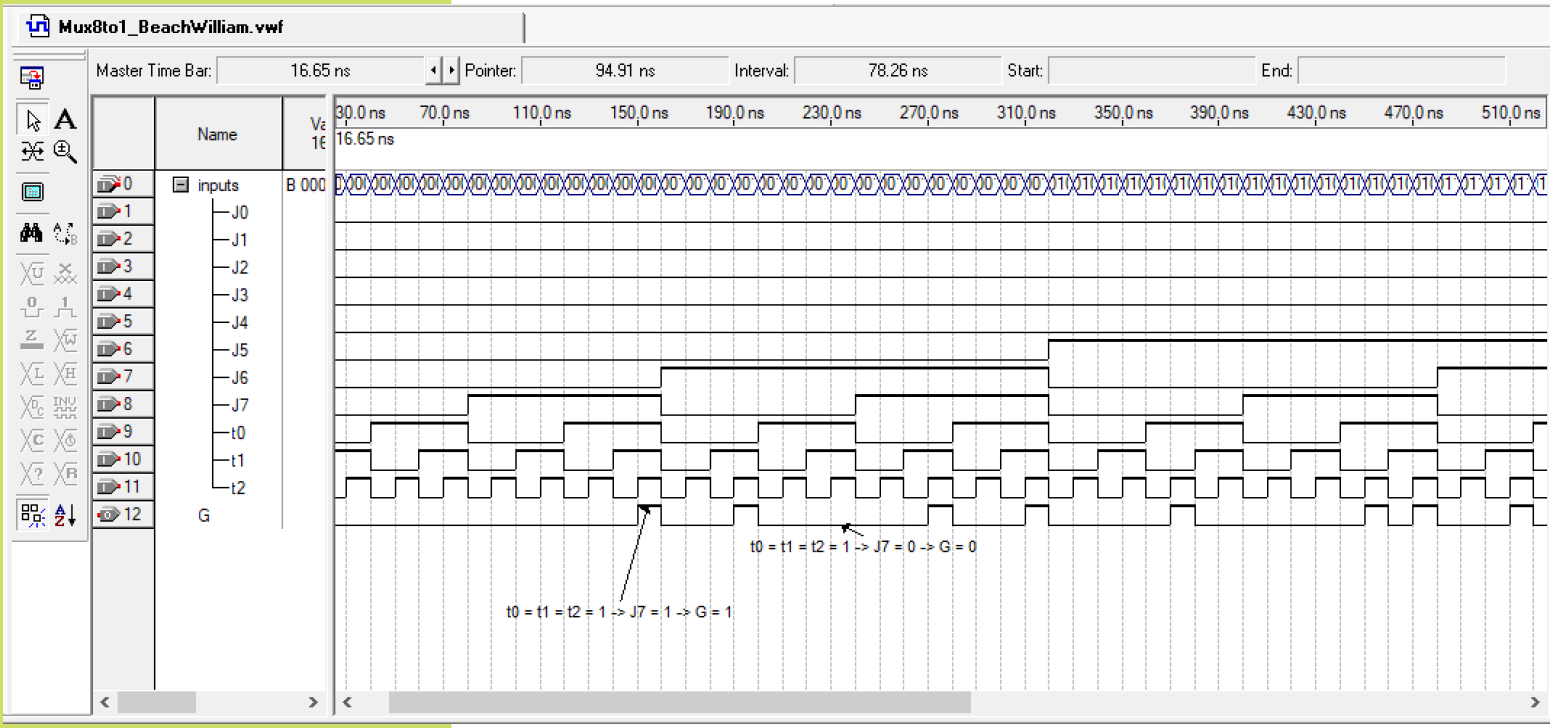


Lab 1 Project settings Mux8to1 in Altera Quartus

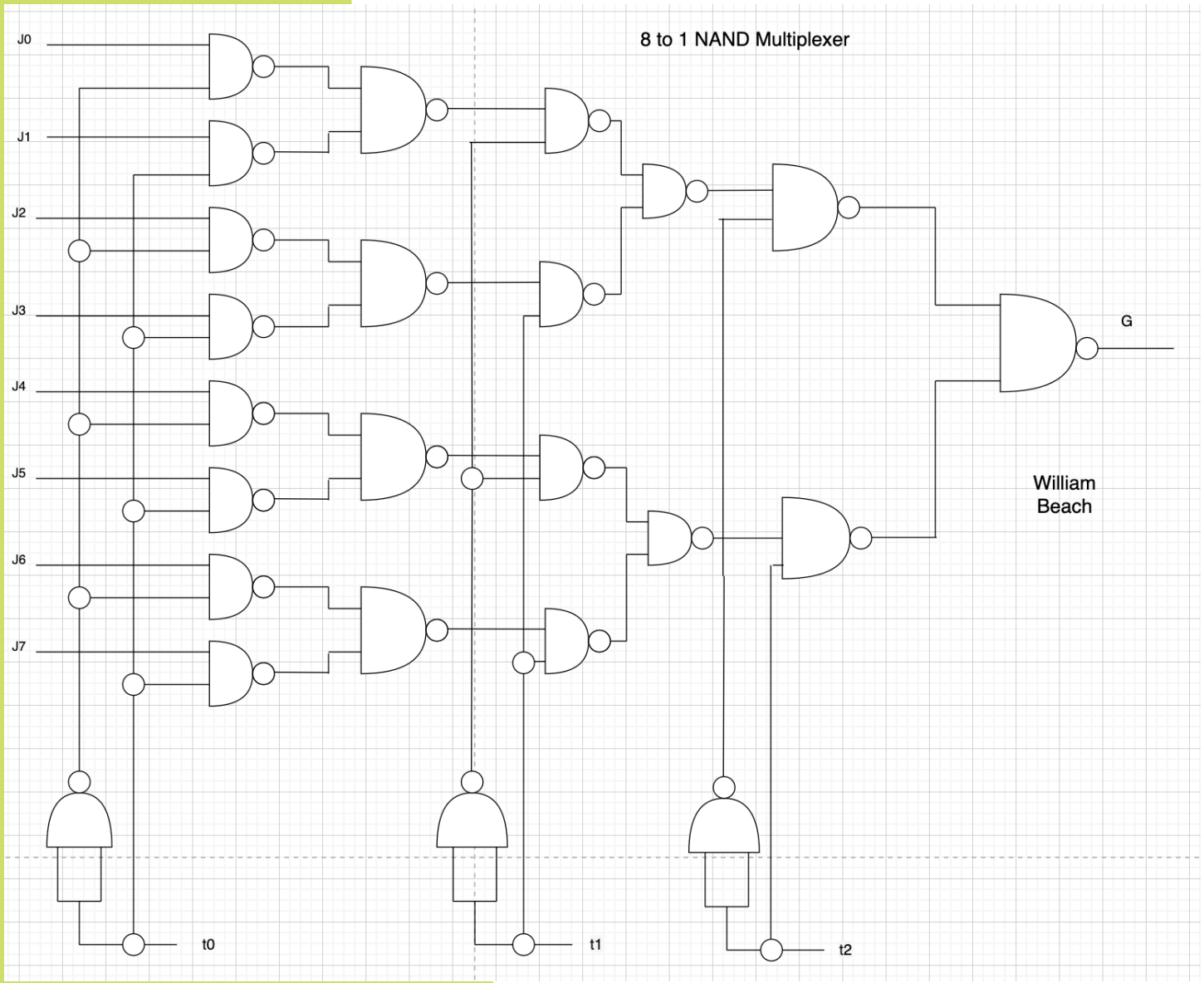
Mux8to1_BeachWilliam.vhd

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ENTITY Mux8tol_BeachWilliam IS
4      PORT (J0, J1, J2, J3, J4, J5, J6, J7, t0, t1, t2 :IN STD_LOGIC;
5            G                                          :OUT STD_LOGIC);
6  END Mux8tol_BeachWilliam;
7
8  ARCHITECTURE LogicFunc2 OF Mux8tol_BeachWilliam IS
9  SIGNAL g1, g2   : STD_LOGIC;
10 COMPONENT Mux4tol_BeachWilliam
11     PORT(I0, I1, I2, I3, s0, s1 : IN STD_LOGIC;
12          F                      : OUT STD_LOGIC);
13 END COMPONENT;
14 COMPONENT Mux2tol_BeachWilliam
15     PORT(x1, x2, s: IN STD_LOGIC;
16          f        : OUT STD_LOGIC);
17 END COMPONENT;
18 BEGIN
19     mux0: Mux4tol_BeachWilliam PORT MAP(I0=>J0, I1=>J1, I2=>J2, I3=>J3, s0=>t0, s1=>t1, F=>g1);
20     mux1: Mux4tol_BeachWilliam PORT MAP(I0=>J4, I1=>J5, I2=>J6, I3=>J7, s0=>t0, s1=>t1, F=>g2);
21     mux2: Mux2tol_BeachWilliam PORT MAP(x1=>g1, x2=>g2, s=>t2, f=>G);
22 END LogicFunc2;
```

VHDL Code for 8 to 1 Multiplexer in Altera Quartus



Vector Waveform Timing Diagram for 8 to 1 Multiplexer in Altera Quartus

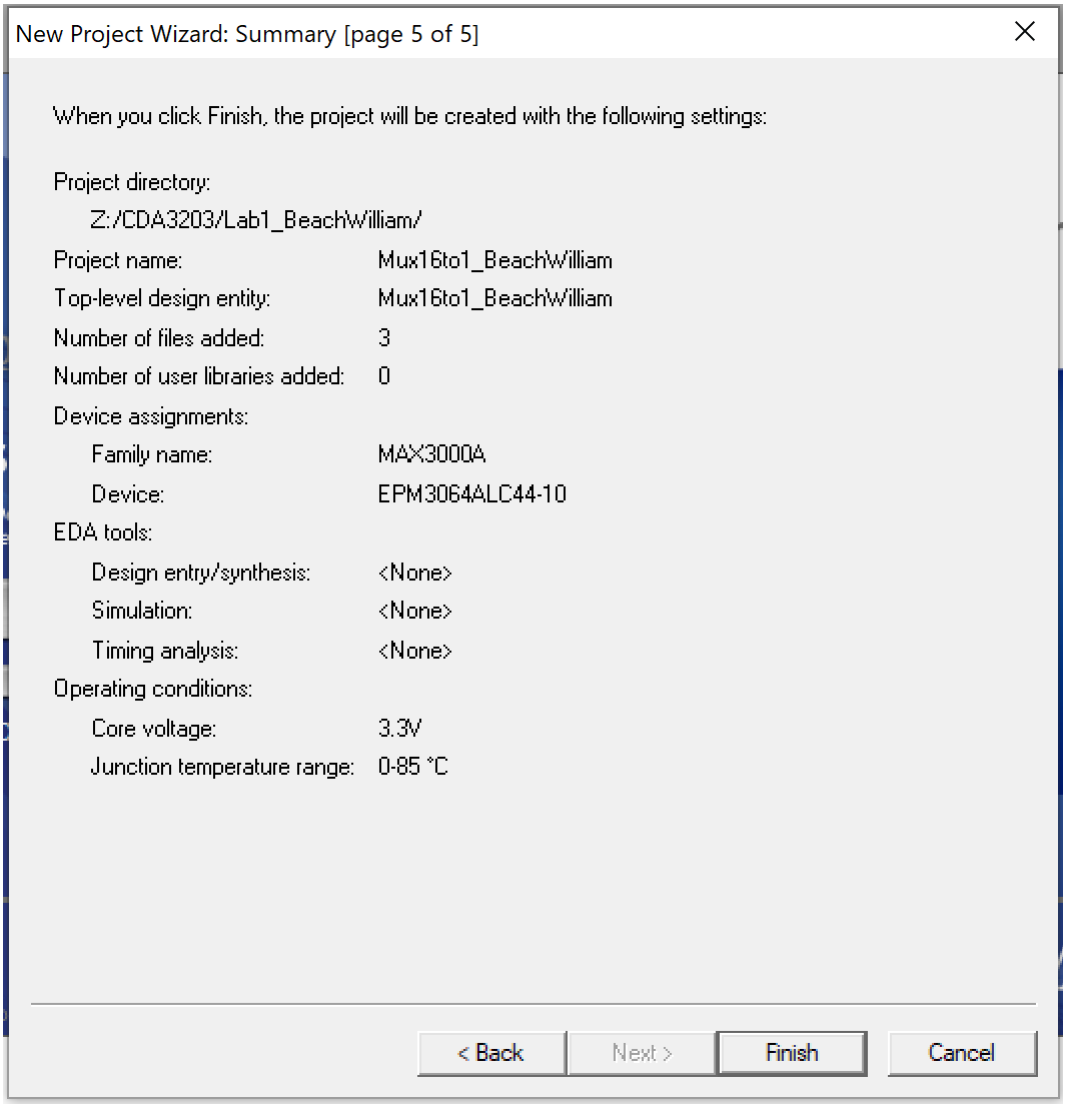


16 to 1 NAND Multiplexer

Truth Table for 8 to 1 Multiplexer

INPUTS				Output
S_0	S_1	S_2	S_3	Y
0	0	0	0	A_0
0	0	0	1	A_1
0	0	1	0	A_2
0	0	1	1	A_3
0	1	0	0	A_4
0	1	0	1	A_5
0	1	1	0	A_6
0	1	1	1	A_7
1	0	0	0	A_8
1	0	0	1	A_9
1	0	1	0	A_{10}
1	0	1	1	A_{11}
1	1	0	0	A_{12}
1	1	0	1	A_{13}
1	1	1	0	A_{14}
1	1	1	1	A_{15}

ttps://www.javatpoint.com/multiplexer-igital-electronics

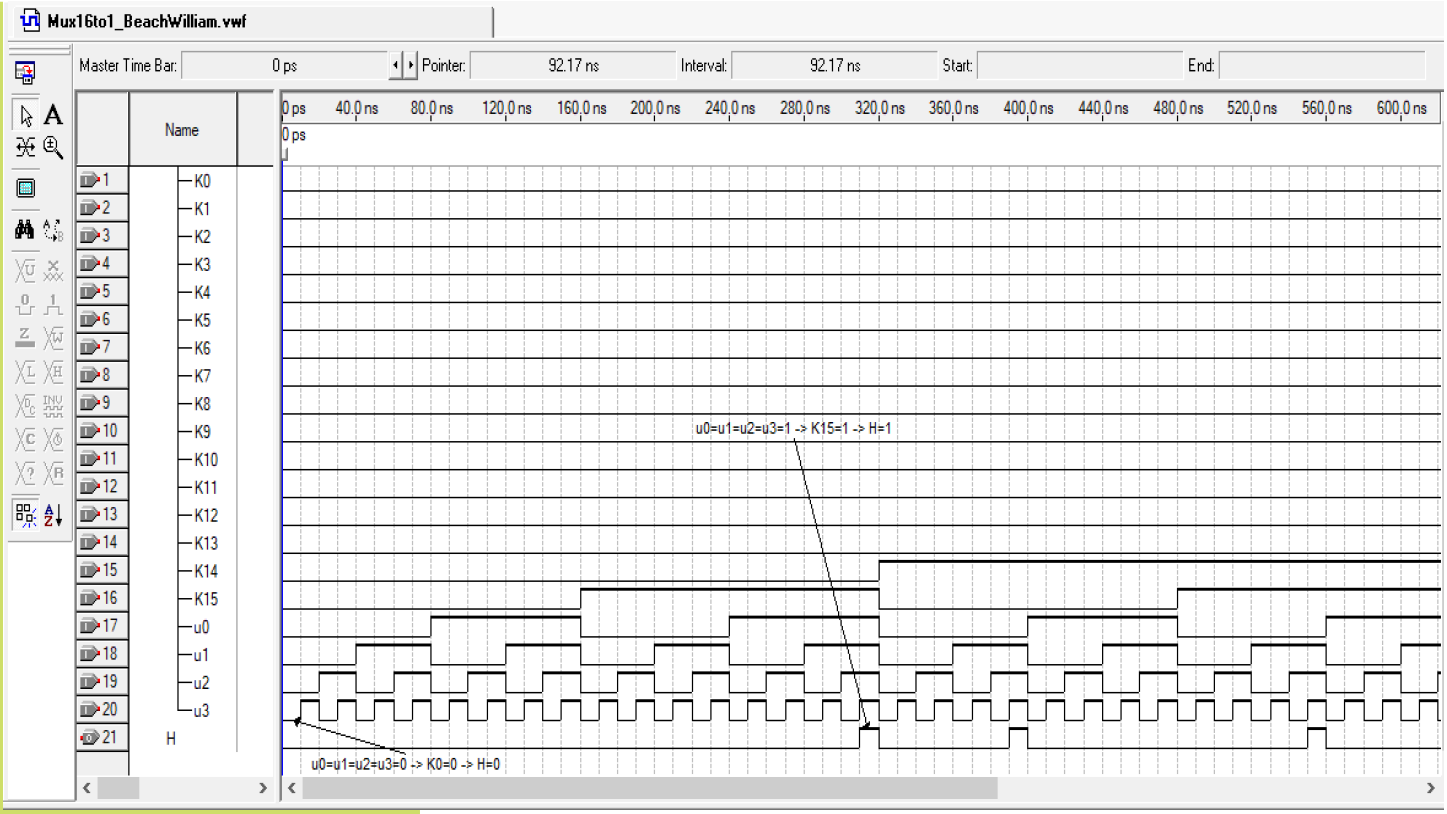


Lab 1 Project settings Mux16to1 in Altera Quartus

Mux16to1_BeachWilliam.vhd

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ENTITY Mux16to1_BeachWilliam IS
4      PORT (K0, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15 : IN STD_LOGIC;
5            u0, u1, u2, u3                                                        : IN STD_LOGIC;
6            H                                                                     : OUT STD_LOGIC);
7  END Mux16to1_BeachWilliam;
8  ARCHITECTURE LogicFunc3 OF Mux16to1_BeachWilliam IS
9  SIGNAL h1, h2 : STD_LOGIC;
10 COMPONENT Mux8to1_BeachWilliam
11     PORT (J0, J1, J2, J3, J4, J5, J6, J7, t0, t1, t2 :IN STD_LOGIC;
12           G                                          :OUT STD_LOGIC);
13 END COMPONENT;
14 COMPONENT Mux2to1_BeachWilliam
15     PORT(x1, x2, s: IN STD_LOGIC;
16          f        : OUT STD_LOGIC);
17 END COMPONENT;
18 BEGIN
19     mux0: Mux8to1_BeachWilliam PORT MAP(J0=>K0, J1=>K1, J2=>K2, J3=>K3, J4=>K4, J5=>K5, J6=>K6, J7=>K7,
20     t0=>u0, t1=>u1, t2=>u2, G=>h1);
21     mux1: Mux8to1_BeachWilliam PORT MAP(J0=>K8, J1=>K9, J2=>K10, J3=>K11, J4=>K12, J5=>K13, J6=>K14, J7=>K15,
22     t0=>u0, t1=>u1, t2=>u2, G=>h2);
23     mux2: Mux2to1_BeachWilliam PORT MAP(x1=>h1, x2=>h2, s=>u3, f=>H);
24 END LogicFunc3;
```

VHDL Code for 16 to 1 Multiplexer in Altera Quartus



Vector Waveform Timing Diagram for 16 to 1 Multiplexer in Altera Quartus