ID1206 HT24
Review Lab for Module #3
Deadline: 2024-12-06

1. Virtual memory simulator

The task to accomplish in this lab is to design, implement, and test a virtual memory simulator that implements demand paging. The simulator must model the following components:

1. Virtual memory comprising N_{page} pages of size C_{page}
2. Physical memory comprising N_{frame} frames of size C_{frame}
3. Page table comprising N_{TLB} entries
4. List of free frames
5. TLB with N_{TLB} entries

For evaluating the simulator use the following parameters:

Parameter	Value
Number of pages N_{page}	256
Page size C_{page}	256 B
Number of frames N_{frame}	256
Page size C_{page}	256 B
Number of TLB entries N_{TLB}	16

Tasks
For completing this assignments, you have to do the following:

1. Implement a simulator complying to the requirements and parameters given in this document.
2. Compare the output with the provided reference data and include a copy in the output in your report.
3. Document the implemented TLB.
4. Document the following statistics:
   - Number of addresses
   - Number of page faults
   - Number of TLB hits

- Number of TLB misses

5. Check how the TLB hit and miss rate changes with the TLB size.

Address translation

Using a TLB and page table, your program will translate virtual addresses to physical addresses. First, the page number is extracted from the virtual address, and the TLB is consulted. In the case of a TLB-hit, the frame number is obtained from the TLB. In the case of a TLB-miss, the page table must be consulted. In the latter case, the frame number is obtained from the page table, or a page fault occurs.

Implement the mapping such that the first page, which is used, uses frame '0', the next page uses frame '1', and so on.

TLB

You are free to select an algorithm that decides about the entry to evict once the TLB is full, e.g. FIFO or LRU.

System initialisation

The following steps are required to initialise the system:

- Setup list of free frames
- Initialise the page table

Input and reference data

The following files are provided:

- `addresses.txt`: Input list of virtual addresses (use only the 16 least significant bits)
- `correct.txt`: Reference data

Hints

- Start without a TLB. For a functional correct virtual memory system only a page table is needed, the TLB is only to improve performance.
- Since the number of pages and frames is identical, you may initially drop the list of free frames and simply use a counter whenever a page fault occurs and a new frame needs to be used.