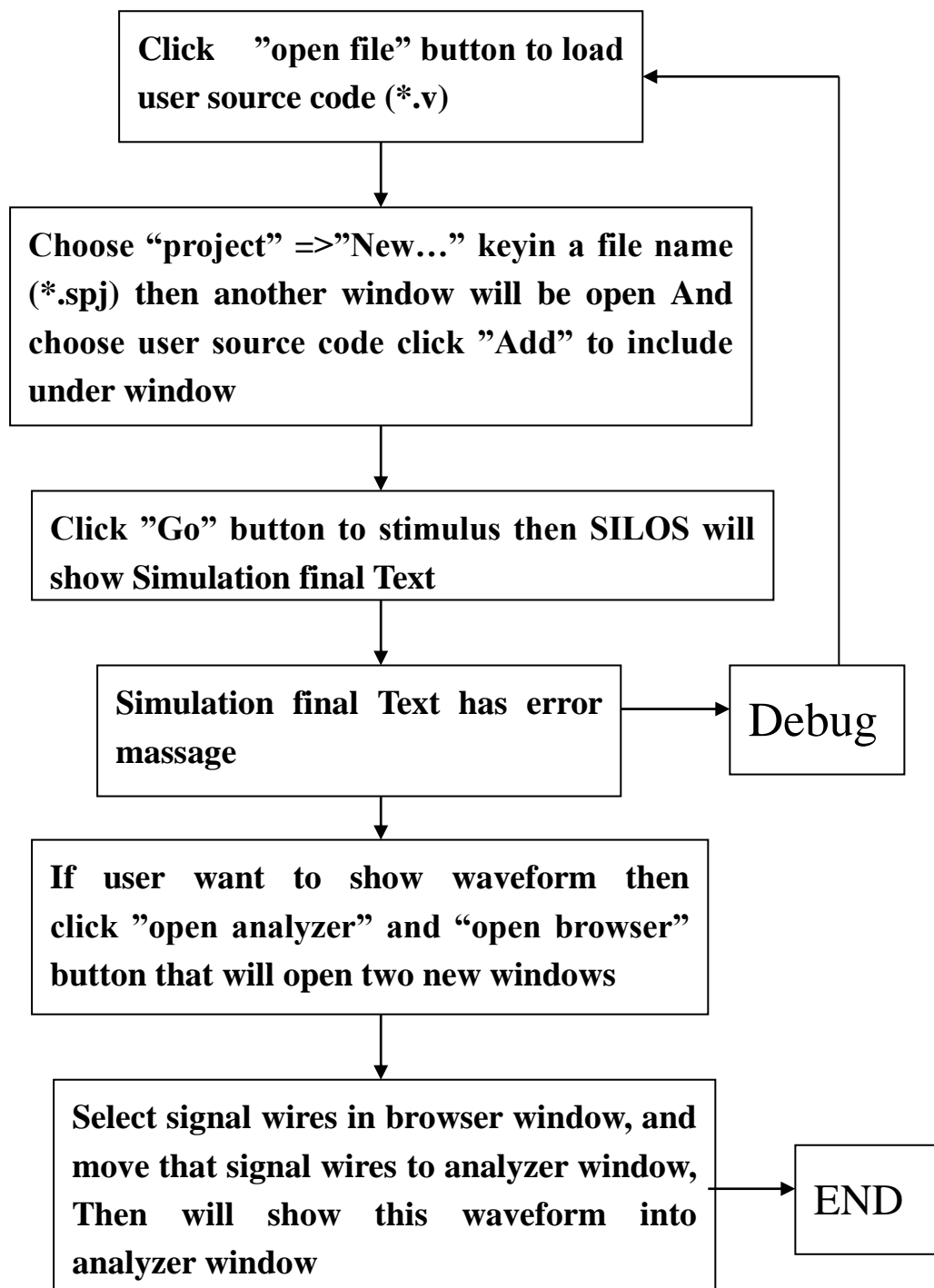


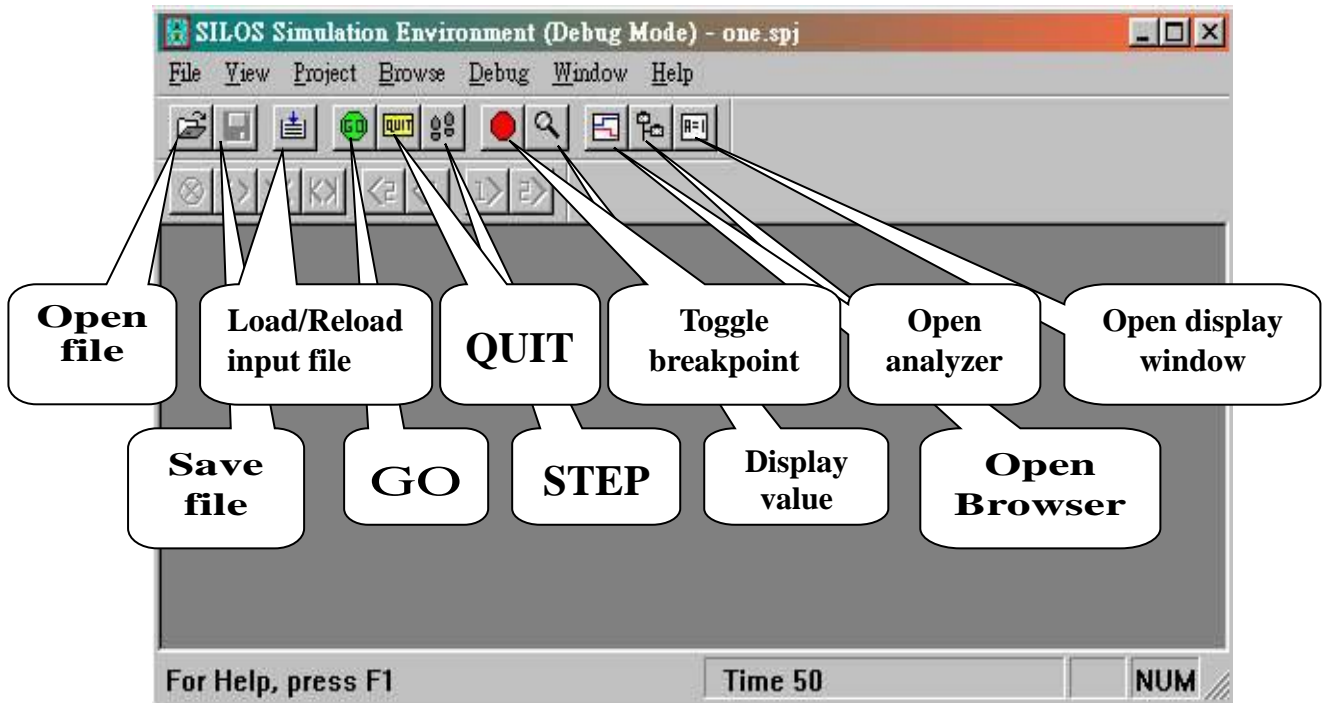
Chapter 1 Verilog Stimulate Environment

1.1 PC Verilog Stimulate Environment

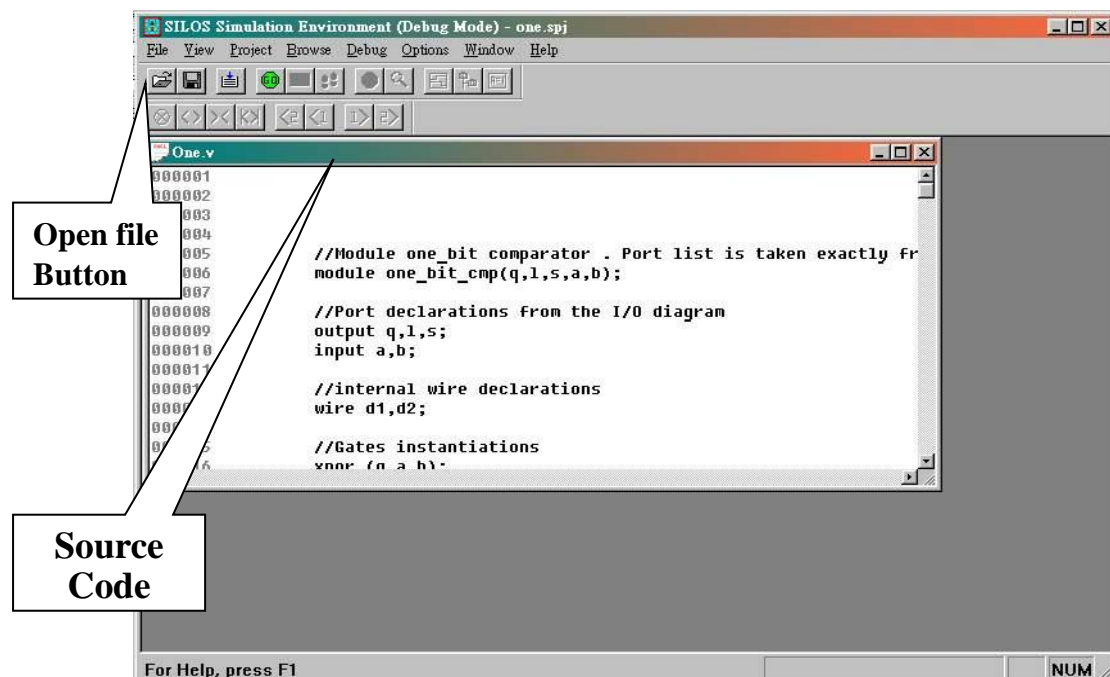
1.1.1 SILOS Environment



Basic Window



Step 1. Click open file button to open source file

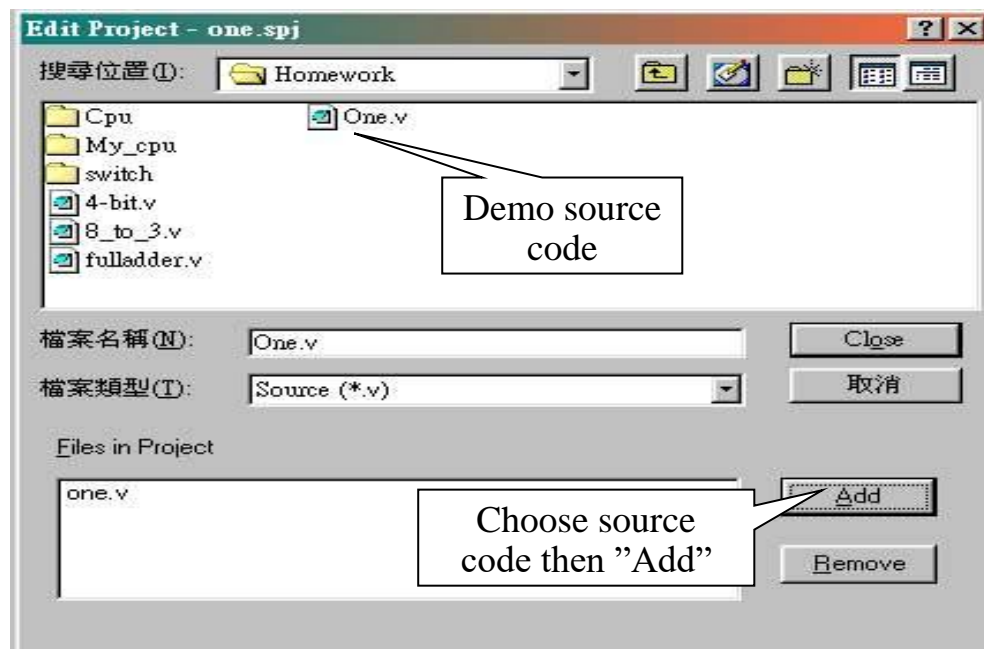


Step2. Choose project => New

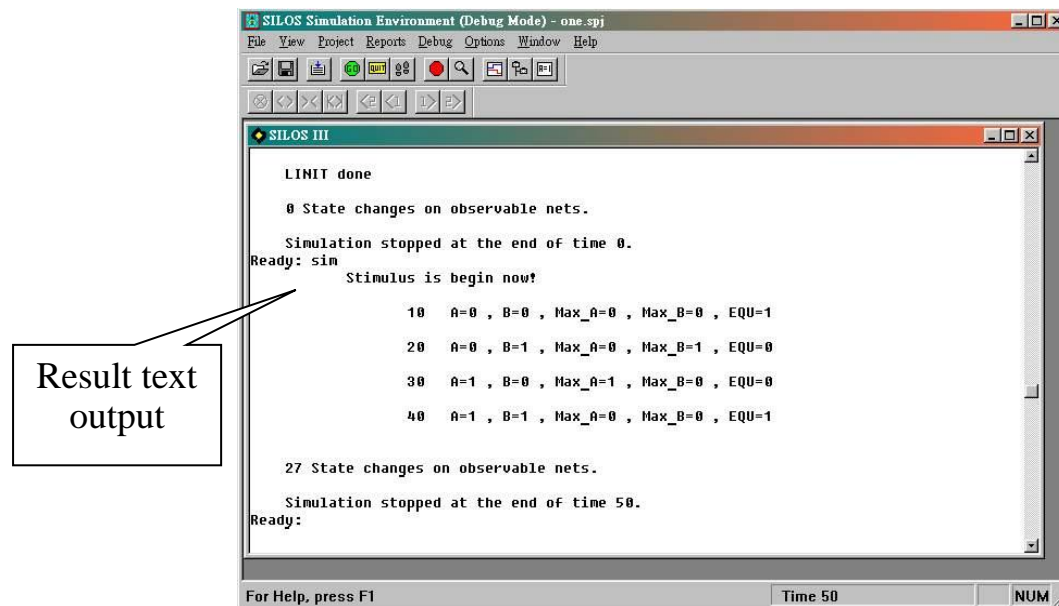
Step3 . keyin file name (*.spj)



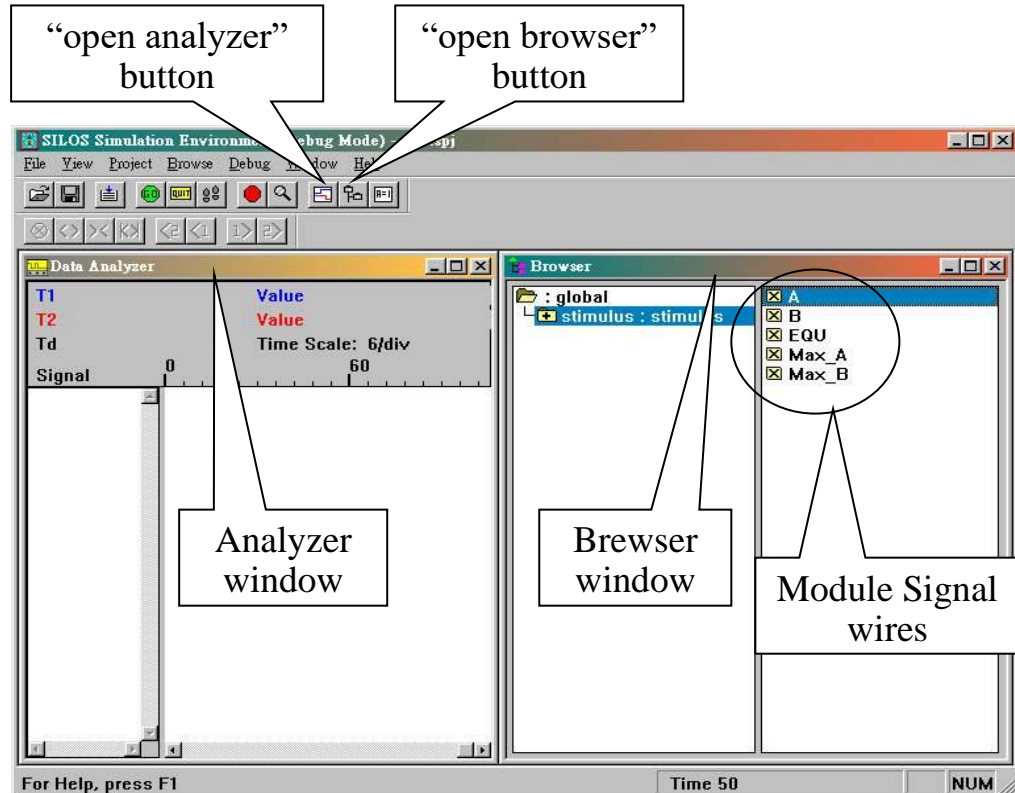
Step4. Choose source code file and Add to under window



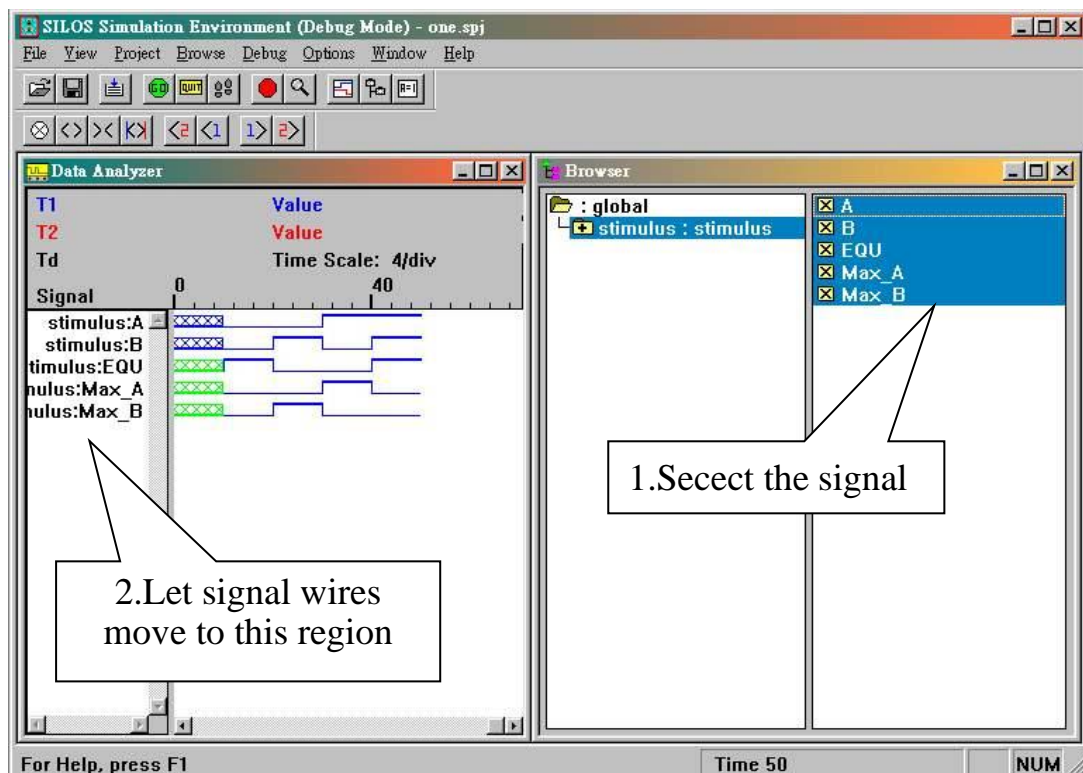
Step 5. Click ”go button if user code is Zero error then will show stimulus final Text



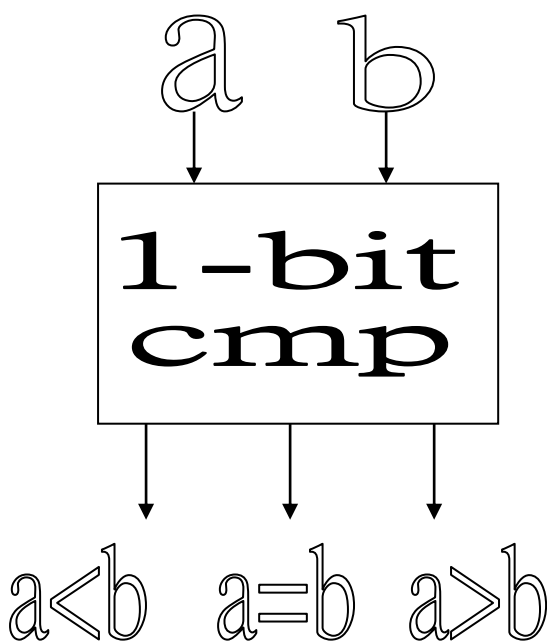
Step 6. Click “open analyzer “ and “open browser” button



Step 7. Select signal wires and that move to analyzer window
“Signal” region, then waveform will display



Demo source code : 1-bit comparator



```
//Module one_bit comparator .
module one_bit_cmp(q,l,s,a,b);

//Port declarations from the I/O diagram
output q,l,s;
input a,b;

//internal wire declarations
wire d1,d2;

//Gates instantiations
xnor (q,a,b);
and (l,a,d1);
not (d1,b);
and (s,b,d2);
not (d2,a);
endmodule
```

```

//Define the stimulus module
module stimulus;

//Declare variable to be connected to inputs
reg A,B;

//Declarate output wire
wire EQU,Max_B,Max_A;

//Instantiate the one-bbit cpmparator
one_bit_cmp  one(EQU,Max_A,Max_B,A,B);

//Display output
initial
begin
$monitor($time," A=%b , B=%b , Max_A=%b , Max_B=%b , EQU=%b \n",
A,B,Max_A,Max_B,EQU);
end

//Stimulus input
initial
begin

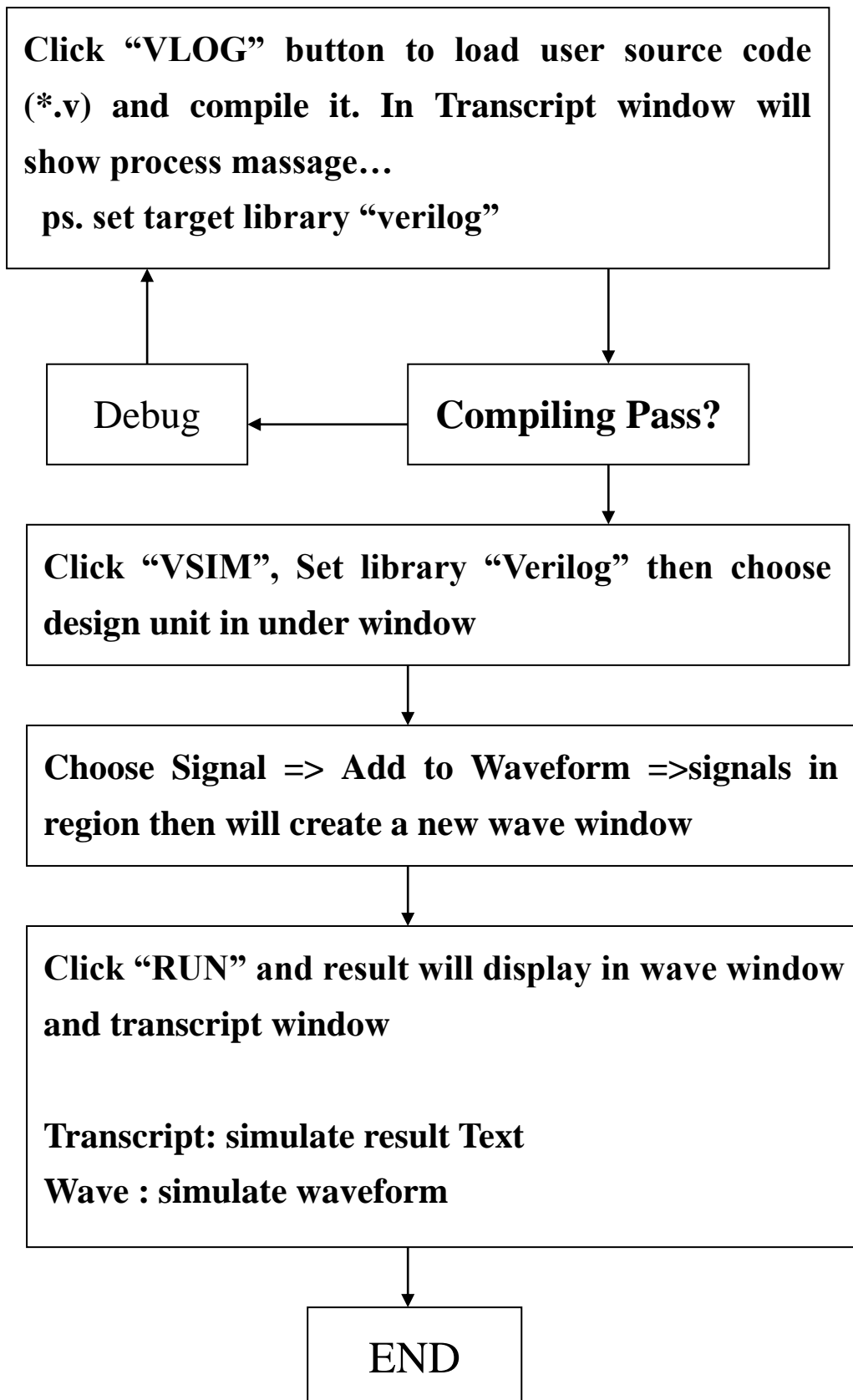
#1  $display("Stimulus is begin now!\n");
#9  A=1'b0 ; B=1'b0 ;
#10 A=1'b0 ; B=1'b1 ;
#10 A=1'b1 ; B=1'b0 ;
#10 A=1'b1 ; B=1'b1 ;
#10 $finish;

end

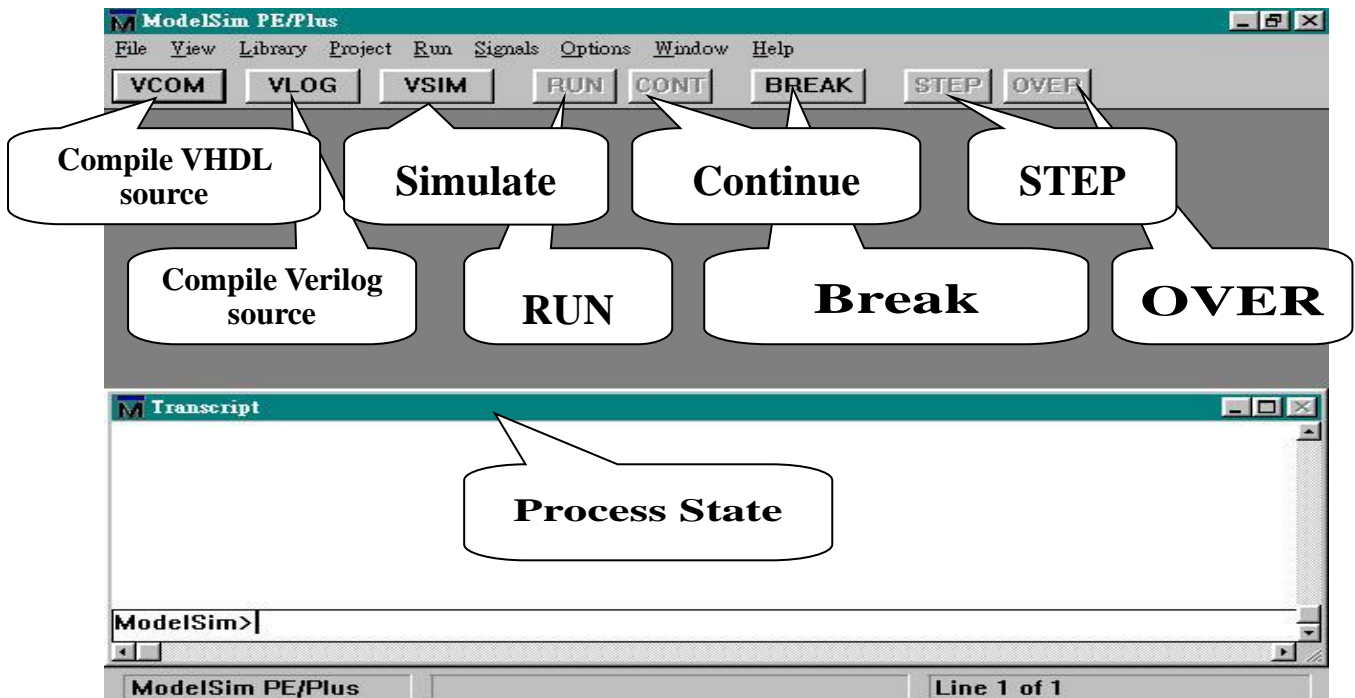
endmodule

```

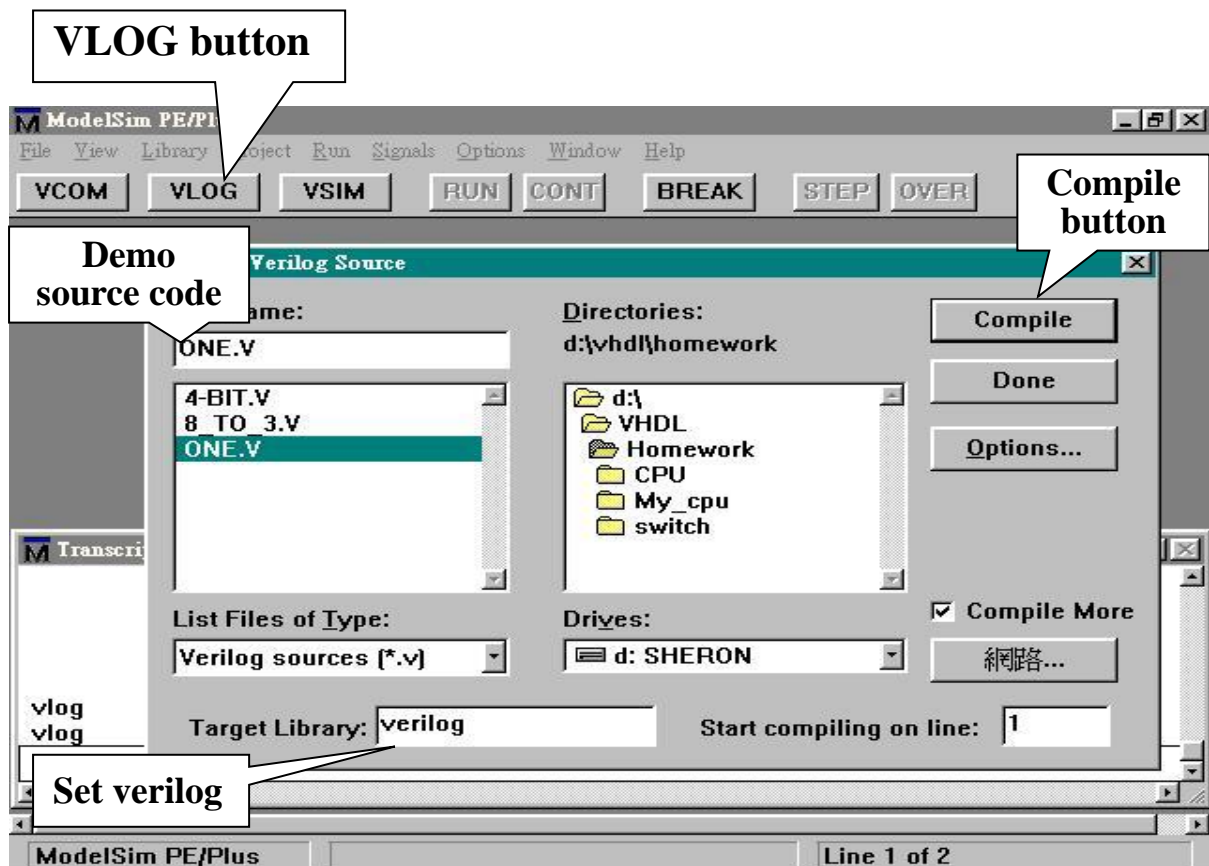
1.1.2 ModelSim PE/Plus Environment



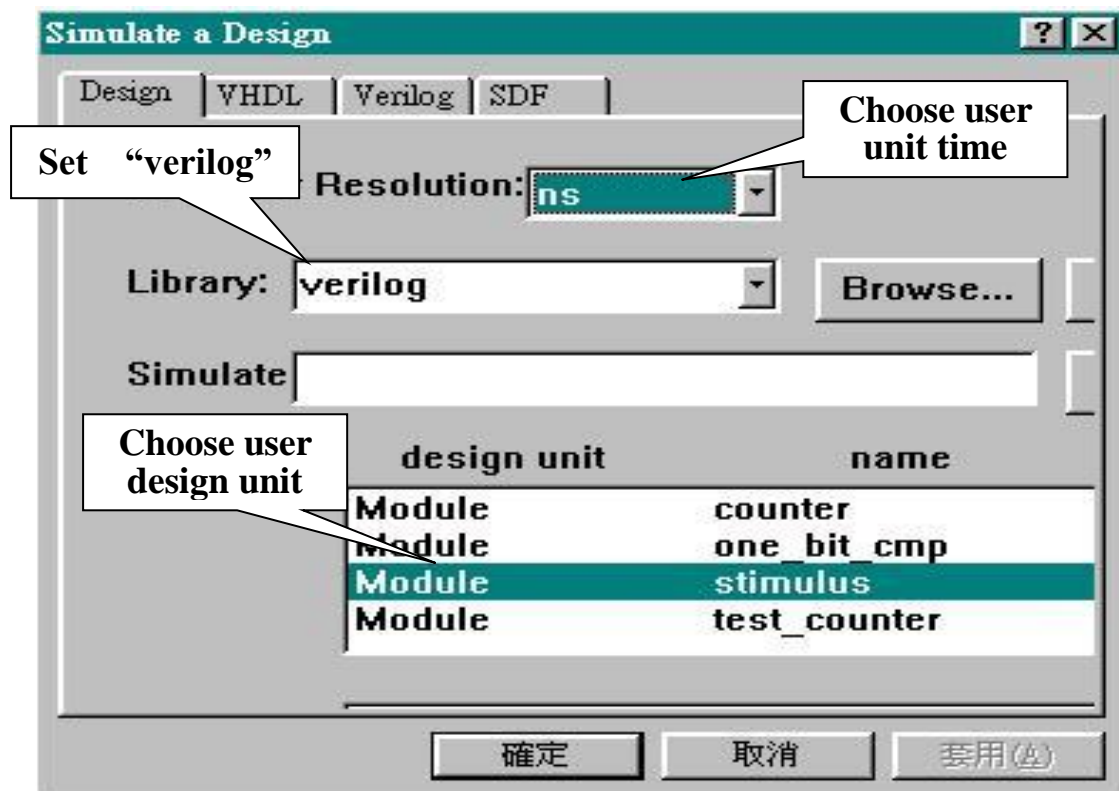
Basic Window



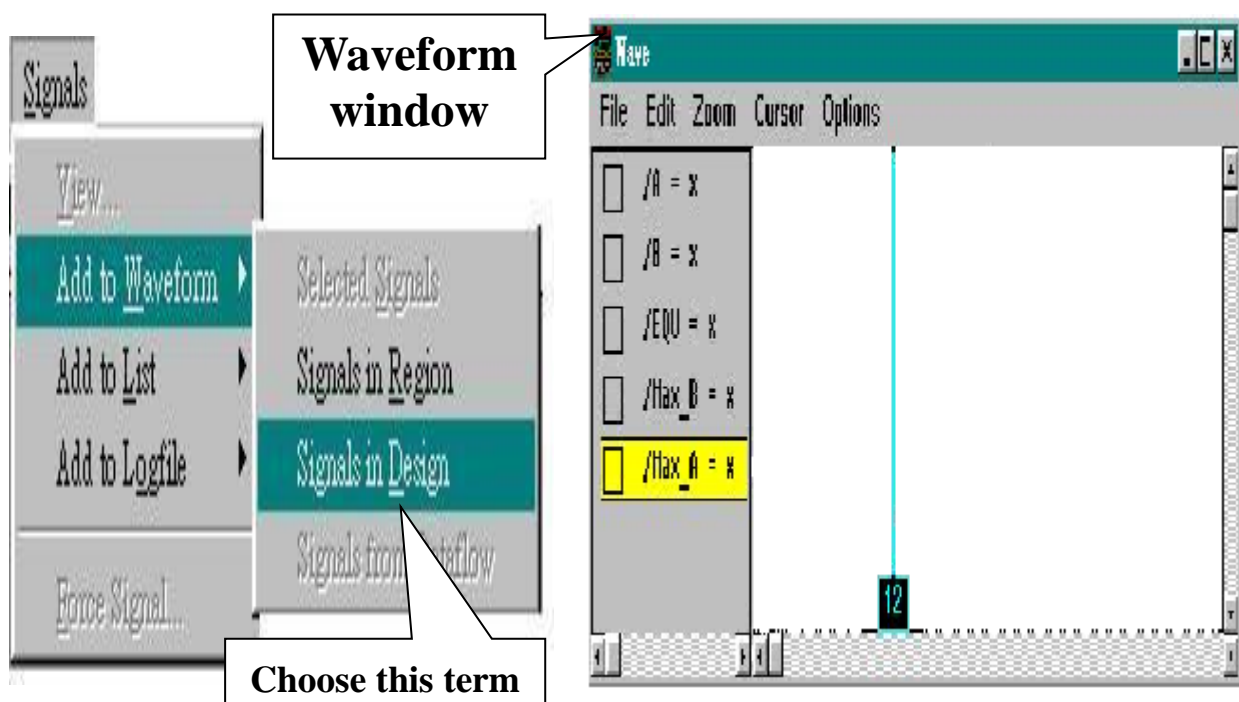
Step1. Click VLOG button and load user source code then Compile
Ps. Set Target Library verilog



Step 2. Click VSIM, set library and choose design unit

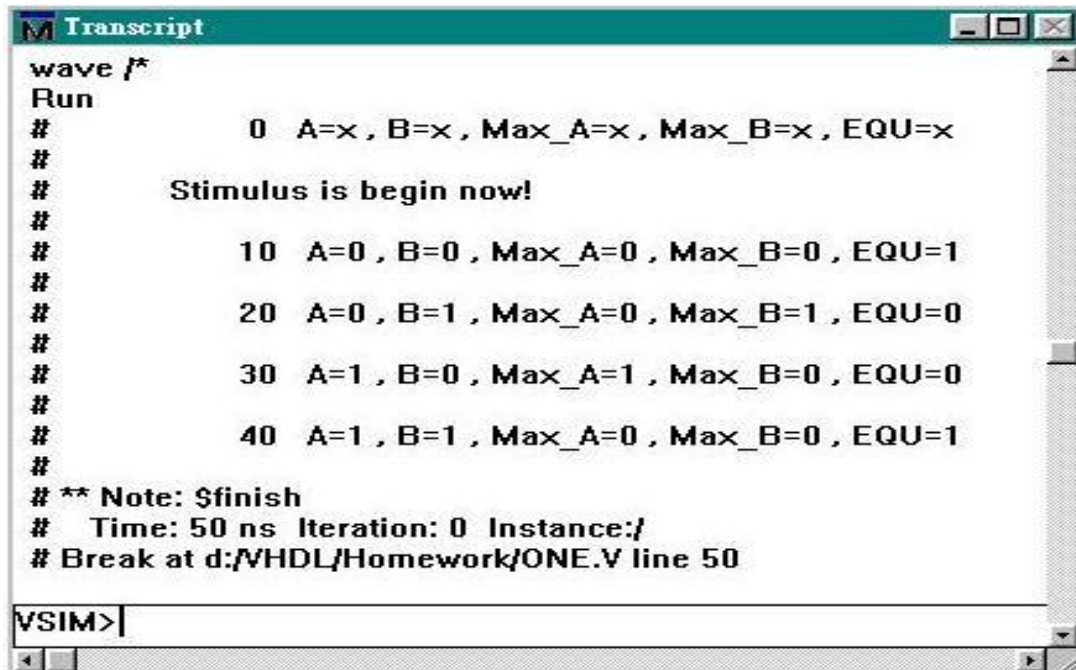


Step 3. Choose signal => Add to Waveform =>Signal in Region then will create a new wave window



Step 4. Click RUN then create Stimulate Text and Stimulate waveform

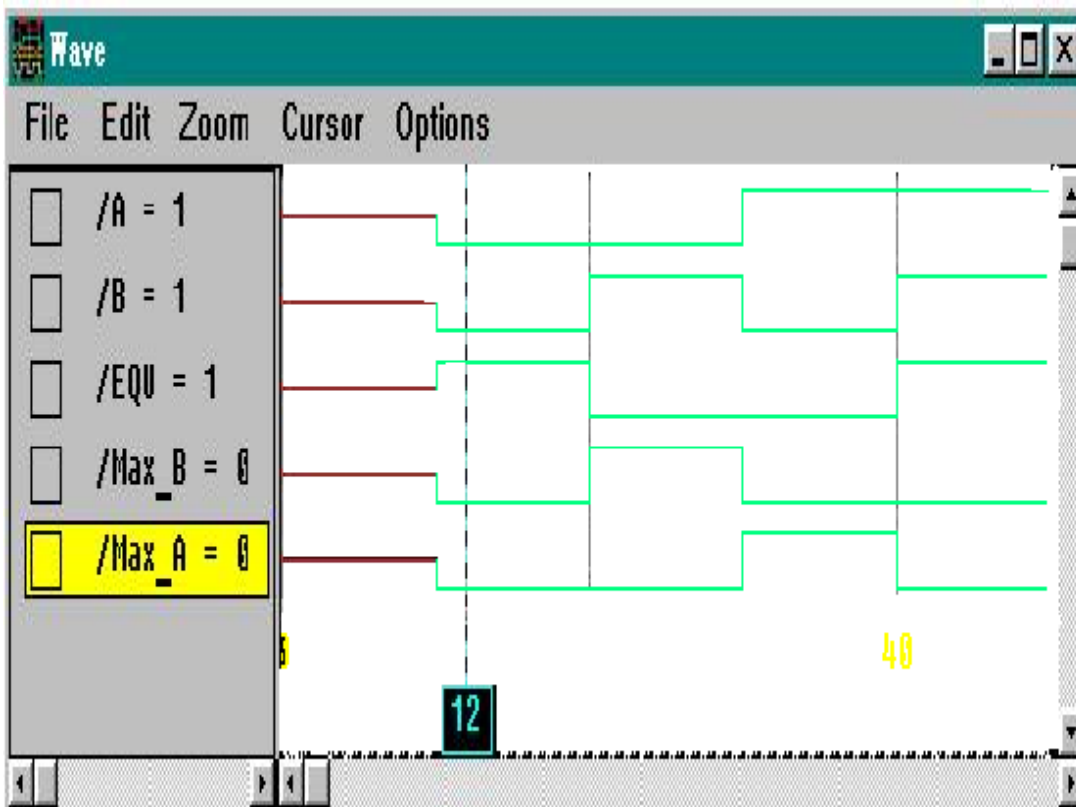
(a). Stimulate Text output



The Transcript window displays the following text:

```
wave /*
Run
#      0  A=x , B=x , Max_A=x , Max_B=x , EQU=x
#
#      Stimulus is begin now!
#
#      10  A=0 , B=0 , Max_A=0 , Max_B=0 , EQU=1
#
#      20  A=0 , B=1 , Max_A=0 , Max_B=1 , EQU=0
#
#      30  A=1 , B=0 , Max_A=1 , Max_B=0 , EQU=0
#
#      40  A=1 , B=1 , Max_A=0 , Max_B=0 , EQU=1
#
# ** Note: $finish
# Time: 50 ns Iteration: 0 Instance:/
# Break at d:/VHDL/Homework/ONE.V line 50
VSIM>
```

(b). Stimulate Waveform output



1.2 Workstation CADENCE Environment

Step1. After finishing the verilog source code, keyin the compiler keyword like below.

```
cad10>  
cad10> verilog adder.v
```

User verilog code file name

Step2. If user verilog source code is no error, then the system will show stimulate result in command tool window like below.

Command tool

Verilog Compiler instruction

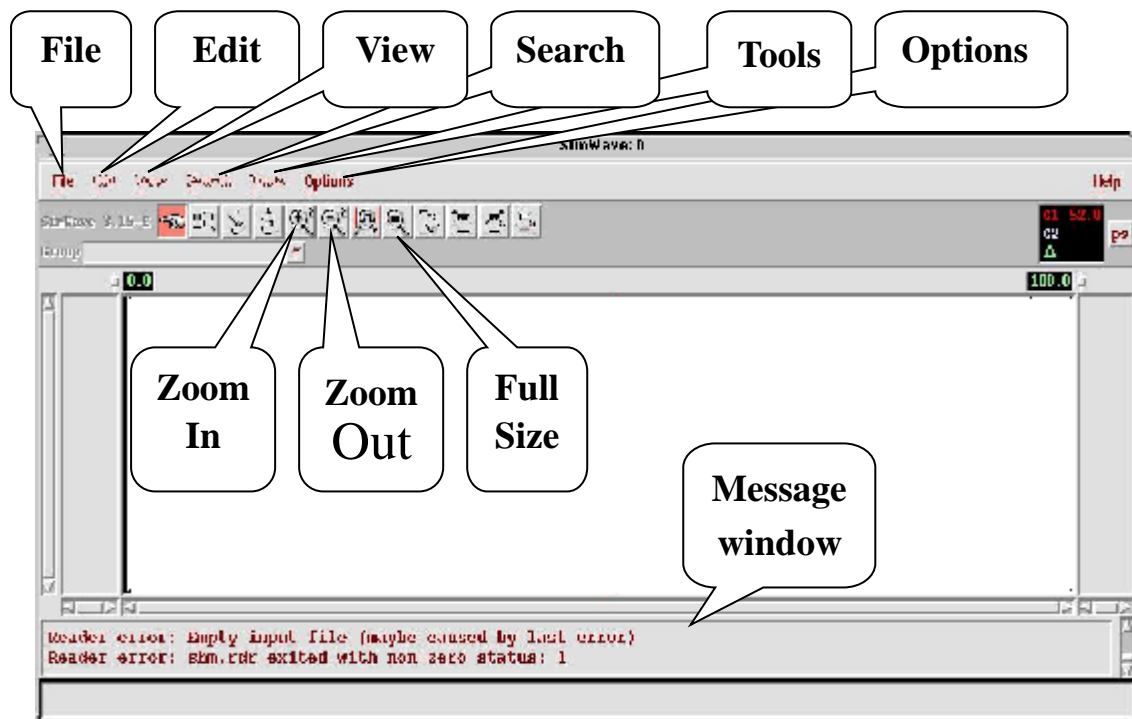
Stimulate text result

```
cmdtool - /bin/csh  
reading [Verilog-SFCOR]  
cad10> cd /cad14_DA/usr/sheumh/y85/u8513004/CDS  
cad10> cd ..  
/cad14_DA/usr/sheumh/y85/u8513004  
cad10> verilog adder.v  
VERILOG-XL 2.5.16 Jul 29, 1999 15:17:50  
  
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Cadence Design Systems, Inc.  
555 River Oaks Parkway  
San Jose, California 95134  
  
For technical assistance please contact the Cadence Response Center at  
1-800-CADENC2 or send email to crc_customers@cadence.com  
  
For more information on Cadence's Verilog-XL product line send email to  
talkverilog@cadence.com  
  
Compiling source file "adder.v"  
Highest level modules:  
stimus  
  
0a=0 b=0 sum=0 carry=0  
10a=1 b=0 sum=1 carry=0  
20a=0 b=1 sum=1 carry=0  
30a=1 b=1 sum=0 carry=1  
  
L40 "adder.v": $finish at simulation time 40  
0 simulation events (use +profile or +listcounts option to count)  
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.0 secs in simulation  
End of VERILOG-XL 2.5.16 Jul 29, 1999 15:17:51  
cad10>
```

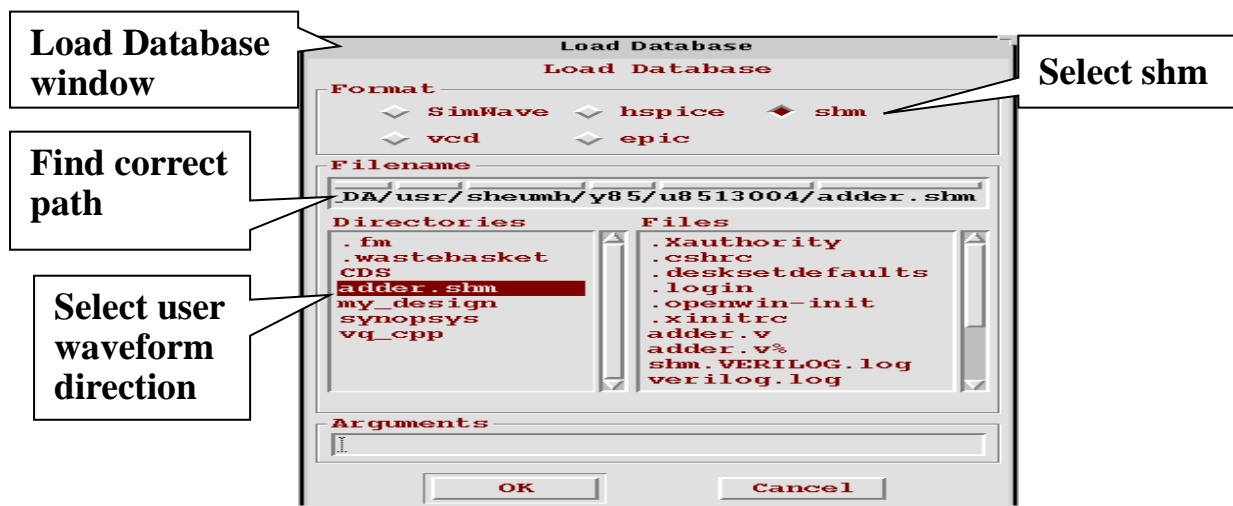
Step3. In Command Tool open the simwave



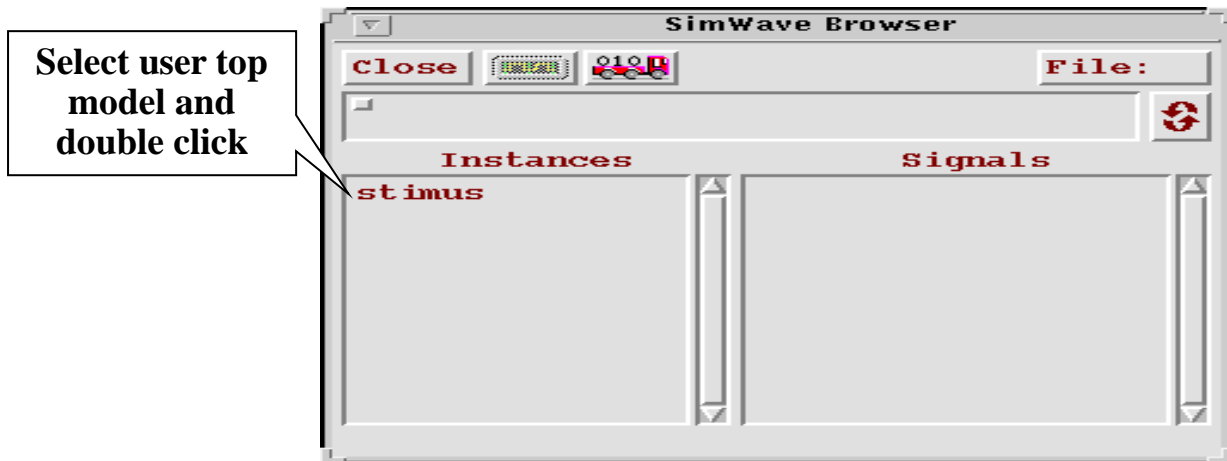
- The simwave window is shown below



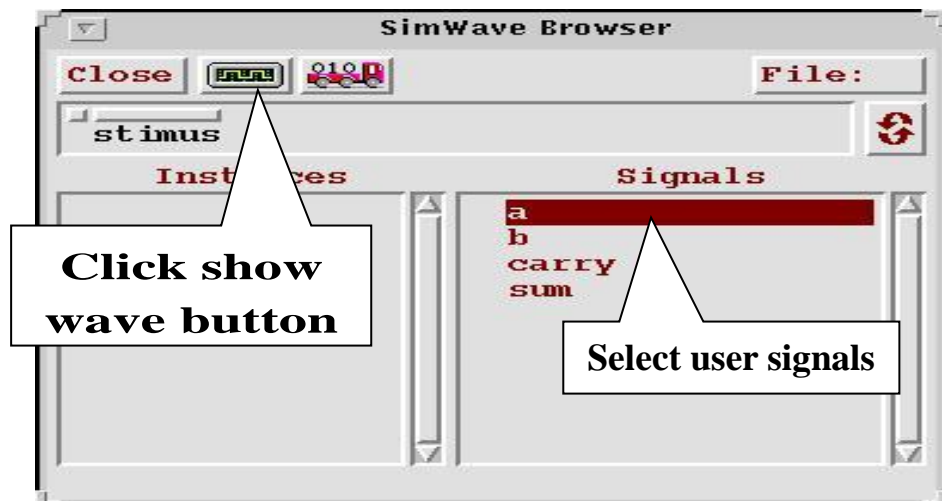
Step4. Click File -> Database -> Load... then open Load window.



Step5. Click bottom Edit -> Add Signals... then will open browser window



Step6. Select 'a' signal in signals region, then click show wave button



Step7. Repeat step6 to pick up all input and output signals, then the *simwave* window will display those signal waveforms.

