Describe cell-based back-end design flow

I. Place & Router (APR): Place and route is a stage in the design of printed circuit boards, integrated circuits, and field-programmable gate arrays. As implied by the name, it is composed of two steps, placement and routing. The first step, placement, involves deciding where to place all electronic components, circuitry, and logic elements in a generally limited amount of space. This is followed by routing, which decides the exact design of all the wires needed to connect the placed components. This step must implement all the desired connections while following the rules and limitations of the manufacturing process.

- Floor plan
  規劃電路每個部分因布置在哪個樓層
- Power Plan
  布置電網，讓每個元件可以獲的充裕的電壓，避免中心電壓過低
- Placement
  將元件布置，以降低可能的壅塞現象
- Clock Tree Synthesis: CTS is the process of insertion of buffers or inverters along the clock paths of ASIC design in order to achieve zero/minimum skew or balanced skew. The goal of CTS is to minimize skew and insertion delay. Apart from these, useful skew is also added in the design by means of buffers and inverters.
- Routing

II. Layout

把完整電路圖輸出

III. SDF

標準延遲格式，用於各 GATE 單元間的延遲情況，用來描述準確的實際電路

IV. Post-Layout Timing Check

輸出後的時間檢查

V. System-level Integration

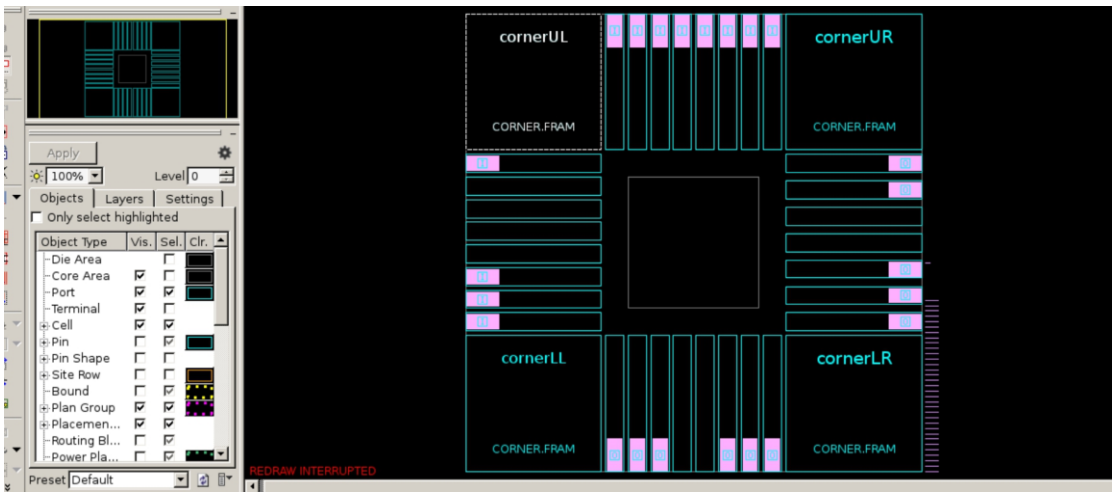
系統層的整合

VI. GDS

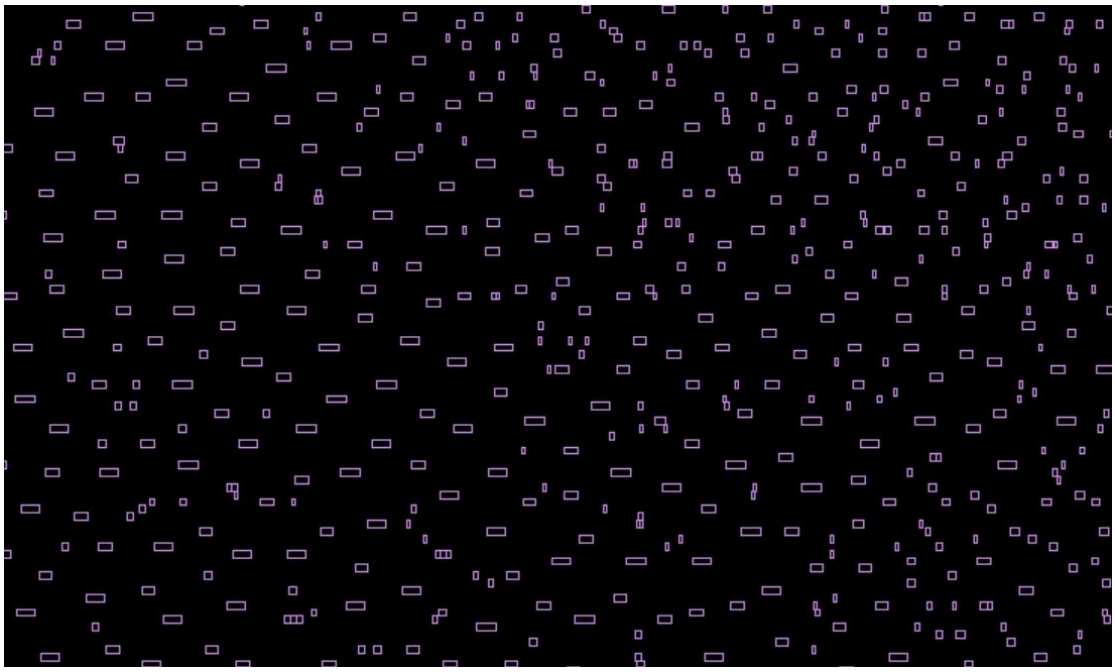
半導體製造商接受的檔案格式

Placement:

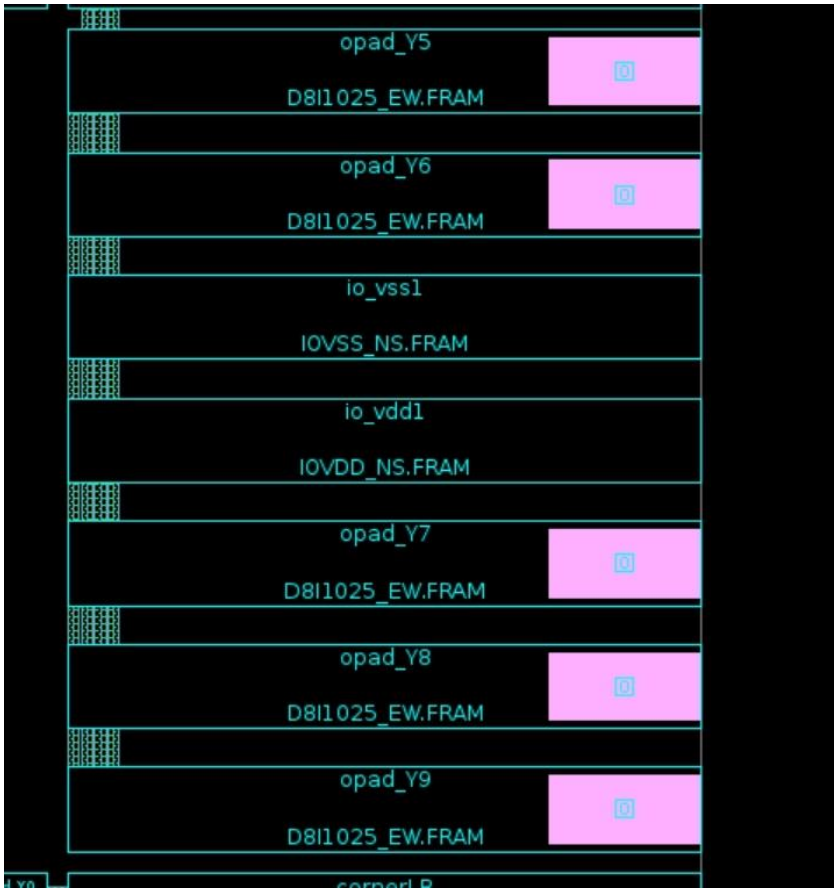
Create Power Pad & Floorplan:



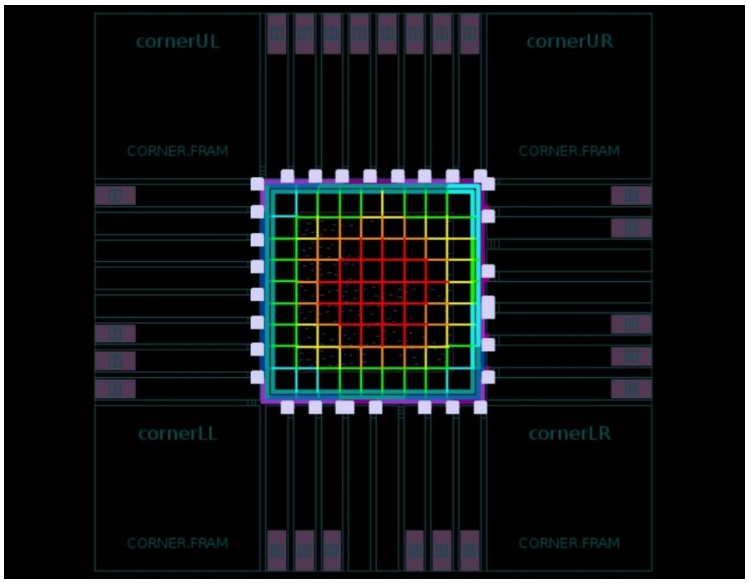
Place Standard Cells:



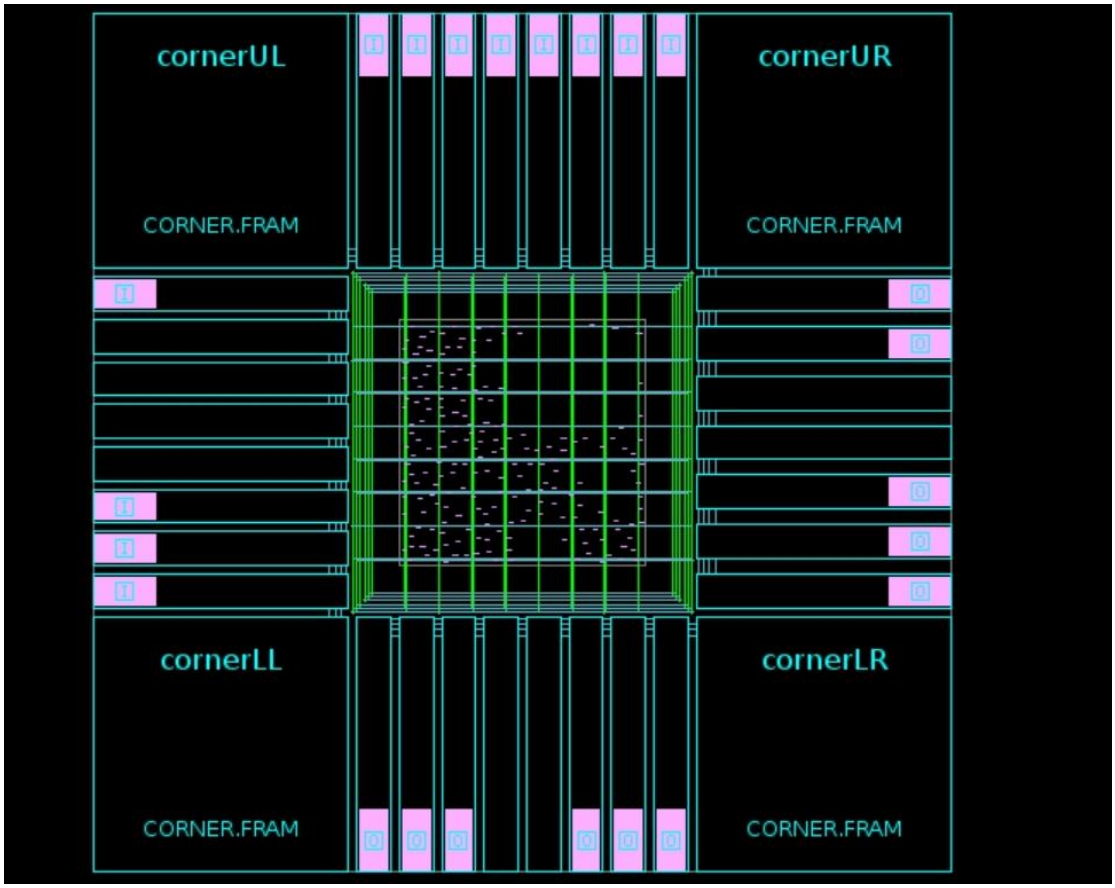
Congestion:



Voltage Drop:



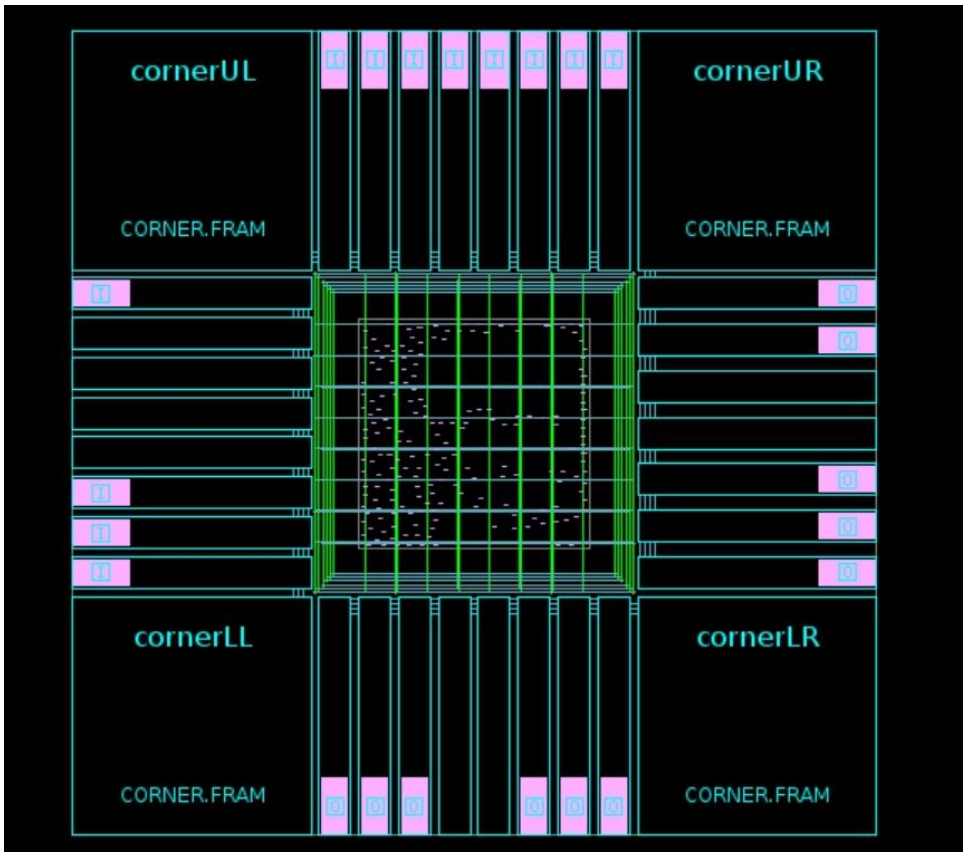
Synthesize Power Network:



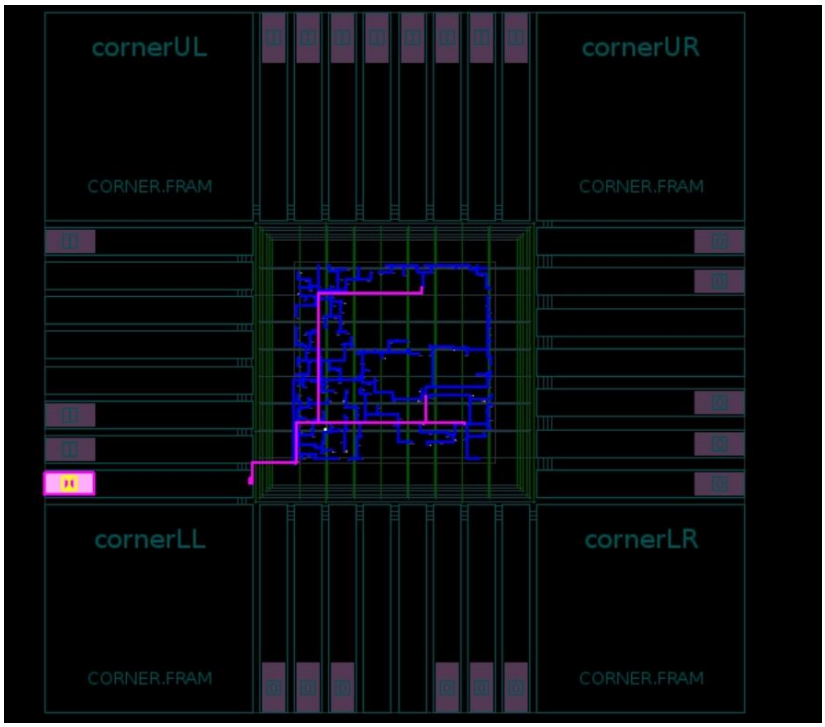
Report Timing:

```
  core/add_25/U1_9/CO (FADDX1_RVT)                        0.11 z      8.94 r
  core/add_25/U1_10/CO (FADDX1_RVT)                       0.11 z      9.04 r
  core/add_25/U1_11/S (FADDX1_RVT)                        0.16 z      9.21 f
  core/add_25/U15/Y (INVX1_RVT)                           0.04 z      9.25 r
  core/add_25/U2/Y (INVX4_RVT)                            0.05 z      9.30 f
  core/add_25/SUM[11] (CS_DW01_add_1)                     0.00 z      9.30 f
  core/Y[8] (CS)                                          0.00 z      9.30 f
  opad_Y8/PADIO (D8I1025_EW)                              1.30 z     10.60 f
  Y[8] (out)                                              0.00 z     10.60 f
  data arrival time                                                  10.60

  clock clk (rise edge)                                  20.00       20.00
  clock network delay (ideal)                             0.50       20.50
  clock uncertainty                                      -0.10       20.40
  output external delay                                   0.00       20.40
  data required time                                                 20.40
  ---------------------------------------------------------------------------
  data required time                                                 20.40
  data arrival time                                                 -10.60
  ---------------------------------------------------------------------------
  slack (MET)                                                        9.80


1
icc_shell>
```

Original CTS:



Fix Clock Tree:




```
****************************************
Report : clock tree
Design : CHIP
Version: N-2017.09
Date   : Mon Dec 11 14:12:42 2017
****************************************

Information: Float pin scale factor for the 'max' operating condition of scenario 'default' is set to 1.000 (CTS-375)

======================= Clock Tree Summary ========================
Clock                Sinks     CTBuffers ClkCells  Skew      LongestPath TotalDRC   BufferArea
-------------------------------------------------------------------------------------------------
clk                  200       8         9         0.0136    2.4303      0             41.9338
1
icc_shell>
```

Report Timing:

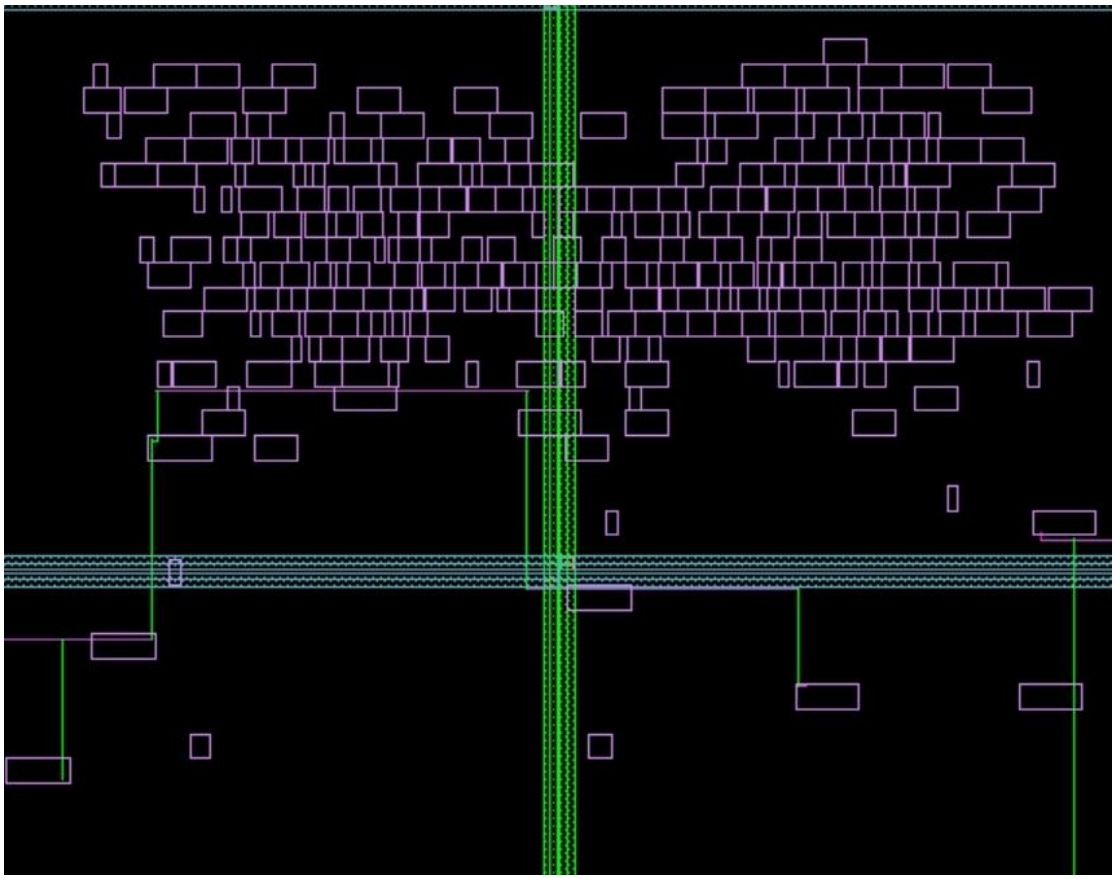
```
  core/add_25/U1_6/CO (FADDX2_RVT)                        0.12 &    12.66 r
  core/add_25/U1_7/CO (FADDX1_RVT)                        0.14 &    12.80 r
  core/add_25/U1_8/CO (FADDX1_RVT)                        0.14 &    12.95 r
  core/add_25/U1_9/S (FADDX2_RVT)                         0.24 &    13.18 f
  core/add_25/SUM[9] (CS_DW01_add_1)                      0.00      13.18 f
  core/Y[6] (CS)                                          0.00      13.18 f
  U7/Y (DELLN1X2_RVT)                                     0.30 &    13.48 f
  U6/Y (NBUFFX4_RVT)                                      0.10 @    13.58 f
  opad_Y6/PADIO (D8I1025_EW)                              1.32 @    14.90 f
  Y[6] (out)                                              0.00      14.90 f
  data arrival time                                                 14.90

  clock clk (rise edge)                                  20.00      20.00
  clock network delay (ideal)                             0.50      20.50
  clock uncertainty                                      -0.10      20.40
  output external delay                                   0.00      20.40
  data required time                                                20.40
  ---------------------------------------------------------------------------
  data required time                                                20.40
  data arrival time                                                -14.90
  ---------------------------------------------------------------------------
  slack (MET)                                                       5.50


1
```

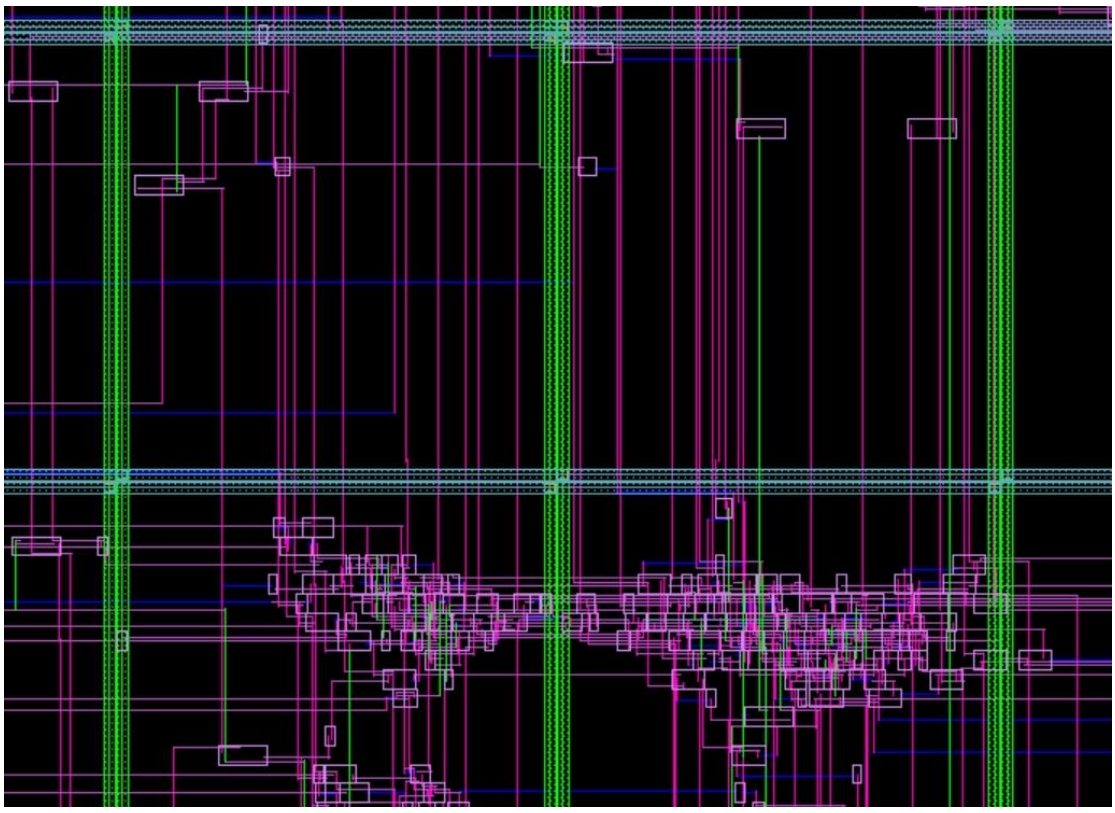
Routing:

Routability:

```
============================================
==    Check for out-of-boundary ports     ==
============================================

>>>>>> No out-of-boundary error found

============================================
==        Check for blocked ports         ==
============================================

>>>>>> Port blocked by layer constraints - min/max and freeze layer settings

>>>>>> Port blocked by check port access

>>>>>> No blocked port found

>>>>>> Net blocked by layer constraints - min/max and freeze layer settings

>>>>>> No blocked net found

End of check_zrt_routability
1
```

```
============================================
==  Check for overlap of standard cells   ==
============================================

>>>>>> No overlap of standard cells found

============================================
==     Check for min-grid violations      ==
============================================

>>>>>> No min-grid violations found


============================================
==    Check for out-of-boundary ports     ==
============================================

>>>>>> No out-of-boundary error found

============================================
==        Check for blocked ports         ==
============================================
```





Overall discussion and your experience report:

藉由這次的實習，我發現到電腦輔助設計功能的強大，不儘可以有效最佳化電網配置，讓晶片內的各元件可以獲得充裕的電力，時脈網路的最佳化配置，也讓各個需要 CLOCK 的元件能充分獲得時脈，讓整個電路更穩定可靠，樓層與路線的布置，也有效降低延遲及稱產成本、溫度等，這些都是傳統數位邏輯設計課程學不到的東西，很謝謝老師給我們這個機會接觸到這麼厲害的工具，讓我們更接近業界的實務應用。