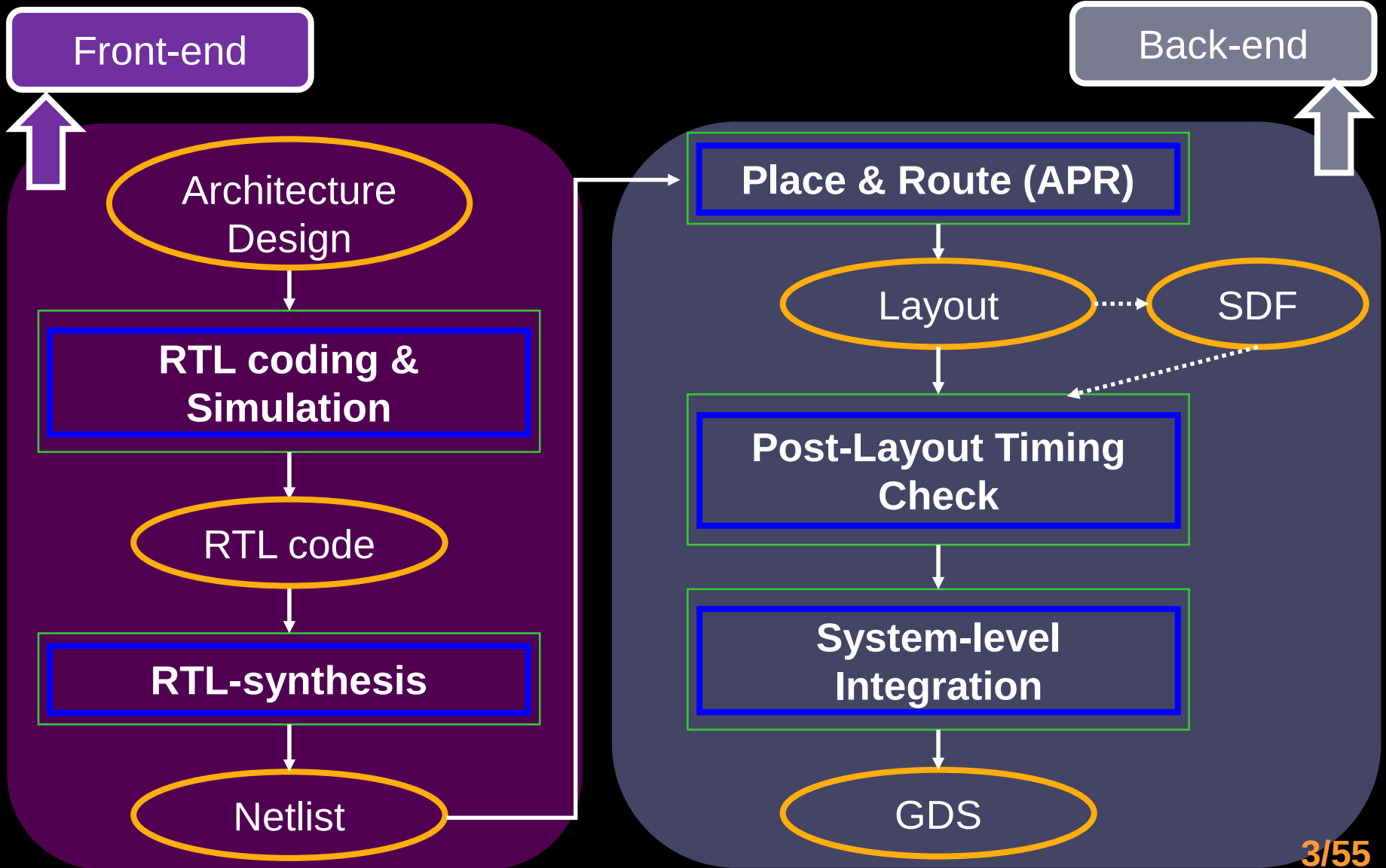
# Cell-based IC Design Flow
# Front-end: Synthesis

**CAD Lab.**

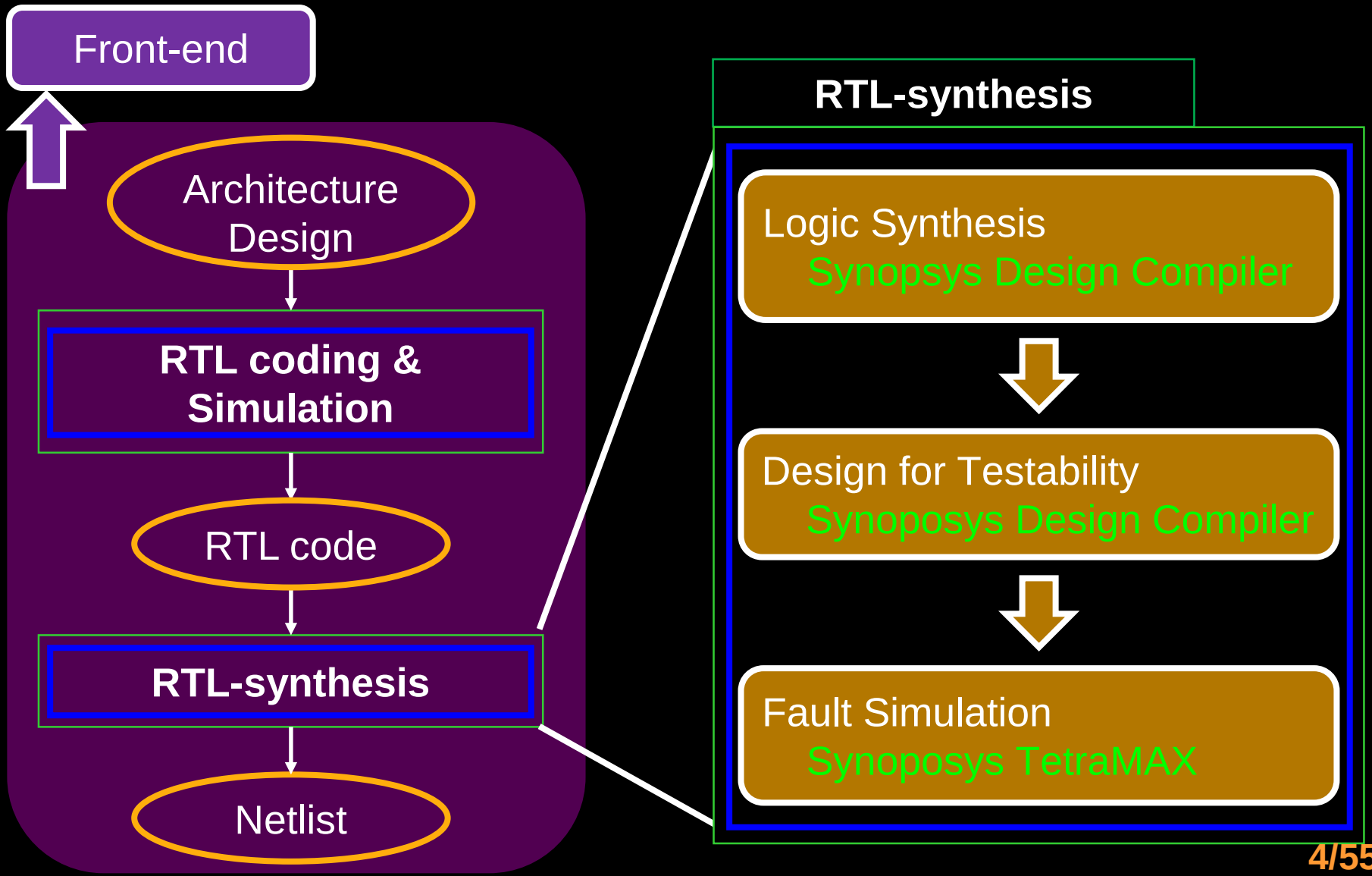
# Outline

- **IC Design Flow**
  - Cell-based Design Flow (Front-end)
  - Environment Setup
- **Logic Synthesis with Design Compiler**
- **Design for Testability with Design Compiler**
- **Fault Simulation with TetraMAX**

# Cell-based Design Flow



# Cell-based Design Flow – Front-end



# What is Synthesis

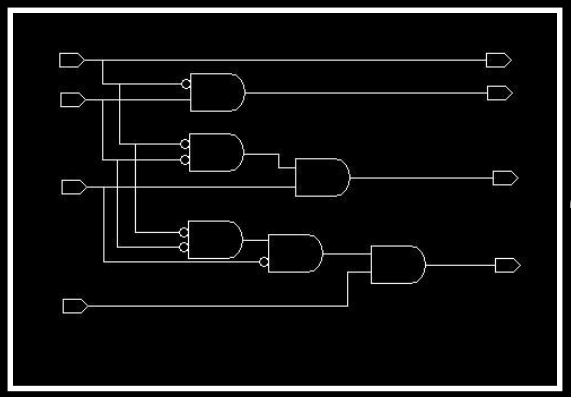
- Synthesis = translation + optimization + mapping

```
Residue = 16'h0000;
If ( high_bits == 2'b10 )
   residue = state_table[i] ;
Else state_table[i] = 16'h0000;
```

HDL Source

( RTL )

Translate (HDL Compiler)

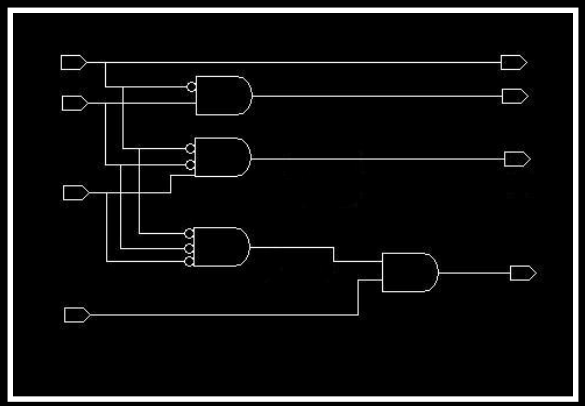


Generic Boolean

( GTECH )

Optimize + Map

(Design Compiler)



Target Technology

# Behavioral HDL

```
module lab1(a,b,c,sel,z);
input [7:0] a,b,c;
input sel;
output [8:0] z;

always @(a or b or c) begin
if (sel) z = a + b;
else z = a + c;
End

endmodule
```

# Gate-level HDL (1/2)

```
module lab1_DW01_add_0 ( A, B, CI, SUM, CO );
  input [8:0] A;
  input [8:0] B;
  output [8:0] SUM;
  input CI;
  output CO;
  wire   \carry[7] , \carry[6] , \carry[5] , \carry[4] , \carry[3] ,
         \carry[2] , \carry[1] ;

  ADDFX2 U1_7 ( .A(A[7]), .B(B[7]), .CI(\carry[7] ), .CO(SUM[8]), .S(SUM[7])
         );
  ADDFX2 U1_6 ( .A(A[6]), .B(B[6]), .CI(\carry[6] ), .CO(\carry[7] ), .S(
        SUM[6]) );
  ADDFX2 U1_5 ( .A(A[5]), .B(B[5]), .CI(\carry[5] ), .CO(\carry[6] ), .S(
        SUM[5]) );
  ADDFX2 U1_4 ( .A(A[4]), .B(B[4]), .CI(\carry[4] ), .CO(\carry[5] ), .S(
        SUM[4]) );
  ADDFX2 U1_3 ( .A(A[3]), .B(B[3]), .CI(\carry[3] ), .CO(\carry[4] ), .S(
        SUM[3]) );
  ADDFX2 U1_2 ( .A(A[2]), .B(B[2]), .CI(\carry[2] ), .CO(\carry[3] ), .S(
        SUM[2]) );
  ADDFX2 U1_1 ( .A(A[1]), .B(B[1]), .CI(\carry[1] ), .CO(\carry[2] ), .S(
        SUM[1]) );
  AND2X1 U1 ( .A(A[0]), .B(B[0]), .Y(\carry[1] ) );
  XOR2X1 U2 ( .A(B[0]), .B(A[0]), .Y(SUM[0]) );
endmodule
```

# Gate-level HDL (2/2)

```
module lab1 ( a, b, c, sel, z );
  input [7:0] a;
  input [7:0] b;
  input [7:0] c;
  output [8:0] z;
  input sel;
  wire   \U1/U1/Z_0 , \U1/U1/Z_1 , \U1/U1/Z_2 , \U1/U1/Z_3 , \U1/U1/Z_4 ,
         \U1/U1/Z_5 , \U1/U1/Z_6 , \U1/U1/Z_7 ;

  lab1_DW01_add_0 r248 ( .A({1'b0, a}), .B({1'b0, \U1/U1/Z_7 , \U1/U1/Z_6 ,
        \U1/U1/Z_5 , \U1/U1/Z_4 , \U1/U1/Z_3 , \U1/U1/Z_2 , \U1/U1/Z_1 ,
        \U1/U1/Z_0 }), .CI(1'b0), .SUM(z) );
  MX2X1 U20 ( .A(c[7]), .B(b[7]), .S0(sel), .Y(\U1/U1/Z_7 ) );
  MX2X1 U21 ( .A(c[6]), .B(b[6]), .S0(sel), .Y(\U1/U1/Z_6 ) );
  MX2X1 U22 ( .A(c[5]), .B(b[5]), .S0(sel), .Y(\U1/U1/Z_5 ) );
  MX2X1 U23 ( .A(c[4]), .B(b[4]), .S0(sel), .Y(\U1/U1/Z_4 ) );
  MX2X1 U24 ( .A(c[3]), .B(b[3]), .S0(sel), .Y(\U1/U1/Z_3 ) );
  MX2X1 U25 ( .A(c[2]), .B(b[2]), .S0(sel), .Y(\U1/U1/Z_2 ) );
  MX2X1 U26 ( .A(c[1]), .B(b[1]), .S0(sel), .Y(\U1/U1/Z_1 ) );
  MX2X1 U27 ( .A(c[0]), .B(b[0]), .S0(sel), .Y(\U1/U1/Z_0 ) );
endmodule
```

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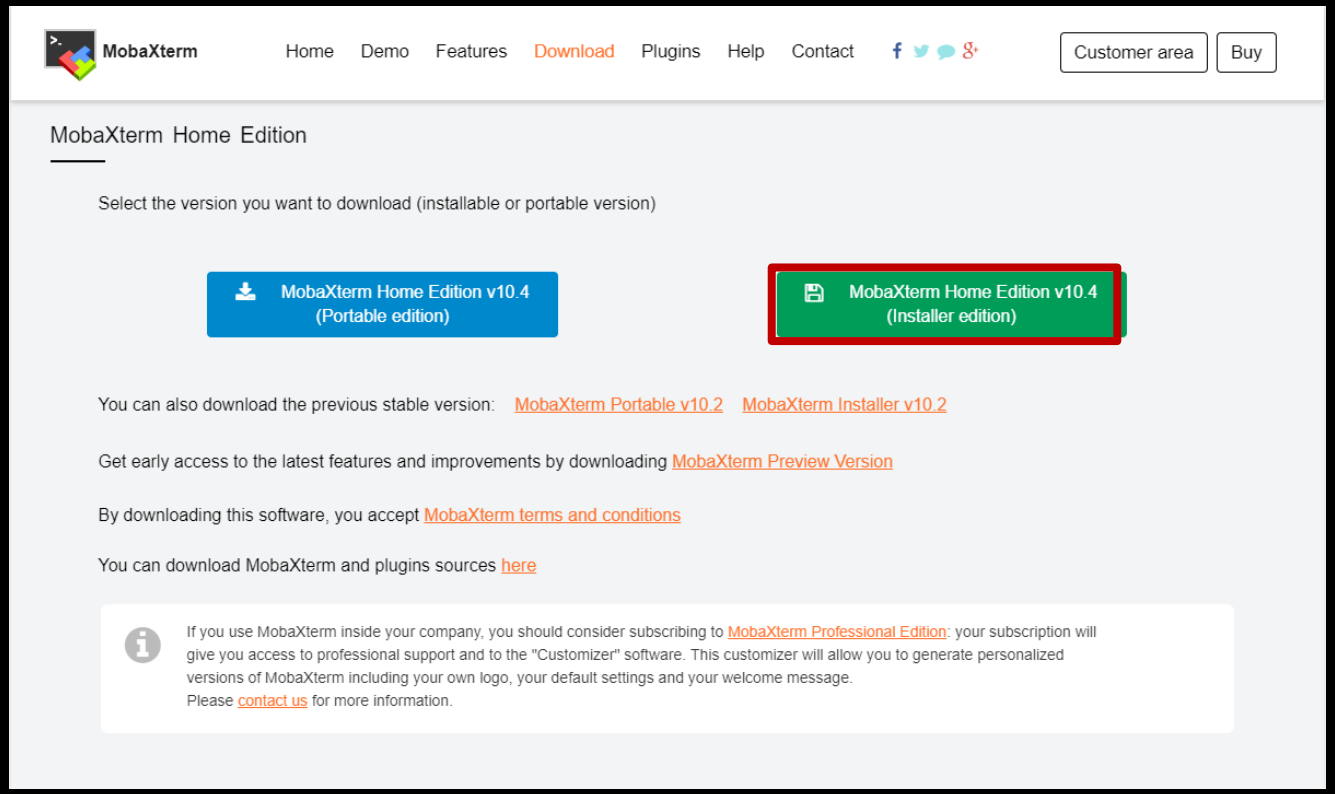
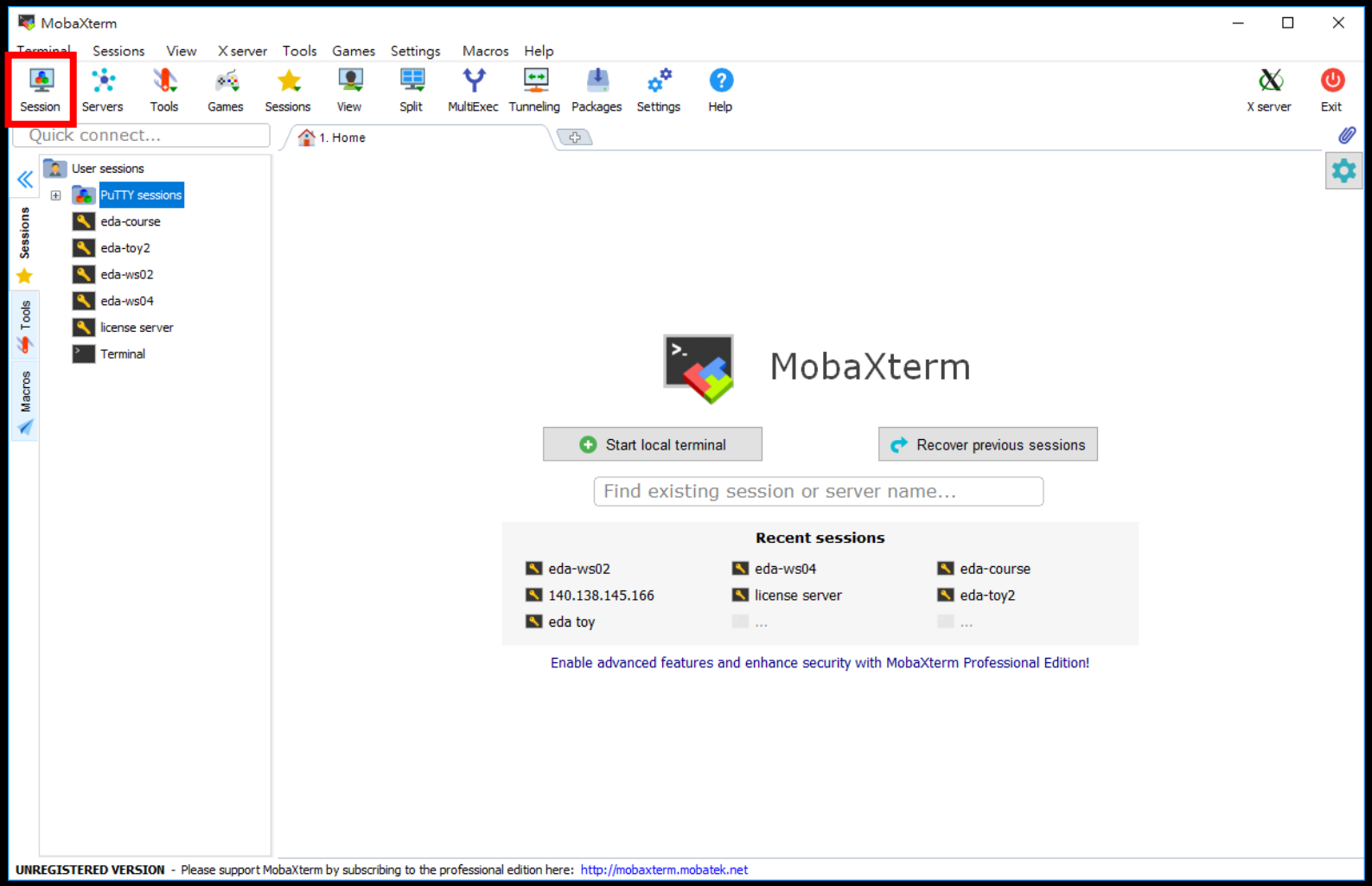
# MobaXterm (1/4)

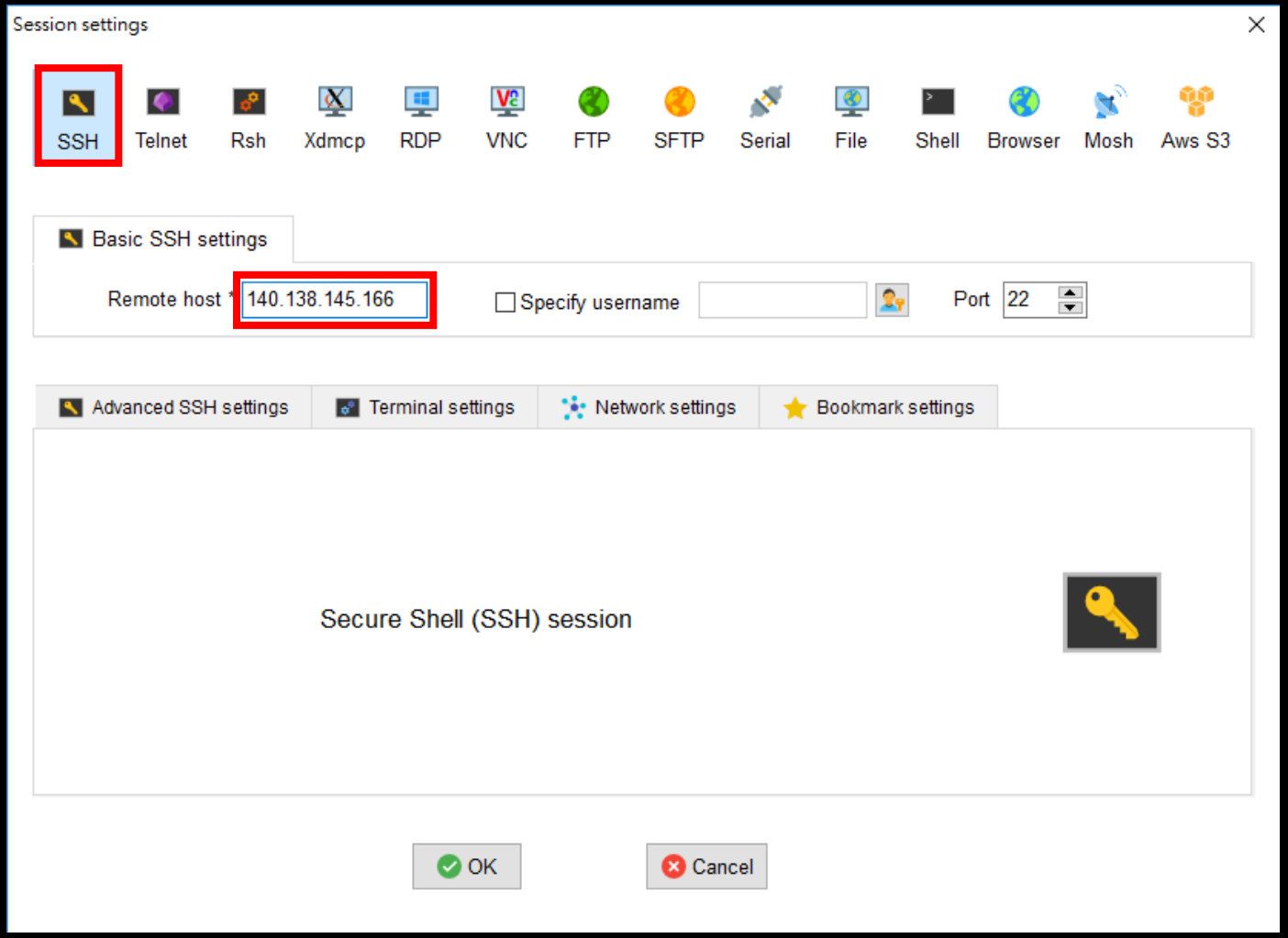
- https://mobaxterm.mobatek.net/download-home-edition.html
- Download installer edition



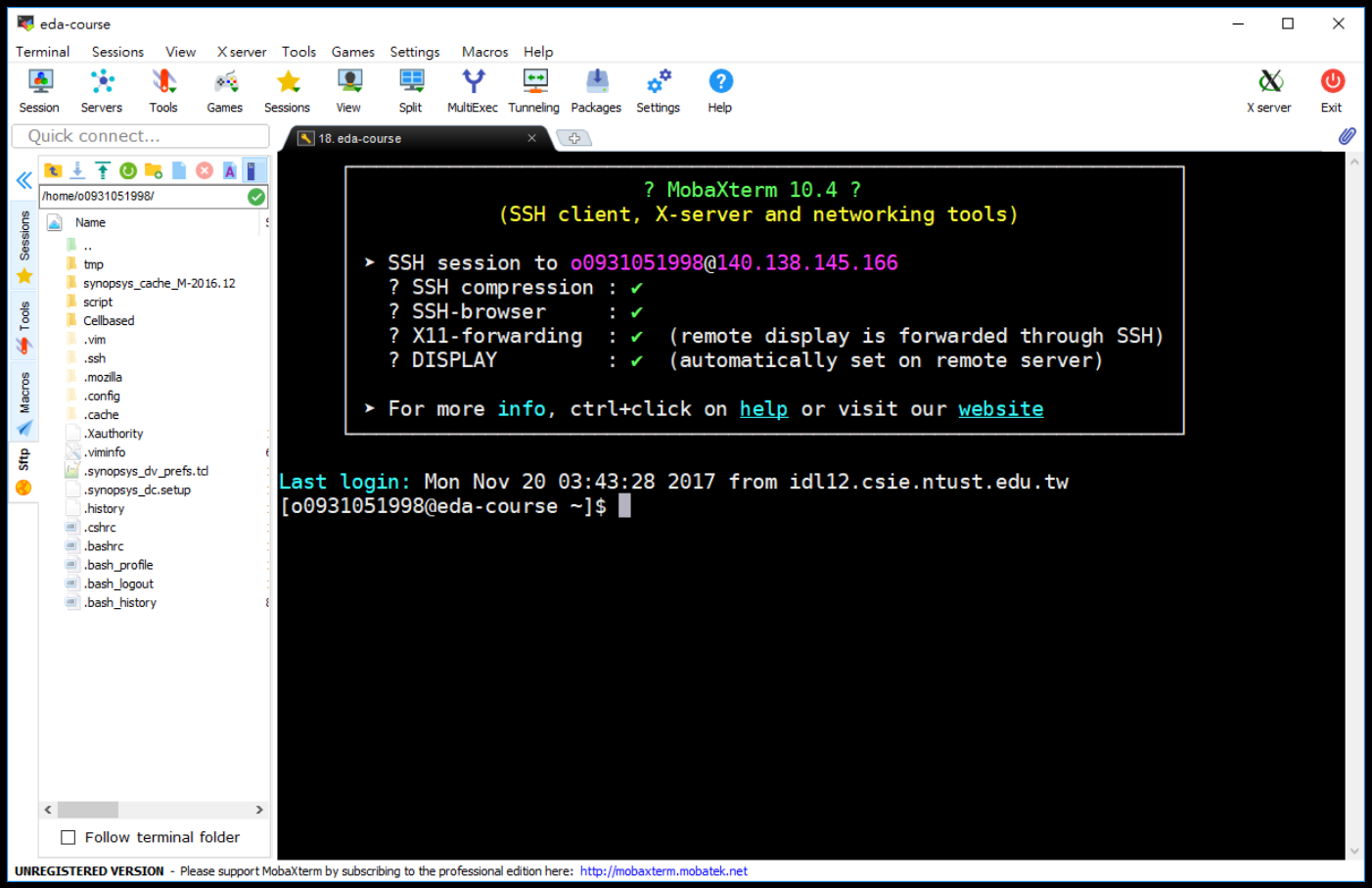
# MobaXterm (2/4)



# MobaXterm (3/4)



# MobaXterm (4/4)



# Linux Commands

- **$> cd: change directory**
- **$> ls: list directory contents**
- **$> mv: move (rename) files**
- **$> cp: copy files and directories**
- **$> man: manual page**
  - $> man cd
  - $> man ls

# Linux Commands (cont.)

- **$> pwd: print name of current/working directory**
  - . → current directory
  - .. → parent directory
  - ~ → home directory

# Environment Setting

- **CAD Tool (Synopsys - Design Vision)**
  - $> csh
  - $> source /usr/cad/synopsys/CIC/synthesis.cshrc
  - $> source /usr/cad/synopsys/CIC/tmax.cshrc
- **Directory and files**
  - $> cp /tmp/Cellbased_frontend_32nm.tar  .
  - $> tar xvf Cellbased_frontend_32nm.tar
  - $> cd Cellbased_frontend_32nm
  - $> cd run/

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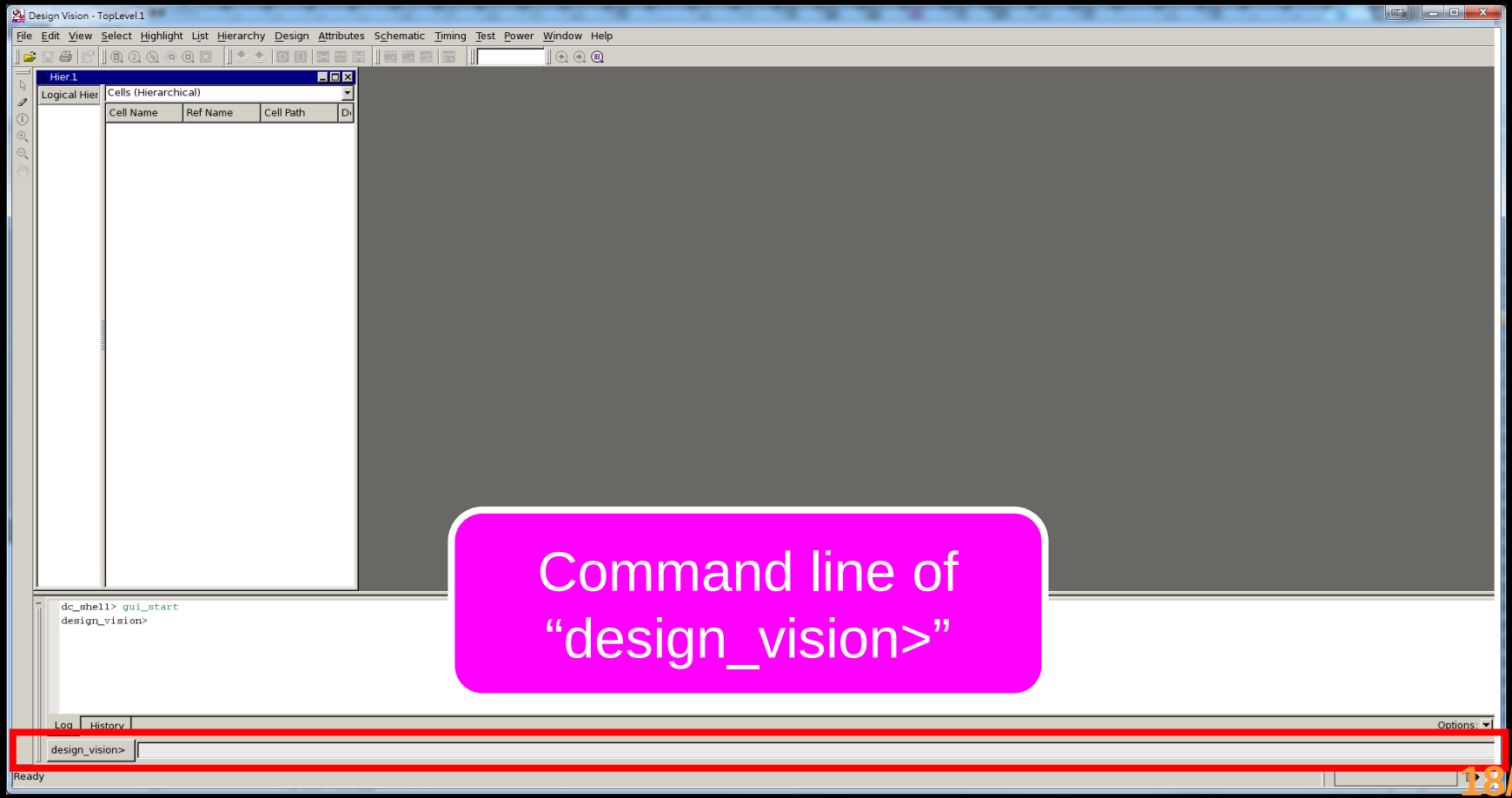
# GUI Interface of Design Compiler

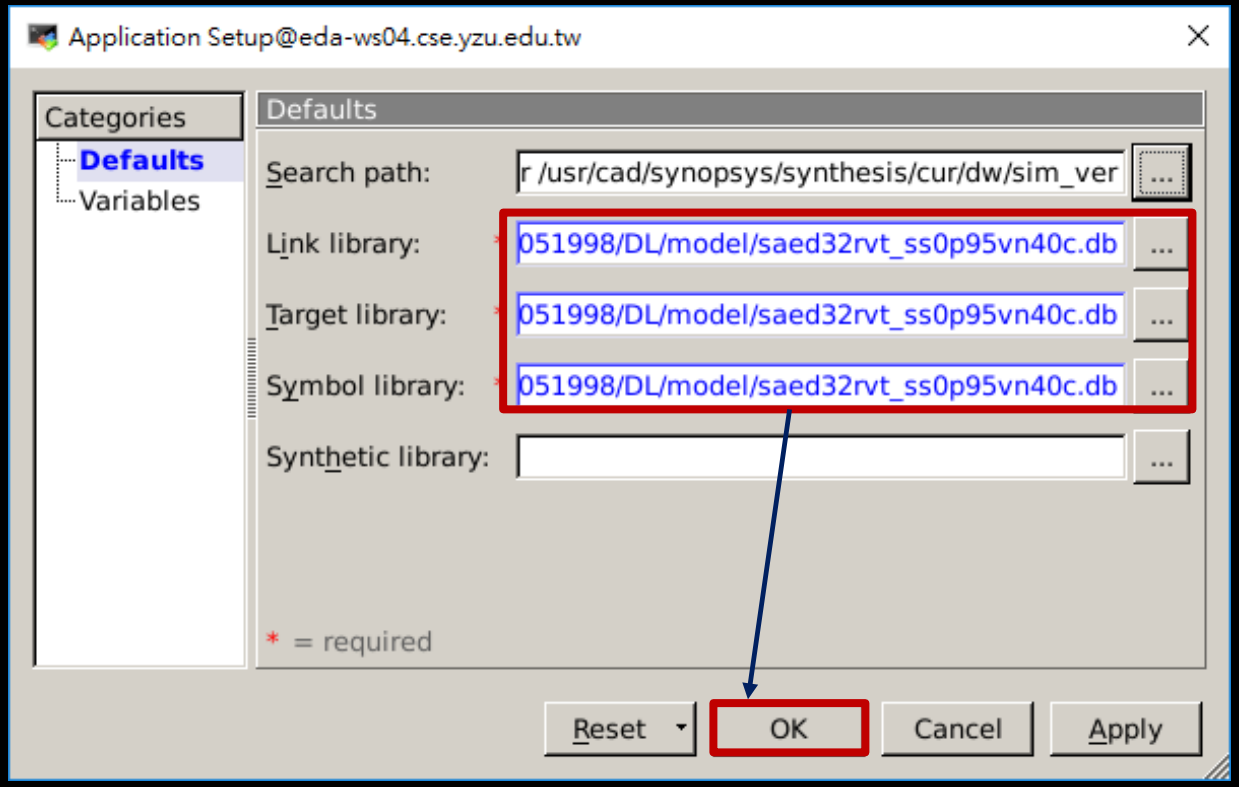
- GUI of Design Compiler is called Design Vision
- $> dv



# Design Vision Setup (1/2)

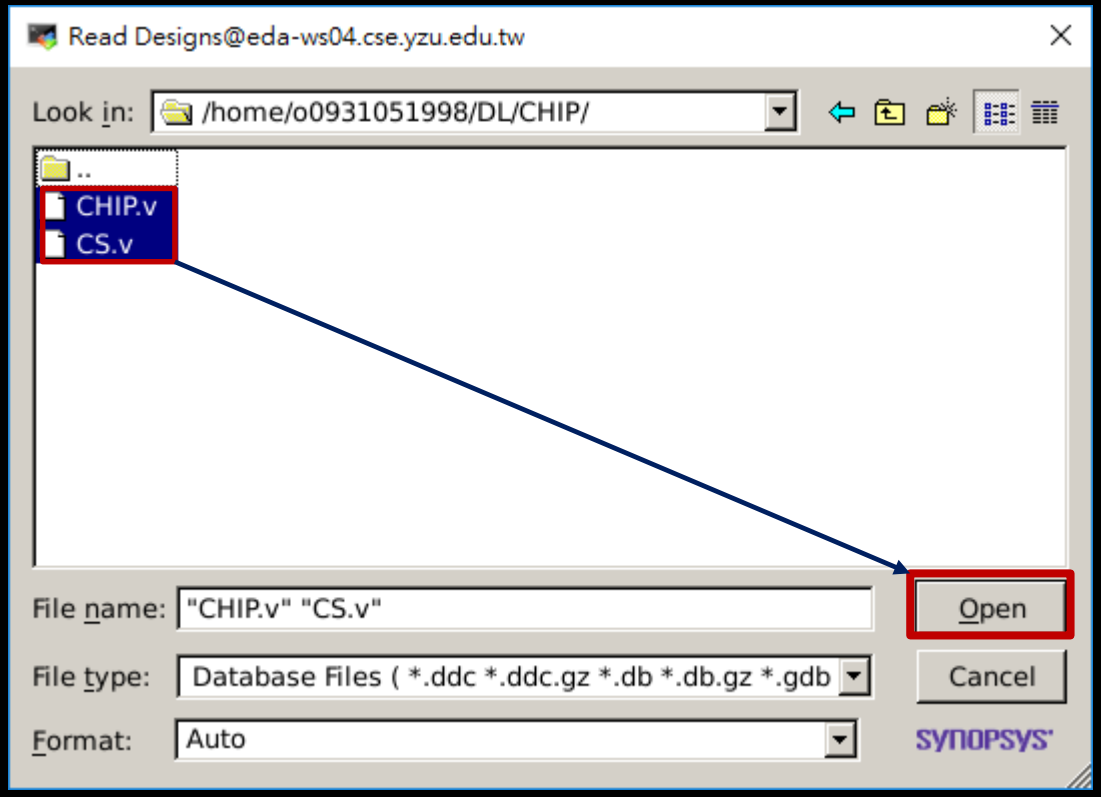
- **File → Setup**
- **Delete the default model “*”, “your_library.db”, “your_library.sdb”**
- **Choose the following four models for link library, target library, and symbol library**
  - saed32io_wb_ff1p16v25c_2p75v.db
  - saed32io_wb_ss0p95vn40c_2p25v.db
  - saed32rvt_ff1p16v25c.db
  - saed32rvt_ss0p95vn40c.db
- **Press “OK”**

# Design Vision Setup (2/2)

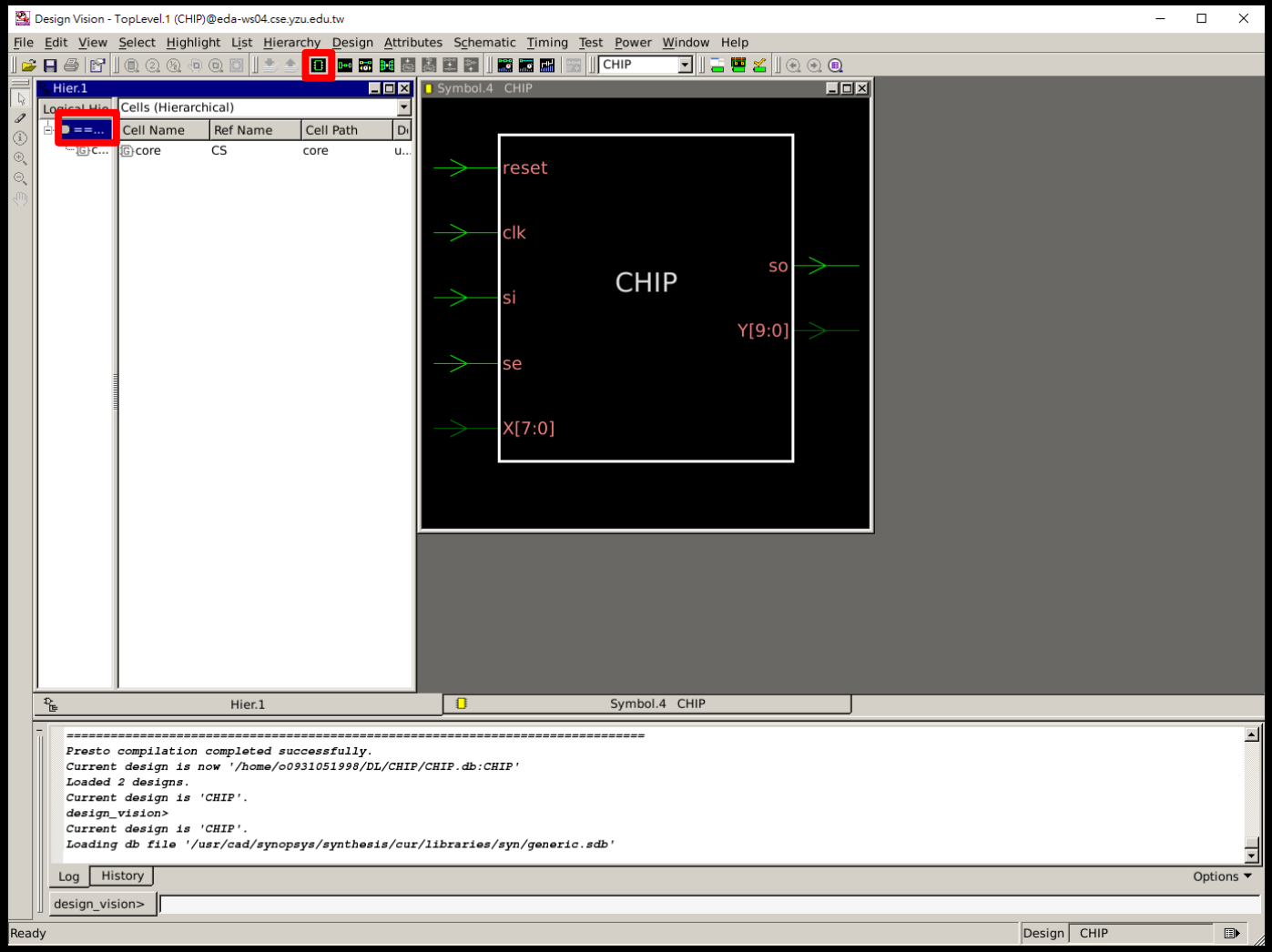


# Read File

- **File → Read**

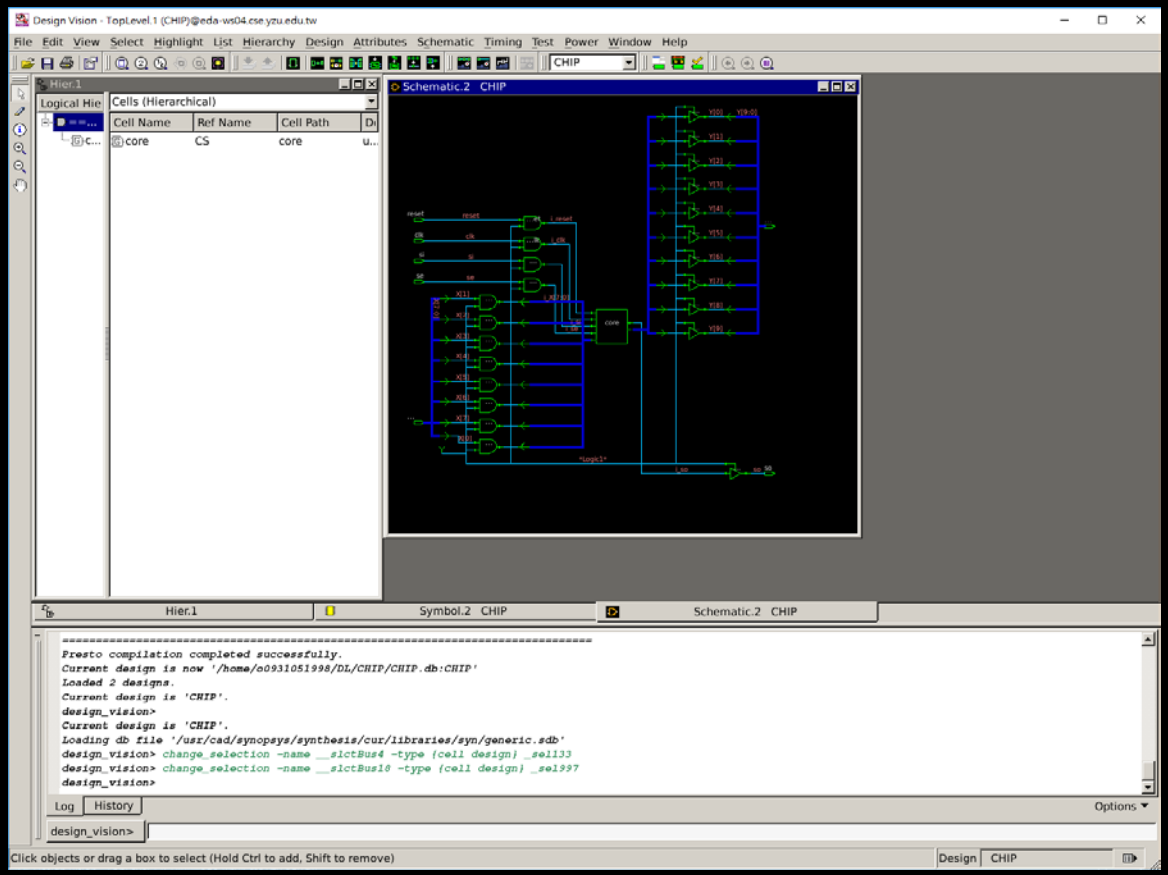


# Symbol View


Design Vision - TopLevel.1 (CHIP)@eda-ws04.cse.yzu.edu.tw
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
CHIP
Hier.1
Cells (Hierarchical)
Cell Name
Ref Name
Cell Path
core
CS
core
Symbol.4 CHIP
reset
clk
si
se
X[7:0]
CHIP
so
Y[9:0]
Hier.1
Symbol.4 CHIP
Presto compilation completed successfully.
Current design is now '/home/o0931051998/DL/CHIP/CHIP.db:CHIP'
Loaded 2 designs.
Current design is 'CHIP'.
design_vision>
Current design is 'CHIP'.
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'
Log
History
Options
design_vision>
Ready
Design
CHIP

# Schematic View

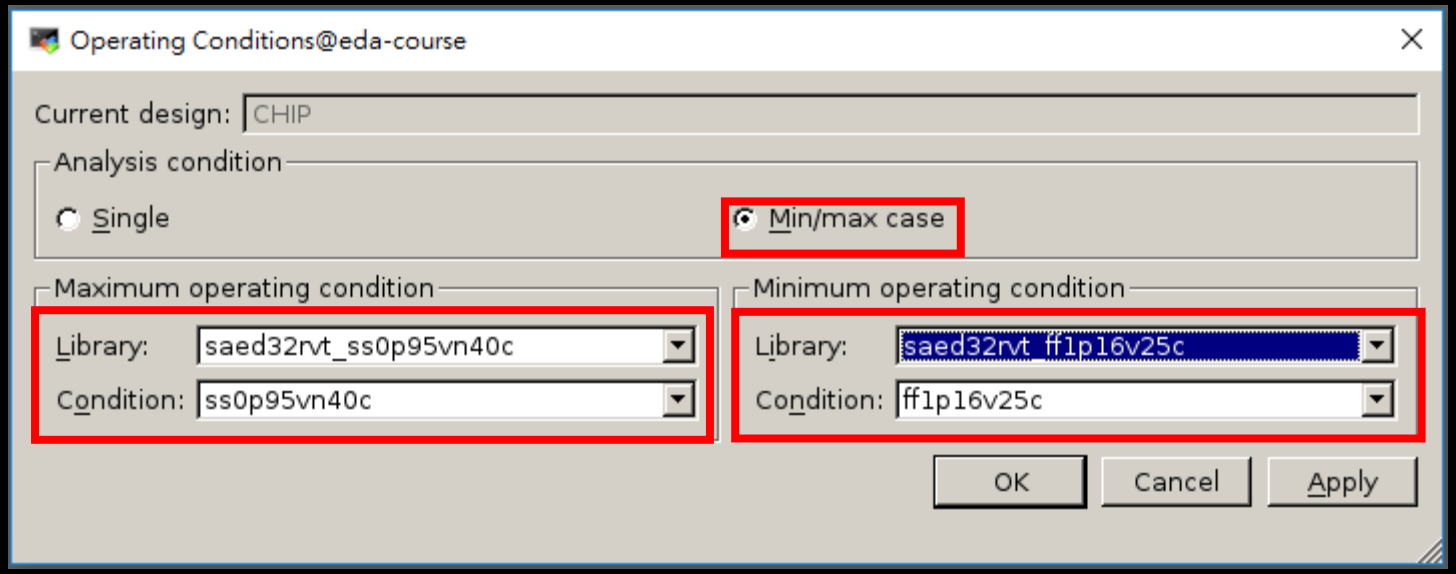
- Double click the symbol view



# Setting Operating Condition (1/2)

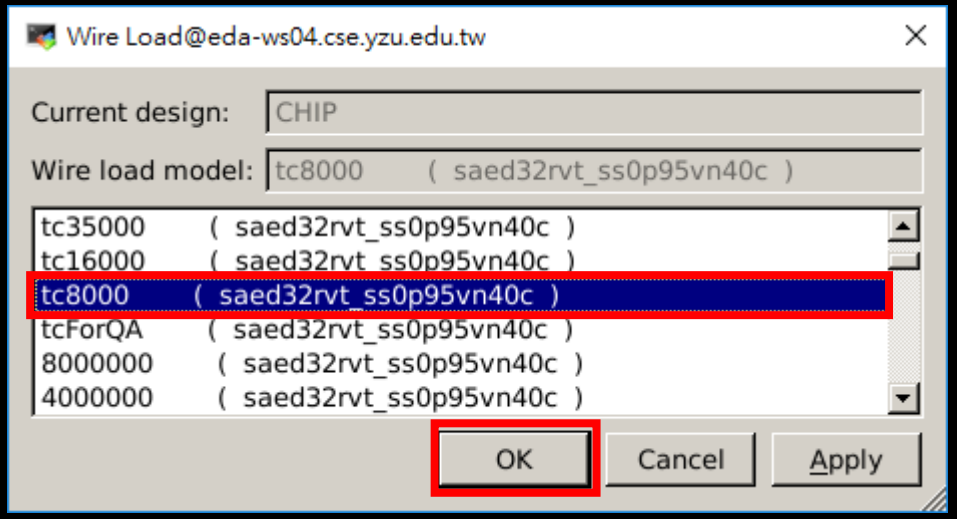
- **Attributes → Operating Environment → Operating Conditions**
- **Select “Min/max case”**
- **Set Maximum operating condition**
  - Library: select “saed32rvt_ss0p95vn40c”
  - Condition: select “ss0p95vn40c”
- **Set Minimum operating condition**
  - Library: select “saed32rvt_ff1p16v25c”
  - Condition: select “ff1p16v25c”

# Setting Operating Condition (2/2)



# Setting Wire Load

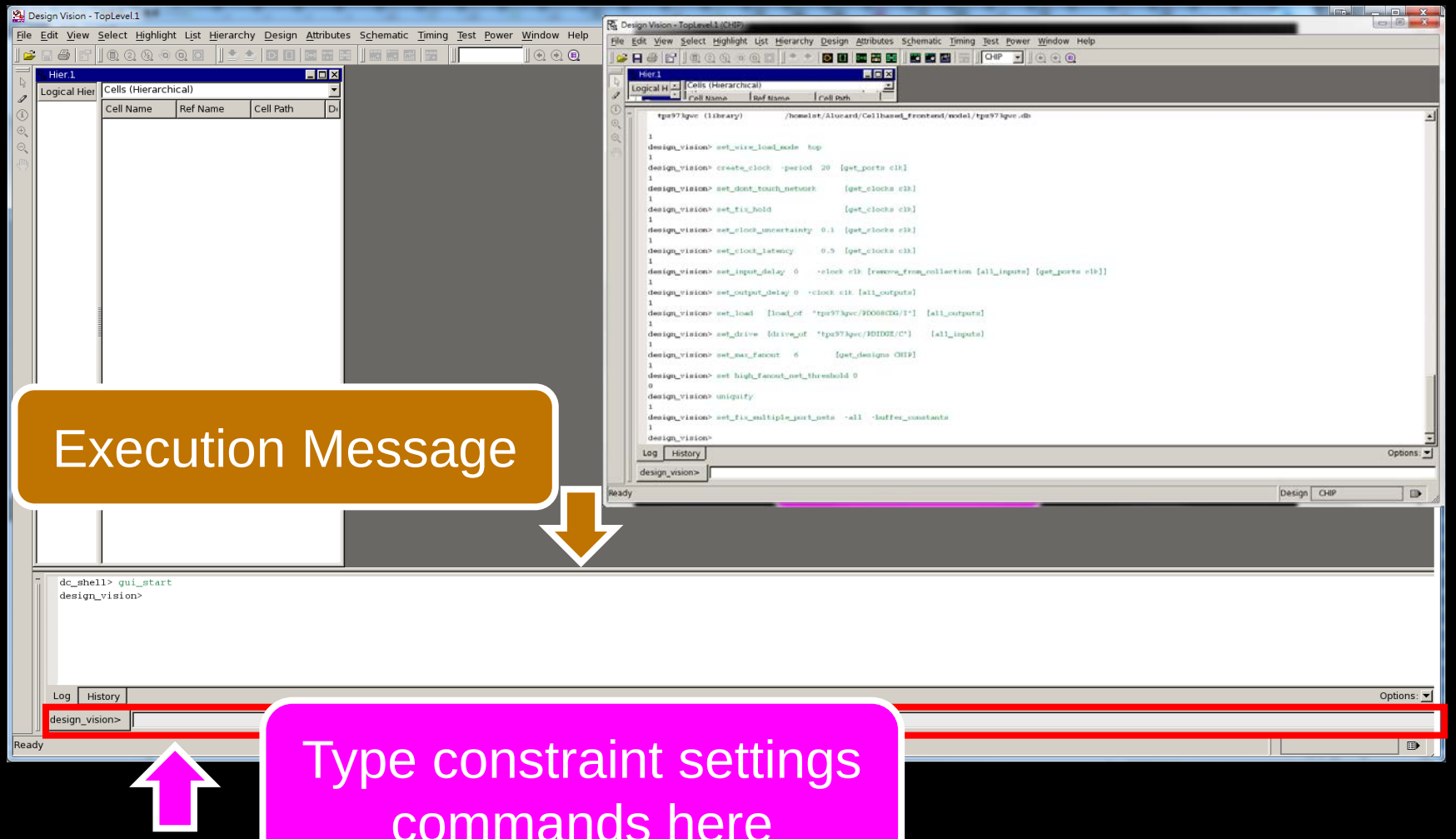
- Attributes → Operating Environment → Wire Load
- Select “tc8000 (saed32rvt_ss0p95vn40c)”



# Setup Constraints (Command)

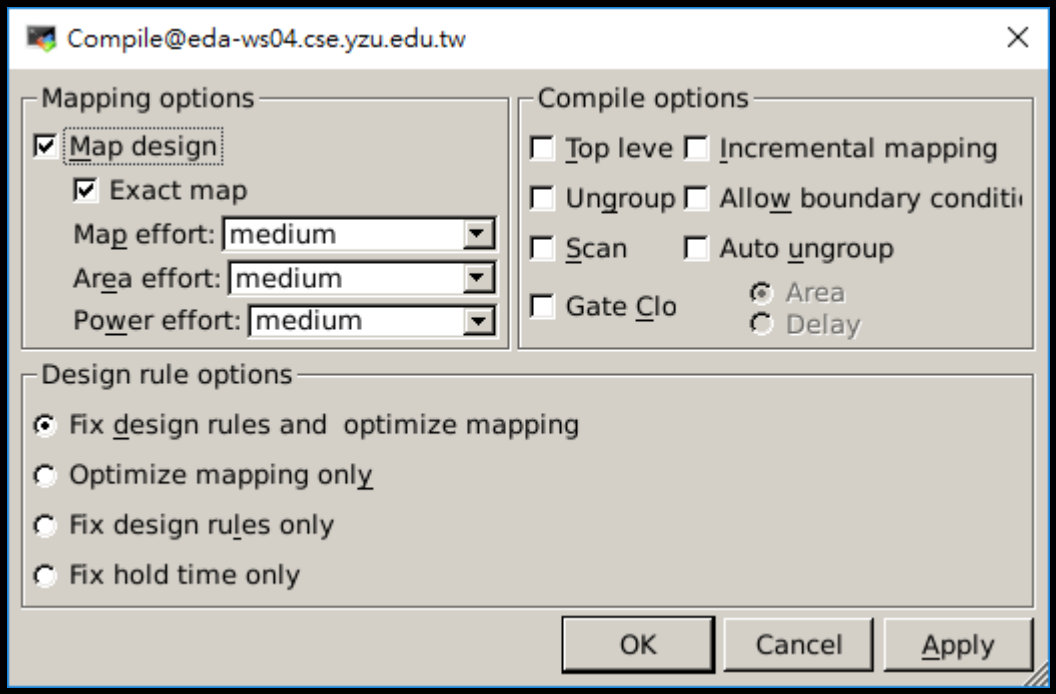
- **design_vision>**
  - current_design [get_designs CHIP]
  - link
  - set_wire_load_mode top
  - create_clock -period 20 [get_ports clk]
  - set_dont_touch_network [get_clocks clk]
  - set_fix_hold [get_clocks clk]
  - set_clock_uncertainty 0.1 [get_clocks clk]
  - set_clock_latency 0.5 [get_clocks clk]
  - set_input_delay 0 -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
  - set_output_delay 0 -clock clk [all_outputs]
  - set_load [load_of "saed32io_wb_ss0p95vn40c_2p25v/D8I1025_EW/DIN "] [all_outputs]
  - set_drive [drive_of "saed32io_wb_ss0p95vn40c_2p25v/I1025_NS/DOUT "] [all_inputs]
  - set_max_fanout 6 [get_designs CHIP]
  - set high_fanout_net_threshold 0
  - uniquify
  - set_fix_multiple_port_nets -all -buffer_constants

# How to Setup Constraints



# Compile Design

- **Optimizes and maps the current_design**
- **Design → Compile Design**
  - default

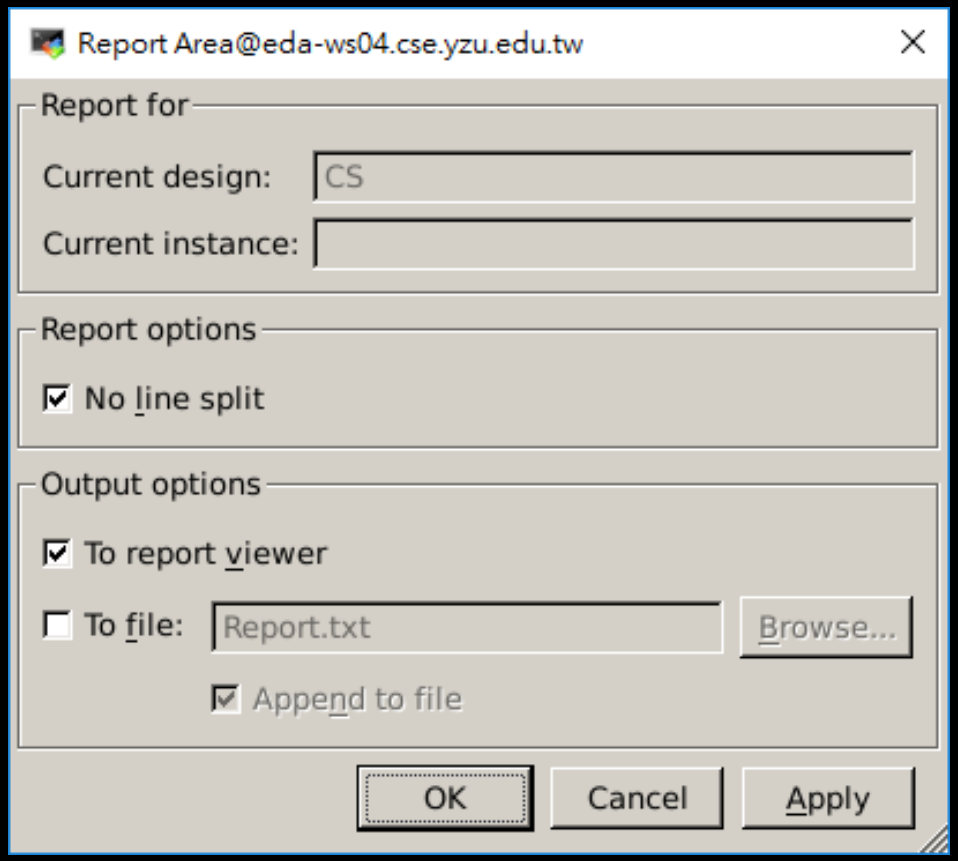


# Report Timing & Area

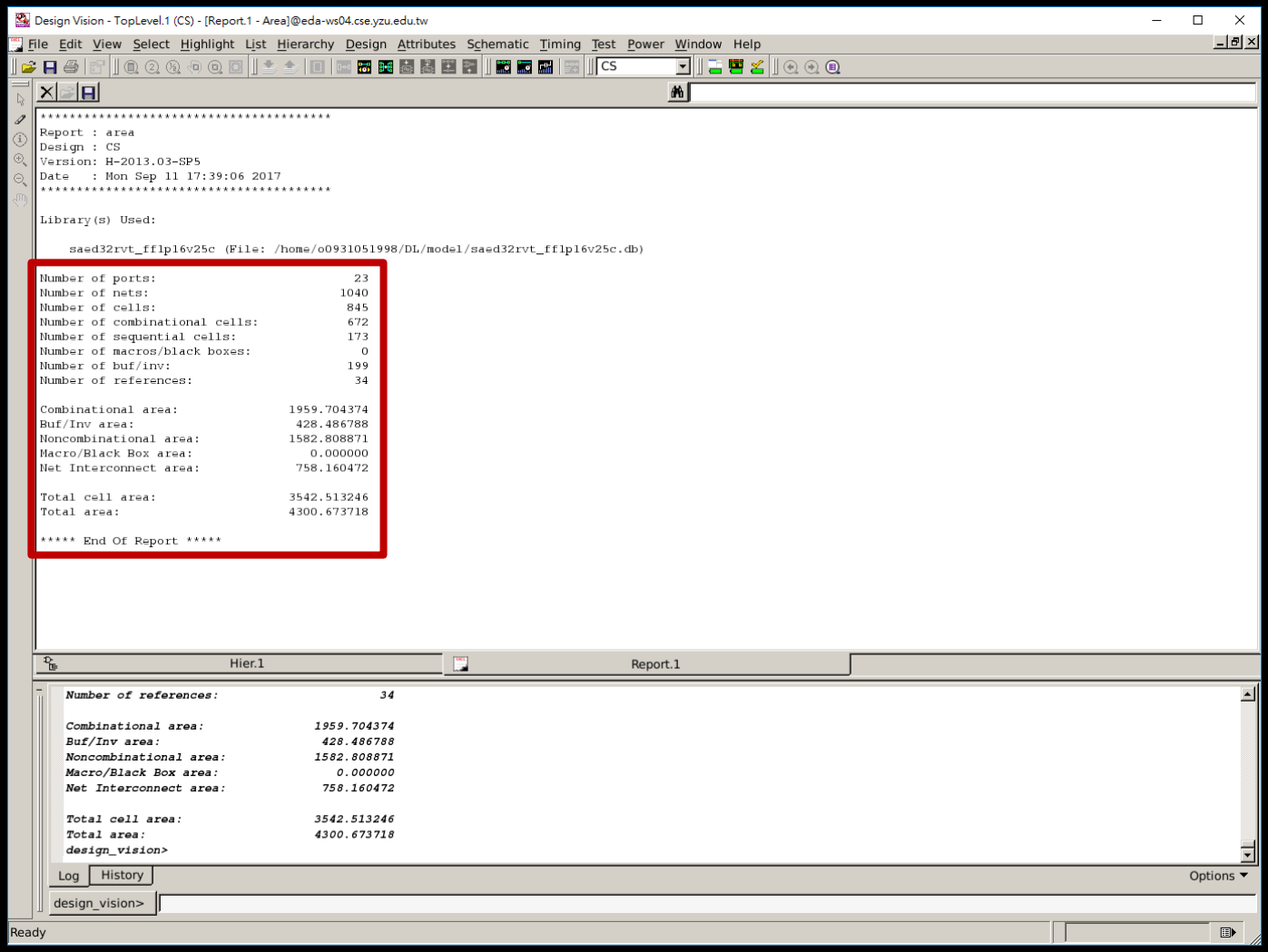
- **Report**
  - Area
  - Timing

# Report Area (1/2)

- **Design → Report Area → OK**

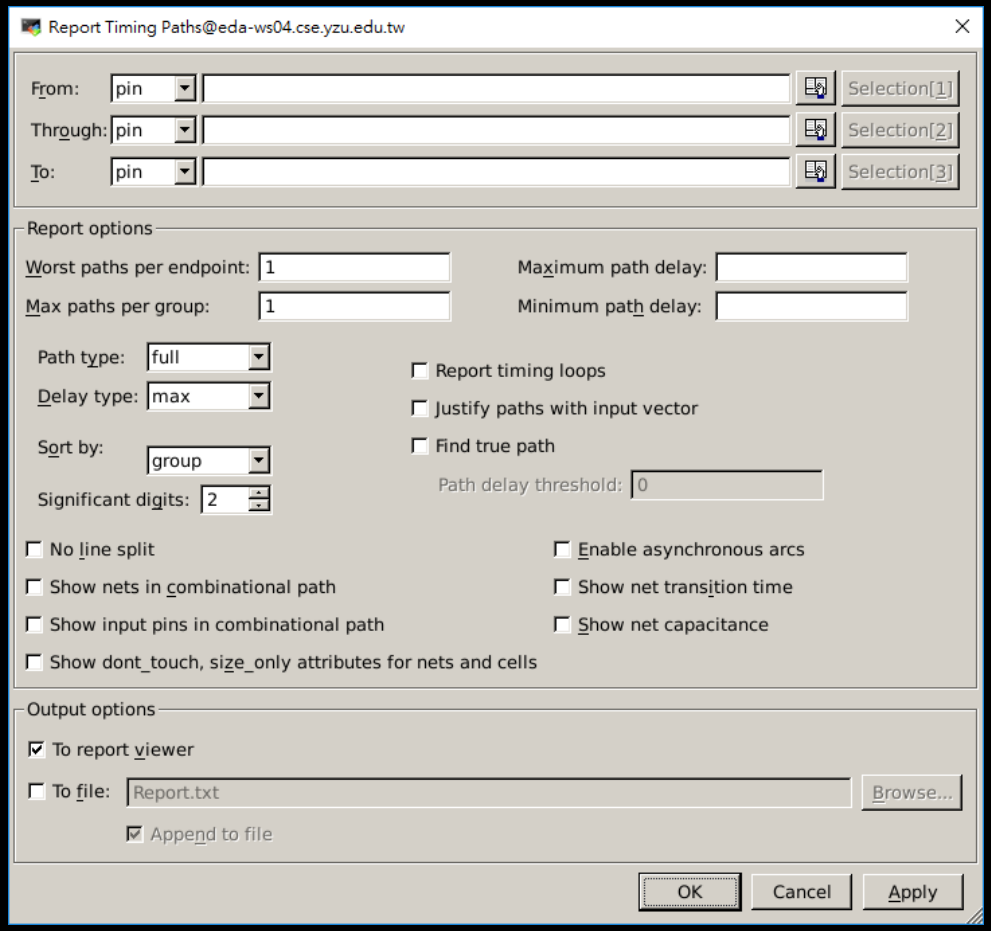


# Report Area (2/2)

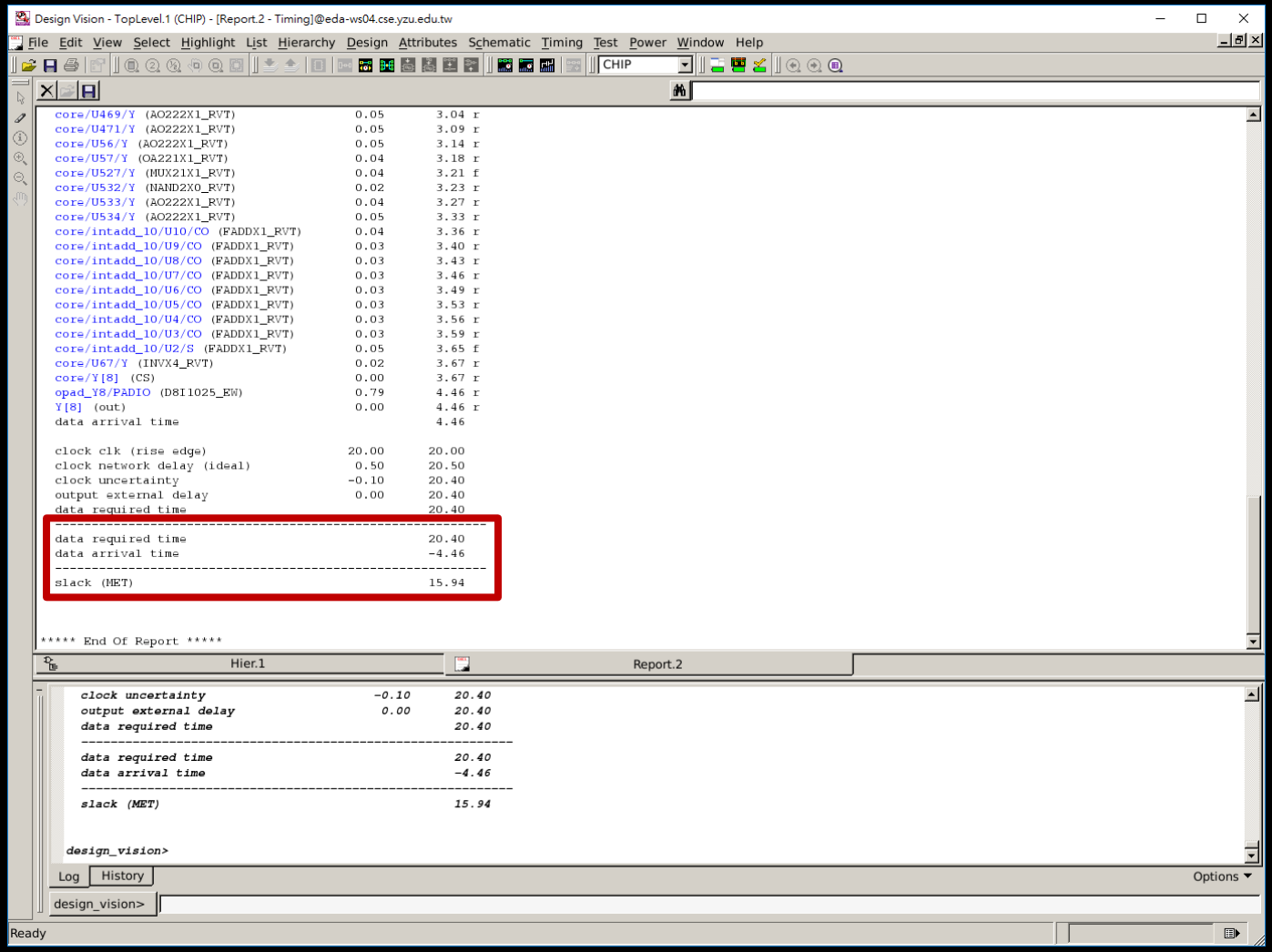


# Report Timing (1/2)

- Timing → Report Timing Path → OK



# Report Timing (2/2)



# Modify Timing Constrain

- **design_vision>**
  - create_clock -period 10 [get_ports clk]
- **Compile Design again and observe the difference.**
  - Tradeoff timing and area.
  - Let the SLACK MET.

# Save File – Gate-level Netlist

- **File → Save as**
  - Type the file_name (ex: CHIP_synth.v)
  - Choose Verilog as file format
- **design_vision>**
  - write_sdc -version 1.2 CHIP_synth.sdc

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# Create Test Protocol (1/2)

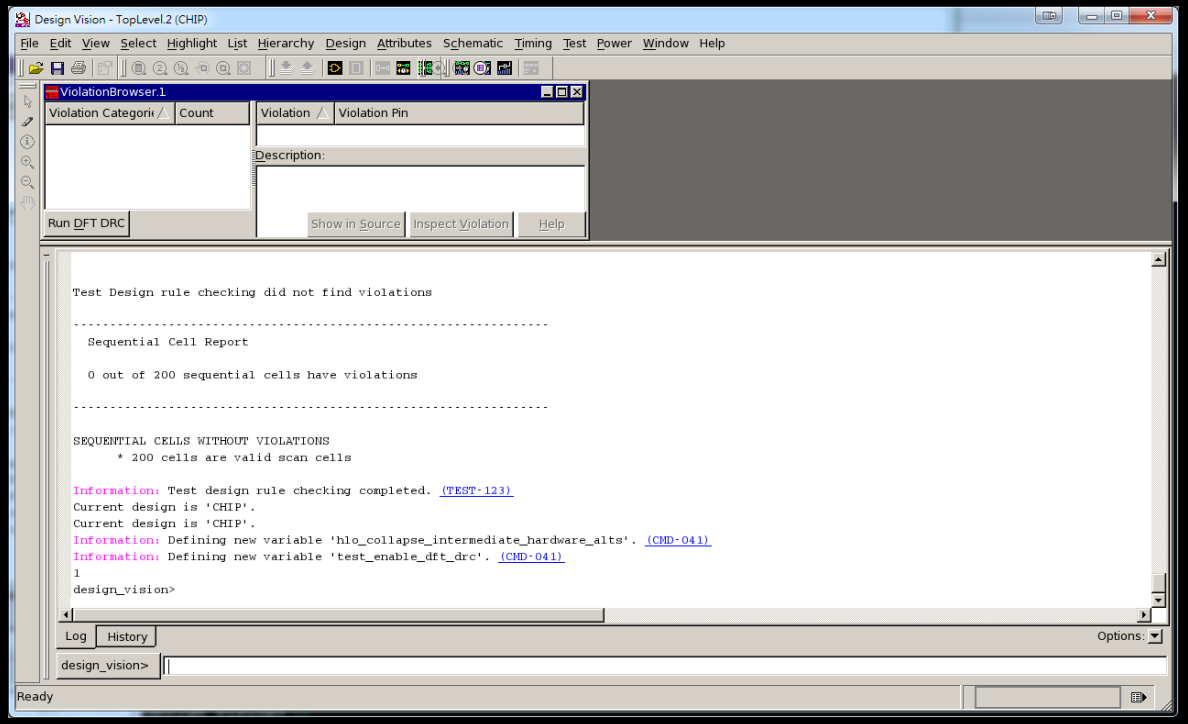
- **design_vision>**
  - current_design [get_designs CS]
  - set_scan_configuration -style multiplexed_flip_flop
  - set test_default_period 100
  - set_dft_signal -view existing_dft -type ScanClock -timing {45 55} -port clk
  - set_dft_signal -view existing -type Reset -active_state 1 -port reset
  - set_scan_configuration -chain_count 1
  - set_scan_configuration -clock_mixing no_mix
  - set_dft_signal -view spec -type ScanDataIn -port si

# Create Test Protocol (2/2)

- **design_vision>**
  - set_dft_signal -view spec -type ScanDataOut -port so
  - set_dft_signal -view spec -type ScanEnable -port se -active_stat 1
  - set_scan_path chain1 -scan_data_in si -scan_data_out so
  - create_test_protocol

# DFT Check (1/2)

- **Pre-DFT DRC**
- **Check scan design rule before scan chain synthesis**
- **design_vision>**
  - dft_drc



# DFT Check (2/2)

```
---------------------------------------------------------------
  DRC Report

  Total violations: 0

---------------------------------------------------------------


Test Design rule checking did not find violations

---------------------------------------------------------------
  Sequential Cell Report

  0 out of 200 sequential cells have violations

---------------------------------------------------------------

SEQUENTIAL CELLS WITHOUT VIOLATIONS
      * 200 cells are valid scan cells
```

# Scan Preview

- **Check scan-path consistency**
- **Determine the chain count**
- **Allocate and orders scan cells**
- **Add connecting hardware**
  - design_vision>
    - preview_dft -show all
    - preview_dft -test_points all

# Scan Preview Report

preview_dft –show all

```
Number of chains: 1
Scan methodology: full_scan
Scan style: multiplexed_flip_flop
Clock domain: no_mix
Scan enable: SE (no hookup pin)


Scan chain 'chain1' (SI --> SO) contains 200 cells



************ Test Point Plan Report ************
Total number of test points  : 0
Number of Autofix test points: 0
Number of Wrapper test points: 0
Number of test modes         : 0
Number of test point enables : 0
Number of data sources       : 0
Number of data sinks         : 0
************************************************

No test points.
```

# Scan Chain Synthesis

- **Scan replacement and insert test points**
- **Optimized the logic**
  - design_vision>
    - insert_dft

```
design_vision> insert_dft
Information: Starting test design rule checking. (TEST-222)
Test Design rule checking did not find violations
Information: Test design rule checking completed. (TEST-123)
  Architecting Scan Chains
  Routing Scan Chains
  Routing Global Signals
  Mapping New Logic
Resetting current test mode
  Beginning Mapping Optimizations
  -------------------------------

   ELAPSED            WORST NEG TOTAL NEG  DESIGN                              MIN DELAY
    TIME      AREA      SLACK     SLACK   RULE COST         ENDPOINT             COST
  --------- --------- --------- --------- --------- ------------------------- ---------


  Beginning Phase 1 Design Rule Fixing  (max_fanout)
  -----------------------------------

   ELAPSED            WORST NEG TOTAL NEG  DESIGN                              MIN DELAY
    TIME      AREA      SLACK     SLACK   RULE COST         ENDPOINT             COST
  --------- --------- --------- --------- --------- ------------------------- ---------
    0:09:12  376920.3      0.06       0.1     176.0 se                           0.00
    0:09:12  376920.3      0.06       0.1     176.0 se                           0.00
    0:09:12  376920.3      0.06       0.1     176.0 se                           0.00
    0:09:12  377635.9      0.06       0.1     158.0 net12986                     0.00
    0:09:12  377635.9      0.06       0.1     158.0 net12986                     0.00
    0:09:12  377635.9      0.06       0.1     158.0 net12986                     0.00
    0:09:12  378351.6      0.06       0.1     140.0 net12985                     0.00
    0:09:12  378351.6      0.06       0.1     140.0 net12985                     0.00
    0:09:12  378351.6      0.06       0.1     140.0 net12985                     0.00
    0:09:12  379067.2      0.06       0.1     122.0 net12984                     0.00
    0:09:12  379067.2      0.06       0.1     122.0 net12984                     0.00
    0:09:12  379067.2      0.06       0.1     122.0 net12984                     0.00
    0:09:12  379782.9      0.06       0.1     104.0 net12983                     0.00
    0:09:12  379782.9      0.06       0.1     104.0 net12983                     0.00
```

# Handoff Design

- **Report scan information**
  - design_vision>
    - report_scan_path -view existing_dft -chain all
    - report_scan_path -view existing_dft -cell all

- **Prepare TetraMax script**
  - design_vision>
    - change_names -hierarchy -rule verilog
    - write -format verilog -hierarchy -out CS_dft.v
    - write -format ddc -hierarchy -output CS.ddc
    - write_scan_def -output CS_scan.def
    - set test_stil_netlist_format verilog
    - write_test_protocol -output CS.spf

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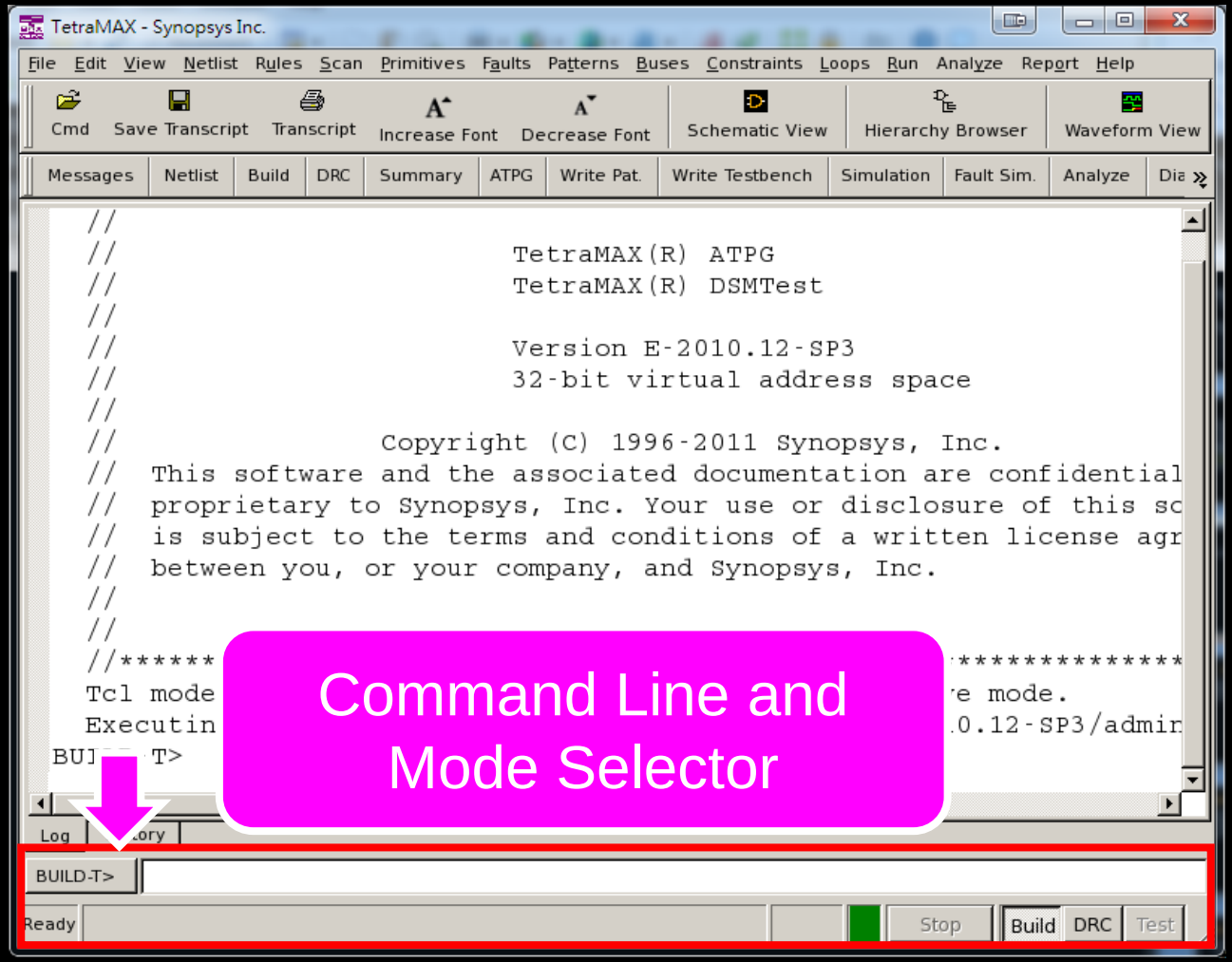
- **Fault Simulation with TetraMAX**

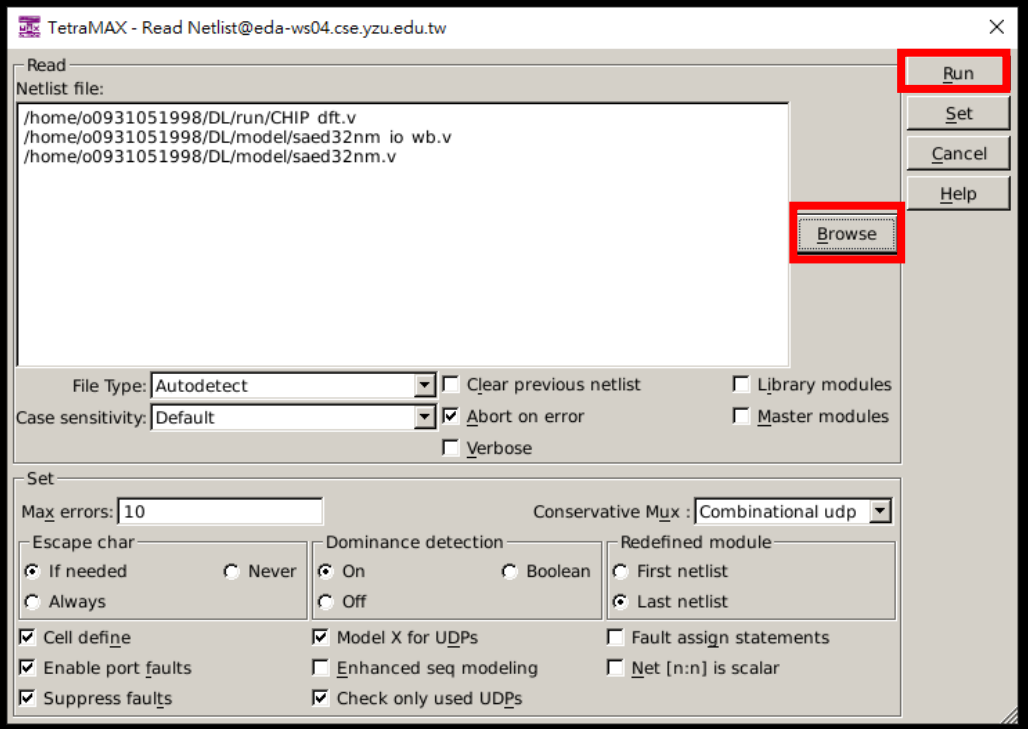
# TetraMAX Interface

- **$> tmax**



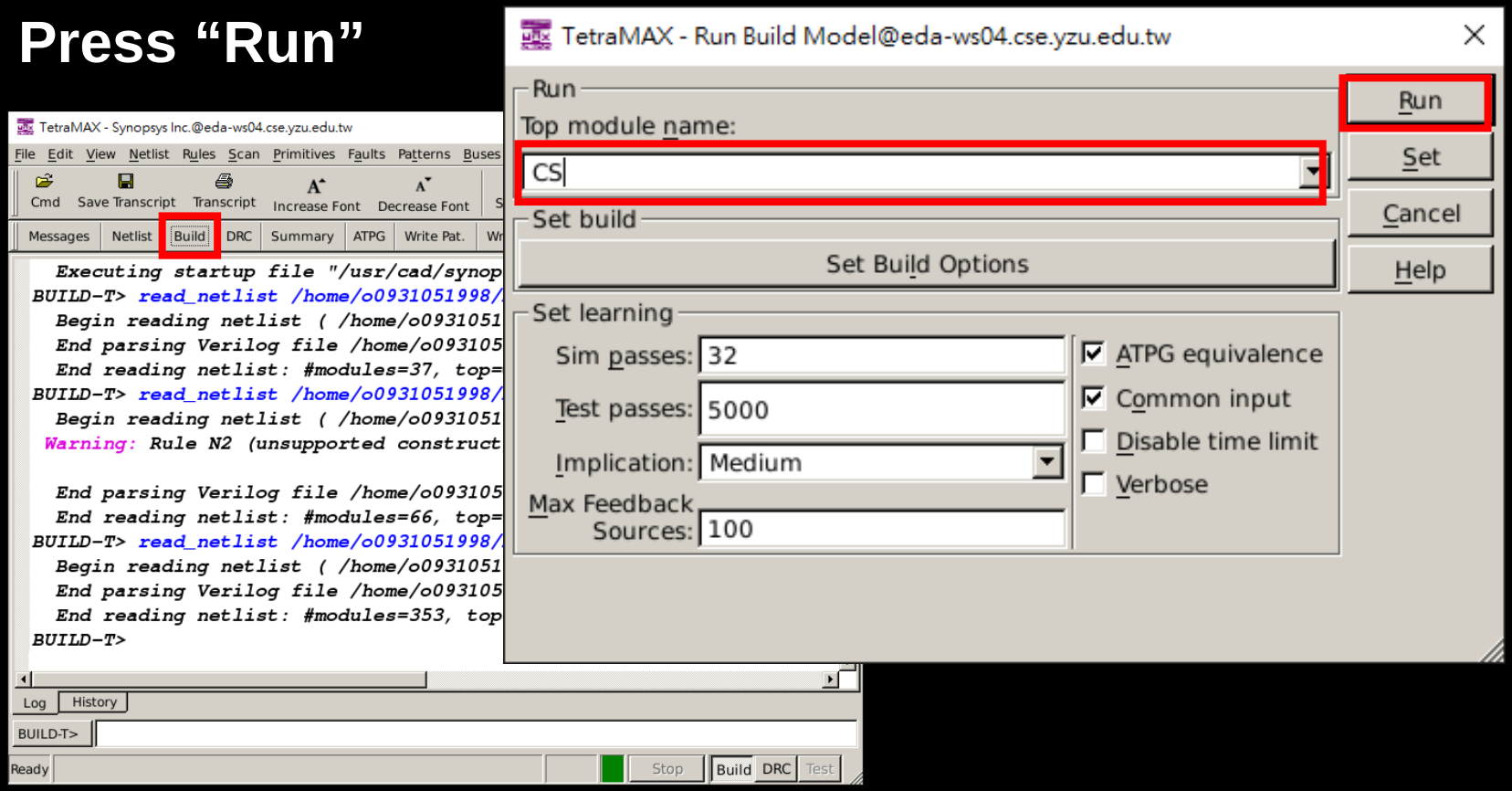
# Build Mode – Read Netlists

- Netlist → Read Netlist
- Click “Browse” →
  Select CS_dft.v & saed32nm_io_wb.v & saed32nm.v
- Press “Run”



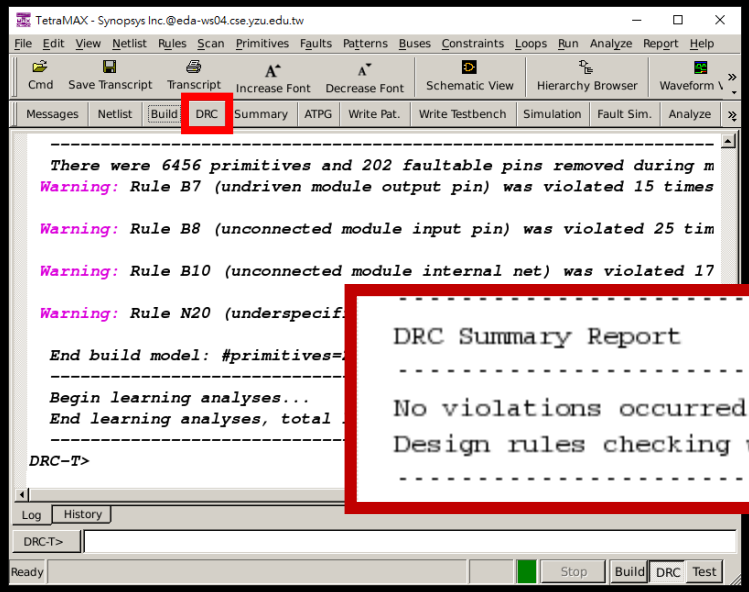
# Build Mode – Choose Top Module

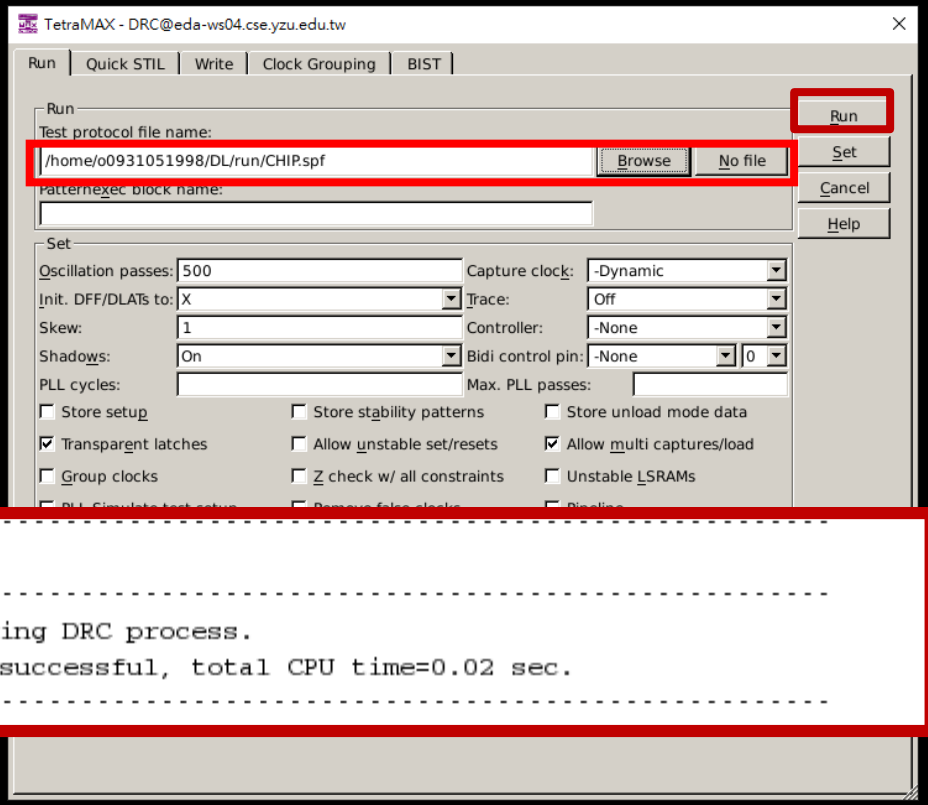
- Click “Build” on main window
- Top module name: Choose “**CS**”
- Press “Run”



# DRC Mode – Choose Test Protocol

- **Click “DRC” on main window**
- **Test protocol file name**
  - Click “Browse”
  - Choose “CS.spf”
- **Press “Run”**




```
DRC Summary Report
------------------------------------------------------------------------------
No violations occurred during DRC process.
Design rules checking was successful, total CPU time=0.02 sec.
------------------------------------------------------------------------------
```

# ATPG (1/3)

- **Populate the design with faults**
  - TEST>
    - add_faults -all
- **Generate ATPG Patterns**
  - TEST>
    - set_patterns -internal
    - run_atpg -auto
- **Report total faults, test pattern count, test coverage**
  - TEST>
    - report_summaries

# ATPG (2/3)

Uncollapsed Stuck Fault Summary Report

| fault class | code | #faults |
|---|---|---|
| Detected | DT | 14918 |
| Possibly detected | PT | 0 |
| Undetectable | UD | 28 |
| ATPG untestable | AU | 0 |
| Not detected | ND | 96 |
| total faults | | 15042 |
| test coverage | | 99.36% |

Pattern Summary Report

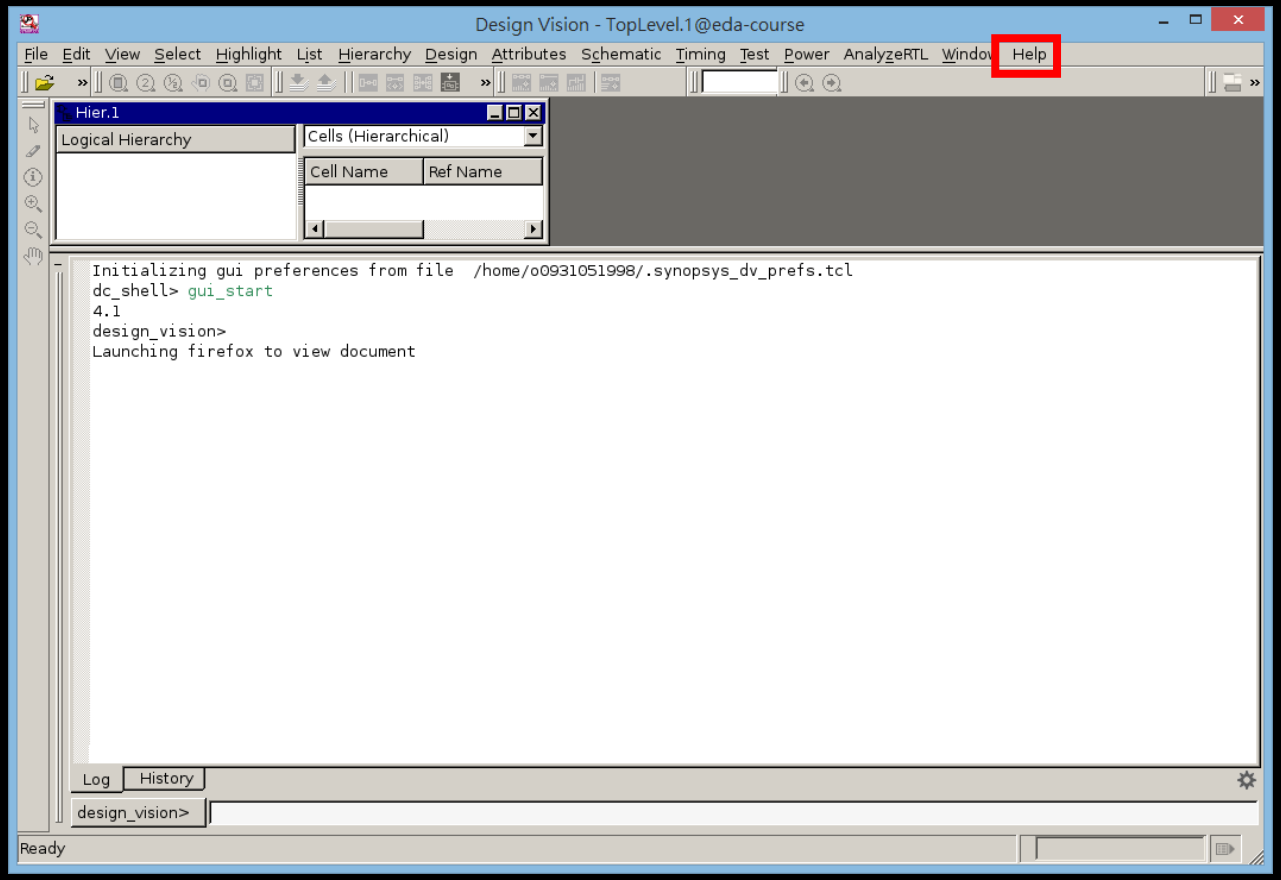
| | |
|---|---|
| #internal patterns | 342 |
| #basic_scan patterns | 342 |

# ATPG (3/3)

- **Saving ATPG Patterns**
  - TEST>
    - write_patterns CS_atpg.v -replace -internal -format stil -serial -vcs

# Help for Design Complier

- Man page, report hotkey bindings, online help



# Help for TetraMAX

- **Command summary, getting started, …**