Digital Logic Design Project 4 – CAD Placement and Route

Due: 23:55, Dec. 22, 2017

Cell-based IC design is a top-down approach to realize circuit implementations in register transfer level (RTL). After the completion of logic synthesis, design for testability (DFT) insertion, automatic test pattern generation (ATPG), and fault coverage simulation, automatic placement and route (APR) is performed to determine physical locations of all circuit components and to interconnect signals in the target design, respectively. In this lab, we are going to conduct cell-based back-end design flow for a small synthesized RTL design, "CHIP_synth.v", by using Synopsys IC Compiler.

Each team submits a tarball file (*.tgz or *.zip) including the following two files:

1- Final layout (CHIP.gds): 20 ns clock period [no DFT]
2- A detailed report (*.pdf) with the following parts:
   A. Describe cell-based back-end design flow
   B. Placement (result and timing report snapshots [0 interconnect delay])
   C. Routing (result, DRC result, and timing report snapshots)
   D. Overall discussion and your experience report
   E. [BONUS] Additional exploration of CAD tools is strongly encouraged