Digital Logic Design Project 1 – Verilog HDL

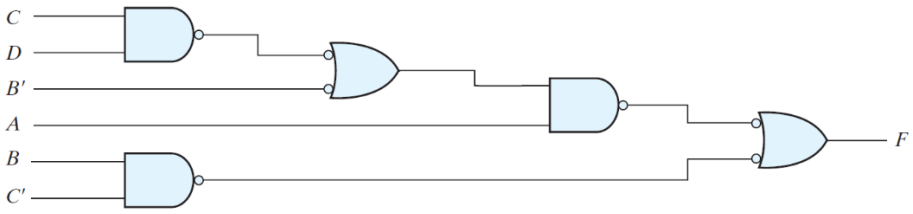
Due: 23:55, Nov. 10, 2017

Write a Verilog gate-level description of the following circuits and perform simulations to verify the correctness of your design. Note that the gate delay is mandatory in your simulation. You may define your own delay time of each logic gate. Please submit your report, which includes the following items, in PDF format:

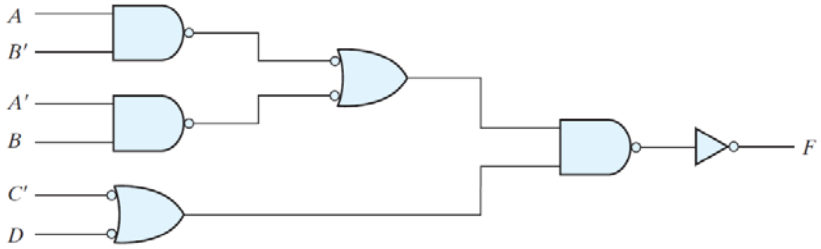
1- The Verilog module of your design.
2- The Verilog test bench to verify your design.
3- The simulation results.

There are 5 circuits below, you only need to complete one of them. Please take modulo 5 operation on your student ID and use the remainder as the index of your own design.

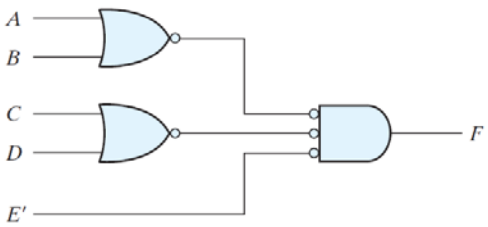
Circuit 0:



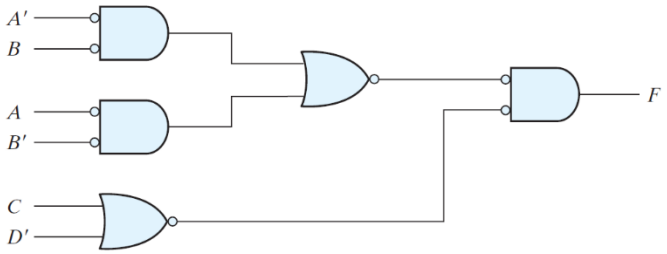
Circuit 1:



Circuit 2:



Circuit 3:



Circuit 4: