Digital Logic Design Project 3 – CAD Synthesis Flow

Due: 23:55, Dec. 8, 2017

Cell-based IC design is a top-down approach to realize circuit implementations from register transfer level (RTL). At the beginning, IC designer implement the target design by using hardware description language (HDL, e.g., Verilog and VHDL). Once the RTL code and pre-synthesis simulation are completed, logic synthesis, design for testability (DFT) insertion, automatic test pattern generation (ATPG), and fault coverage simulation are conducted to optimize target design in terms of area and delay before performing automatic placement and routing. In this lab, we are going to conduct cell-based front-end design flow for a small RTL design, "CHIP.v", by using two commercial tools, Synopsys Design Compiler and Synopsys TetraMAX ATPG.

Each team submits a tarball file (*.tgz or *.zip) including the following three files:

1- Final netlist (CHIP_synth.v): 20 ns clock period [no DFT]
2- Constraint file (CHIP_synth.sdc): 20 ns clock period [no DFT]
3- A detailed report (*.pdf) with the following parts:
   A. Describe cell-based front-end design flow
   B. Area and timing reports: both 20 ns and 10 ns clock periods [no DFT]
   C. Total faults, test pattern count, and test coverage: 20 ns clock period [DFT]
   D. Overall discussion and your experience report
   E. [BONUS] Additional exploration of CAD tools is strongly encouraged