

Digital Logic Design Project 2 – Verilog HDL

Due: 23:55, Dec. 1, 2017

Write a Verilog behavioral description of an eight-bit arithmetic logic unit (ALU) and perform simulations to verify the correctness of your design. The circuit has a three-bit select bus (Sel), two eight-bit input datapaths (A[7:0] and B[7:0]), and one eight-bit output datapath (y[7:0]). The circuit module performs the arithmetic and logic operations listed below.

Sel	Operation	Description
000	$y = 8'b0$	Minimum value
001	$y = A \& B$	Bitwise AND
010	$y = A B$	Bitwise OR
011	$y = A \wedge B$	Bitwise exclusive OR
100	$y = \sim A$	Bitwise complement
101	$y = A - B$	Subtract
110	$y = A + B$	Add (Assume A and B are unsigned)
111	$y = 8'hFF$	Maximum value

Please submit your report, which includes the following items, in PDF format:

- 1- The Verilog module of your design.
- 2- The Verilog test bench to verify your design.
 - a. Use \$dumpvars system task for visualized waveform
 - b. Use \$display/\$write system tasks
 - c. Use \$monitor system task
 - d. Use \$time system task
- 3- The simulation results.