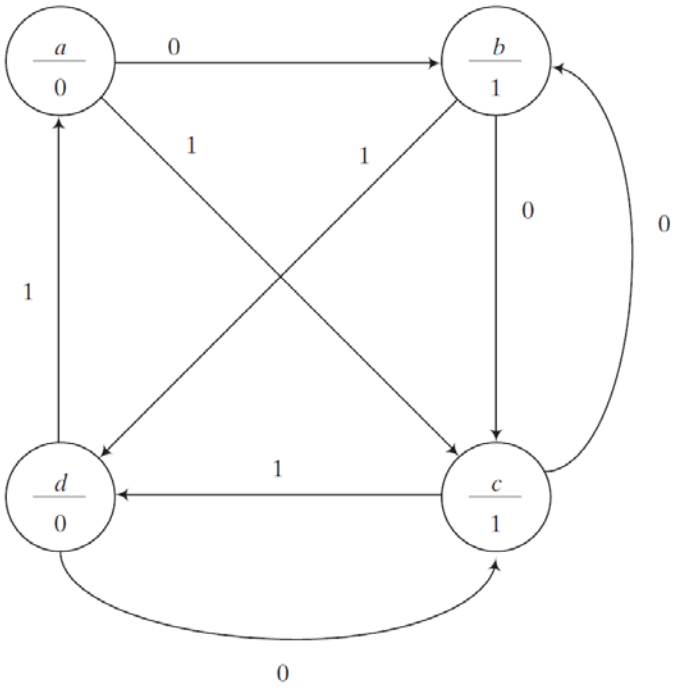
Digital Logic Design Project 3 – Verilog HDL

Due: 23:55, Jan. 7, 2018

Write a Verilog behavioral description of the Moore FSM described by the following figure and perform simulations to verify the correctness of your design. There are 4 states (a, b, c, and d) in the circuit. The circuit has a one-bit input and a one-bit output.



Please submit your report, which includes the following items, in PDF format:

1- The Verilog module of your design.
2- The Verilog test bench to verify your design.
   a. Use $dumpvars system task for visualized waveform
3- The simulation results.