

William Yoon

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Education

Cornell University, B.S. in Electrical and Computer Engineering	GPA: 3.41/4.0	<i>Expected Dec 2024</i>
Cornell University, M.E. in Electrical and Computer Engineering	GPA: 3.75/4.0	<i>Expected May 2025</i>
<ul style="list-style-type: none">• Relevant Courses: Computer Architecture, High-Level Digital Design Automation, Microcontrollers, Computer Networks & Telecommunications, Embedded Systems, Data Structures & Functional Programming, Digital Logic• Teaching Assistant: Computer Architecture, Embedded Systems, Computer Networks & Telecommunications		

Experience

Amazon Web Services (AWS)	Seattle, WA
<i>Software Development Engineer Intern</i>	<i>May 2024 – August 2024</i>
<ul style="list-style-type: none">• Developed an automated ticket processing bot capable of deriving CloudWatch query links, retrieving alarm information, and producing retrieval-augmented generated (RAG) based solutions from Canary Test failures• Designed the bot's integrated workflow/infra: SNS, SQS, Lambda, CloudWatch, Bedrock, DynamoDB, and IAM• Reduced on-call team's ticket triaging and investigation labor costs, with estimated savings of 3-5 hours per week	
Qualcomm	San Diego, CA
<i>Software Engineering Intern</i>	<i>May 2023 – August 2023</i>
<ul style="list-style-type: none">• Implemented a Dockerfile static/dynamic parser that is capable of deriving knowable configuration values, interpolating statements based on user input, and accounting for warnings through test driven development• Generated a custom unit testing repository to validate an internal lossless image format, detecting 2 major issues	
Cornell Zhang Research Group	Ithaca, NY
<i>Research Assistant</i>	<i>January 2023 – Present</i>
<ul style="list-style-type: none">• Created unit tests to verify the source location of math, operation, and logic functions within Allo, a python-based programming infrastructure that provides an abstraction for hardware compilation using an MLIR compiler• Integrated a butterfly FFT algorithm using Allo and utilized optimization techniques to minimize latency by 70x	
Cornell University Autonomous Underwater Vehicle	Ithaca, NY
<i>Electrical Subteam Member</i>	<i>October 2021 – Present</i>
<ul style="list-style-type: none">• Designed, populated, and programmed an LED circuit board that utilizes two RGBW LED strips and the RS-232 serial communication protocol to indicate vehicle pressure and levelness• Added a fourth transducer to allow elevation readings and optimized the signal integrity of a hydrophone board	

Projects

Microservices-Based Network Monitoring Platform - (Gem5, Service Weaver, Go, Python)
<ul style="list-style-type: none">• Deployed a simplified model for monitoring load generated network calls on x86 systems simulated by Gem5• Employed Service Weaver to create microservices that gather performance metrics like latency, packet loss, and throughput, to automate an RPC communication stack, and to eventually find hardware performance bottlenecks
Keyword Spotting Inference Acceleration - (C++, Vivado)
<ul style="list-style-type: none">• Integrated a 16-layer keyword spotting convolution neural network onto a Zedboard and utilized HLS optimization techniques, such as loop tiling, pipelining, and array reshaping, to speed-up latency by 290x
Catching Lightning in an IMU - (C)
<ul style="list-style-type: none">• Generated an on-lattice diffusion limited aggregation program using the RP2040 and an IMU that is capable of using hand motions to speed-up and tilt over 7000 pixels, displaying natural processes like snowflake formations• Circuit Cellar Publication: circuitcellar.com/article-materials-and-resources/november-issue-412-circuit-cellar-2/

Skills

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- **Languages:** C, C++, Python, Docker, CUDA, System Verilog, Verilog, Java, TypeScript, JavaScript, OCaml, Go
 - **Programs:** PCB Schematic Design (KiCad), LTspice XVII, Quartus, ModelSim, Vivado, Gem5, ServiceWeaver