Progetto di Reti Logiche

William Zeni
matricola 10613915

Cristina Urso
matricola 10599689

30 aprile 2021

Sommario

Progetto sostenuto presso il Politecnico di Milano, diretto dal professor Gianluca Palermo nell'anno 2021.

1 introduction

1.1 Scopo del progetto

Write somenthing here

1.2 Specifiche generali

Write somenthing here

1.3 Interfaccia del componente

Write somenthing here

1.4 Dati e Descrizione memoria

Write somenthing here

2 Desing Pattern

2.1 Scelte Progettuali

Write somenthing here

2.2 Descrizione degli Stati

2.2.1 START

Write somenthing here

2.2.2 INIT

Write somenthing here

2.2.3 ABILIT READ

Write somenthing here

2.2.4 ABILIT WRITE

Write somenthing here

2.2.5 WAIT MEM

Write something here

2.2.6 GET RC

Write something here

2.2.7 GET DIM

Write something here

2.2.8 READ PIXEL

Write something here

2.2.9 GET MINMAX

Write something here

2.2.10 GET DELTA

Write something here

2.2.11 CALC SHIFT

Write something here

2.2.12 GET PIXEL

Write something here

2.2.13 CALC NEWPIXEL

Write something here

2.2.14 WRITE PIXEL

Write something here

2.2.15 DONE

Write something here

2.2.16 WAITINGPIC

Write something here

3 Risultati dei Test

Write something here

4 Conclusioni

Write something here