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Office Hours: Fridays: 10:00 AM - 1:00 PM ( online support )

Office Room: online

I. Course Prefix / Number: CSC 204

Course Name: Computer Architecture and Organization

Credits: 3 ( 3 lecture; 1 lab )

II. PREREQUISITE:

Recommended CSC 155 or higher - numbered CSC course or instructor's consent.

III. COURSE (CATALOG) DESCRIPTION:

A survey of the various levels of hierarchical computer architecture and design. The analysis of internal and external memory models, busses, I/O peripherals, CISC and RISC processor strategies are covered. Additional topics include the instruction formats and addressing schemes of microprocessors such as Intel Pentium and Power PC architectures, vectorizing multiprocessors and multicomputer systems.

IV. LEARNING OBJECTIVES:

A. Review the historical development of computers and computer architectures.

B. Understand information representation, error detection/correction schemes and digital logic.

C. Identify the basic components of computer organization and understand how they work together.

D. Learn the format of instruction sets and the operation of the instruction cycle.

E. Survey the hierarchical internal and external memory organization strategies.

F. Recognize current superscalar microprocessor and multiprocessor models in today's market.

V. ACADEMIC INTEGRITY AND STUDENT CONDUCT:

Students and employees at Oakton Community College are required to demonstrate academic integrity and follow Oakton’s Code of Academic Conduct. This code prohibits:

• cheating,

• plagiarism (turning in work not written by you, or lacking proper citation),

• falsification and fabrication (lying or distorting the truth),

• helping others to cheat,

• unauthorized changes on official documents,

• pretending to be someone else or having someone else pretend to be you,

• making or accepting bribes, special favors, or threats, and

• any other behavior that violates academic integrity.

There are serious consequences to violations of the academic integrity policy. Oakton’s policies and procedures provide students a fair hearing if a complaint is made against you. If you are found to have violated the policy, the minimum penalty is failure on the assignment and, a disciplinary record will be established and kept on file in the office of the Vice President for Student Affairs for a period of 3 years.

Please review the Code of Academic Conduct and the Code of Student Conduct, both located online at: [www.oakton.edu/studentlife/student-handbook.pdf](http://www.oakton.edu/studentlife/student-handbook.pdf)

VI. OUTLINE OF TOPICS:

A. Background and Introductions

1. performance metrics

2. arithmetic representation

a. integer

b. floating point

B. Organization of Computer Systems

1. bus strategies

2. internal memory and cache hierarchies

3. external memory

a. disk

b. tape

4. I / O channels and processors

C. CPU Components

1. register organization

a. RISC / CISC strategies

2. pipeline/superscalar processors

3. instruction sets and addressing formats

D. Current Architectures

1. commodity microprocessors

a. Intel

b. Power PC

2. multiprocessors

3. multicomputers

VII. METHODS OF INSTRUCTION:

Lectures, class discussion, individual and group projects, and use of a computer laboratory.

All of the supplementary course documentation can be found from the Content link via D2L. Your D2L login is the same as your Oakton login.

The D2L login is here: [**https://d2l.oakton.edu**](https://d2l.oakton.edu)

All of the work to be submitted for a grade is placed into an appropriate Dropbox folder via D2L.

VIII. COURSE PRACTICES REQUIRED:

Reading of the text is required for a solid understanding of the material. Use of a computer laboratory is necessary to learn the design of software and practice programming.

IX. INSTRUCTIONAL MATERIALS:

Required Textbook:

The Essentials of Computer Organization and Architecture, Enhanced Fourth Edition by Null and Lobur, Jones & Bartlett Learning, 2015 ISBN: 9781284074482

Supplemental ePDF:

An Introduction to MIPS Assembly Language to Accompany The Essentials of Computer Organization and Architecture, ISBN: 9781284120936

X. METHODS OF EVALUATING STUDENT PROGRESS:

Quizzes, written homework, computer assignments, major examinations and a final examination will be used.

Grading Scale: 100 % to 90 % is an A , 89 % to 80 % is a B , 79 % to 70 % is a C , 69 % to 60 % is a D and 59 % to 0 % is an F .

Grade Determination: Your final course grade will be based on the following:

Homework 15 % , Quizzes 15 % , Unit Exams 20 % , Lab Projects 30 % , Final Exam 20 % .

Late submission policy: a deduction of up to 20 % of an assignment score may be applied for late submittal of assignments.

XI. OTHER COURSE INFORMATION:

DISABILITIES

If you have a documented learning, psychological, or physical disability you may be entitled to reasonable academic accommodations or services. To request accommodations or services, contact the Access and Disability Resource Center at the Des Plaines or Skokie campus. All students are expected to fulfill essential course requirements. The College will not waive any essential skill or requirement of a course or degree program.

Oakton Community College is committed to maintaining a campus environment emphasizing the dignity and worth of all members of the community, and complies with all federal and state Title IX requirements.

Resources and support for

• pregnancy-related and parenting accommodations; and

• victims of sexual misconduct

can be found at: [www.oakton.edu/title9](http://www.oakton.edu/title9)

Resources and support for LGBTQ+ students can be found at: [www.oakton.edu/lgbtq](http://www.oakton.edu/lgbtq)

Additional Items of Note:  
  
(a) You are responsible for any classes that you miss. Have telephone numbers of others in the class; get assignments, notes, deadlines etc. from them.   
  
(b) Changes to this syllabus may be made when deemed appropriate and without notice.

(c) Tutors are available by appointment in room DP 2400 .

(d) Points will be deducted on assignments that are submitted past the due date.

(e) Bulk assignment submissions will not be accepted.

(f) Use of smartphone devices for non - emergency purposes, during the lecture / lab sessions, is prohibited.

(g) Laptop / computer use during classroom lecture time is to be restricted to related course materials and / or Web sites. Completion of homework or lab assignments during the class lectures is not allowed.

**Tentative Weekly Outline of Course Topics**

|  |  |  |
| --- | --- | --- |
| **Week** | **Chapter(S)** | **Key Topics** |
|  |  |  |
| 1 | 1 | Components, Hierarchy and History of a Computer |
| 2 | 2 | Number Systems: integers, floating - point standard, character codes |
| 2 | 3 | Boolean Algebra and Digital Logic including K - Maps |
| 3 | 4 | CPU Organization, System Bus, Clocks, Instruction Processing, Intel and MIPS Architectures |
| 4 | 5 | Instruction Formats, Instruction Types, MARIE, Intel and MIPS Instruction Sets |
| 5 | 6 | Cache Memory, Virtual Memory: paging, segmentation |
| 6 | 7 | Input / Output |
| 7 | 8 | Java Virtual Machine |
| 7 | 9 | RISC Machines, Parallel and Multiprocessor Architectures, Parallel Processing |
| 8 | 11 | Benchmarking |

**Tentative Course Topic Reading Schedule**

|  |  |  |
| --- | --- | --- |
| **Week** | **Chapter** | **Subject** |
| **1** | **Chapter 1** | **Introduction** |
| **1** | **Chapter 2** | **Data Representation in Computer Systems** |
| **2** | **Chapter 3** | **Boolean Algebra and Digital Logic** |
| **3** | **Chapter 4** | **MARIE: An Introduction to a Simple Computer** |
| **3** | **Chapter 5** | **A Closer Look at Instruction Set Architecture** |
| **4** | **Chapter 6** | **Memory** |
| **5** | **Chapter 7** | **Input / Output and Storage Systems** |
| **5** | **Chapter 8** | **System Software** |
| **6** | **Chapter 9** | **Alternative Architectures** |
| **6** | **Chapter 10** | **Topics in Embedded Systems** |
| **7** | **Chapter 11** | **Performance Measurement and Analysis** |
| **7** | **Chapter 12** | **Network Organization and Architecture** |
| **8** | **Chapter 13** | **Selected Storage Systems and Interfaces** |
| **8** | **Appendix A** | **Data Structures and the Computer** |