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| Instructor |  | Due Date |  |

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| Part | **1** | **2** | **3** | **4** | Total |
| *Maximum Points* | **25** points | **25** points | **25** points | **25** points | **100**G101010 pointsG |
| ***Your Score*** |  |  |  |  |  |

**Textbook Reading Assignment**

Thoroughly read Chapter(s) 6 in your Computer Architecture and Organization textbook.

**Part 1 Glossary Terms - Computer Memory**

Define, in detail, each of these glossary terms from the realm of computer architecture and computer topics, in general. If applicable, use examples to support your definitions. Consult your notes

or course textbook(s) as references or the Internet by visiting Web sites such as:

[**http://www.ask.com**](http://www.ask.com) or [**http://www.webopedia.com**](http://www.webopedia.com/)

**(a) Associative Memory**

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**(b) EPROM**

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**(c) EPROM**

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**(d) Memory Hierarchy**

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**(e) Virtual Memory**

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**Part 2 Exercises - Computer Memory**

For each of the following, enter True or False.

\_\_\_\_\_ **(1)** All cache mapping schemes require a main memory address to have an offset field.

\_\_\_\_\_ **(2)** It is important to know if a computer is byte or word addressable because we need to know how many addresses are contained in main memory, cache and in each block when doing cache mapping.

\_\_\_\_\_ **(3)** Caching breaks down when programs exhibit good locality.

\_\_\_\_\_ **(4)** The two types of cache write policies are write - through and write - back.

\_\_\_\_\_ **(5)** A unified cache is a cache that holds both data and instructions.

\_\_\_\_\_ **(6)** When a computer uses paging, there must be a page table for every process.

\_\_\_\_\_ **(7)** Memory segmentation can result in internal fragmentation, while paging can result in external fragmentation.

\_\_\_\_\_ **(8)** Assuming an 8 - bit virtual address with pages of 32 bytes, the virtual address format is 5 bits for the page and 3 bits for the offset.

\_\_\_\_\_ **(9)** Cache replacement policies are necessary to determine which block in cache should be the victim block.

\_\_\_\_\_ **(10)** Information can be retrieved fastest from a hard disk as compared to magnetic tapes, optical disks and USB flash drives.

**Part 3 Exercises - Computer Memory**

**(1)** Suppose we have a byte - addressable computer using direct mapping with 16 - bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

**(2)** Suppose we have a byte - addressable computer using direct mapping with 16 - bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

**(3)** Suppose we have a byte - addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

**(4)** Consider a byte - addressable computer with 24 - bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24 - bit memory address if the computer uses 4 - way set associative mapping.

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| --- | --- | --- |
| Tag | Set | Offset |
| ? | ? | ? |

**(5)** Consider a byte - addressable computer with 24 - bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24 - bit memory address if the computer uses direct mapping.

|  |  |  |
| --- | --- | --- |
| Tag | Set | Offset |
| ? | ? | ? |

**Part 4 Exercises - Computer Memory**

Write a complete answer for each of these.

**(1)** Does a TLB miss always indicate that a page is missing from memory?   
 Explain your answer.

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**(2)** If you are a computer builder trying to make your system as price - competitive as possible, what features and organization would you select for its memory hierarchy?

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**(3)** If you are a computer buyer trying to get the best performance from a system, what features would you look for in its memory hierarchy?

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**(4)** Name two ways that, as a programmer, you can improve cache performance.

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**(5)** Look up a specific vendor’s specifications for memory and report the memory access time, cache access time and cache hit rate ( and any other data the vendor provides ) .

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