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| Instructor | ***Luke Papademas*** | Due Date | **6/30** |

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| Part | **1** | **2** | **3** | **4** | Total |
| *Maximum Points* | **25** points | **25** points | **25** points | **25** points | **100**G101010 pointsG |
| ***Your Score*** |  |  |  |  |  |

**Textbook Reading Assignment**

Thoroughly read Chapter(s) 6 in your Computer Architecture and Organization textbook.

**Part 1 Glossary Terms - Computer Memory**

Define, in detail, each of these glossary terms from the realm of computer architecture and computer topics, in general. If applicable, use examples to support your definitions. Consult your notes

or course textbook(s) as references or the Internet by visiting Web sites such as:

[**http://www.ask.com**](http://www.ask.com) or [**http://www.webopedia.com**](http://www.webopedia.com/)

**(a) Associative Memory**

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| Associative memory is memory whose locations are identified by content not address and is specifically designed to be searched in parallel. |

**(b) EPROM**

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| This is Erasable Programmable Read-Only Memory. It is a type of programmable read-only memory that can be reprogrammed. |

**(c) EPROM**

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| Electrically erasable PROM is a type of PROM that can be erased by applying an electric field. |

**(d) Memory Hierarchy**

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| The memory hierarchy is designed to handle the disparities of different types of memory in a computer. The memory hierarchy consists of the following base types of memory – registers, cache, main memory, secondary memory, and off-line bulk memory. |

**(e) Virtual Memory**

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| Memory that increases the available memory a computer can use by extending the address space from RAM to the hard drive. The area of the hard disks that stores the excess address space is called a page file. It is implemented through a process called paging that divides memory and programs into the same sized blocks. |

**Part 2 Exercises - Computer Memory**

For each of the following, enter True or False.

\_\_T\_\_\_ **(1)** All cache mapping schemes require a main memory address to have an offset field.

\_\_T\_\_\_ **(2)** It is important to know if a computer is byte or word addressable because we need to know how many addresses are contained in main memory, cache and in each block when doing cache mapping.

\_F\_\_\_\_ **(3)** Caching breaks down when programs exhibit good locality.

\_T\_\_\_\_ **(4)** The two types of cache write policies are write - through and write - back.

\_T\_\_\_\_ **(5)** A unified cache is a cache that holds both data and instructions.

\_T\_\_\_\_ **(6)** When a computer uses paging, there must be a page table for every process.

\_F\_\_\_\_ **(7)** Memory segmentation can result in internal fragmentation, while paging can result in external fragmentation.

\_F\_\_\_\_ **(8)** Assuming an 8 - bit virtual address with pages of 32 bytes, the virtual address format is 5 bits for the page and 3 bits for the offset.

\_T\_\_\_\_ **(9)** Cache replacement policies are necessary to determine which block in cache should be the victim block.

\_T\_\_\_\_ **(10)** Information can be retrieved fastest from a hard disk as compared to magnetic tapes, optical disks and USB flash drives.

**Part 3 Exercises - Computer Memory**

**(1**) Suppose we have a byte - addressable computer using direct mapping with 16 - bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

The offset field is 3 bits.

**(2)** Suppose we have a byte - addressable computer using direct mapping with 16 - bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

The block field is 5 bits.

**(3)** Suppose we have a byte - addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

The tag field is 8 bits.

**(4)** Consider a byte - addressable computer with 24 - bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24 - bit memory address if the computer uses 4 - way set associative mapping.

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| Tag | Set | Offset |
| 10 | 9 | 5 |

**(5)** Consider a byte - addressable computer with 24 - bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24 - bit memory address if the computer uses direct mapping.

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| --- | --- | --- |
| Tag | Set | Offset |
| 8 | 11 | 5 |

**Part 4 Exercises - Computer Memory**

Write a complete answer for each of these.

**(1)** Does a TLB miss always indicate that a page is missing from memory?   
 Explain your answer.

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| **No, it is possible that the page was not one of the most recent page lookup values and therefore it was not in the TLB. If it is not in the TLB, the page could be found in the page table. If it is not in memory, then a page fault is generated and the access is restarted when the page fault is complete.** |

**(2)** If you are a computer builder trying to make your system as price - competitive as possible, what features and organization would you select for its memory hierarchy?

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| **To make a system price competitive, the designer should make use of off-line storage which would allow them to only use a small number of fast chips.** |

**(3)** If you are a computer buyer trying to get the best performance from a system, what features would you look for in its memory hierarchy?

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| **A computer buyer should look for a system that makes use of more system and online storage as opposed to one with more offline storage.** |

**(4)** Name two ways that, as a programmer, you can improve cache performance.

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| **To improve cache performance, a programmer can use smaller data types to minimize the amount of memory required to store data for the program. They can also use data structures that access memory linearly.** |

**(5)** Look up a specific vendor’s specifications for memory and report the memory access time, cache access time and cache hit rate ( and any other data the vendor provides ) .

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| **I was not able to find memory access times for processors, but I did find this information on intel’s website:**  <https://ark.intel.com/products/37147/Intel-Core-i7-920-Processor-8M-Cache-2_66-GHz-4_80-GTs-Intel-QPI> Performance  * # of Cores4 * # of Threads8 * Processor Base Frequency2.66 GHz * Max Turbo Frequency2.93 GHz * Cache8 MB SmartCache * Bus Speed4.8 GT/s QPI * # of QPI Links1 * TDP130 W * VID Voltage Range0.800V-1.375V  Max Memory Size (dependent on memory type)24 GB  * Memory TypesDDR3 800/1066 * Max # of Memory Channels3 * Max Memory Bandwidth25.6 GB/s * Physical Address Extensions36-bit * ECC Memory Supported ‡No |