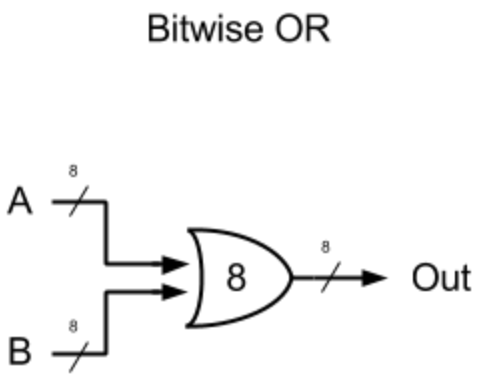
William "Chris" Fenton
CSF - Digital Logic
HW3

1. Draw the block component for the 8-bit Bitwise Or dataflow component.



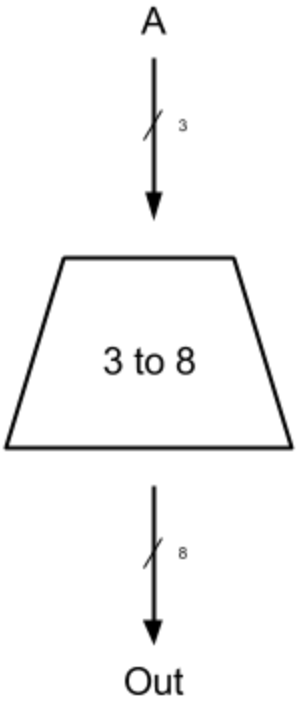
2. Build a logic table that for a 3-bit Bounded Integer Increment function.

A[3:0]	Out[3:0]
000	001
001	010
010	011
011	100
100	101
101	110
111	000

3. Give the logic equations for each of the three outputs of the 3-bit Bounded Integer Increment signals in the previous problem.

A	Out
A[0]	~A[0]
A[2]	A[0] XOR A[1]
A[3]	(A[0] AND A[1]) XOR A[3]

4. Draw the block component for the octal decoder.



5. Give the function table for the octal decoder.

A	Out[7:0]
0	1000 0000
1	0100 0000
2	0010 0000
3	0001 0000
4	0000 1000
5	0000 0100
6	0000 0010
7	0000 0001

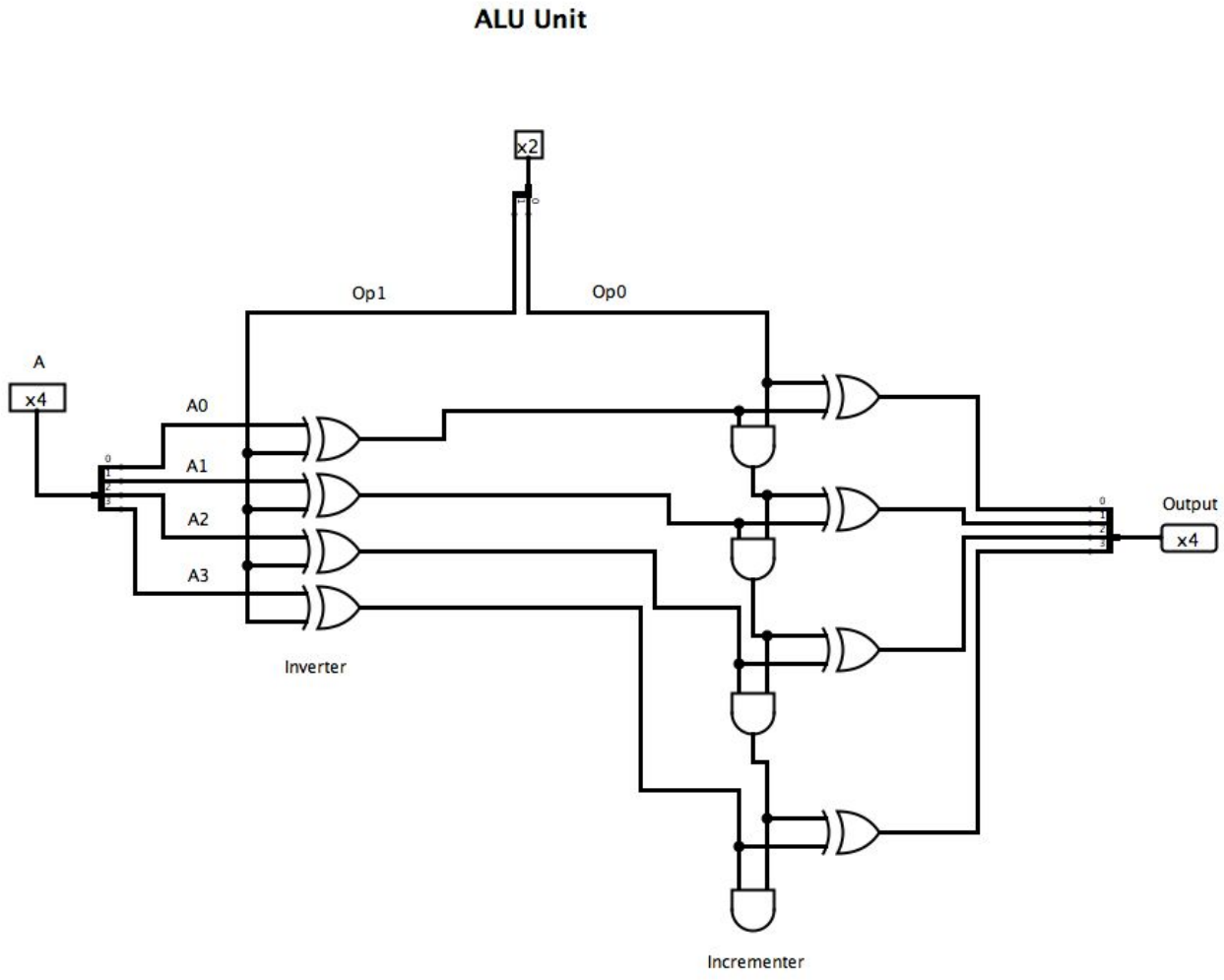
6. Give the internal logic for the 2-to-1 multiplexer on 4-bit data paths.

Data Path	Out
0	(!Sel && A[0]) OR (Sel && B[0])
1	(!Sel && A[1]) OR (Sel && B[1])
2	(!Sel && A[2]) OR (Sel && B[2])
3	(!Sel && A[3]) OR (Sel && B[3])

7. This problem is about the Tiny ALU component. Give the output bit pattern of the component for the following values of the input signals:
(a) k = 10110111, Op = 00
(b) k = 10110111, Op = 01
(c) k = 10110111, Op = 10
(d) k = 10110111, Op = 11

A	Op	Out
1011 0111	00	1011 0111
1011 0111	01	1011 1000
1011 0111	10	0100 1000
1011 0111	11	0100 1001

8. Draw the detailed logic diagram for a 4-bit version of the Tiny ALU component. Label the two bit Op signal inputs as Op1 and Op0, where zero is the least significant bit. Label the individual input signals of the A bus as a3, a2, a1, a0 from most to least significant.



9. Give the logic expression for the 4-bit Tiny ALU component that you constructed in the previous problem. You will need expressions for the four output signals Out3, Out2, Out1, Out0 in terms of the six input signals.

Output	Function
Out0	(Op0) XOR (A0 XOR Op1)
Out1	(Op0 && (A0 XOR Op1)) XOR (A1 XOR Op1)
Out2	(Op0 && (A1 XOR Op1)) XOR (A2 XOR Op1)
Out3	(Op0 && (A2 XOR Op1)) XOR (A3 XOR Op1)

10. Suppose you wanted to build a 3-to-1 multiplexer. How many select bits would you need? Give the function table for a 3-to-1 multiplexer. Hint: you are entitled to signify some outputs as Undefined.

You need 3 select bits.

A	B	C	Sel	Out
x	y	z	000	undefined
x	y	z	001	undefined
x	y	z	010	undefined
x	y	z	011	z
x	y	z	100	undefined
x	y	z	101	y
x	y	z	110	x
x	y	z	111	undefined

11. How many select bits are needed for an 8-to-1 multiplexer? What decoder component is used to implement an 8-to-1 multiplexer?

You need 3 select bits. The octal decoder.