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HW5
CSF - Digital Logic

1. What is the next state and the output of the Counter component if the current state is 0x2E, the A input bus is 0xBF and the Load signal is 0?

2F

2. What is the output of the DFF component at time t + 1 if the input to the DFF Component at time t is 1? When does the state of the DFF component change?

The output is the value of the input, labeled A. The state changes on the clock edge.

3. In the cross-coupled Nor gates in Section 5.2, what are the inputs and outputs of the Nor gates if the input A is 1?

After the top Nor gate has inputs of 1 and 1 and and output of 0. The bottom Nor gate has inputs of 0 and 0 and an output of 1 that is the final output.

4. Consider an 8-bit register that holds a value of 0xED at time t. If the X input is 0xBB at time t, then what is the state of the register at time t+1 if the Load signal is 1?

The value of X gets written to the register, so the value in this case is now 0xBB.

5. Consider the Tiny Register-Transfer Machine in Section 5.5. If the contents of registers A, B, C, D are 0x2F, 0xED, 0x1F, 0xA1 at time t respectively, then what are the contents of registers A, B, C, D at time t+1 if the control code is Sel=11, Op=11, LALBLCLD =0111.

A=0x2F, B=0x42, C=0xE0, D=5E

6. Give the Control Code and the corresponding Register Transfer notation for the action in the previous problem.

Control Code			Action
Sel	Op	LaLbLcLd	f(src)->dst
11	11	0111	neg(B) -> B, C, D

7. Consider the Tiny Register-Transfer Machine in Section 5.5. If the contents of registers A,B,C,D are 0x2F,0xED,0x1F,0xA1 at time t respectively, then what are the contents of registers A, B, C, D after the following three register transfer actions. Assume that each action after the first happens on the values from the previous action.

inc(A) -> B, C, D
inc(B) -> C, D
C -> A, B

A=31, B=31, C=31, D=-93

8. Give the Control Codes for the three actions in Exercise 7.

T1=00010111, T2=01010011, T3=10001100

9. Give an execution trace for the sequence of RT actions in Exercise 7. Use the table format of the Sample Execution Trace in Section 5.6.

Time	Register Values				Control Code			Action
	A	B	C	D	Sel	Op	ABCD	
0	47	-19	29	-95				Initial Reg Values
1	47	-18	30	-94	00	01	0111	inc(A) -> B,C,D
2	47	-18	31	-93	01	01	0011	inc(B) -> C,D
3	31	31	31	-93	10	00	1100	C -> A, B

10. Give an explanation for why each of the last three RT actions in the Two-port Adder Example in Section 5.7 is illegal.

Only the register selected with the Dmux code can be used as the destination.

11. Give an execution trace for the following sequence of RT actions for the Two-port Adder given in Section 5.7. Use the table format for the Two-port Adder given in Section 5.8. Assume the initial values of Exercise 7.

add(A,C) -> A
sub(B, A) -> B

Time	Register Values				Control Code			Action
	A	B	C	D	Dmux	Rmux	Sub	
0	47	-19	29	-95				Initial Reg Values
1	66	-19	29	-95	00	10	0	add(A,C) -> A
2	66	-85	29	-95	01	00	1	sub(B,A) -> B

12. Give an explanation for why each of the last six RT actions in the Adder with Accumulator example table at the end of Section 5.7 is illegal.

Because the datapath returning to the A-D registers is an output of the accumulator register. The actions can only take one data register as an input due to the mux. The other input must be stored in the accumulator.

13. Give an execution trace for the following sequence of RT actions for the Adder with Accumulator given at the end of Section 5.7. Use the table format for the Adder with Accumulator given in Section 5.8. Assume the initial values of Exercise 7.

D -> Acc
sub(Acc, B) -> Acc
add(Acc, C) -> Acc
Acc -> A

Time	Register Values					Control Code					Action
	A	B	C	D	Acc	ABC D	Rmux	Dmux	Acc	Sub	
0	47	-19	29	-95							Initial Reg Values
1	47	-19	29	-95	-95	0000	11	1	1	0	D -> Acc
2	47	-19	29	-95	-76	0000	01	0	1	1	sub(Acc,B) -> Acc
3	47	-19	29	-95	105	0000	10	0	1	0	add(Acc,C) -> Acc
4	105	-19	29	-95	105	1000	00	0	0	0	Acc -> A