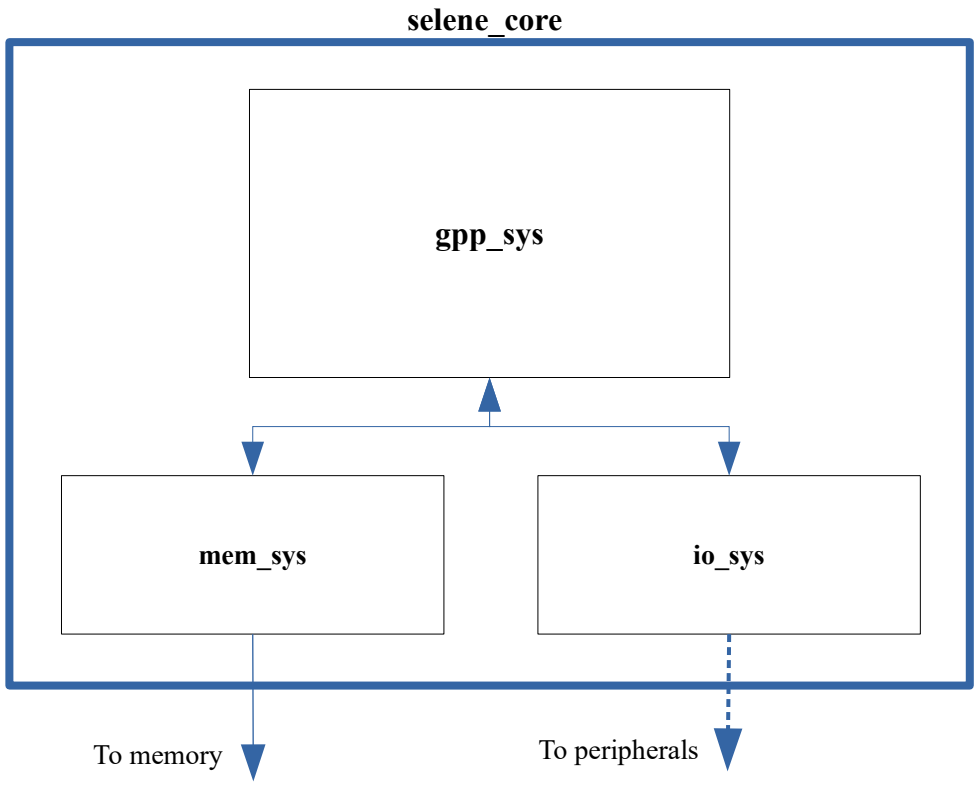
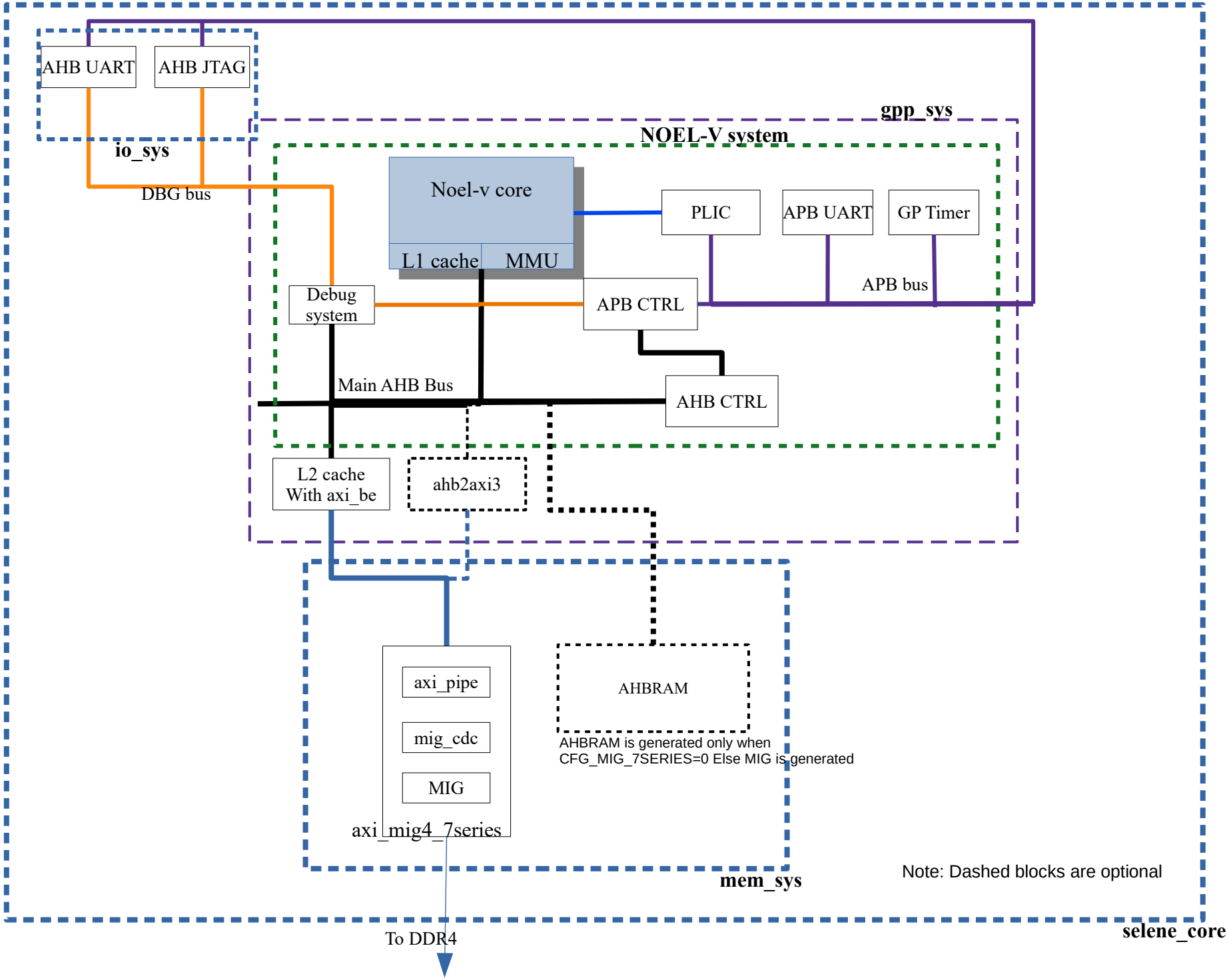

selene_core
gpp_sys
mem_sys
io_sys
To memory
To peripherals


AHB UART
AHB JTAG
io_sys
DBG bus
gpp_sys
NOEL-V system
Noel-v core
L1 cache
MMU
PLIC
APB UART
GP Timer
APB bus
Debug system
APB CTRL
Main AHB Bus
AHB CTRL
L2 cache With axi_be
ahb2axi3
axi_pipe
mig_cdc
MIG
axi_mig4_7series
AHBRAM
AHBRAM is generated only when CFG_MIG_7SERIES=0 Else MIG is generated
mem_sys
Note: Dashed blocks are optional
To DDR4
selene_core

# Selene-xilinx-vcu118 design memory map(Tentative)

| Address range | size | core | Comment |
|---|---|---|---|
| 0x00000000 | 1 Mbyte | AHBROM | |
| 0x20000000 | 1 Mbyte | Test report module | |
| 0x40000000 | 16 Mbyte | AHBRAM | L2cache and MIG is mapped here,If MIG generation is enabled. |
| 0x80000000 | 1 Mbyte | AHB/APB Bridge | |
| 0x80000100 | 256 byte | APBUART | |
| 0x80000200 | 256 byte | GRVERSION | |
| 0x80000300 | 256 byte | GPTIMER | |
| 0x80000500 | 256 byte | GRGPIO | |
| 0x80000E00 | 256 byte | AHBUART | |
| 0x80000F00 | 256 byte | AHBSTAT | |
| 0x84000000 | 64 Mbyte | PLIC | |
| 0x90000000 | 256 Mbyte | Debug module | |
| 0xe0100000 | 1 Mbyte | CLINT | |
| 0xFFF00000 | 1 Mbyte | AHB arbiter/multiplexer | I/O area |
| 0xFFF00000 | 128 Kbyte | AMBA Trace buffer | |
| 0xFFFFF000 | 4 kbyte | AHB arbiter/multiplexer | Configuration area |

**Note: Please note that the memory map is tentative, since the noelv system memory map is not frozen. This may change in the future**