



CC2650 SimpleLink™ 多标准无线 MCU

1 器件概述

1.1 特性

- 微控制器
 - 强大的 ARM® Cortex®-M3
 - EEMBC CoreMark® 评分: 142
 - 高达 48MHz 的时钟速度
 - 128KB 系统内可编程闪存
 - 8KB 缓存静态 RAM (SRAM)
 - 20KB 超低泄漏电流 SRAM
 - 2 引脚 JTAG 和 JTAG 调试
 - 支持无线升级 (OTA)
- 超低功耗传感器控制器
 - 可独立于系统其余部分自主运行
 - 16 位架构
 - 20KB 超低泄漏电流代码和数据 SRAM
- 高效代码尺寸架构, ROM 中装载驱动程序、Bluetooth® 低功耗控制器、IEEE 802.15.4 MAC、和 引导加载程序
- 封装符合 RoHS 标准
 - 4mm × 4mm RSM QFN32 (10 个 GPIO)
 - 5mm × 5mm RHB QFN32 (15 个 GPIO)
 - 7mm × 7mm RGZ QFN48 (31 个 GPIO)
- 外设
 - 所有数字外设引脚均可连接任意 GPIO
 - 4 个通用定时器模块 (8 × 16 位或 4 × 32 位, 均采用 PWM)
 - 12 位模数转换器 (ADC)、200MSPS、8 通道模拟多路复用器
 - 持续时间比较器
 - 超低功耗模拟比较器
 - 可编程电流源
 - UART
 - 2x SSI (SPI、μW 和 TI)
 - I²C
 - I2S
 - 实时时钟 (RTC)
 - AES-128 安全模块
 - 真随机数发生器 (TRNG)
 - 10、15 或 31 个 GPIO, 具体取决于所用封装选项
 - 支持 8 个电容感测按钮
 - 集成温度传感器
- 外部系统
 - 片上内部 DC-DC 转换器
 - 极少的外部组件
 - 与 SimpleLink CC2590 和 CC2592 范围扩展器无缝集成
 - 与采用 4mm × 4mm 和 5mm × 5mm QFN 封装的 SimpleLink CC13xx 引脚兼容
- 低功耗
 - 宽电源电压范围
 - 正常工作电压: 1.8V 至 3.8V
 - 外部稳压器模式: 1.7V 至 1.95V
 - 有源模式 RX: 5.9mA
 - 有源模式 TX (0dBm): 6.1mA
 - 有源模式 TX (+5dBm): 9.1mA
 - 有源模式 MCU: 61μA/MHz
 - 有源模式 MCU: 48.5 CoreMark/mA
 - 有源模式传感器控制器: 8.2μA/MHz
 - 待机电流: 1μA (RTC 运行, RAM/CPU 保持)
 - 关断电流: 100nA (发生外部事件时唤醒)
- 射频 (RF) 部分
 - 2.4GHz RF 收发器, 符合 Bluetooth 低功耗 (BLE) 4.1 规范及 IEEE 802.15.4 PHY 和 MAC
 - 出色的接收器灵敏度 (BLE 对应 -97dBm, 802.15.4 对应 -100dBm)、可选择性和阻断性能
 - 最高达 +5dBm 的可编程输出功率
 - 单端或差分 RF 接口
 - 适用于符合各项全球射频规范的系统
 - ETSI EN 300 328 (欧洲)
 - EN 300 440 2 类 (欧洲)
 - FCC CFR47 第 15 部分 (美国)
 - ARIB STD-T66 (日本)
- 工具和开发环境
 - 功能全面的低成本开发套件
 - 针对不同 RF 配置的多种参考设计
 - 数据包监听器 PC 软件
 - Sensor Controller Studio
 - SmartRF™ Studio
 - SmartRF Flash Programmer 2
 - IAR Embedded Workbench® (用于 ARM)
 - Code Composer Studio™



1.2 应用

- 消费类电子产品
- 移动电话附件
- 运动和健身设备
- 人机接口设备 (HID) 应用
- 家庭和楼宇自动化
- 照明控制
- 警报和安全
- 电子货架标签
- Proximity Tag
- 医疗
- 遥控
- 无线传感器网络

1.3 说明

CC2650 是一款面向 Bluetooth Smart、ZigBee® 和 6LoWPAN，以及 ZigBee® RF4CE 远程控制应用的无线 MCU。

此器件属于 CC26xx 系列的经济高效型超低功耗 2.4GHz RF 器件。极低的有源 RF 和 MCU 电流以及低功耗模式流耗可确保卓越的电池使用寿命，允许采用小型纽扣电池在能源采集型应用中使用。

CC2650 含有一个 32 位 ARM Cortex-M3 处理器，与主处理器工作频率同为 48MHz，具有丰富的外设功能集，包括一个独特的超低功耗传感器控制器，适用于在系统处于休眠模式时连接外部传感器和/或自主采集模拟和数字数据。

凭此特性，CC2650 成为广泛的工业、消费类电子和医疗产品中各类应用的理想选择。

Bluetooth 低功耗控制器和 IEEE 802.15.4 MAC 嵌入在 ROM 中，并在 ARM Cortex-M0 处理器上单独运行。此架构可改善整体系统性能和功耗，并释放闪存以供应用。

Bluetooth Smart 和 ZigBee 协议栈可从 www.ti.com.cn 免费获取。

器件信息⁽¹⁾

器件型号	封装	封装尺寸
CC2650F128RGZ	RGZ (QFN48)	7.00mm x 7.00mm
CC2650F128RHB	RHB (QFN32)	5.00mm x 5.00mm
CC2650F128RSM	RSM (QFN32)	4.00mm x 4.00mm

(1) 更多信息请参见 节 9，机械封装和可订购产品信息。

1.4 功能方框图

节 1.4 显示了 CC2650 的方框图。

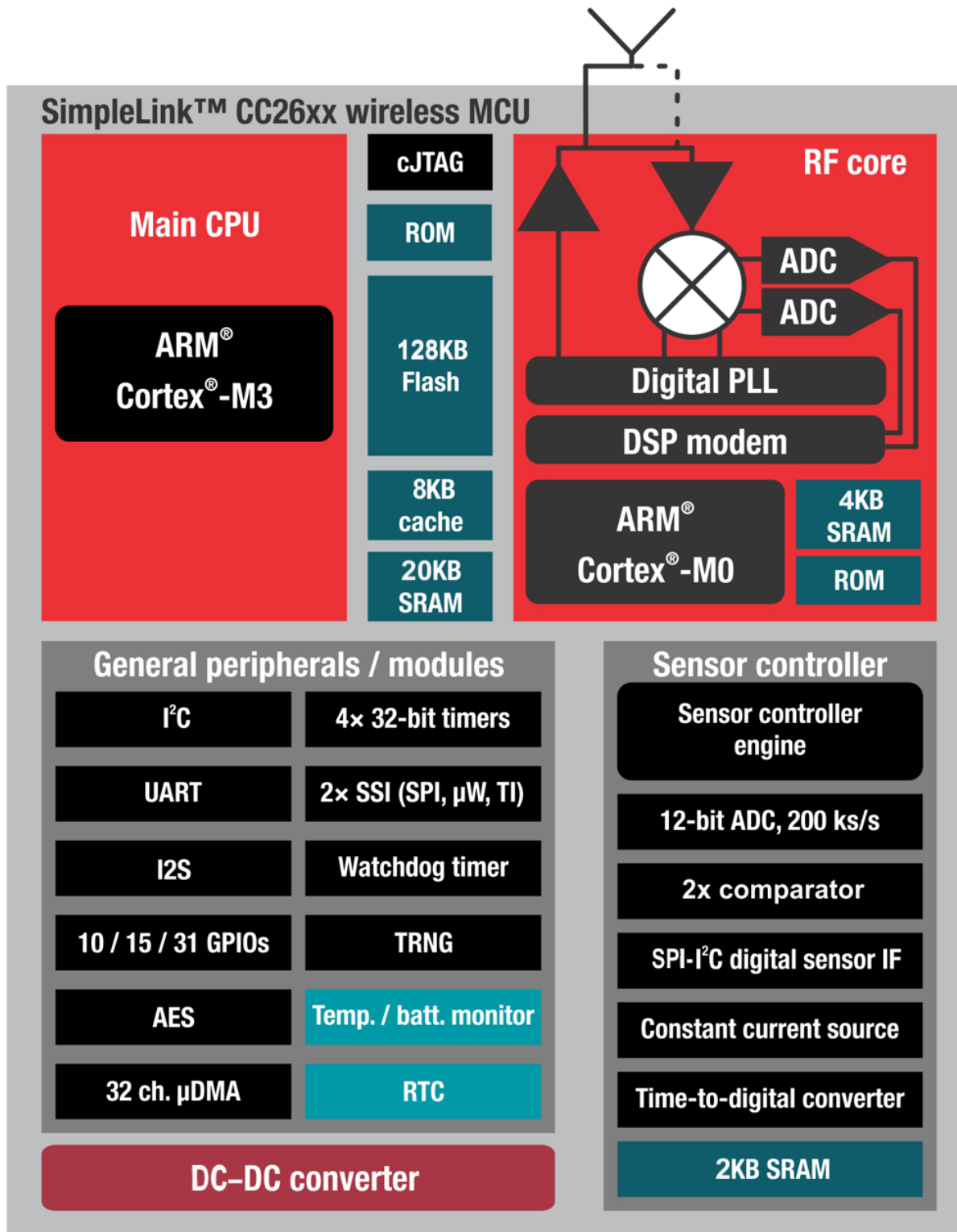


图 1-1. 方框图

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2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

日期	修订版本	注释
2015 年 2 月	*	最初发布版本

3 Device Comparison

Table 3-1. Device Family Overview

DEVICE	PHY SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE ⁽¹⁾
CC2650F128xxx	Multi-Protocol ⁽²⁾	128	20	31, 15, 10	RGZ, RHB, RSM
CC2640F128xxx	<i>Bluetooth</i> low energy	128	20	31, 15, 10	RGZ, RHB, RSM
CC2630F128xxx	IEEE 802.15.4 Zigbee(/6LoWPAN)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2620F128xxx	IEEE 802.15.4 (RF4CE)	128	20	31, 15, 10	RGZ, RHB, RSM

(1) Package designator replaces the xxx in device name to form a complete device name, RGZ is 7-mm x 7-mm QFN48, RHB is 5-mm x 5-mm QFN32, and RSM is 4-mm x 4-mm QFN32.

(2) The CC2650 supports all PHYs and can be reflashed to run all the supported standards.

4 Terminal Configuration and Functions

NOTE

I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

4.1 Pin Diagram – RSM Package

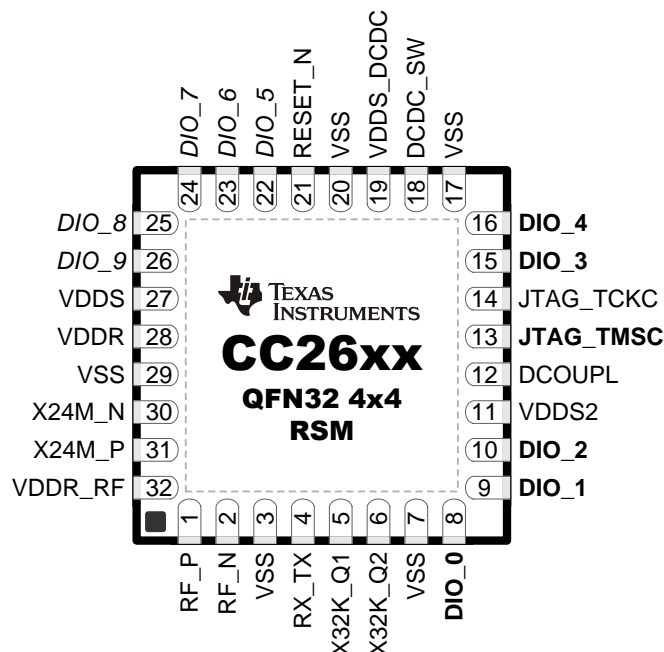


Figure 4-1. RSM (4 mm × 4 mm) Pinout, 0.4-mm Pitch

4.2 Signal Descriptions – RSM Package

Table 4-1. Signal Descriptions – RSM Package

PIN NAME	PIN	PIN TYPE	DESCRIPTION
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RX_TX	4	RF I/O	Optional bias pin for the RF LNA
VDDSD	27	Power	1.8 V to 3.8 V main chip supply ⁽¹⁾
VDDSD2	11	Power	1.8 V to 3.8 V GPIO supply ⁽¹⁾
VDDSDCDC	19	Power	1.8 V to 3.8 V DC/DC supply. Tie to ground for external regulator mode (1.7 V to 1.95 V operation)
VDDR	28	Power	1.7 V to 1.95 V supply, typically connect to output of internal DC/DC ⁽²⁾⁽³⁾
VDDR_RF	32	Power	1.7 V to 1.95 V supply, typically connect to output of internal DC/DC ⁽⁴⁾⁽³⁾
DCOUPL	12	Power	1.27 V regulated digital-supply decoupling capacitor ⁽³⁾
VSS	3, 7, 17, 20, 29	Power	Ground

(1) See 8.2, technical reference manual for more details.

(2) If internal DC/DC is not used, this pin is supplied internally from the main LDO.

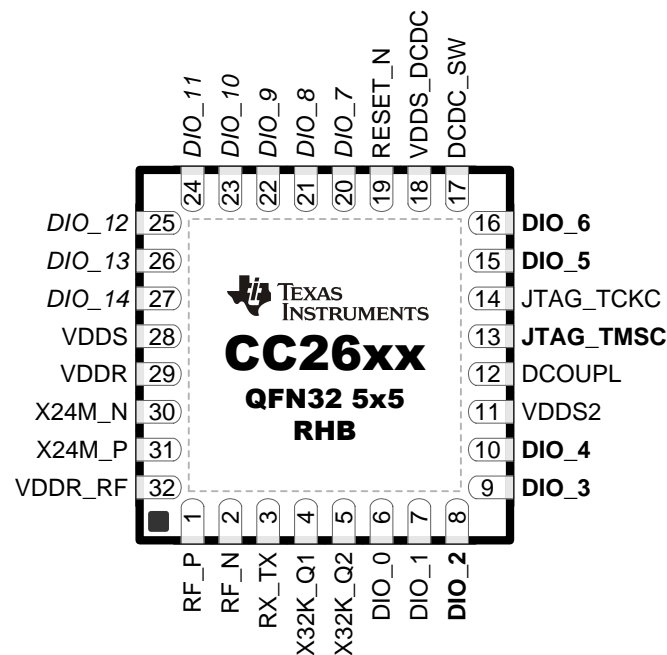
(3) Do not supply external circuitry from this pin.

(4) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

Table 4-1. Signal Descriptions – RSM Package (continued)

PIN NAME	PIN	PIN TYPE	DESCRIPTION
DCDC_SW	18	Power	Output from internal DC/DC ⁽¹⁾ . Tie to ground for external regulator mode (1.7 V to 1.95 V operation)
EGP		Power	Ground – Exposed Ground Pad
RESET_N	21	Digital input	Reset, active-low. No internal pullup
DIO_0	8	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_1	9	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_2	10	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_3	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_4	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_5	22	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_6	23	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_7	24	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_8	25	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_9	26	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMSC	13	Digital I/O	JTAG TMS
JTAG_TCKC	14	Digital I/O	JTAG TCK
X32K_Q1	5	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	6	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2

4.3 Pin Diagram – RHB Package

**Figure 4-2. RHB (5 mm × 5 mm) Pinout, 0.5-mm Pitch**

4.4 Signal Descriptions – RHB Package

Table 4-2. Signal Descriptions – RHB Package

PIN NAME	PIN	PIN TYPE	DESCRIPTION
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
VDDS	28	Power	1.8 V to 3.8 V main chip supply ⁽¹⁾
VDDS2	11	Power	1.8 V to 3.8 V GPIO supply ⁽¹⁾
VDDS_DCDC	18	Power	1.8 V to 3.8 V DC/DC supply
VDDR	29	Power	1.7 V to 1.95 V supply, typically connect to output of internal DC/DC ⁽²⁾⁽³⁾
VDDR_RF	32	Power	1.7 V to 1.95 V supply, typically connect to output of internal DC/DC ⁽⁴⁾⁽³⁾
DCOUP_L	12	Power	1.27 V regulated digital-supply decoupling ⁽³⁾
DCDC_SW	17	Power	Output from internal DC/DC ⁽¹⁾
EGP		Power	Ground – Exposed Ground Pad
RESET_N	19	Digital input	Reset, active-low. No internal pullup
DIO_0	6	Digital I/O	GPIO, Sensor Controller
DIO_1	7	Digital I/O	GPIO, Sensor Controller
DIO_2	8	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_3	9	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_4	10	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_5	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_6	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_7	20	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_8	21	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_9	22	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_10	23	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_11	24	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_12	25	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_13	26	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_14	27	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMSC	13	Digital I/O	JTAG TMS, High drive capability
JTAG_TCKC	14	Digital I/O	JTAG TCK
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2

(1) See [Section 8.2](#), technical reference manual for more details.

(2) If internal DC/DC is not used, this pin is supplied internally from the main LDO.

(3) Do not supply external circuitry from this pin.

(4) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.5 Pin Diagram – RGZ Package

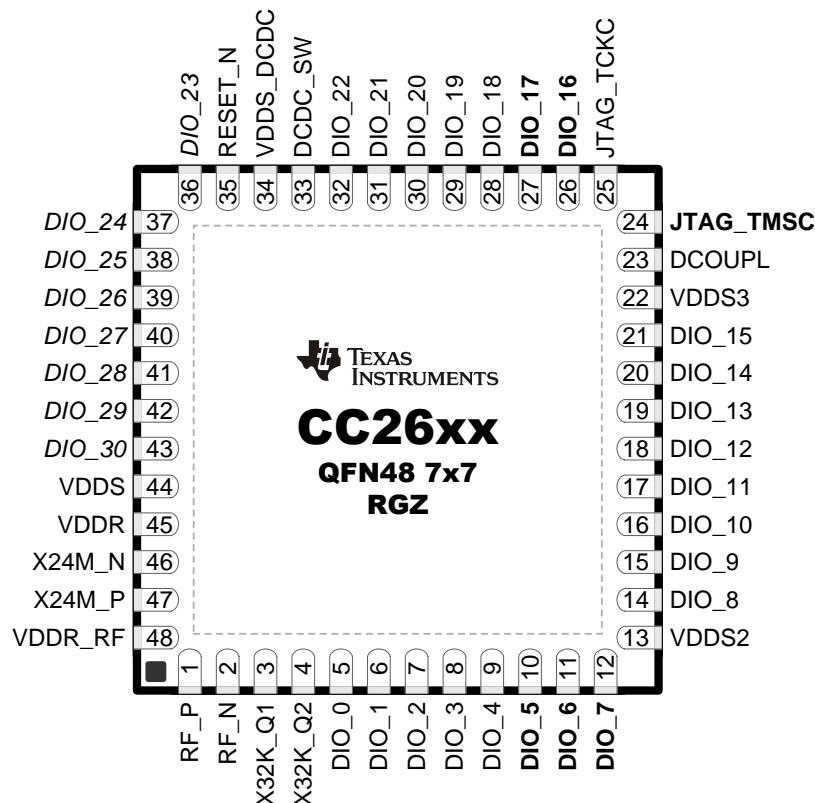


Figure 4-3. RGZ (7 mm × 7 mm) Pinout, 0.5-mm Pitch

4.6 Signal Descriptions – RGZ Package

Table 4-3. Signal Descriptions – RGZ Package

PIN NAME	PIN	PIN TYPE	DESCRIPTION
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
VDDSD	44	Power	1.8 V to 3.8 V main chip supply ⁽¹⁾
VDDSD2	13	Power	1.8 V to 3.8 V DIO supply ⁽¹⁾
VDDSD3	22	Power	1.8 V to 3.8 V DIO supply ⁽¹⁾
VDDSDCDC	34	Power	1.8 V to 3.8 V DC/DC supply
VDDDR	45	Power	1.7 V to 1.95 V supply, typically connect to output of internal DC/DC ⁽²⁾⁽³⁾
VDDDR_RF	48	Power	1.7 V to 1.95 V supply, typically connect to output of internal DC/DC ⁽⁴⁾⁽³⁾
DCOUPL	23	Power	1.27 V regulated digital-supply decoupling capacitor ⁽³⁾
EGP		Power	Ground – Exposed Ground Pad
DCDC_SW	33	Power	Output from internal DC/DC ⁽¹⁾
RESET_N	35	Digital input	Reset, active-low. No internal pullup
DIO_0	5	Digital I/O	GPIO, Sensor Controller

(1) See 节 8.2, technical reference manual for more details.

(2) If internal DC/DC is not used, this pin is supplied internally from the main LDO.

(3) Do not supply external circuitry from this pin.

(4) If internal DC/DC is not used, this pin must be connected to VDDDR for supply from the main LDO.

Table 4-3. Signal Descriptions – RGZ Package (continued)

PIN NAME	PIN	PIN TYPE	DESCRIPTION
DIO_1	6	Digital I/O	GPIO, Sensor Controller
DIO_2	7	Digital I/O	GPIO, Sensor Controller
DIO_3	8	Digital I/O	GPIO, Sensor Controller
DIO_4	9	Digital I/O	GPIO, Sensor Controller
DIO_5	10	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_6	11	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_7	12	Digital I/O	GPIO, Sensor Controller, High drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, High drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, High drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_24	37	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_25	38	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_26	39	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_27	40	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_28	41	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_29	42	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_30	43	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMISC	24	Digital I/O	JTAG TMISC, High drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCKC
X32K_Q1	3	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	4	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

[over operating free-air temperature range (unless otherwise noted)] Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

		MIN	MAX	UNIT
Supply voltage, VDD ⁽³⁾	VDDR supplied by internal DC/DC regulator or internal GLDO	−0.3	4.1	V
Supply voltage, VDD ⁽³⁾ and VDDR	External regulator mode (VDD and VDDR pins connected on PCB)	−0.3	2.25	V
Voltage on any digital pin ⁽⁴⁾		−0.3	VDD+0.3, max 4.1	V
Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P		−0.3	VDDR+0.3, max 2.25	V
Voltage on ADC input (V _{in})	Internal fixed or relative reference, voltage scaling enabled	−0.3	VDD	V
	Internal fixed reference, voltage scaling disabled	−0.3	1.49	
	Internal relative reference, voltage scaling disabled	−0.3	VDD / 2.9	
	External reference, voltage scaling enabled	−0.3	min (V _{ref} × 2.9, VDD)	
	External reference, voltage scaling disabled	−0.3	V _{ref}	
Voltage on external ADC reference (V _{ref})		−0.3	1.6	V
Input RF level			+5	dBm
T _{stg}	Storage temperature	−40	150	°C

(1) All voltage values are with respect to VDD, unless otherwise noted.

(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) VDD2 and VDD3 needs to be at the same potential as VDD.

(4) Including analog capable DIO.

5.2 ESD Ratings

			VALUE	UNIT
V _{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾	All pins	±2500
		Charged device model (CDM), per JESD22-C101 ⁽²⁾	RF pins	±750
			non-RF pins	±750

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

The operating conditions for CC2650 are listed below.

		MIN	MAX	UNIT
Ambient temperature range		−40	85	°C
Operating supply voltage (VDD and VDDR), external regulator mode	For operation in 1.8-V systems (VDD and VDDR pins connected on PCB, internal DC/DC cannot be used)	1.7	1.95	V
Operating supply voltage (VDD)	For operation in battery-powered and 3.3-V systems (internal DC/DC can be used to minimize power consumption)	1.8	3.8	V
Rising supply voltage slew rate		0	100	mV/us
Falling supply voltage slew rate		0	20	mV/us

Recommended Operating Conditions (continued)

The operating conditions for CC2650 are listed below.

		MIN	MAX	UNIT
Falling supply voltage slew rate, with low-power flash settings ⁽¹⁾			3	mV/us
Positive temperature gradient in standby ⁽²⁾	No limitation for negative temperature gradient, or outside standby mode		5	°C/s

- (1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22 μ F VDDS input capacitor (see [Figure 7-1](#)) should be used to ensure compliance with this slew rate.
- (2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature. See [Section 5.15](#)

5.4 Thermal Characteristics

NAME	DESCRIPTION	RSM (°C/W) ⁽¹⁾	RHB (°C/W) ⁽¹⁾	RGZ (°C/W) ⁽¹⁾
Θ_{JA}	Junction-to-ambient thermal resistance	36.9	32.8	29.6
Θ_{JCTop}	Junction-to-case (top) thermal resistance	30.3	24.0	15.7
Θ_{JB}	Junction-to-board thermal resistance	7.6	6.8	6.2
Ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	0.3
Ψ_{JB}	Junction-to-board characterization parameter	7.4	6.8	6.2
Θ_{JCbott}	Junction-to-case (bottom) thermal resistance	2.1	1.9	1.9

- (1) °C/W = degrees Celsius per watt.

5.5 Electrical Characteristics

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$ with internal DC-DC converter, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{core}	Core current consumption	Reset. RESET_N pin asserted		100		nA
		Shutdown. No clocks running, no retention		150		
		Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF		1		μA
		Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF		1.2		
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF		2.5		
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF		2.7		
		Idle. Supply Systems and RAM powered.		550		
		Active. Core running CoreMark		1.45 mA + 31 μA/MHz		mA
		Radio RX ⁽¹⁾		5.9		
		Radio RX ⁽²⁾		6.1		
		Radio TX, 0 dBm output power ⁽¹⁾		6.1		
		Radio TX, 5 dBm output power ⁽²⁾		9.1		
I _{peri}	Peripheral Current Consumption (Adds to core current I _{core} for each peripheral unit activated) ⁽³⁾					
	Peripheral power domain	Delta current with domain enabled		20		μA
	Serial power domain	Delta current with domain enabled		13		μA
	RF Core	Delta current with power domain enabled, clock enabled, RF Core Idle		237		μA
	μDMA	Delta current with clock enabled, module idle		130		μA
	Timers	Delta current with clock enabled, module idle		113		μA
	I ² C	Delta current with clock enabled, module idle		12		μA
	I2S	Delta current with clock enabled, module idle		36		μA
	SSI	Delta current with clock enabled, module idle		93		μA
	UART	Delta current with clock enabled, module idle		164		μA

(1) Single-ended RF mode optimized for size and power consumption. Measured on CC2650EM-4XS

(2) Differential RF mode optimized for RF performance. Measured on CC2650EM-5XD

(3) I_{peri} not supported in Standby and Shutdown

5.6 General Characteristics

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wake-up and Timing					
Idle -> Active			14		μs
Standby -> Active			151		μs
Shutdown -> Active			1015		μs
Flash Memory					
Supported flash erase cycles before failure		100			k Cycles
Flash page/sector erase current	Average delta current		12.6		mA
Flash page/sector erase time ⁽¹⁾			8		ms
Flash page/sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash write time ⁽¹⁾	4 bytes at a time		8		μs

(1) This number is dependent on Flash aging and will increase over time and erase cycles

5.7 1-Mbps GFSK (Bluetooth Low Energy) – RX

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, $\text{BER} = 10^{-3}$		-97		dBm
Receiver sensitivity	Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, $\text{BER} = 10^{-3}$		-96		dBm
Receiver saturation	Differential mode. Measured at the CC2650EM-5XD SMA connector, $\text{BER} = 10^{-3}$		4		dBm
Receiver saturation	Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, $\text{BER} = 10^{-3}$		0		dBm
Co-channel rejection ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer in channel, $\text{BER} = 10^{-3}$		-6		dB
Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at $\pm 1\text{ MHz}$, $\text{BER} = 10^{-3}$		7 / 3 ⁽²⁾		dB
Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at $\pm 2\text{ MHz}$, $\text{BER} = 10^{-3}$		34 / 25 ⁽²⁾		dB
Selectivity, $\pm 3\text{ MHz}$ ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at $\pm 3\text{ MHz}$, $\text{BER} = 10^{-3}$		38 / 26 ⁽²⁾		dB
Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at $\pm 4\text{ MHz}$, $\text{BER} = 10^{-3}$		42 / 29 ⁽²⁾		dB
Selectivity, $\pm 5\text{ MHz}$ or more ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at $\geq \pm 5\text{ MHz}$, $\text{BER} = 10^{-3}$		32		dB
Selectivity, Image frequency ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at image frequency, $\text{BER} = 10^{-3}$		25		dB
Selectivity, Image frequency $\pm 1\text{ MHz}$ ⁽¹⁾	Wanted signal at -67 dBm, modulated interferer at $\pm 1\text{ MHz}$ from image frequency, $\text{BER} = 10^{-3}$		3 / 26 ⁽²⁾		dB
Out-of-band blocking ⁽³⁾	30 MHz to 2000 MHz		-20		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		-5		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		-8		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		-8		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		-34		dBm

(1) Numbers given as I/C dB

(2) X / Y, where X is +N MHz and Y is -N MHz

(3) Excluding one exception at $F_{\text{wanted}} / 2$, per Bluetooth Specification

1-Mbps GFSK (*Bluetooth Low Energy*) – RX (*continued*)

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions, 30 to 1000 MHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		-71		dBm
Spurious emissions, 1 to 12.75 GHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		-62		dBm
RSSI dynamic range			70		dB
RSSI accuracy			± 4		dB

5.8 1-Mbps GFSK (*Bluetooth Low Energy*) – TX

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Differential mode, delivered to a single-ended 50- Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50- Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50- Ω load through a balun		-21		dBm
Spurious emission conducted measurement	$f < 1\text{ GHz}$, outside restricted bands		-43		dBm
	$f < 1\text{ GHz}$, restricted bands ETSI		-65		dBm
	$f < 1\text{ GHz}$, restricted bands FCC		-76		dBm
	$f > 1\text{ GHz}$, including harmonics		-46		dBm
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				

5.9 1-Mbps GFSK (*Bluetooth Low Energy*) – Common RX/TX

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency error tolerance	Difference between center frequency of the received RF signal and local oscillator frequency.	-350	350		kHz
Data rate error tolerance		-750	750		ppm

5.10 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – RX

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, PER = 1%		-100		dBm
Receiver sensitivity	Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, PER = 1%		-97		dBm
Receiver saturation	Measured at the CC2650EM-5XD SMA connector, PER = 1%		+4		dBm
Adjacent channel rejection	Wanted signal at -82 dBm, modulated interferer at $\pm 5\text{ MHz}$, PER = 1%		39		dB
Alternate channel rejection	Wanted signal at -82 dBm, modulated interferer at $\pm 10\text{ MHz}$, PER = 1%		52		dB
Channel rejection, $\pm 15\text{ MHz}$ or more	Wanted signal at -82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		57		dB
Blocking/desensitization, 5 MHz from upper band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB

IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – RX (continued)

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocking/desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking/desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking/desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking/desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking/desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking/desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking/desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Spurious emissions, 30 to 1000 MHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–71		dBm
Spurious emissions, 1 to 12.75 GHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–62		dBm
Frequency error tolerance	Difference between center frequency of the received RF signal and local oscillator frequency		>200		ppm
RSSI dynamic range			100		dB
RSSI accuracy			± 4		dB

5.11 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – TX

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Delivered to a single-ended 50 Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50-Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50 Ω load through a balun		−21		dBm
Error vector magnitude	At maximum output power		2%		
Spurious emission conducted measurement	f < 1 GHz, outside restricted bands		−43		dBm
	f < 1 GHz, restricted bands ETSI		−65		
	f < 1 GHz, restricted bands FCC		−76		
	f > 1 GHz, including harmonics		−46		
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				

5.12 24-MHz Crystal Oscillator (XOSC_HF)⁽¹⁾

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			24		MHz
Crystal frequency tolerance ⁽²⁾		-40		40	ppm
ESR Equivalent series resistance			20	60	Ω
CL Crystal load capacitance		5		9	pF
Start-up time ⁽³⁾			150		μs

(1) Probing or otherwise stopping the XTAL while the DC-DC converter is enabled may cause permanent damage to the device.

(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance. As per Bluetooth and IEEE 802.15.4 specification

(3) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection

5.13 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32.768		kHz
Crystal frequency tolerance, Bluetooth low energy applications		-250		250	ppm
ESR Equivalent series resistance			30	100	k Ω
CL Crystal load capacitance		6		12	pF

5.14 48-MHz RC Oscillator (RCOSC_HF)

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			48		MHz
Uncalibrated frequency accuracy			$\pm 1\%$		
Calibrated frequency accuracy ⁽¹⁾			$\pm 0.25\%$		
Start-up time			5		μs

(1) Accuracy relatively to the calibration source (XOSC_HF).

5.15 32-kHz RC Oscillator (RCOSC_LF)

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency			32.8		kHz
Temperature coefficient			50		ppm/ $^{\circ}\text{C}$

5.16 ADC Characteristics⁽¹⁾

$T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V_{DDS}	V
	Resolution			12		Bits
	Sample rate				200	ksps
	Offset	Internal 4.3 V equivalent reference ⁽²⁾		2		LSB
	Gain error	Internal 4.3 V equivalent reference ⁽²⁾		2.4		LSB
DNL ⁽³⁾	Differential nonlinearity			>-1		LSB
INL ⁽⁴⁾	Integral nonlinearity			± 3		LSB
ENOB	Effective number of bits	Internal 4.3 V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		9.8		Bits
		VDDS as reference, 200 ksps, 9.6-kHz input tone		10		
		Internal 1.44 V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3 V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		-65		dB
		VDDS as reference, 200 ksps, 9.6-kHz input tone		-69		
		Internal 1.44 V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		-71		
SINAD / SNDR	Signal-to-noise and distortion ratio	Internal 4.3 V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		60		dB
		VDDS as reference, 200 ksps, 9.6-kHz input tone		63		
		Internal 1.44 V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		69		
SFDR	Spurious-free dynamic range	Internal 4.3 V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		67		dB
		VDDS as reference, 200 ksps, 9.6-kHz input tone		72		
		Internal 1.44 V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		73		
	Conversion time	Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles
	Current consumption	Internal 4.3 V equivalent reference ⁽²⁾		0.66		mA
	Current consumption	VDDS as reference		0.75		mA
	Internal reference voltage	Internal 4.3 V equivalent reference ⁽²⁾		1.44		V
	Internal reference voltage	VDDS as reference		$V_{\text{DDS}} / 2.82$		V

(1) Using IEEE Std 1241™-2010 for terminology and test methods.

(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V

(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5 depending on device, see [Figure 5-15](#)

(4) For a typical example, see [Figure 5-16](#)

5.17 Temperature Sensor

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		$^{\circ}\text{C}$
Range		-40		85	$^{\circ}\text{C}$
Accuracy			± 5		$^{\circ}\text{C}$
Supply voltage coefficient ⁽¹⁾			3.2		$^{\circ}\text{C}/\text{V}$

(1) Automatically compensated when using supplied driver libraries.

5.18 Battery Monitor

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^{\circ}\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V

Battery Monitor (continued)

Measured on Texas Instruments CC2650EM-5XD reference design with $T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy			13		mV

5.19 Continuous Time Comparator

$T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
External reference voltage		0		V_{DDS}	V
Internal reference voltage	DCOUPPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from -10 mV to $+10\text{ mV}$		0.72		μs
Current consumption when enabled ⁽¹⁾			8.6		μA

(1) Additionally the bias module needs to be enabled when running in standby mode.

5.20 Low-Power Clocked Comparator

$T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32		kHz
Internal reference voltage, $V_{\text{DDS}} / 2$			1.49 - 1.51		V
Internal reference voltage, $V_{\text{DDS}} / 3$			1.01 - 1.03		V
Internal reference voltage, $V_{\text{DDS}} / 4$			0.78 - 0.79		V
Internal reference voltage, $\text{DCOUPPL} / 1$			1.25 - 1.28		V
Internal reference voltage, $\text{DCOUPPL} / 2$			0.63 - 0.65		V
Internal reference voltage, $\text{DCOUPPL} / 3$			0.42 - 0.44		V
Internal reference voltage, $\text{DCOUPPL} / 4$			0.33 - 0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from -50 mV to $+50\text{ mV}$		<1		clock-cycle
Current consumption when enabled			362		nA

5.21 Programmable Current Source

$T_c=25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25 - 20		μA
Resolution			0.25		μA
Current consumption ⁽¹⁾	Including current source at maximum programmable output		23		μA

(1) Additionally the bias module needs to be enabled when running in standby mode.

5.22 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_A = 25^{\circ}\text{C}$, $V_{\text{DD5}} = 1.8\text{ V}$					
GPIO VOH at 8-mA load	IOCURR=2, high drive GPIOs only		1.54		V
GPIO VOL at 8-mA load	IOCURR=2, high drive GPIOs only		0.26		V
GPIO VOH at 4-mA load	IOCURR=1		1.58		V
GPIO VOL at 4-mA load	IOCURR=1		0.21		V
GPIO pullup current	Input mode, pullup enabled, $V_{\text{pad}}=0\text{V}$		71.7		μA
GPIO pulldown current	Input mode, pulldown enabled, $V_{\text{pad}}=V_{\text{DD5}}$		21.1		μA
GPIO high/low input transition, no hysteresis	IH=0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH=1, transition voltage for input read as 0→1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH=1, transition voltage for input read as 1→0		0.74		V
GPIO input hysteresis	IH=1, difference between 0→1 and 1→0 points		0.33		V
$T_A = 25^{\circ}\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$					
GPIO VOH at 8-mA load	IOCURR=2, high drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR=2, high drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR=1		2.72		V
GPIO VOL at 4-mA load	IOCURR=1		0.28		V
$T_A = 25^{\circ}\text{C}$, $V_{\text{DD5}} = 3.8\text{ V}$					
GPIO pullup current	Input mode, pullup enabled, $V_{\text{pad}}=0\text{V}$		277		μA
GPIO pulldown current	Input mode, pulldown enabled, $V_{\text{pad}}=V_{\text{DD5}}$		113		μA
GPIO high/low input transition, no hysteresis	IH=0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH=1, transition voltage for input read as 0→1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH=1, transition voltage for input read as 1→0		1.54		V
GPIO input hysteresis	IH=1, difference between 0→1 and 1→0 points		0.4		V

5.23 Control Input AC Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{\text{DD5}} = 1.7\text{ V}$ to 3.8 V , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET_N low duration		1			μs

5.24 Synchronous Serial Interface (SSI) Characteristics

$T_c=25^{\circ}\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER NO.	PARAMETER	PARAMETER NAME	MIN	TYP	MAX	UNIT
S1	$t_{\text{clk_per}}$	SSIClk cycle time	12		65024	system clocks

5.25 Typical Characteristics

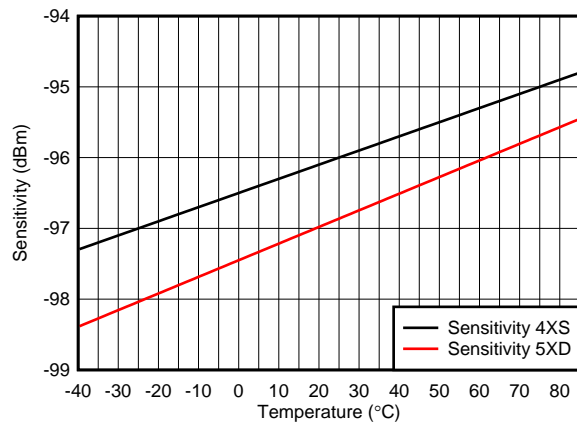


Figure 5-1. BLE Sensitivity vs Temperature

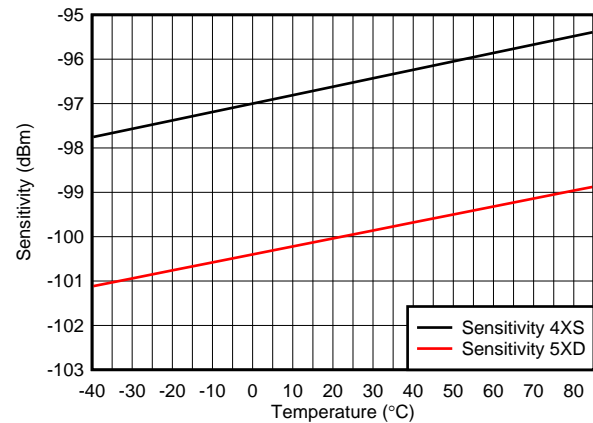


Figure 5-2. IEEE 802.15.4 Sensitivity vs Temperature

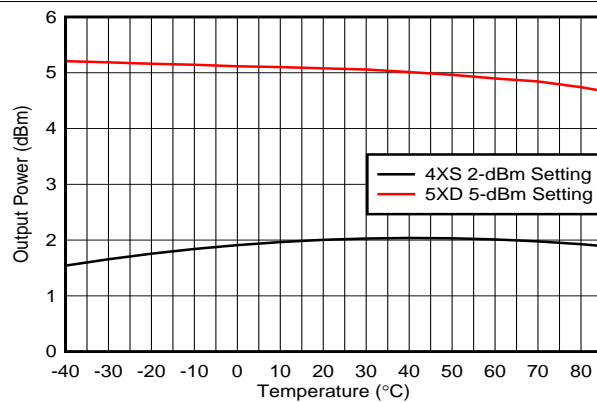
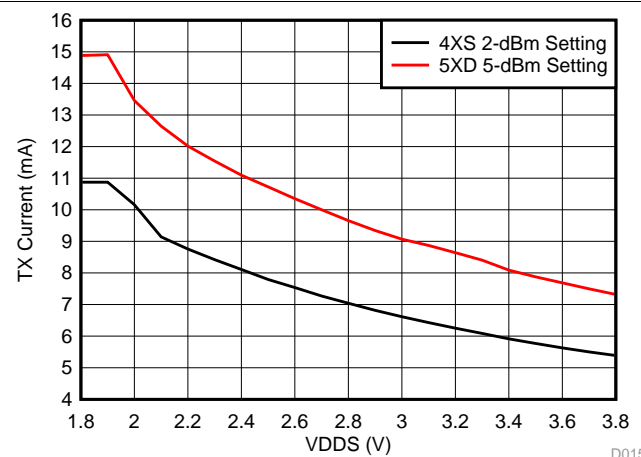
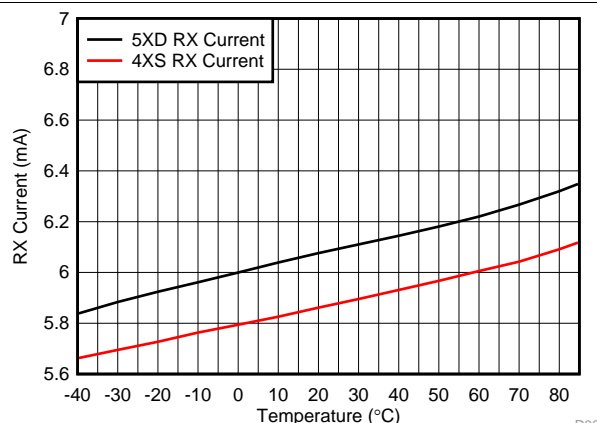


Figure 5-3. Output Power vs Temperature



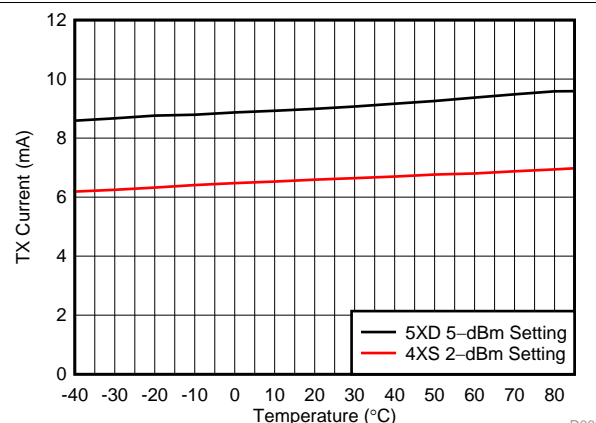
D015

Figure 5-4. Transmit Current Consumption vs. Supply Voltage (VDD5)



D001

Figure 5-5. RX Mode Current Consumption vs Temperature



D002

Figure 5-6. TX Mode Current Consumption vs Temperature

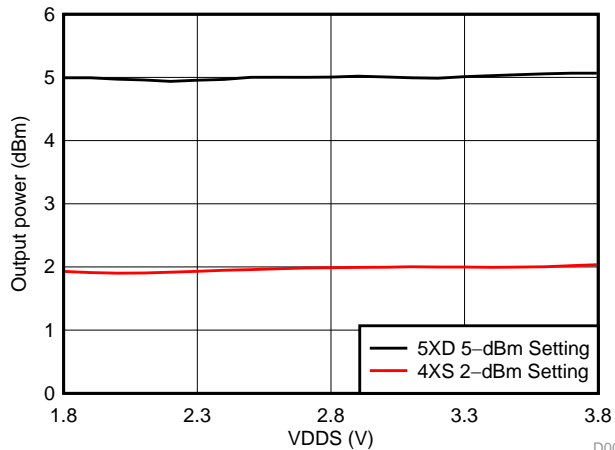


Figure 5-7. TX Output Power vs Supply Voltage (VDD5)

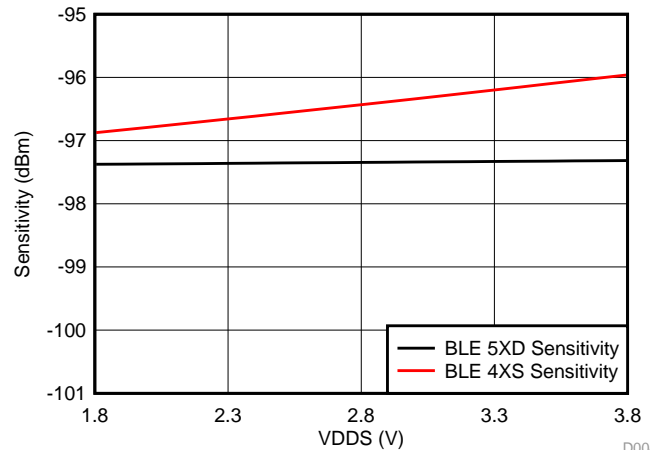


Figure 5-8. BLE Sensitivity vs Supply Voltage (VDD5)

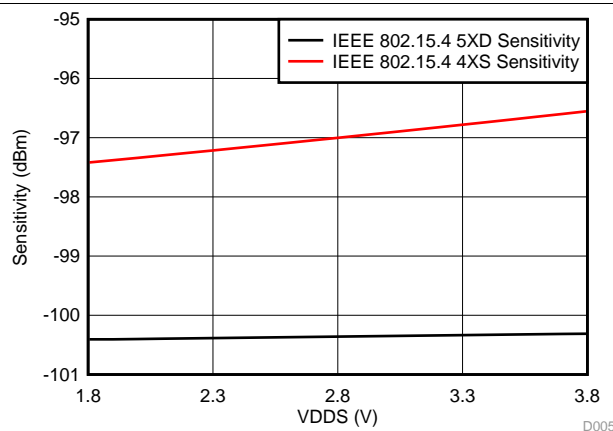


Figure 5-9. IEEE 802.15.4 Sensitivity vs Supply Voltage (VDD5)

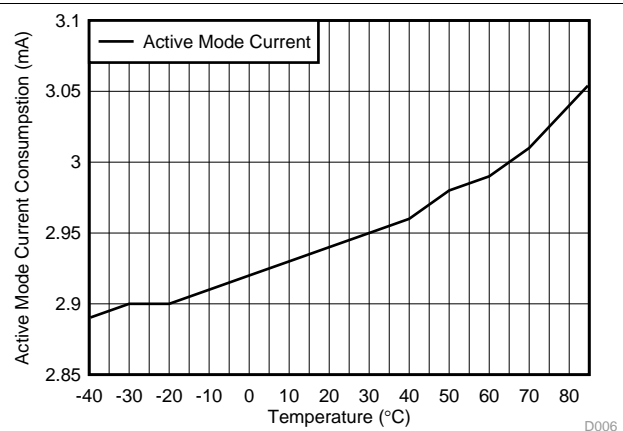


Figure 5-10. Active Mode Current Consumption vs Temperature

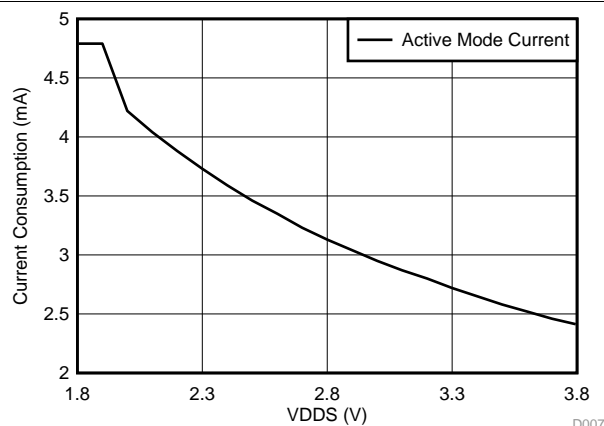


Figure 5-11. Active Mode Current Consumption vs Supply Voltage (VDD5)

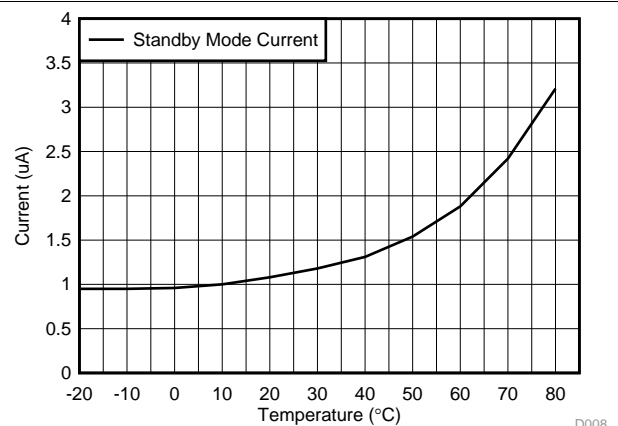


Figure 5-12. Standby Mode Current Consumption With RCOSC RTC vs Temperature

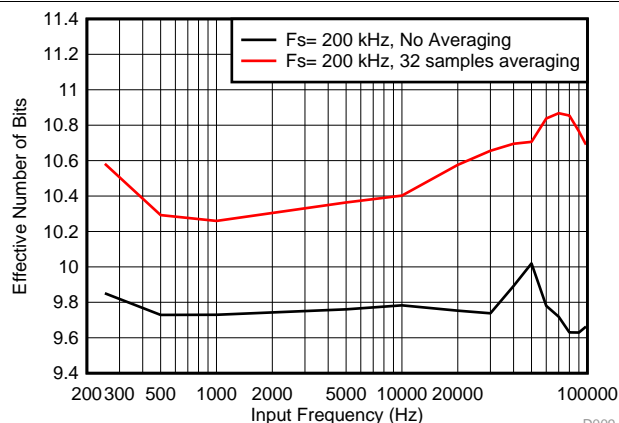


Figure 5-13. Effective Number of Bits vs Input Frequency (Internal Reference, No Scaling)

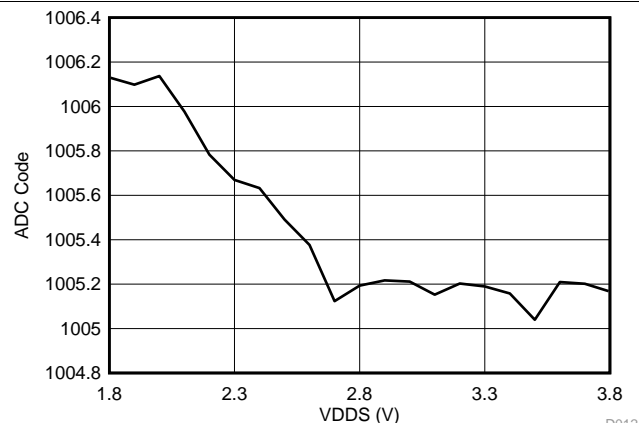


Figure 5-14. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

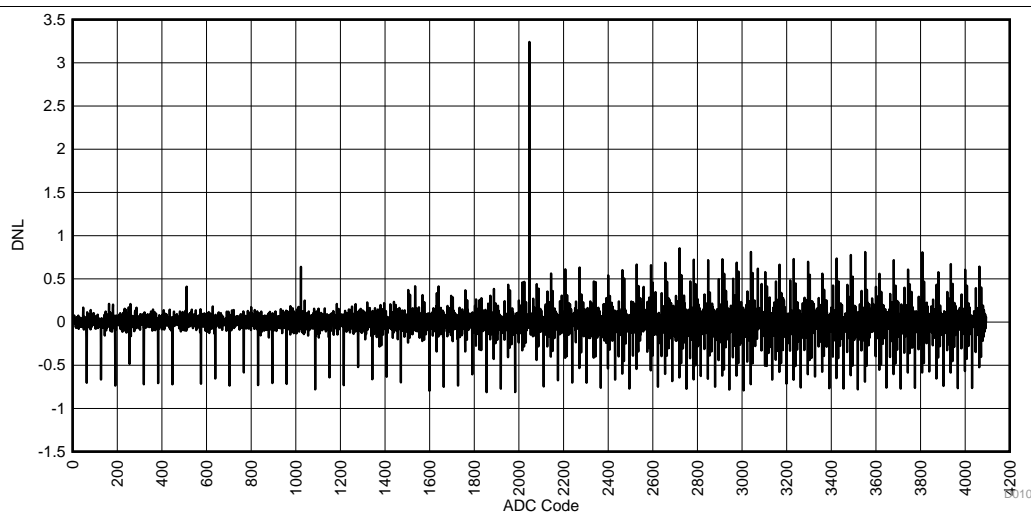


Figure 5-15. DNL vs. ADC Code (Internal Reference, No Scaling)

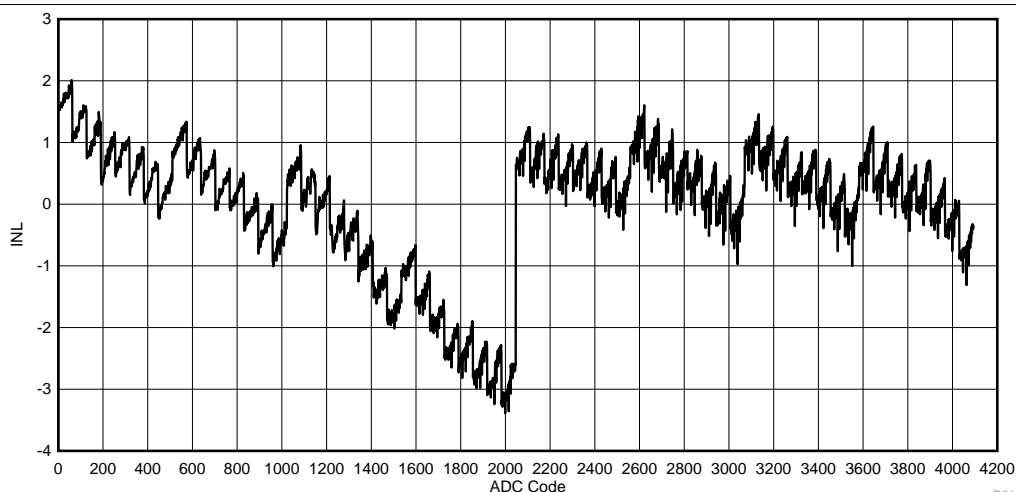
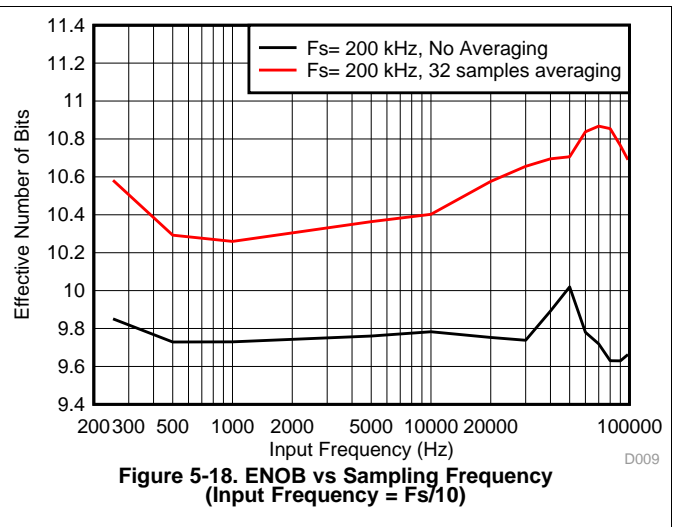
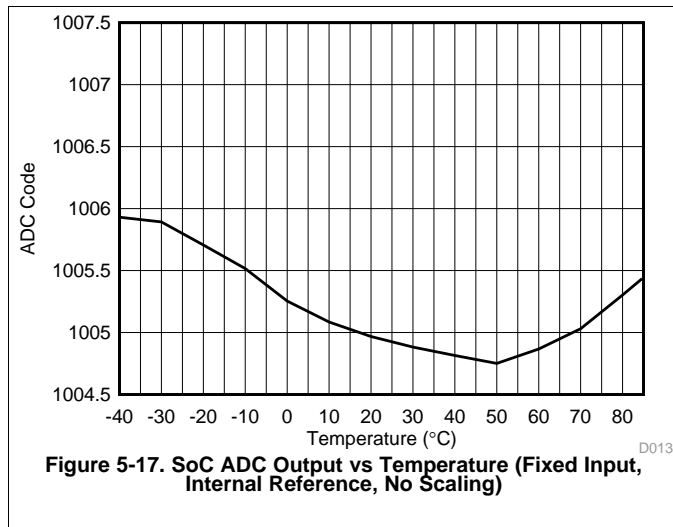


Figure 5-16. INL vs. ADC Code (Internal Reference, No Scaling)



6 Detailed Description

6.1 Overview

节 1.4 shows a block diagram of the core modules of the CC26xx product family.

6.2 Main CPU

The SimpleLink CC2650 Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

CM3 features include:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32 bit instruction set delivers the high performance expected of a 32 bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
 - Single-cycle multiply instruction and hardware divide
 - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
 - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.3 RF Core

The RF Core contains an ARM Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (802.15.4 RF4CE and ZigBee, *Bluetooth* Low Energy) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The ARM Cortex-M0 processor is not programmable by customers.

6.4 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main CM3 CPU.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and typical use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs and bit-banged I²C and/or SPI
- UART communication for sensor reading or debugging
- Capacitive sensing
- Waveform generation
- Pulse counting
- Keyboard scan
- Quadrature decoder for polling rotation sensors
- Oscillator calibration

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200 ksamples/s ADC with 8 inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI/I²C digital interface.
- The analog modules can be connected to up to 8 different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1. GPIOs Connected to the Sensor Controller⁽¹⁾

ANALOG CAPABLE	7 × 7 RGZ DIO#	5 × 5 RHB DIO#	4 × 4 RSM DIO#
Y	30	14	
Y	29	13	
Y	28	12	
Y	27	11	9
Y	26	9	8
Y	25	10	7
Y	24	8	6
Y	23	7	5
N	7	4	2
N	6	3	1
N	5	2	0
N	4	1	
N	3	0	
N	2		
N	1		
N	0		

(1) Depending on the package size, up to 16 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules

6.5 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI RTOS kernel, Driverlib and lower layer protocol stack software (802.15.4 MAC and *Bluetooth* Low Energy Controller). It also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.7 Power Management

To minimize power consumption, the CC2650 supports a number of power modes and power management features (see [Table 6-2](#)).

Table 6-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.45 mA + 31 µA/MHz	550 µA	1 µA	0.15 µA	0.1 µA
Wake-up Time to CPU Active ⁽¹⁾	–	14 µs	151 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on Pin Edge	Available	Available	Available	Available	Off
Wake-up on Reset Pin	Available	Available	Available	Available	Available

(1) Not including RTOS overhead

In Active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [Table 6-2](#)).

In Idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into Active mode.

In Standby, only the AON (Always-on) domain is active. An external wake event, RTC event, or Sensor Controller event is required to bring the device back to Active. MCU peripherals with retention do not need to be reconfigured when waking up again and the CPU will continue execution from where it went into Standby. All GPIOs are latched in Standby.

In Shutdown, the device is entirely turned off, including the AON domain and Sensor Controller, I/Os are latched with the value they had before entering Shutdown. A change of state on any I/O pin defined as a "wake from Shutdown pin" will wake up the device and function as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU. This means that the main CPU does not have to wake up to for example execute an ADC sample or poll a digital sensor over SPI, and saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the Sensor Controller and choose which peripherals are controlled and which conditions will wake up the main CPU.

6.8 Clock Systems

The CC2650 supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. *Bluetooth* low energy requires a slow-speed clock with better than ± 500 ppm accuracy if the device is to enter any sleep mode while maintaining a connection. The internal 32-kHz RC oscillator can in some use cases be compensated to meet the requirements. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48 MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768 kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in [Section 4](#)).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps and is compatible with the *Bluetooth* HCI specifications.

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I²C interface is used to communicate with devices compatible with the I²C standard. The I²C interface is capable of 100 kHz and 400 kHz operation, and can serve as both I²C master and I²C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (μ DMA) controller. The μ DMA controller provides a way to offload data transfer tasks from the CM3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The μ DMA controller can perform transfer between memory and peripherals. The μ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the μ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except for in Shutdown (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

6.10 System Architecture

Depending on the product configuration, CC26xx can function either as a Wireless Network Processor (WNP – an IC running the wireless protocol stack, with the application running on a separate MCU), or as a System-on-Chip (SoC), with the application and protocol stack running on the ARM CM3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application Circuit

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Few external components are required for the operation of the CC2650 device. [Figure 7-1](#) shows a typical application circuit. For a complete reference design, see the product folder on [www.ti.com](#).

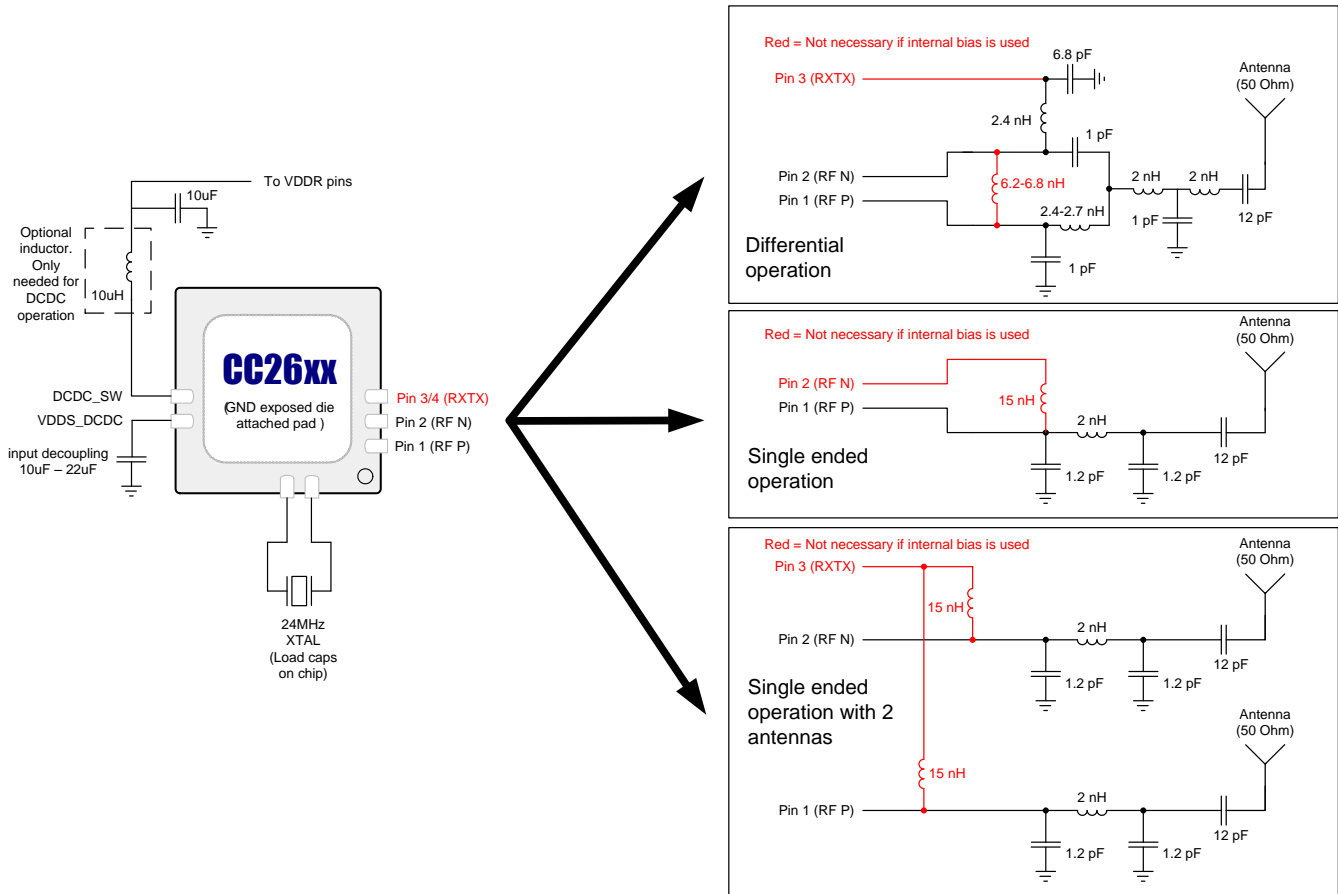


Figure 7-1. CC2650 Application Circuit

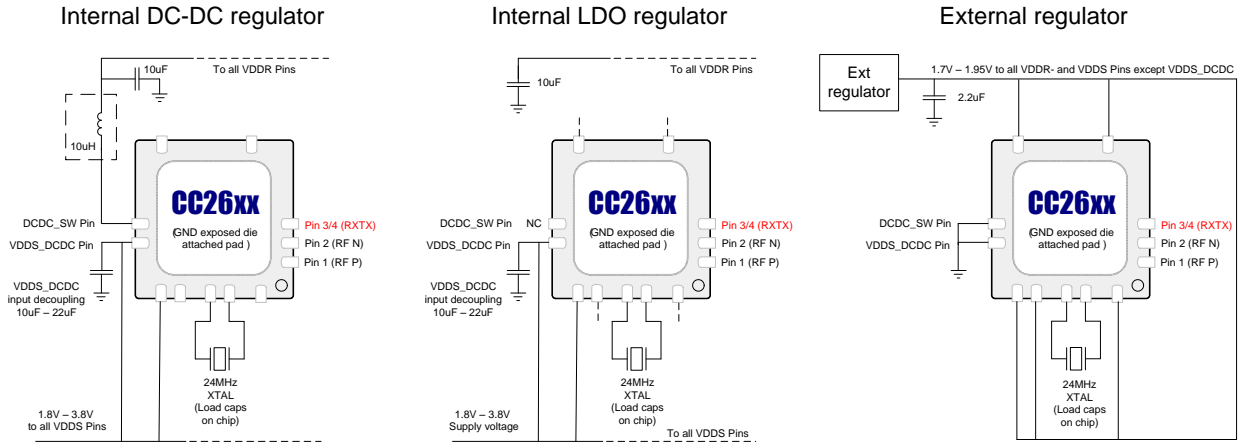


Figure 7-2. Supply Voltage Configurations

Power supply decoupling capacitors are not shown. Digital I/Os not included. Pin positions, and component values are not final. For detailed overview of power supply decoupling and wiring, see the TI reference designs and the CC26xx technical reference manual (节 8.2).

Figure 7-1 shows that the RF front end can be used both differentially and single-endedly with the option of having internal or external biasing. These options allow for various trade-offs between cost, board-space, and RF performance. Differential operation with external bias gives the best performance while single-ended operation with internal bias gives the least amount of external components and the lowest power consumption.

8 器件和文档支持

8.1 器件支持

8.1.1 开发支持

TI 提供大量的开发工具，其中包括评估处理器性能、生成代码、开发算法工具、以及完全集成和调试软件及硬件模块的工具。

以下产品为开发 CC2650 器件应用提供支持：

软件工具：

SmartRF Studio 7:

SmartRF Studio 是一款 PC 应用程序，可帮助无线电系统设计人员评估早期设计过程的 RF-IC。

- 测试无线数据包收发功能，连续波收发功能
- 将相关数据写入支持的评估板或调试器，评估定制板上的 RF 性能
- 可以不搭配任何硬件使用，但此时只能生成、编辑并导出无线配置设置
- 可与德州仪器 (TI) CCxxxx 系列 RF-IC 的多款开发套件搭配使用

Sensor Controller Studio:

Sensor Controller Studio 为 CC26xx 传感器控制器提供开发环境。此传感器控制器是 CC26xx 系列中的一款专用功率优化型 CPU，可独立于系统 CPU 状态自主执行简单的后台任务。

- 允许使用 C 语言这类编程语言实现传感器控制器任务算法
- 输出传感器控制器接口驱动程序，其中整合了生成的传感器控制器机械代码和相关定义
- 通过使用集成传感器控制器任务测试和调试功能实现快速开发 这有助于实现有效的传感器数据和算法验证可视化。

IDE 和编译器:

Code Composer Studio:

- 带有项目管理工具和编辑器的集成开发环境
- Code Composer Studio (CCS) 6.1 及更高版本内置对 CC26xx 系列器件的支持功能。
- 优先支持的 XDS 调试器：XDS100v3、XDS110 和 XDS200
- 与 TI-RTOS 高度集成，支持 TI-RTOS 对象视图

IAR ARM Embedded Workbench

- 带有项目管理工具和编辑器的集成开发环境
- IAR EWARM 7.30.3 及更高版本内置对 CC26xx 系列器件的支持功能。
- 广泛的调试器支持，支持 XDS100v3、XDS200、IAR I-Jet 和 Segger J-Link
- 带有项目管理工具和编辑器的集成开发环境
- 适用于 TI-RTOS 的 RTOS 插件

有关 CC2650 平台开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com。有关定价和购买信息，请联系最近的 TI 销售办事处或授权分销商。

8.1.2 器件命名规则

为了标明产品开发周期的各个产品阶段，TI 为所有部件号和/或日期代码添加了前缀。每个器件都具有以下三个前缀/标识中的一个：X、P 或无（无前缀）（例如，CC2650 正在批量生产；因此未分配前缀/标识）。

器件开发进化流程：

- | | |
|----------|-----------------------------------|
| X | 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。 |
| P | 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。 |
| 无 | 完全合格的芯片模型的生产版本。 |

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如，*RSM*）。

要获得 CC2650 器件（采用 *RSM*、*RHB* 或 *RGZ* 封装类型）的订购部件号，请参见本文档的“封装选项附录”（TI 网站www.ti.com），或者联系您的 TI 销售代表。

8.2 文档支持

以下文档介绍 CC2650。www.ti.com 网站上提供了这些文档的副本。

SWCU117 技术参考手册。德州仪器 (TI) CC26xx 系列产品

SWRS058 芯片勘误表。德州仪器 (TI) CC26xx™ 系列产品

8.2.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范 and 标准且不一定反映 TI 的观点；请见 TI 的[使用条款](#)。

TI E2E™ 在线社区 **TI 工程师对工程师 (E2E) 社区**。此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。

德州仪器 (TI) 嵌入式处理器维基网站 **德州仪器 (TI) 嵌入式处理器维基网站**。此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

8.3 其他信息

德州仪器 (TI) 为工业和消费类应用中所使用的专有应用和标准无线应用提供各种经济实用的低功耗射频解决方案。其中包括适用于 1GHz 以下频段和 2.4GHz 频段的射频收发器、射频发送器、射频前端和片上系统以及各种软件解决方案。

此外，德州仪器 (TI) 还提供广泛的相关支持，例如开发工具、技术文档、参考设计、应用专业技术、客户支持、第三方服务以及大学计划。

低功耗射频 **E2E** 在线社区设有技术支持论坛并提供视频和博客，您有机会在此与全球同领域工程师交流互动。

凭借丰富的供选产品解决方案、可实现的最终应用以及广泛的技术支持，德州仪器 (TI) 能够为您提供最全面的低功耗射频产品组合。

8.3.1 德州仪器 (TI) 低功耗射频网站

德州仪器 (TI) 的低功耗射频网站提供所有最新产品、应用和设计笔记、FAQ 部分、新闻资讯以及活动更新。请访问 www.ti.com/lprf。

8.3.2 低功耗射频在线社区

- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

访问：www.ti.com/lprf-forum 立即体验。

8.3.3 德州仪器 (TI) 低功耗射频开发者网络

德州仪器 (TI) 建立了一个大型低功耗射频开发合作伙伴网络，帮助客户加快应用开发。此网络中包括推荐的公司、射频顾问和独立设计工作室，他们可提供一系列硬件模块产品和设计服务，其中包括：

- 射频电路、低功耗射频和 ZigBee 设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

如果需要有关模块、工程服务或开发工具的帮助：

请搜索[低功耗射频开发者网络](http://www.ti.com/lprfnetwork)查找适合的合作伙伴。www.ti.com/lprfnetwork

8.3.4 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，您能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问：www.ti.com/lprfnewsletter 立即注册

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Bluetooth is a registered trademark of Bluetooth SIG, Inc.
CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.
IEEE Std 1241 is a trademark of Institute of Electrical and Electronics Engineers, Incorporated.
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8.5 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

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8.7 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

9 机械封装和可订购信息

9.1 封装信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2650F128RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2650 F128	Samples
CC2650F128RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2650 F128	Samples
CC2650F128RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2650 F128	Samples
CC2650F128RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2650 F128	Samples
CC2650F128RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2650 F128	Samples
CC2650F128RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2650 F128	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

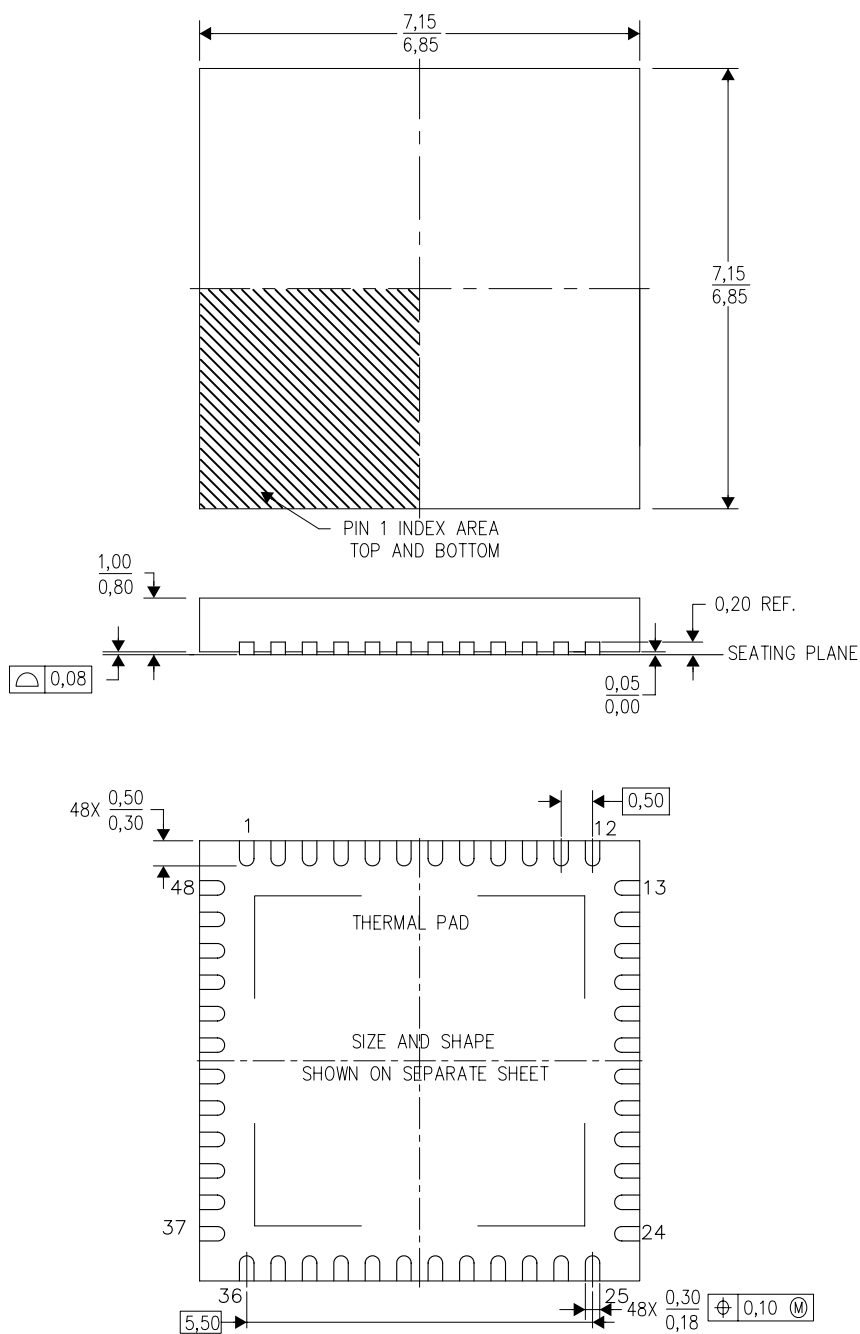
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

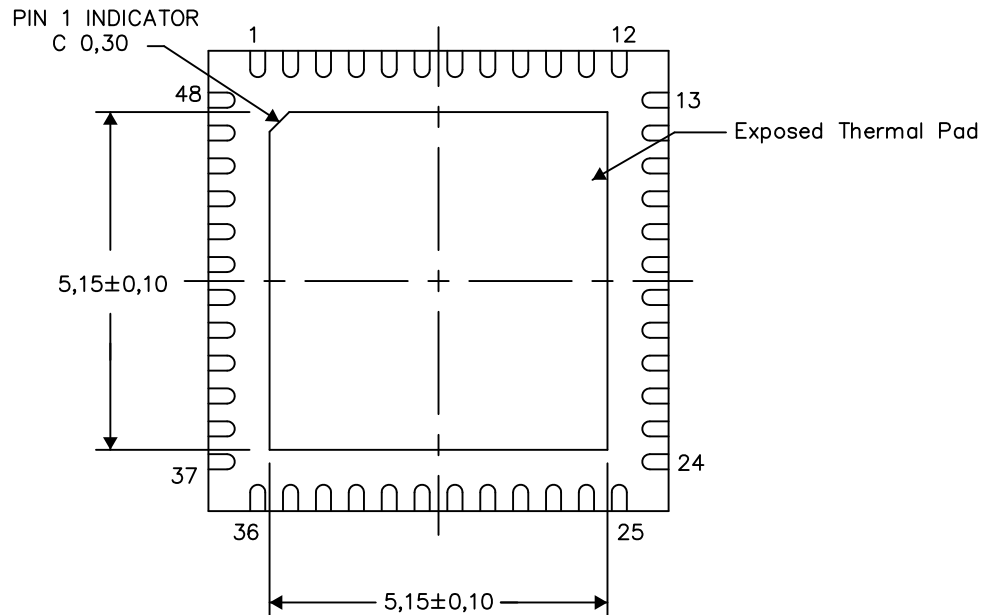
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

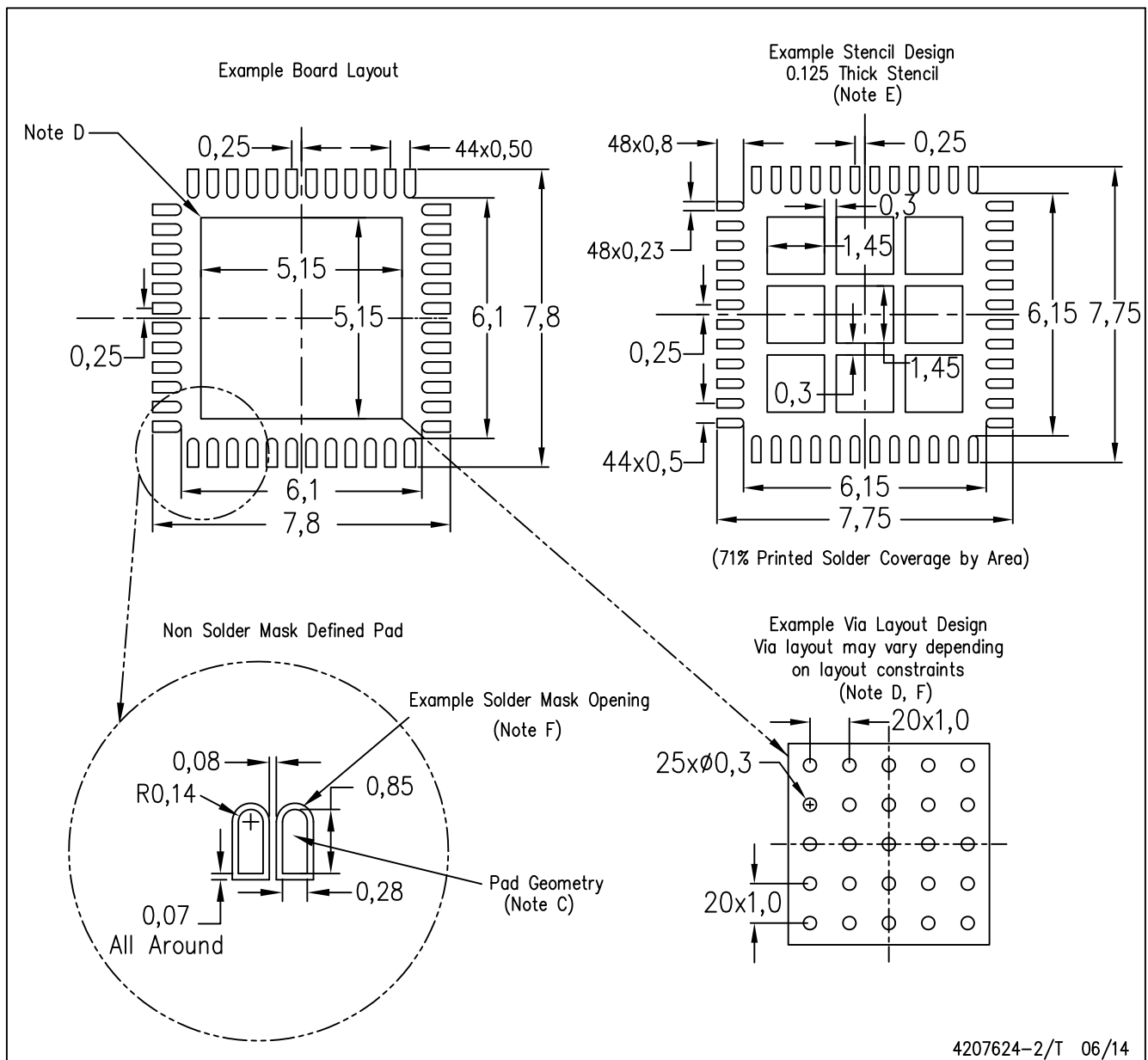
Exposed Thermal Pad Dimensions

4206354-2/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

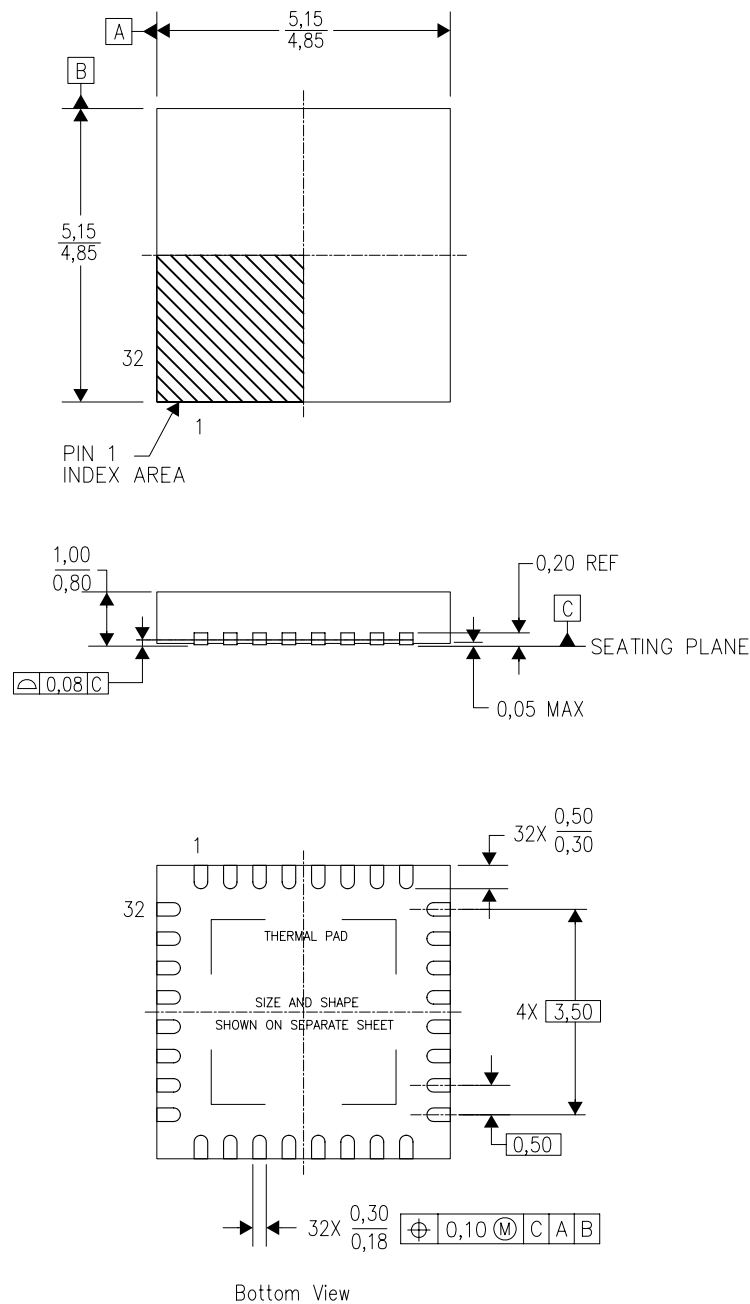
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD

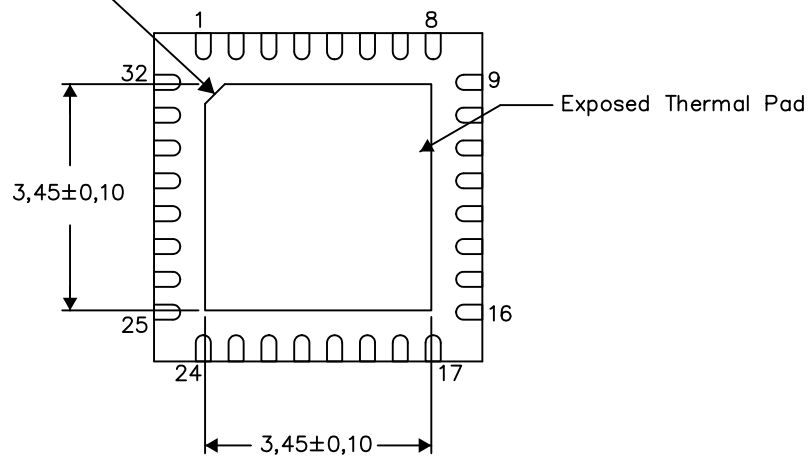
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
(OPTIONAL)



Bottom View

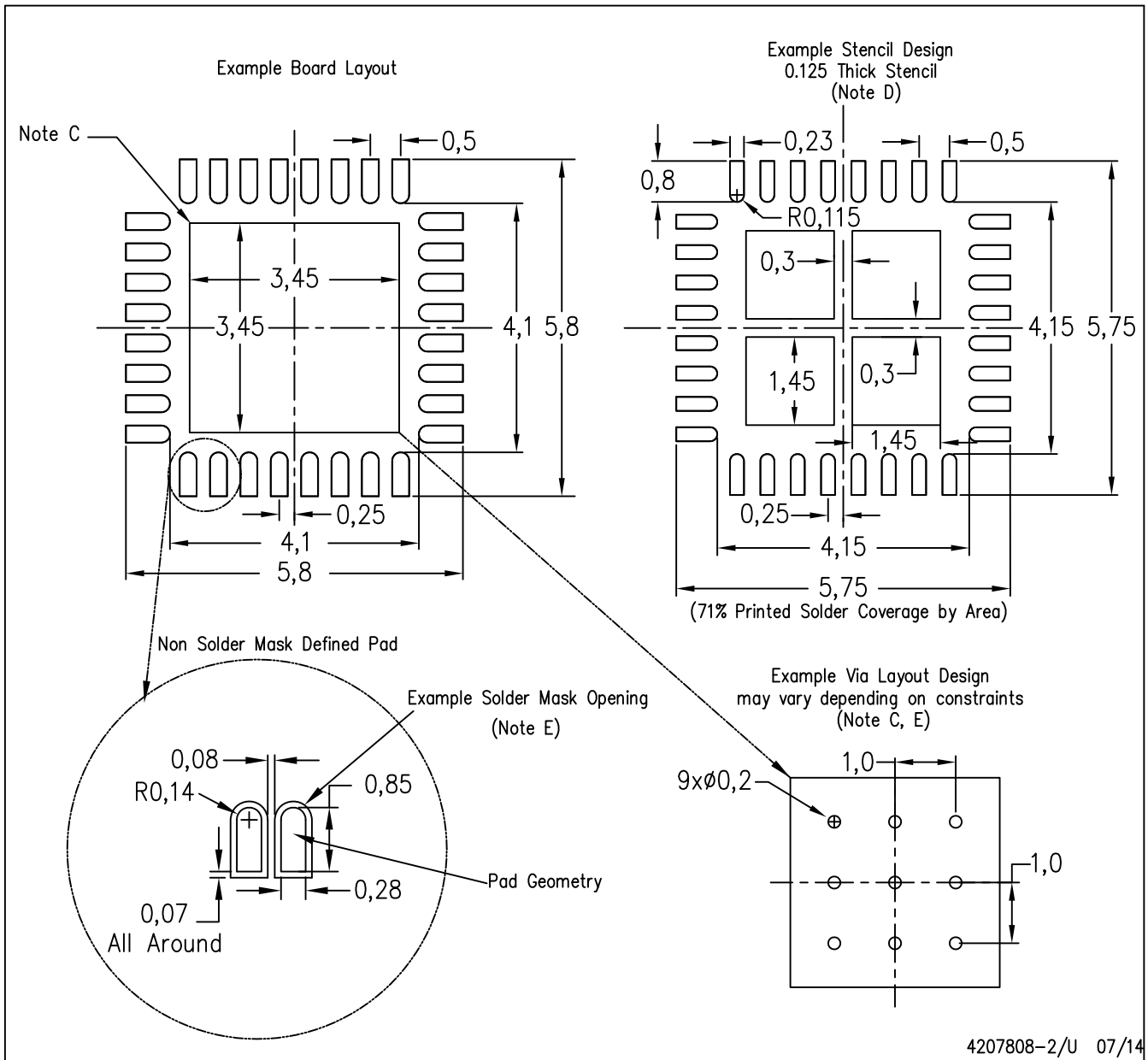
Exposed Thermal Pad Dimensions

4206356-2/AB 07/14

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

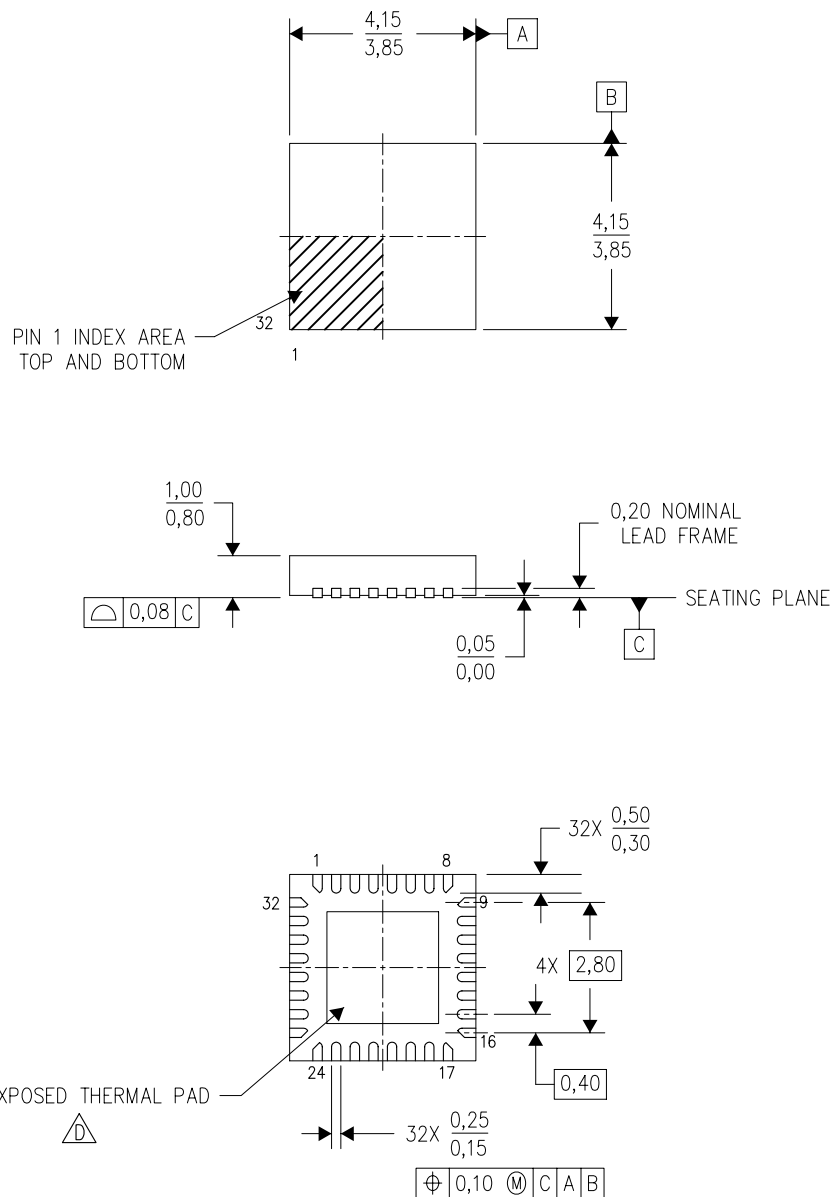
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207560/B 03/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

RSM (S-PVQFN-N32)

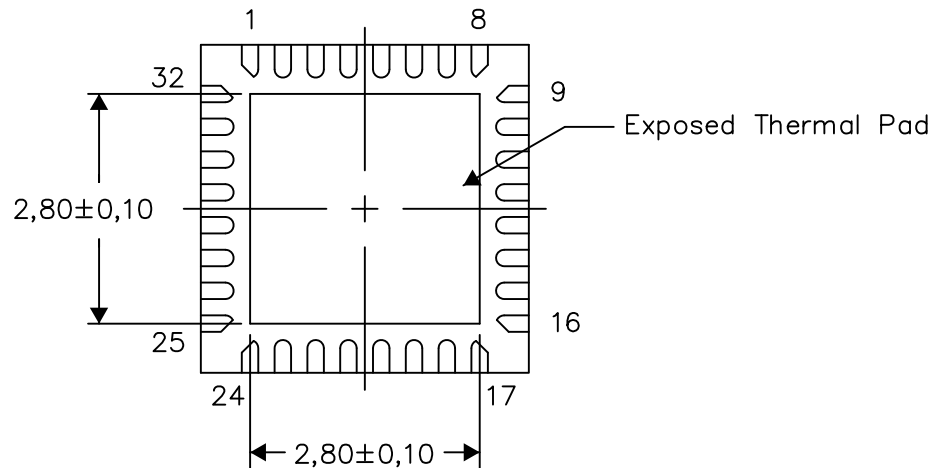
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

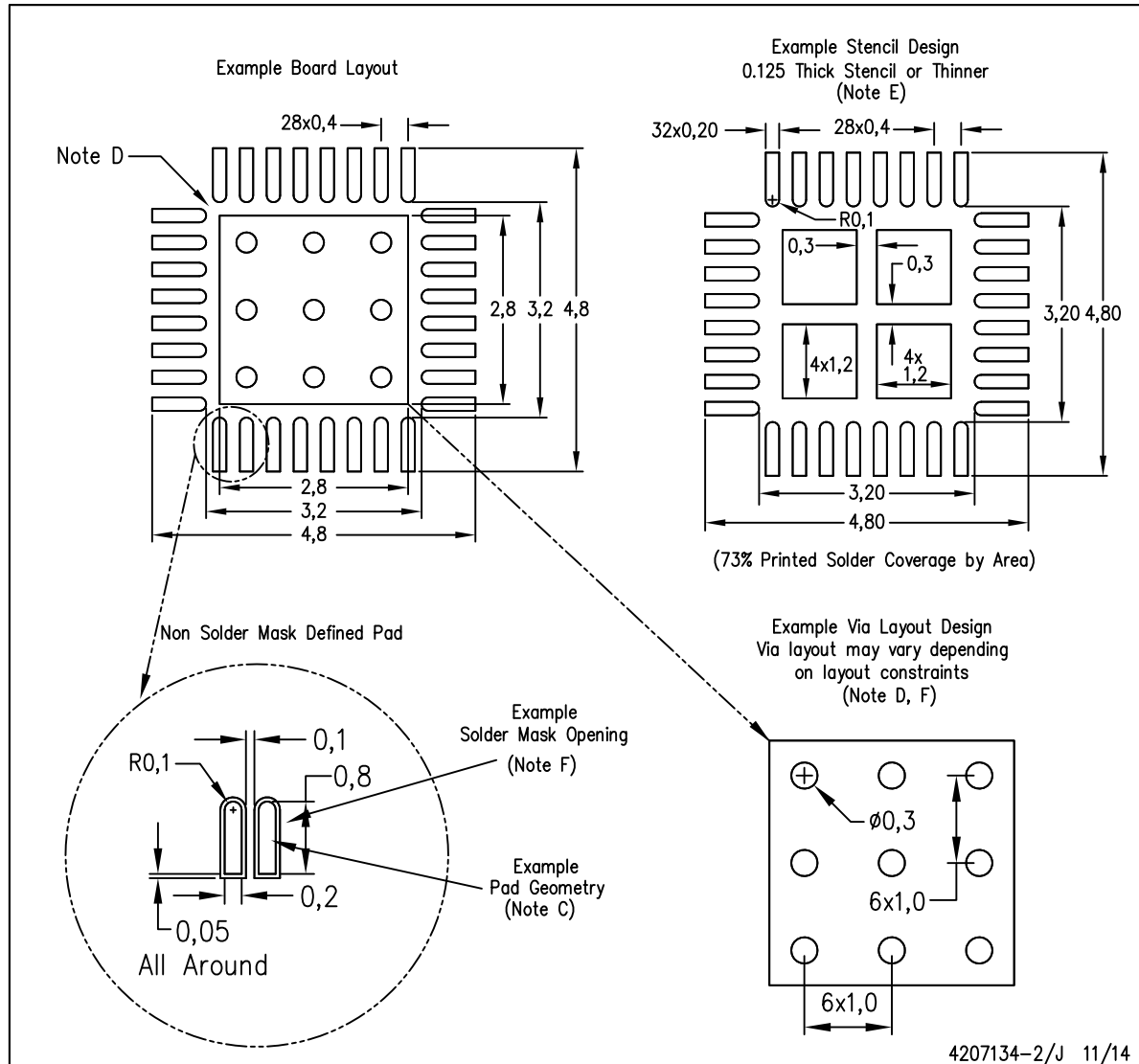
Exposed Thermal Pad Dimensions

4207868-2/1 07/14

NOTE: All linear dimensions are in millimeters

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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