GreenRio microarchitecture performance improvement

1. Finishing your Greenrio performance model (frontend, backend, and uncore part)
   The backend model and the uncore model have not been completed yet, and will be uploaded to the cmodel folder later.
2. Searching for original Greenrio performance issues/bugs by comparing against the model, the more the better
   The improvement points of the original Greenrio：
   1. 指令集方面：The original Greenrio只支持RISC-V I extension，为使得Greenrio能适用于更多场景，可以在此基础上增加对M（整数乘除法）、A（原子扩展）、C（压缩扩展）、D（双精度浮点扩展）等扩展指令的支持。
   2. RISC-V特权架构方面：RISC-V有三种模式，分别是U、S和M模式。The original Greenrio只支持最基本的M（Machine）模式，可以增加对U（User）、S（Supervisor）两种模式的支持。
   3. Branch prediction：The accuracy of original Greenrio‘s branch prediction is not high enough，可以从以下两个角度尝试进一步提高Branch prediction的准确率：
      1）收集程序运行的跳转信息：基于程序运行的上下文往往是相关的
      2）收集目标跳转指令更多的历史信息：构建更多位数的state，使用更精确（往往更复杂）的状态转移函数
   4. Single issue: 可以将单发射改为双发射，以此进一步提升架构的性能

EDA flow(Greenrio core RTL to GDS flow by openlane)

1. GDS generation - 10%

```
[SUCCESS]: Flow complete.
```

   1)使用Magic由上一步Routing得到的def文件输出GDSII格式文件

the log of GDSII with Magic：RUN_2023.01.17_13.52.52/logs/signoff/26-gdsii.log

```
Magic 8.3 revision 324 - Compiled on Thu Sep 15 11:38:02 UTC 2022.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(vendor): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Using technology "sky130A", version 1.0.341-2-gde752ec
Reading LEF data from file /work/stu/yaowei/workspace/OpenLane/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_
This action cannot be undone.
LEF read, Line 78 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 79 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 112 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 114 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 115 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 121 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 122 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 123 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 156 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 164 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 165 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 167 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
```

2)使用Klayout由上一步Routing得到的def文件输出GDSII格式文件
the log of GDSII with KLayout：
RUN_2023.01.17_13.52.52/logs/signoff/27-gdsii-klayout.log

```
Input: /openlane/designs/hehe/runs/RUN_2023.01.17_13.52.52/results/routing/hehe.def
Output: /openlane/designs/hehe/runs/RUN_2023.01.17_13.52.52/results/signoff/hehe.klayout.gds
Design: hehe
Technology File: /work/stu/yaowei/workspace/OpenLane/pdks/sky130A/libs.tech/klayout/tech/sky130A.lyt
GDS File List: ['/work/stu/yaowei/workspace/OpenLane/pdks/sky130A/libs.ref/sky130_fd_sc_hd/gds/sky130_fd_sc_hd.gds']
LEF File: /openlane/designs/hehe/runs/RUN_2023.01.17_13.52.52/tmp/merged.nom.lef

[INFO] Clearing cells...
[INFO] Merging GDS files...
    /work/stu/yaowei/workspace/OpenLane/pdks/sky130A/libs.ref/sky130_fd_sc_hd/gds/sky130_fd_sc_hd.gds
[INFO] Copying toplevel cell 'hehe'
WARNING: no fill config file specified
[INFO] Checking for missing GDS...
[INFO] All LEF cells have matching GDS cells
[INFO] Writing out GDS '/openlane/designs/hehe/runs/RUN_2023.01.17_13.52.52/results/signoff/hehe.klayout.gds'
[INFO] Done.

```

3)The final GDSII file can be found under：
RUN_2023.01.17_13.52.52/results/final/gds/hehe.gds

2. Signoff report generation: pass DRC/LVS check - 15%

Pass DRC/LVS :
1)the log of DRC: RUN_2023.01.17_13.52.52/logs/signoff/33-drc.log
2)the log of LVS: RUN_2023.01.17_13.52.52/logs/signoff/32lvs.lef.log

1. Briefly describe what DRC is：
   DRC(Design Rule Check)用于检查版图中各掩膜层图形的各种尺寸是否合乎设计规则的要求。版图的设计规则是根据具体工艺线所能生产的最小图形尺寸、最细线条宽度及线条间的间距来确定的，是集成电路版图设计工程师和工艺师之间的桥梁，可以说DRC是否通过基本上决定了工艺厂能否生产这个芯片。

   The DRC problems you have encountered：
   (I have not encountered such a problem)

   The common solutions：
   在进行版图的设计规则检查时主要是针对两个方面进行检查的：

   - 同一层的几何图形的宽度及间距
     对于同一层的设计规则检查时，情况比较简单，只需进行最小尺寸及最小宽度的检查
   - 不同层图形之间的间距及套刻间距
     不同层的套刻间距检查时，情况就比较复杂了。两个不同版图层的图形之间无非有四种关系：即完全嵌套、相交、相切及完全相分离。我们需要根据不同层图形间的相互关系定义出 DRC 所需的虚拟层，因此有必要对各层的图形进行一定的逻辑操作 (AND, NOT, OR, SIZE) 。 然后按照设计规则对其进行相应的检查。 可采用**diva**对所设计的版图进行检查。

2. Briefly describe what LVS is：
   LVS(Layout Versus Schematics)验证用于检查版图和电路是否匹配，检查版图网表与电路原理图网表是否一致，即所画版图器件连接与相应的电路图连接关系的一致性检查。如果LVS不通过，很多 sign off 步骤无法完成，比如反标（Back Annotation）流程就依赖于 LVS，而现阶段，时序 sign off 基本上都在用反标流程。换句话说，LVS决定了芯片的功能是否和设计预期一致，同时也在很大程度上决定了性能是否满足需求。

   the LVS problems you have encountered：
   遇到两类the LVS problems：

   - 失配器件
     失配器件：有的器件在版图中有，但在原理图中没有，或在原理

图中有而版图中没有

- 节点不一致和器件不一致
  1)节点不一致：版图与电路中各有一节点，这两个节点所连器件情况很相似，但又不完全相同。
  2)器件不一致：版图与电路中各有一器件，这两个器件相同，所接节点情况很相似，但又不完全相同。

The common solutions：
在完成 LVS 后要根据检查结果所报告的各种错误，修改版图，直到二者在结构上达到完全的一致。采用 **dracula** 对 SRAM 的版图进行了 LVS 检查，版图设计与原理图完全匹配。

3）Briefly analyze your signoff results in the lab report：

- 芯片版图的面积：3733856.064 um^2
- 此次flow的时钟频率：50MHz
- 各种gate的数量：

AND	DFF	NAND	NOR	OR	XOR	XNOR	MUX
3140	311	287	792	3449	1057	191	20763

- power：-1?
- Number of Error
  - Drc error：0
  - Lvs error：0
  - Antenna error: 0
- Number of warning：3
  [WARNING]: There are max slew violations in the design at the typical corner.
  [WARNING]: There are max fanout violations in the design at the typical corner.
  [WARNING]: There are max capacitance violations in the design at the typical corner.
- Number of violations:
  - Magic violations：0
  - TritonRoute violations：0
  - Antenna violations：0

- MinHole violations：0
- OffGrid violations：0
- MetSpc violations：0
- Short violations：0

If a warning/error still exists, point them out：
There are 3 warning/error still exists

- [WARNING]: There are max slew violations in the design at the typical corner.

- [WARNING]: There are max fanout violations in the design at the typical corner.

- [WARNING]: There are max capacitance violations in the design at the typical corner.

  3.There should be no setup or hold timing violations - 15%
  （1）No setup violations - 7.5%
  setup time：在触发器的时钟有效沿之前，数据输入端信号必须保持稳定的最短时间。如果setup time不够，数据将不能在这个时钟有效沿被打入触发器。
  setup violation的修复方法：
  ① T_clk：增加T_clk，也就是降频
  ② T_dp：优化组合逻辑延时，具体包括：
  a. 增加一个中间触发器来切割Timing Path，分割组合逻辑延时（流水线结构）
  b. 对于有较大负载的节点可以考虑插buffer、逻辑复制的方法来优化扇出，减少关键路径上的负载（插Buffer，逻辑复制）
  c. 小Cell换成大Cell，更换更大驱动的Cell，增强驱动能力
  d. 更换SVT/LVT的Cell
  ③ T_skew：采用positive skew(T_skew >0)，但是要注意可能引入的hold问题，以及前后级的margin问题
  ④ T_ck2q：更换更快的时序逻辑单元，如HVT->LVT
  before modification，there is setup timing violation：

```
[INFO]: Created metrics report at 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/metrics.csv'.
[WARNING]: There are max slew violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max capacitance violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are hold violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.min.rpt'.
[WARNING]: There are setup violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.max.rpt'.
[SUCCESS]: Flow complete.
```

after modification，the setup timing violation was solved.

```
[INFO]: Created metrics report at 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/metrics.csv'.
[WARNING]: There are max slew violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max capacitance violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/signoff/24-rcx_sta.slew.rpt'.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
```

（2）No hold violations - 7.5%

hold time：在触发器的时钟有效沿之后，数据输入端信号必须保持稳定的最短时间。如果hold time不够，数据同样不能被打入触发器。

hold violation的修复方法：

① T_dp：增加组合路径延时，通过插buffer、插delay cell、更换驱动、更换阈值的方法（组合逻辑深度的增加会增加芯片的面积、布线资源、功耗，可能产生在慢速工艺库条件下建立时间违例）

② T_skew：减小skew，甚至采用negative skew，但需做好时钟树的balance。

③ 插入低电平有效的锁存器(Lock-up Latch)：高电平期间，锁存器输出保持不变，相当于人为将数据推迟了半个时钟周期，以保证满足hold时间要求。

before modification，there is hold timing violation：

```
[INFO]: Created metrics report at 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/metrics.csv'.
[WARNING]: There are max slew violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max capacitance violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are hold violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.min.rpt'.
[WARNING]: There are setup violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.13_13.40.54/reports/signoff/24-rcx_sta.max.rpt'.
[SUCCESS]: Flow complete.
```

after modification，the setup hold violation was solved.

```
[INFO]: Created metrics report at 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/metrics.csv'.
[WARNING]: There are max slew violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/signoff/24-rcx_sta.slew.rpt'.
[WARNING]: There are max capacitance violations in the design at the typical corner. Please refer to 'designs/hehe/runs/RUN_2023.01.17_13.52.52/reports/signoff/24-rcx_sta.slew.rpt'.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
```