積體電路設計 HW2 report

B10505047 電機四 邱郁喆

1. Spice Source Code (input 以 0001+0001 為例)

```
* 4-bit ripple adder

.lib 'cic018.l' tt

***inverter***
.subckt inverter in out vdd gnd
MM1 out in gnd gnd N_18 l=0.18u w=0.25u
MM2 out in vdd vdd P_18 l=0.18u w=0.75u
.ends inverter

***full adder***
.subckt FullAdder A B Cin S C0 vdd gnd
* Mxxx nd ng ns nb mname <l=val> <w=val> <m=val>
M1  D1  A   vdd vdd P_18 l=0.18u w=0.75u m=1
M2  D1  B   vdd vdd P_18 l=0.18u w=0.75u m=1
M3  D2  Cin D1  vdd P_18 l=0.18u w=0.75u m=1
M4  D2  Cin D3  gnd N_18 l=0.18u w=0.25u m=1
M5  D3  A   gnd gnd N_18 l=0.18u w=0.25u m=1
M6  D3  B   gnd gnd N_18 l=0.18u w=0.25u m=1
M7  D4  A   vdd vdd P_18 l=0.18u w=0.75u m=1
M8  D2  B   D4  vdd P_18 l=0.18u w=0.75u m=1
M9  D2  B   D5  gnd N_18 l=0.18u w=0.25u m=1
M10 D5  A   gnd gnd N_18 l=0.18u w=0.25u m=1
M11 D6  A   vdd vdd P_18 l=0.18u w=0.75u m=1
M12 D6  B   vdd vdd P_18 l=0.18u w=0.75u m=1
M13 D6  Cin vdd vdd P_18 l=0.18u w=0.75u m=1
M14 D7  D2  D6  vdd P_18 l=0.18u w=0.75u m=1
M15 D7  D2  D8  gnd N_18 l=0.18u w=0.25u m=1
M16 D8  A   gnd gnd N_18 l=0.18u w=0.25u m=1
M17 D8  B   gnd gnd N_18 l=0.18u w=0.25u m=1
M18 D8  Cin gnd gnd N_18 l=0.18u w=0.25u m=1
M19 D9  A   vdd vdd P_18 l=0.18u w=0.75u m=1
M20 D10 B   D9  vdd P_18 l=0.18u w=0.75u m=1
M21 D7  Cin D10 vdd P_18 l=0.18u w=0.75u m=1
M22 D7  Cin D11 gnd N_18 l=0.18u w=0.25u m=1
M23 D11 B   D12 gnd N_18 l=0.18u w=0.25u m=1
M24 D12 A   gnd gnd N_18 l=0.18u w=0.25u m=1

* Use inverters for C0 and S
Xinv1 D2 C0 vdd gnd inverter
Xinv2 D7 S  vdd gnd inverter

.ends FullAdder

***4-bit ripple adder***
.subckt RippleAdder A1 B1 A2 B2 A3 B3 A4 B4 Cin S1 S2 S3 S4 Cout vdd gnd
XFA1 A1 B1 Cin S1 C1   vdd gnd FullAdder
XFA2 A2 B2 C1  S2 C2   vdd gnd FullAdder
XFA3 A3 B3 C2  S3 C3   vdd gnd FullAdder
XFA4 A4 B4 C3  S4 Cout vdd gnd FullAdder
.ends RippleAdder

***instantiate ripple adder***
XRippleAdder A1 B1 A2 B2 A3 B3 A4 B4 Cin S1 S2 S3 S4 Cout vdd gnd RippleAdder

***independent source***
VDD vdd 0 DC 1.8V
VSS gnd 0 DC 0V
* Input sources for A = 0001, B = 0001, Cin = 0
* PULSE ( V1 V2 Tdelay Trise Tfall Pwidth Period )
VA1 A1 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
VA2 A2 0 DC 0V
VA3 A3 0 DC 0V
VA4 A4 0 DC 0V

VB1 B1 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
VB2 B2 0 DC 0V
VB3 B3 0 DC 0V
VB4 B4 0 DC 0V

VCin Cin 0 DC 0V

.op
.option post

.tran 1n 1u

.probe v(S1) v(S2) v(S3) v(S4) v(Cout)

.end
```

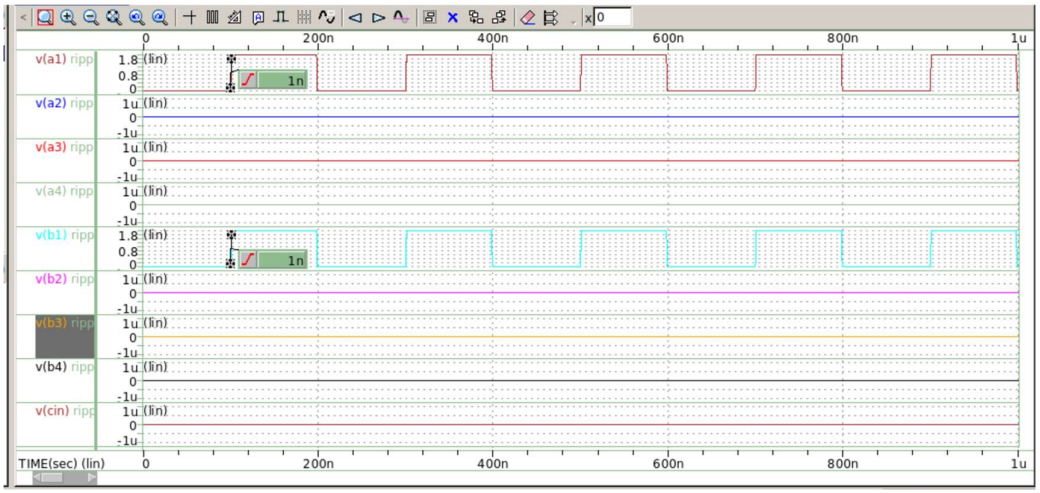
若 input 為 1111 + 0001，則 61-69 行：

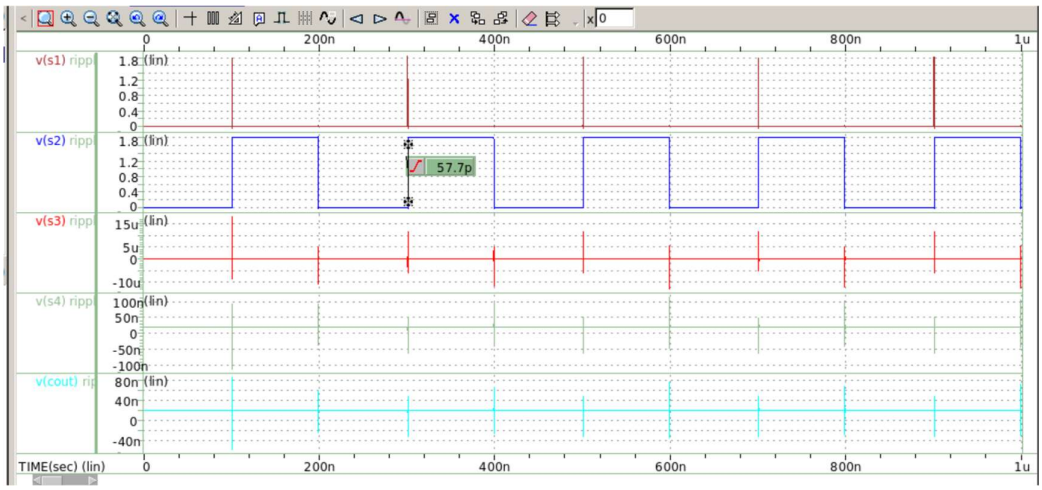
```
61  VA1 A1 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
62  VA2 A2 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
63  VA3 A3 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
64  VA4 A4 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
65
66  VB1 B1 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
67  VB2 B2 0 DC 0V
68  VB3 B3 0 DC 0V
69  VB4 B4 0 DC 0V
```

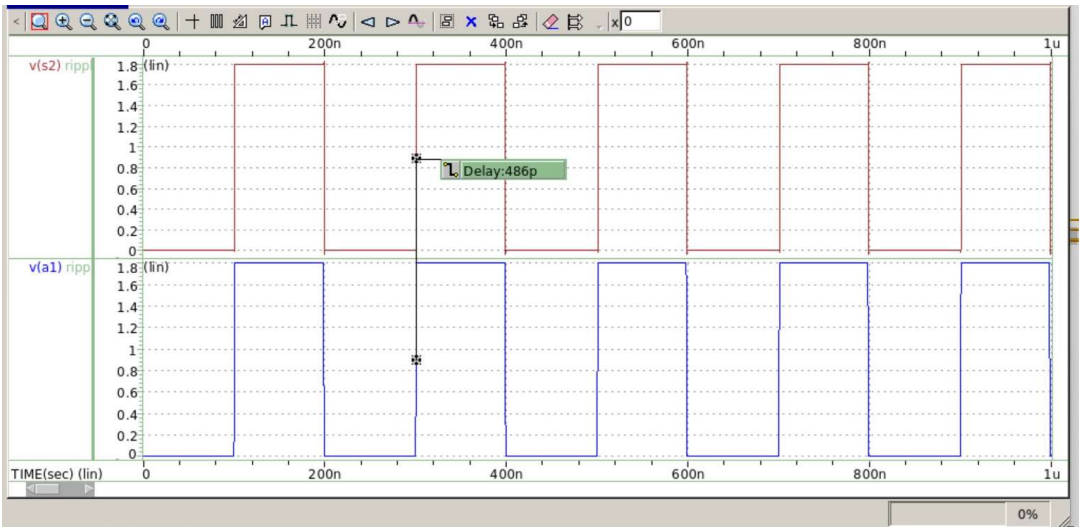
若 input 為 0101 + 1010，則 61-69 行：

```
61  VA1 A1 0 DC 0V
62  VA2 A2 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
63  VA3 A3 0 DC 0V
64  VA4 A4 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
65
66  VB1 B1 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
67  VB2 B2 0 DC 0V
68  VB3 B3 0 PULSE(0V 1.8V 100ns 1.25ns 1.25ns 97ns 200ns)
69  VB4 B4 0 DC 0V
```

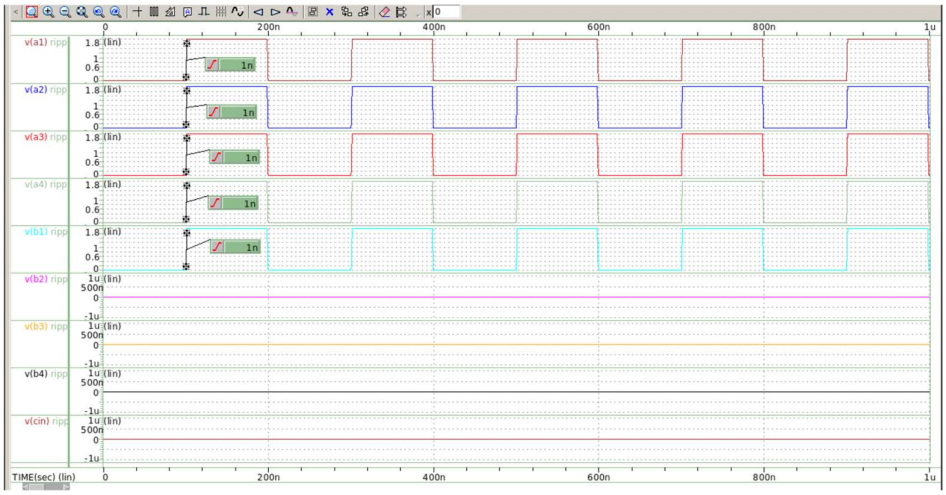
2. a) 0001 + 0001

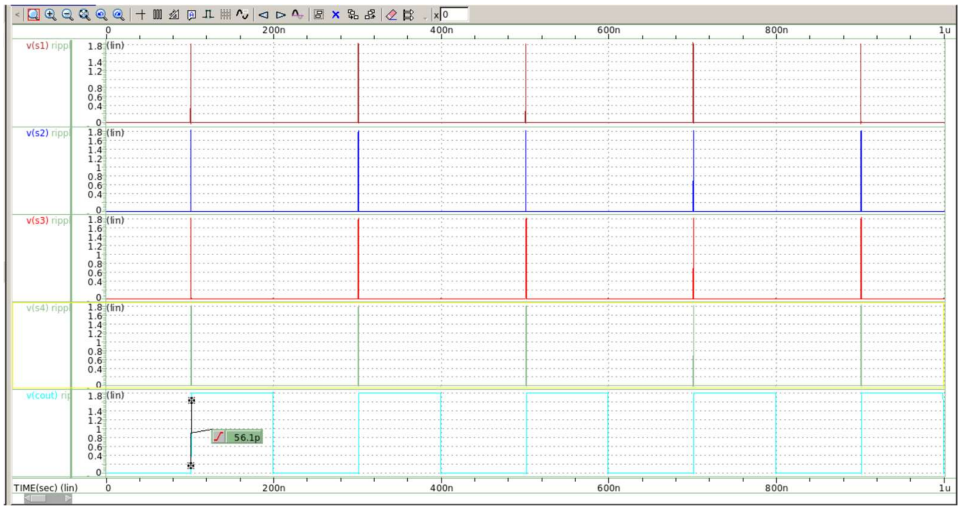


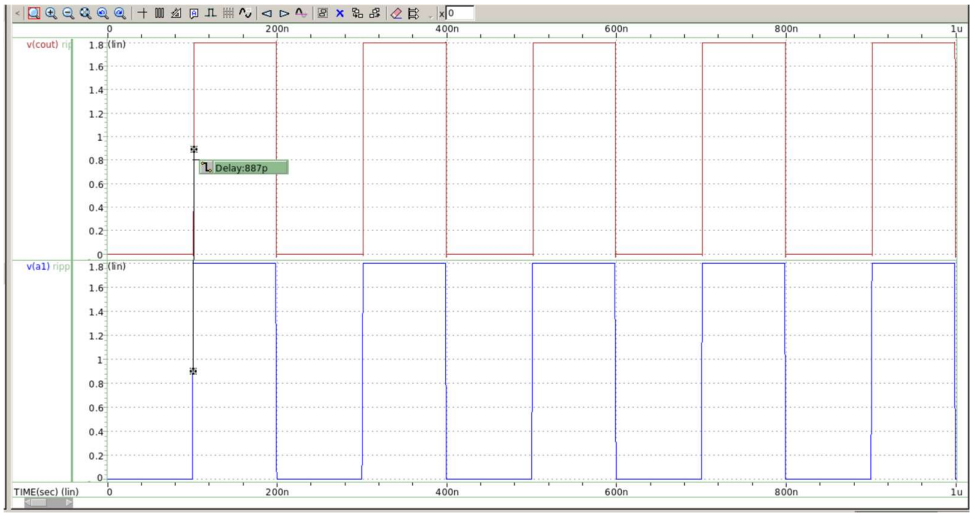



v(s2) ripp
v(a1) ripp
(lin)
Delay:486p
TIME(sec) (lin)
0
200n
400n
600n
800n
1u
0%

b) 1111 + 0001

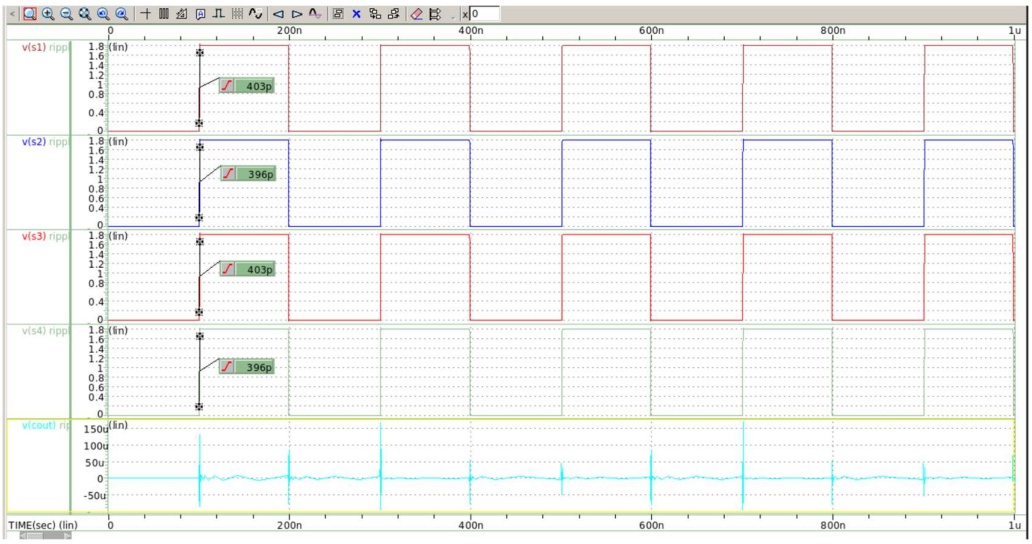

v(a1) ripp
v(a2) ripp
v(a3) ripp
v(a4) ripp
v(b1) ripp
v(b2) ripp
v(b3) ripp
v(b4) ripp
v(cin) ripp
1n
TIME(sec) (lin)

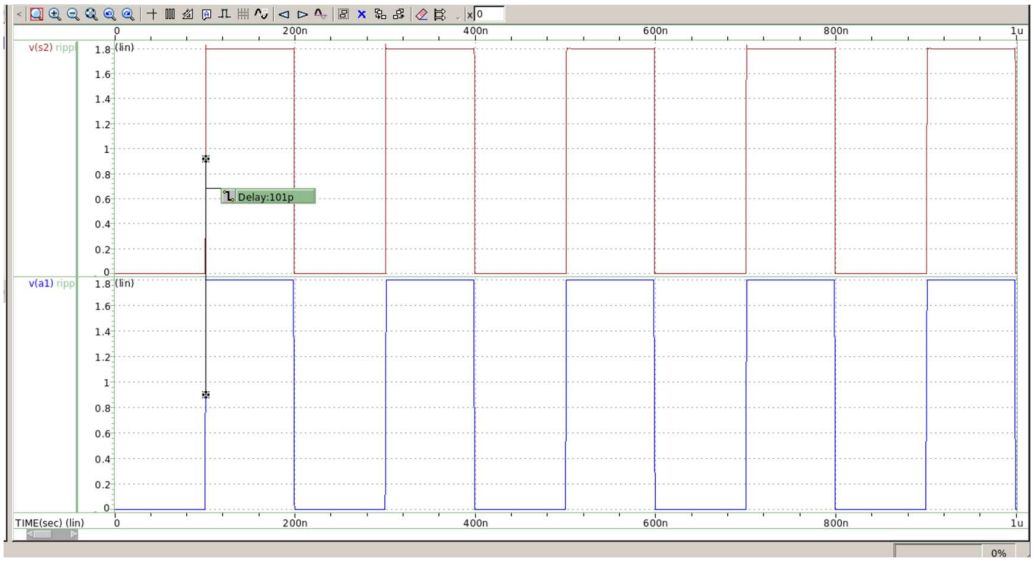

v(s1) ripp
v(s2) ripp
v(s3) ripp
v(s4) ripp
v(cout) rip
56.1p
TIME(sec) (lin)


v(cout)
v(a1)
Delay:887p
TIME(sec) (lin)

c) 0101 + 1010


v(a1)
v(a2)
v(a3)
v(a4)
v(b1)
v(b2)
v(b3)
v(b4)
v(cin)
1n
TIME(sec) (lin)


v(s1)
v(s2)
v(s3)
v(s4)
v(cout)
403p
396p
TIME(sec) (lin)



3. a) Output delay is the delay from a1 to s2, which is 486ps.
   b) Output delay is the delay from a1 to cout, which is 887ps.
   c) Output delay is the delay from a1 to s2, which is 101ps.