Stellaris® LM3S9B92 RevB1 Errata

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Date	Revision	Description

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Erratum Number	Erratum Title	Revision(s) Affected

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1 JTAG

1.1 JTAG INTEST instruction does not work

Description:

Workaround:

Silicon Revision Affected:

Fixed:

1.2 The Recover Locked Device sequence does not work as expected

Description:

Workaround:

1.

2.

3.

4.

Silicon Revision Affected:

Fixed:

2 System Control

2.1 Sleep and Deep-Sleep mode not usable at higher speeds when ISRs reside in Flash memory

Description:

Workaround:

1.

2.

Silicon Revision Affected:

Fixed:

2.2 Device Capabilities registers may not accurately reflect available signals

Description:

DC3 DC4 DC5 DC8

Workaround:

Silicon Revision Affected:

Fixed:

2.3 The PIOSC is not trimmed by the factory

Description:

Workaround:

Silicon Revision Affected:

Fixed:

3 Internal Memory

3.1 Cumulative page erases may introduce bit errors in Flash memory

Description:

Workaround:

1.

2.

Silicon Revision Affected:

Fixed:

3.2 Flash Write Buffer does not function above 50 MHz

Description:

Workaround:

Silicon Revision Affected:

Fixed:

4 ROM

4.1 Ethernet fails to connect when using the Boot Loader software in ROM

Description:

Workaround:

Silicon Revision Affected:

Fixed:

4.2 Some ROM functions are unsupported

Description:

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Workaround:

Silicon Revision Affected:

Fixed:

4.3 ROM mapping check for the Boot loader does not function properly

Description:

Workaround:

Silicon Revision Affected:

Fixed:

4.4 ROM_I2CMasterErr function is incorrect

Description:

I2CMCS

Workaround:

Silicon Revision Affected:

Fixed:

4.5 ROM_SSIConfigSetExpClk function is incorrect

Description:

Workaround:

Silicon Revision Affected:

Fixed:

4.6 ROM_USBFIFOFlush function is incorrect

Description:

Workaround:

Silicon Revision Affected:

Fixed:

4.7 The option to force the ROM boot loader to execute at reset with an external pin does not function

Description:

PORT PIN **Boot Configuration (BOOTCFG)**

Workaround:

Silicon Revision Affected:

Fixed:

5 µDMA

5.1 The µDMA controller fails to generate capture mode DMA requests from Timer A in the Timer modules

Description:

Workaround:

Silicon Revision Affected:

Fixed:

6 GPIO

6.1 Port B [1:0] pins require external pull-up resistors

Description:

Workaround:

Silicon Revision Affected:

Fixed:

6.2 Schmitt input feature does not function correctly

Description:

Workaround:

Silicon Revision Affected:

Fixed:

7 EPI

7.1 EPI dual-chip select function does not work

Description:

CSCFG

CSCFG **EPI Host-Bus 8 Configuration 2 (EPIHB8CFG2)**

CSCFG

CSCFG

Workaround:

Silicon Revision Affected:

Fixed:

7.2 EPI Host-Bus 16 mode does not work

Description:

MODE **EPI Configuration (EPICFG)**

Workaround:

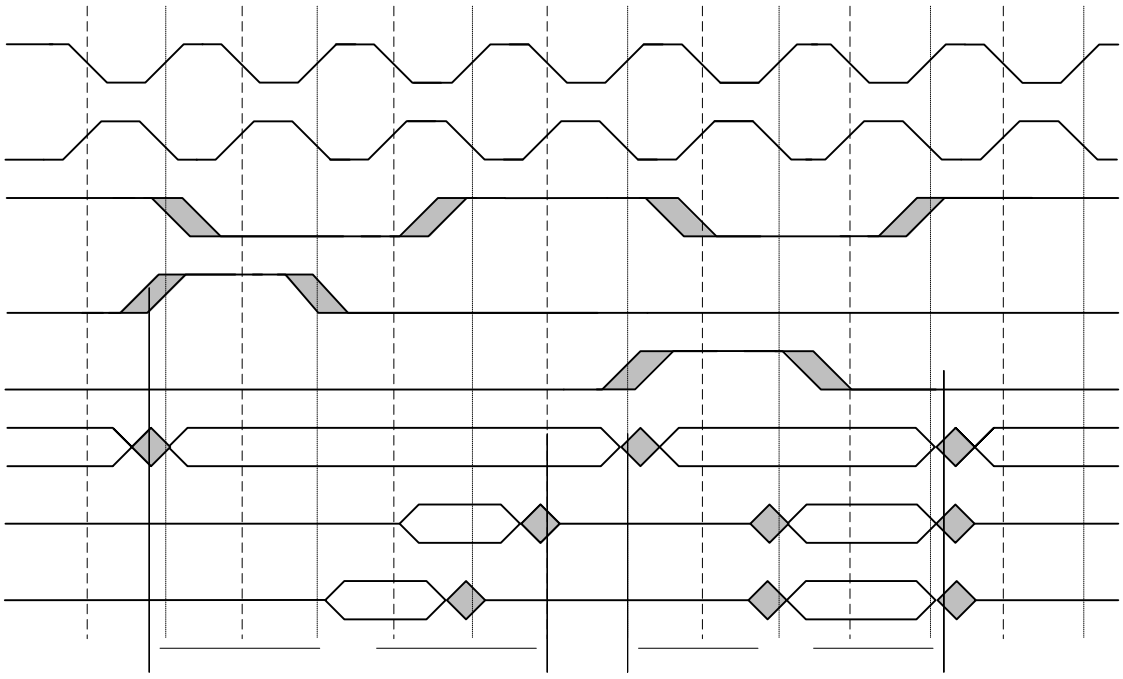
Silicon Revision Affected:

Fixed:

7.3 Clock signal in EPI General-Purpose mode is inverted

Description:

Figure 1. Timing Differences Between Rev B and Rev C Devices



Workaround:

Silicon Revision Affected:

Fixed:

8 General-Purpose Timer

8.1 The General-Purpose Timer match register does not function correctly in 32-bit mode

Description:

GPTM Timer A Match (GPTMTAMATCHR)

Workaround:

Silicon Revision Affected:

Fixed:

8.2 A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode

Description:

Workaround:

Silicon Revision Affected:

Fixed:

8.3 A spurious DMA request is generated when the timer rolls over the 16-bit boundary

Description:

Workaround:

Silicon Revision Affected:

Fixed:

8.4 The value of the prescaler register is not readable in Edge-Count mode

Description:

GPTM Timer n (GPTMTnR)
GPTM Timer n Prescale (GPTMTnPR)

Workaround:

Silicon Revision Affected:

Fixed:

8.5 ADC trigger and Wait-on-Trigger may assert when the timer is disabled

Description:

GPTM Timer n Match (GPTMTnMATCHR)
TnOTE **GPTM Control (GPTMCTL)**
TnEN **GPTMCTL**
GPTMTnMATCHR
TnWOT **GPTM Timer n Mode (GPTMTnMR)**

Workaround:

TnOTE

Silicon Revision Affected:

Fixed:

8.6 Wait-on-Trigger does not assert unless the TnOTE bit is set

Description:

TnOTE **GPTMCTL**

Workaround:

TnWOT **GPTM Timer n Mode (GPTMTnMR)**
TnOTE **GPTMCTL**
TnOTE

Silicon Revision Affected:

Fixed:

8.7 Do not enable match and timeout interrupts in 16-bit PWM mode

Description:

Workaround:

GPTMTnMR **GPTMIMR**

Silicon Revision Affected:

Fixed:

8.8 Do not use µDMA with 16-bit PWM mode

Description:

Workaround:

Silicon Revision Affected:

Fixed:

8.9 Writing the GPTMTnV register does not change the timer value when counting up

Description:

GPTM Timer n Value (GPTMTnV)

Workaround:

Silicon Revision Affected:

Fixed:

8.10 The prescaler does not work correctly when counting up in periodic or one-shot mode

Description:

Workaround:

Silicon Revision Affected:

Fixed:

8.11 Snapshot must be enabled in both Timer A and B when in 32-bit snapshot mode

Description:

GPTM Timer A (GPTMTAR)

Workaround:

TASNAPS TBSNAPS **GPTM Timer A Mode (GPTMTAMR)**
GPTMTAR

Silicon Revision Affected:

Fixed:

9 Watchdog Timer 1

9.1 Writes to Watchdog Timer 1 module WDTLOAD register sometimes fail

Description:

Watchdog Load (WDTLOAD) WRC **WDTCTL1**

Workaround:

WDTLOAD

Silicon Revision Affected:

Fixed:

10 ADC

10.1 ADC hardware averaging produces erroneous results in differential mode

Description:

Workaround:

Silicon Revision Affected:

Fixed:

10.2 The ADCSPC register does not function

Description:

ADC Sample Phase Control (ADCSPC)

Workaround:

Silicon Revision Affected:

Fixed:

11 UART

11.1 UART Smart Card (ISO 7816) mode does not function

Description:

UnTX

Workaround:

Silicon Revision Affected:

Fixed:

11.2 When in IrDA mode, the UnRx signal requires configuration even if not used

Description:

UnRx

Workaround:

UnRx

UnRx UnRx

Silicon Revision Affected:

Fixed:

11.3 Phantom interrupts occur in Smart Card mode

Description:

UARTRIS **UARTMIS**

Workaround:

PERIS

PEMIS

Silicon Revision Affected:

Fixed:

11.4 The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled

Description:

RTRIS **UART Raw Interrupt Status (UARTRIS)**
RTIM **UART Interrupt Mask (UARTIM)** RTIM
RTRIS

Workaround:

RTIM

RTRIS

Silicon Revision Affected:

Fixed:

12 SSI

12.1 An interrupt is not generated when using µDMA with the SSI module if the EOT bit is set

Description:

EOT **SSICR1**

Workaround:

Silicon Revision Affected:

Fixed:

13 I2S

13.1 Some bits in the I2SMCLKCFG register do not function

Description:

RXI TXI **I2SMCLKCFG**
RXI TXI RXI TXI

Workaround:

Silicon Revision Affected:

Fixed:

13.2 I²S SCLK signal is inverted in certain modes

Description:

Workaround:

1. I2S0TXSCK I2S0TXWS

2.

Silicon Revision Affected:

Fixed:

14 Ethernet Controller

14.1 Ethernet receive packet corruption may occur when using optional auto-clock gating

Description:

ACG **Run-Mode Clock Configuration (RCC)**

Workaround:

ACG **RCC**

Silicon Revision Affected:

Fixed:

14.2 Ethernet packet loss with cables longer than 50 meters

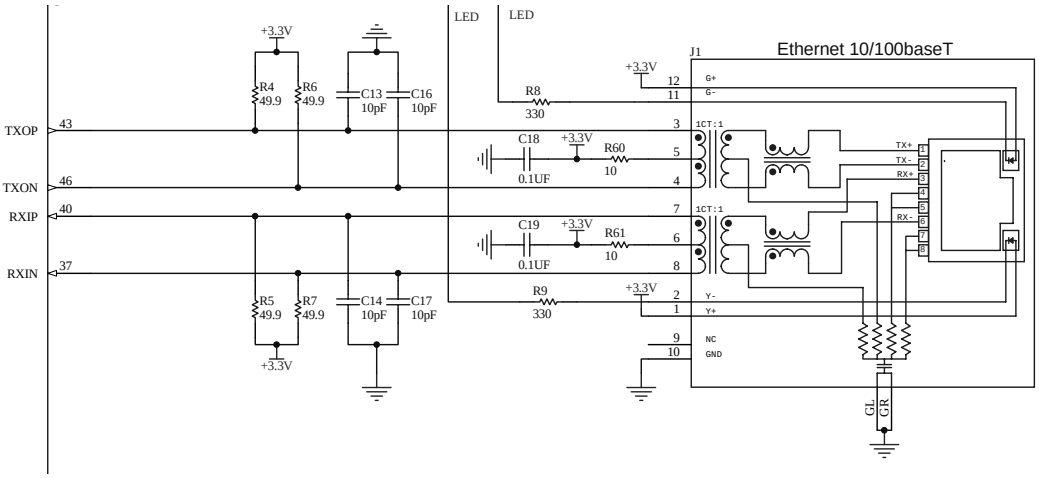
Description:

Workaround:

1.

2.

Figure 2. Recommended Center-Tap Connections



Silicon Revision Affected:

Fixed:

14.3 Ethernet PHY interrupts do not function correctly

Description:

Workaround:

Silicon Revision Affected:

Fixed:

14.4 Encoding error in the Ethernet MAC LED Encoding (MACLED) register

Description:

LED0	LED1	**Ethernet MAC LED Encoding (MACLED)**

Workaround:

Silicon Revision Affected:

Fixed:

15 USB

15.1 USB0ID and USB0VBUS signals are required to be connected regardless of mode

Description:

DEVMODOTG	**USB General-Purpose Control and Status (USBGPCS)**

Workaround:

USB0VBUS USB0ID
DEVMOD **USB**

General-Purpose Control and Status (USBGPCS)

Silicon Revision Affected:

Fixed:

15.2 Latch-up may occur if power is applied to the VBUS pin but not to VDD

Description:

Workaround:

USB0VBUS

Silicon Revision Affected:

Fixed:

16 PWM

16.1 PWM generation is incorrect with extreme duty cycles

Description:

PWM Load (PWMnLOAD)

PWM0 Compare A (PWM0CMPA)

PWM0CMPA

Workaround:

PWMnLOAD

Silicon Revision Affected:

Fixed:

16.2 Sync of PWM does not trigger "zero" action

Description:

PWM Generator Control (PWM0GENA) `ActZero`

PWM Time Base Sync (PWMSYNC)

Workaround:

Silicon Revision Affected:

Fixed:

16.3 PWM "zero" action occurs when the PWM module is disabled

Description:

Workaround:

Silicon Revision Affected:

Fixed:

16.4 PWM Enable Update register bits do not function

Description:

ENUPDn **PWM Enable Update (PWMENUPD)**

Workaround:

Silicon Revision Affected:

Fixed:

17 Electrical Characteristics

17.1 Momentarily exceeding V_{IN} ratings on any pin can cause latch-up

Description:

$\overline{RST}$ $\overline{WAKE}$

Figure 3. Incorrect Reset Circuitry

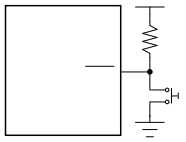
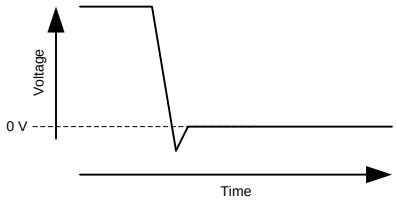
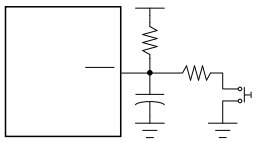


Figure 4. Excessive Undershoot Voltage on Reset



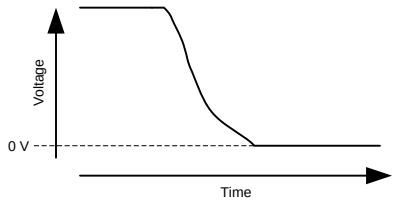
Workaround:

Figure 5. Recommended Reset Circuitry



RST

Figure 6. Recommended Voltage on Reset



Silicon Revision Affected:

Fixed:

17.2 Power-on event may disrupt operation

Description:

Workaround:

Figure 7. Configuration of External Regulator

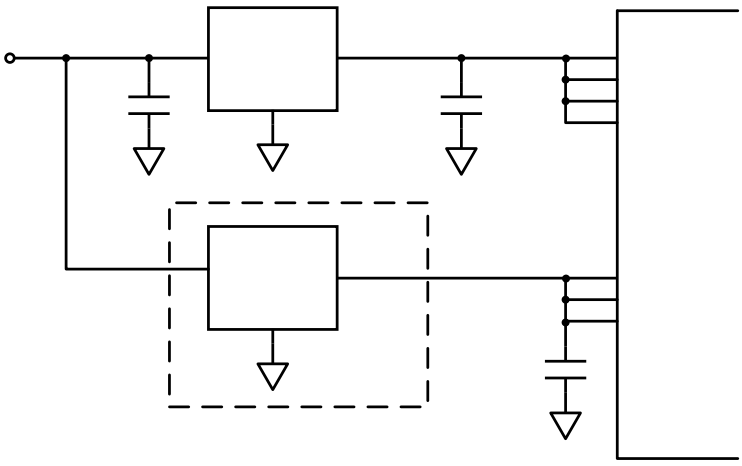
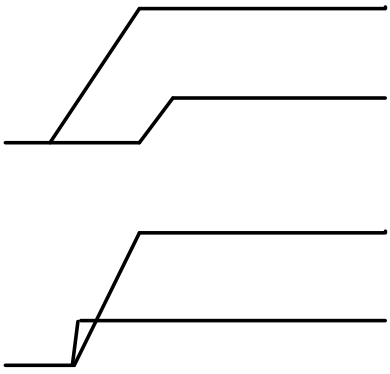


Figure 8. VDDC Sequencing Requirements



Silicon Revision Affected:

Fixed:


TEXAS
INSTRUMENTS
ARM
POWERED
Cortex
Intelligent Processors by ARM

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