CMPEN331 – Quiz 2

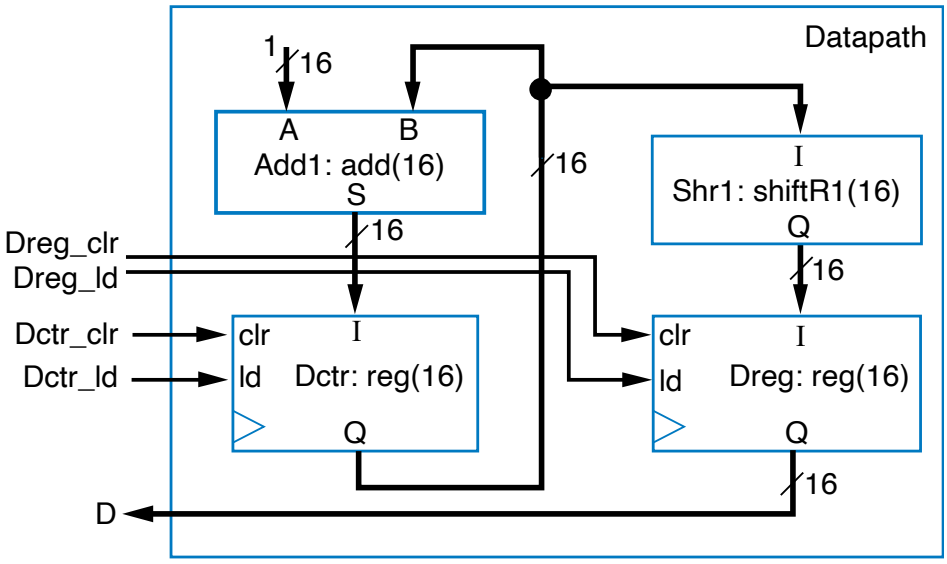
Section: **Major:**

Name: **Email:**

1. Create

```
module mux_8 ( sel, a0, a1, a2, a3, a4, a5, a6, a7, out);
input [2:0] sel;
input [7:0] a0;
input [7:0] a1;
input [7:0] a2;
input [7:0] a3;
input [7:0] a4;
input [7:0] a5;
input [7:0] a6;
input [7:0] a7;
output reg [7:0] out;
always @(*)
case (sel)
      3'b000 : out= a0;
      3'b001 : out= a1;
      3'b010 : out= a2;
      3'b011 : out= a3;
      3'b100 : out= a4;
      3'b101 : out= a5;
      3'b110 : out= a6;
      3'b111 : out= a7;
endcase
endmodule
```

1. Draw



A. First,

```
`timescale 1ns / 1ps
module FSM(
    input X,
    input Clk,
    output reg Z
    );

reg [2:0] CState=0, NxState;
parameter Reset=0, S0=1, S1=1, S2=2, S3=3, S4=4, S5=5;

always @(posedge Clk)
    CState<=NxState;

always @(*)begin
    case(CState)
        Reset:begin
            if(X)begin
                NxState=S3;Z=0;
            end
            else begin
                NxState=S0;Z=0;
            end
        end
        S0:begin
            if(X)begin
                NxState=S1;Z=0;
            end
            else begin
                NxState=S0;Z=0;
            end
        end
        S1:begin
            if(X)begin
                NxState=S2;Z=1;
            end
            else begin
                NxState=S4;Z=0;
            end
        end
        S2:begin
            if(X)begin
                NxState=S3;Z=0;
            end
            else begin
                NxState=S4;Z=0;
            end
        end
        S3:begin
            if(X)begin
                NxState=S3;Z=0;
            end
            else begin
                NxState=S4;Z=0;
            end
        end
        S4:begin
            if(X)begin
                NxState=S5;Z=1;
            end
            else begin
                NxState=S0;Z=0;
            end
        end
        S5:begin
            if(X)begin
                NxState=S2;Z=1;
            end
            else begin
                NxState=S1;Z=0;
```

```
70                end
71            end
72        endcase
73    end
74    endmodule
75
```