

CV-8052 Soft-Core Special Function Registers (SFRs)

The 8052 soft processor includes all the standard 8052 SFRs. Some additional SFRs were added to provide access to some of the resources in the Altera DE0-CV board. These are the additional SFRs:

| SFR | Address | Description |
|----------|---------|---|
| HEX0 | 91H | Seven segment display 0 |
| HEX1 | 92H | Seven segment display 1 |
| HEX2 | 93H | Seven segment display 2 |
| HEX3 | 94H | Seven segment display 3 |
| HEX4 | 8EH | Seven segment display 4 |
| HEX5 | 8FH | Seven segment display 5 |
| LEDRA | E8H | LEDs LEDR0 to LEDR7 (bit addressable). |
| LEDRB | 95H | LEDs LEDR8 to LEDR15. |
| SWA | E8H | Switches SW0 to SW7 (bit addressable). |
| SWB | 95H | Switches SW8 to SW15. |
| KEY | F8H | KEY1=KEY.1, KEY2=KEY.2, etc. |
| LCD_CMD | D8H | Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 |
| | | X X X X ON RS EN RW |
| LCD_DATA | D9H | Input/output port to LCD |
| LCD_MOD | DAH | Write 0FFH to make LCD_DATA an output |
| P0MOD | 9AH | Input/Output mode bits for port 0 |
| P1MOD | 9BH | Input/Output mode bits for port 1 |
| P2MOD | 9CH | Input/Output mode bits for port 2 |
| P3MOD | 9DH | Input/Output mode bits for port 3 |

Pin Assignments

All the standard 8052 I/O pins are assigned to the expansion headers of the Altera DE0-CV board. By default all the port pins (P0 to P3) are configured as inputs. To configure any of the pins of a port as an output write 1 to the corresponding bit in the PxMOD register described above. For example to make P0.0 and P0.7 outputs and leave P0.1 to P0.6 as inputs, write 81H to P0MOD. These are the pin assignments:

| JP1 | | |
|--------------------|-----------|-----------------------------|
| <i>LCD_DATA[0]</i> | 1 | 2 <i>LCD_DATA[1]</i> |
| <i>LCD_DATA[2]</i> | 3 | 4 <i>LCD_DATA[3]</i> |
| <i>LCD_DATA[4]</i> | 5 | 6 <i>LCD_DATA[5]</i> |
| <i>LCD_DATA[6]</i> | 7 | 8 <i>LCD_DATA[7]</i> |
| <i>LCD_EN</i> | 9 | 10 <i>LCD_RS</i> |
| <i>5V</i> | 11 | 12 <i>GND</i> |
| <i>LCD_RW</i> | 13 | 14 <i>TXD</i> |
| <i>LCD_ON</i> | 15 | 16 <i>RXD</i> |
| <i>FL_DQ[0]</i> | 17 | 18 <i>FL_DQ[1]</i> |
| <i>FL_DQ[2]</i> | 19 | 20 <i>FL_DQ[3]</i> |
| <i>FL_DQ[4]</i> | 21 | 22 <i>FL_DQ[5]</i> |
| <i>FL_DQ[6]</i> | 23 | 24 <i>FL_DQ[7]</i> |
| <i>FL_RST_N</i> | 25 | 26 <i>FL_WE_N</i> |
| <i>FL_OE_N</i> | 27 | 28 <i>FL_CE_N</i> |
| <i>3.3V</i> | 29 | 30 <i>GND</i> |
| <i>TDO</i> | 31 | 32 <i>TDI</i> |
| <i>TCS</i> | 33 | 34 <i>TCK</i> |
| <i>Not used</i> | 35 | 36 <i>Not used</i> |
| <i>T0</i> | 37 | 38 <i>T1</i> |
| <i>T2</i> | 39 | 40 <i>T2EX</i> |

| JP2 | | |
|-----------------|-----------|---------------------------|
| <i>P0.0</i> | 1 | 2 <i>P0.1</i> |
| <i>P0.2</i> | 3 | 4 <i>P0.3</i> |
| <i>P0.4</i> | 5 | 6 <i>P0.5</i> |
| <i>P0.6</i> | 7 | 8 <i>P0.7</i> |
| <i>P1.0</i> | 9 | 10 <i>P1.1</i> |
| <i>5V</i> | 11 | 12 <i>GND</i> |
| <i>P1.2</i> | 13 | 14 <i>P1.3</i> |
| <i>P1.4</i> | 15 | 16 <i>P1.5</i> |
| <i>P1.6</i> | 17 | 18 <i>P1.7</i> |
| <i>P2.0</i> | 19 | 20 <i>P2.1</i> |
| <i>P2.2</i> | 21 | 22 <i>P2.3</i> |
| <i>P2.4</i> | 23 | 24 <i>P2.5</i> |
| <i>P2.6</i> | 25 | 26 <i>P2.7</i> |
| <i>P3.0</i> | 27 | 28 <i>P3.1</i> |
| <i>3.3V</i> | 29 | 30 <i>GND</i> |
| <i>P3.2</i> | 31 | 32 <i>P3.3</i> |
| <i>P3.4</i> | 33 | 34 <i>P3.5</i> |
| <i>P3.6</i> | 35 | 36 <i>P3.7</i> |
| <i>INT0</i> | 37 | 38 <i>INT1</i> |
| <i>Not Used</i> | 39 | 40 <i>Not used</i> |