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A Novel Service-Based System-on-Chip Architecture

Using On-Chip Networks with Smart Packets and Dynamically Reconfigurable Logic

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Overview

- On-Chip Networks
- Smart Packets
- Self-Reconfigurable Logic
- Service-based SoC

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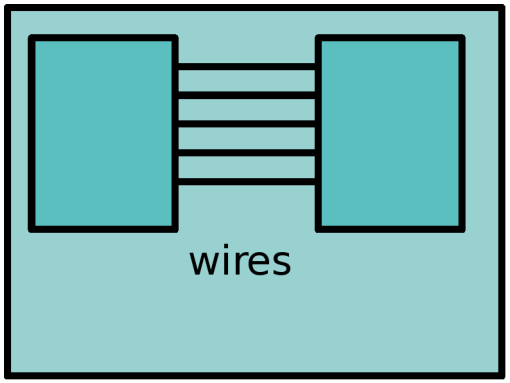
Novel System-on-Chip Architecture

1. On-Chip Networks

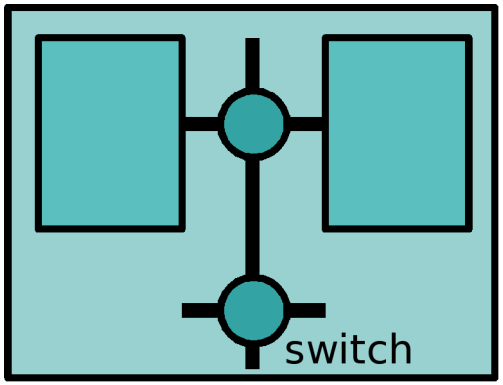
Outcome	Novelty	Benefit
Novel architecture for very large Integrated Circuits	• Network-type interconnections • Self-routing network	Open up full potential of today's LSI technology

Current:



Conventional interconnect

Proposal:



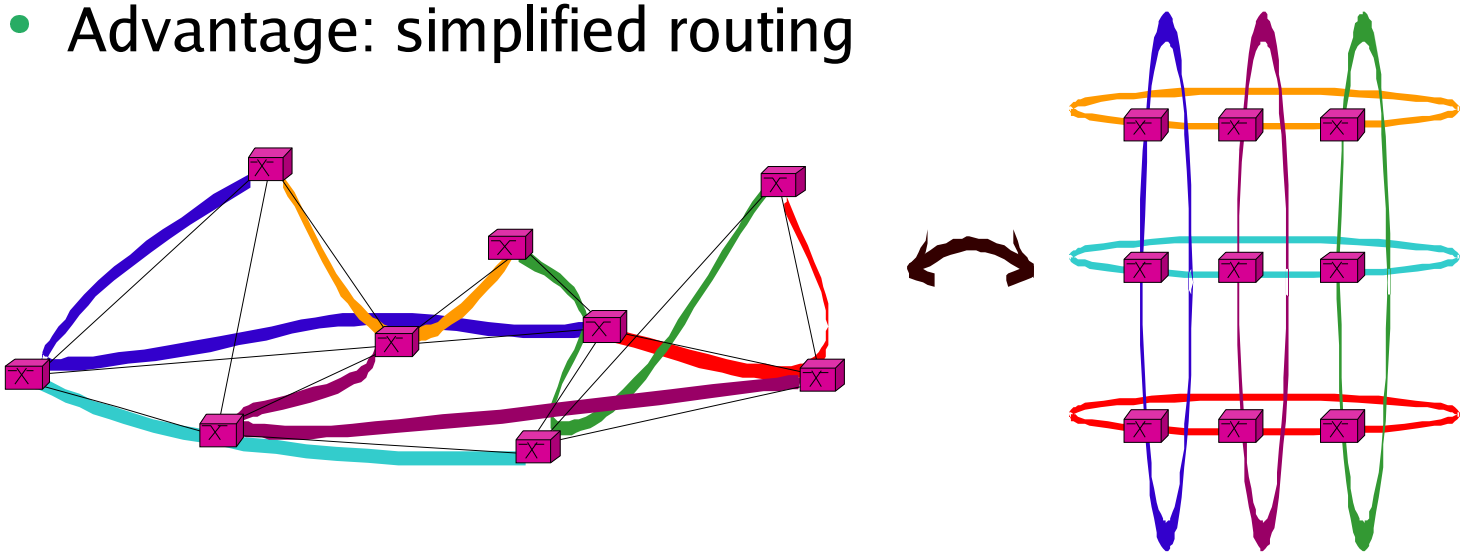
On-chip network

Applications:

- Network processors
- Electronic assistive technology

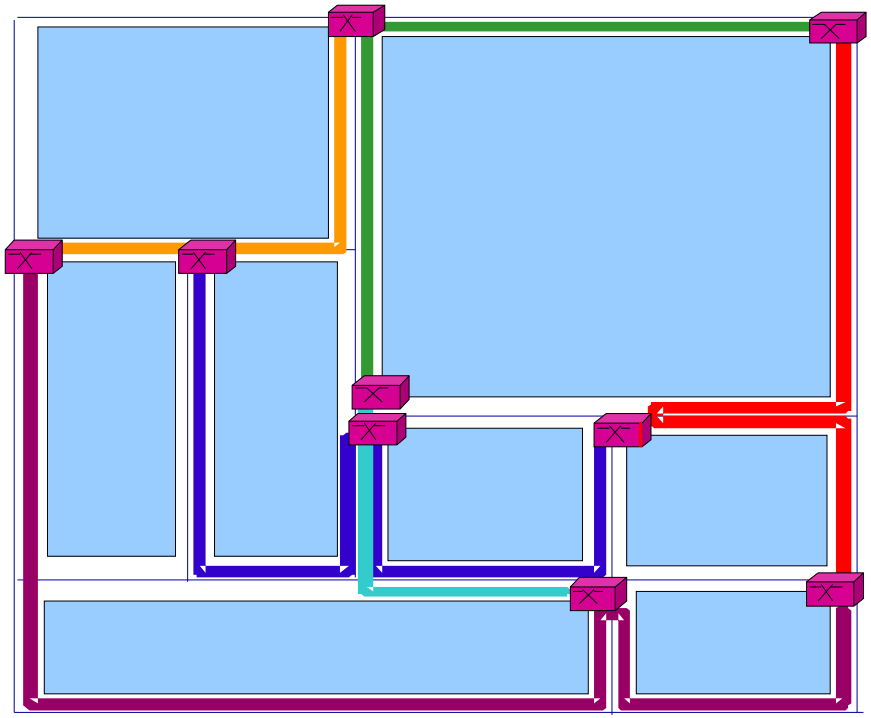
On-Chip Networks
Self-Routing Networks

- Self-routing networks:
  - Packets can reach their destination without per-hop routing table lookup
  - In principle, a regular topology is required
  - But in many cases, an irregular physical topology can be mapped onto a regular virtual topology
  - Advantage: simplified routing

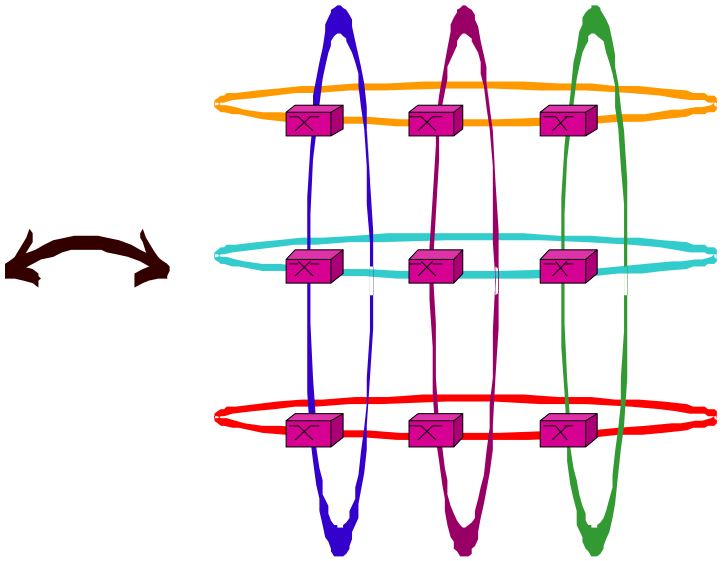


On-Chip Networks
Self-Routing Networks

On-chip network topology



Virtual topology

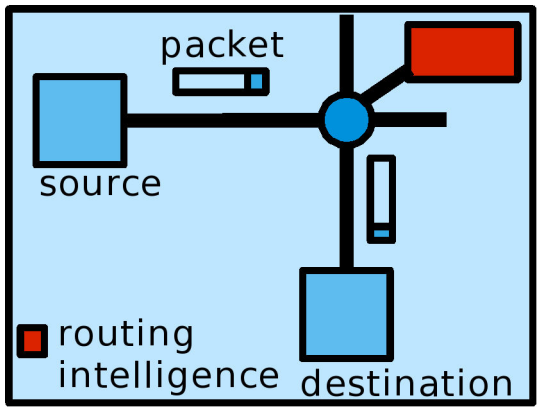


Novel System-on-Chip Architecture

2. Smart Packets

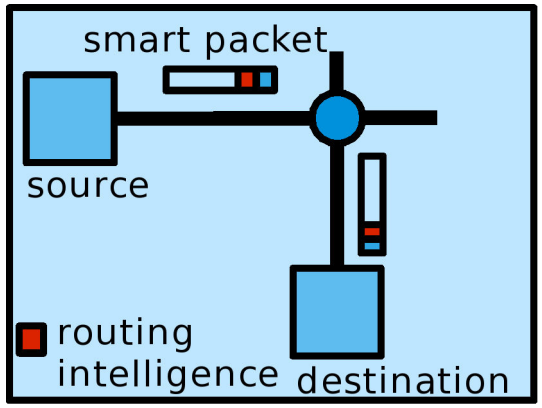
Outcome	Novelty	Benefit
Novel organisation and management of communication networks	• Self-organising • Routers require no intelligence	• No central management • Simpler, cheaper network infrastructure

Current:



Managed network

Proposal:



Self-organising network

Applications:

- Wireless Internet
- Simpler office networks

Smart Packet Networks

- Smart Packets and Self-aware Networks
  - Packets carry executable content
  - Network organisation is determined by packet programs, network is completely self-organising
  - Advantages: Reduces hardware, configuration and management resources to a minimum.

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Ad-Hoc Networks

- Ad-hoc and self-organising networks
  - Networks without centralised management (e.g. wireless LAN with laptops and without servers)
  - Peer-to-peer rather than client-server
  - Routing information is distributed amongst the nodes
  - Advantages:
    - Reduces cost of management and configuration
    - Ease of use for the end user

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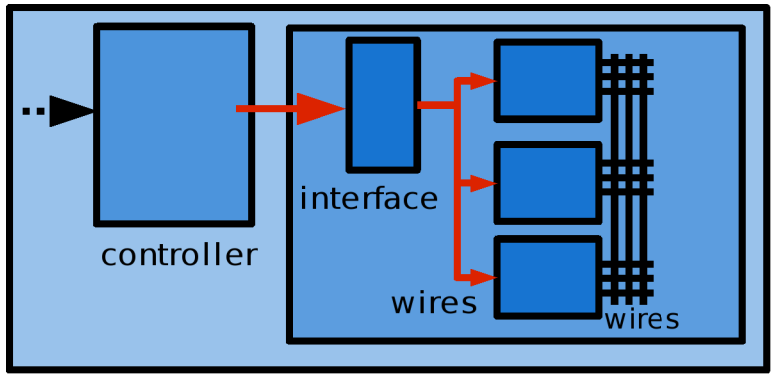
Novel System-on-Chip Architecture

3. Self-Reconfigurable Logic

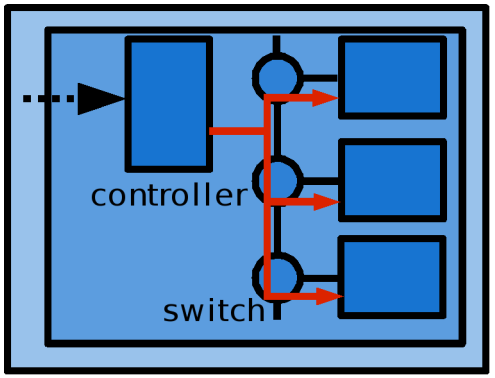
Outcome	Novelty	Benefit
Novel architecture for multifunctional self-reconfigurable Integrated Circuits	• Self-reconfigurable, no external agent • Packet-based reconfiguration	Smaller, multifunctional products with lower power consumption

Current:



Reconfigurable logic

Proposal:



Packet-based self-reconfigurable logic

Applications:

- PDAs
- Mobile technologies

Self-Reconfigurable Logic

- Reconfigurable logic: e.g. FPGA
- Dynamic Reconfiguration: whilst the circuit is operating
- Self-reconfiguration: without external agent
  - Examples:
    - On-the-fly protocol conversion
    - Image manipulation

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Smart Packets and self-reconfigurable logic

- Packet program can be executed at different levels
- Use the packet program to configure a custom circuit
- Circuit performs all necessary operations on the packet (e.g. Switching)
- Simplified, the network node is reduced to a dynamically reconfigurable FPGA

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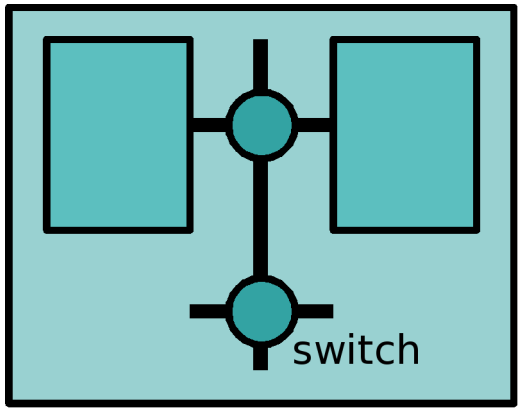
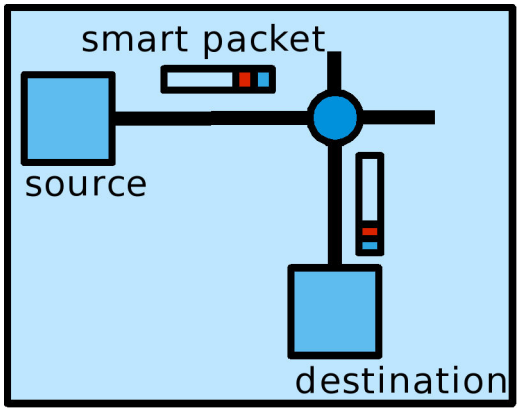
Novel System-on-Chip Architecture

➡ Service-Based System-on-Chip Architecture

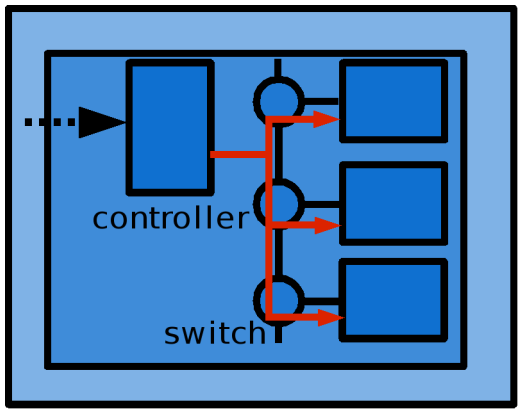
Outcome	Novelty	Benefits
• Novel System-on-Chip architecture • Prototypes of design tools	• Perform tasks by combining services • Synergy of on-chip smart packet networks and self-reconfigurable logic	• Larger and more complex designs • Flexible, fast and area-efficient



1. On-chip network



2. Self-organising network



3. Self-reconfigurable logic

Novel System-on-Chip Architecture

- Service-based System-on-a-Chip with on-Chip Network
  - Uses the concept of services as used in IP networking
  - System-on-a-Chip with packet routing
  - Uses a self-routing network
  - Self-routing requires mapping of the irregular physical topology onto a regular virtual topology

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Novel System-on-Chip Architecture

- Apply smart packets concept to SoC design
- Results in a completely new way of organising a SoC
- Smart packets carry both the information to be processed and the information to create the processing unit
- Requires very advanced FPGA - or ASIC with embedded FPGA

Conclusion

Proposal for a Novel Service-Based System-on-Chip Architecture: