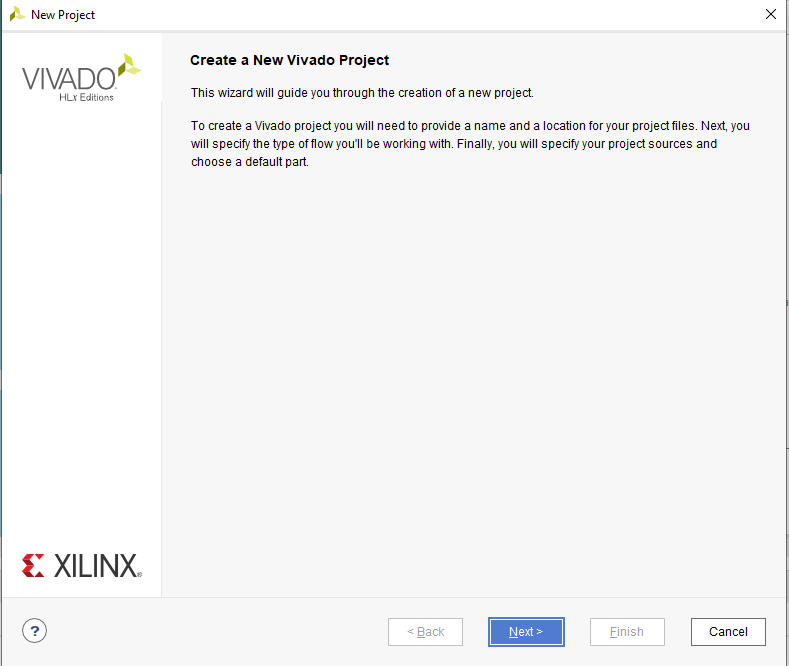
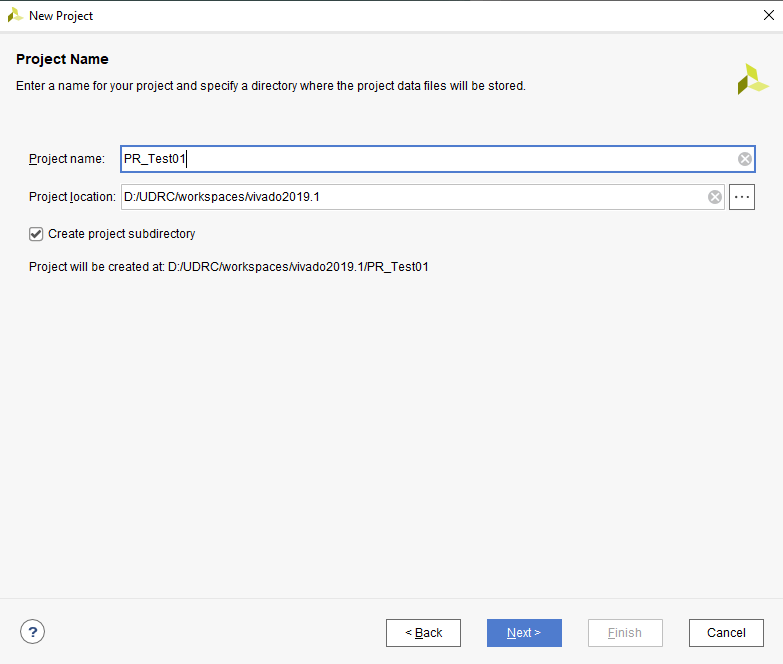
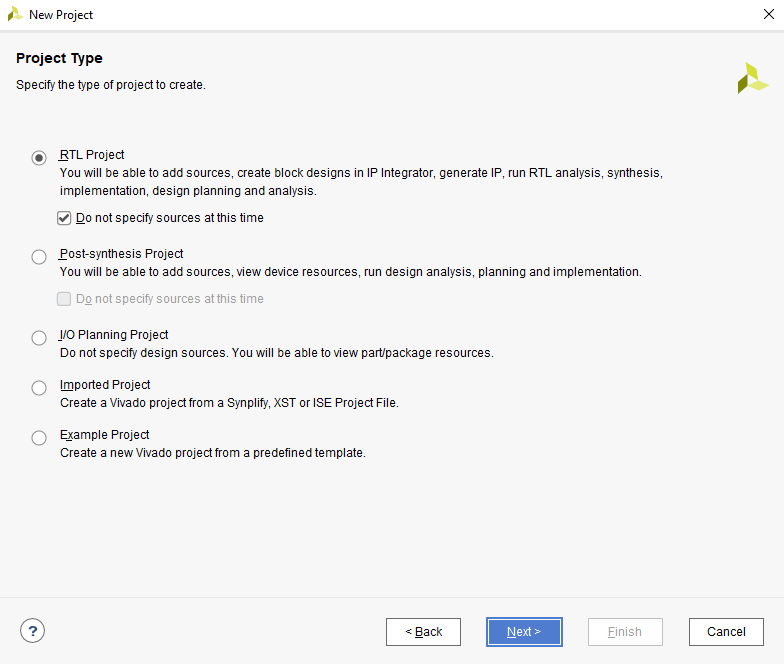
**PR/DFX Project Flow**

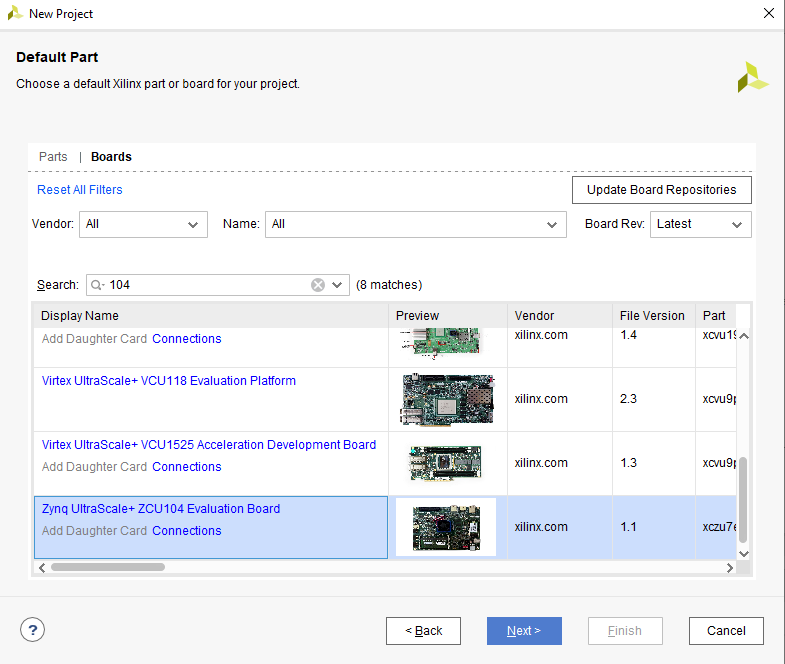
The example is targeting ZCU104 Ultrascale+ MPSoC and using Vivado 2019.1. Notice that the it is still called Partial Reconfiguration (PR) in version 2019.1, while it is changed to Dynamic Function eXchange since version 2019.2. Both PR and DFX are of similar design flow. This could also be extended to ZCU102 and ZCU106 by using different .xdc constraint files.

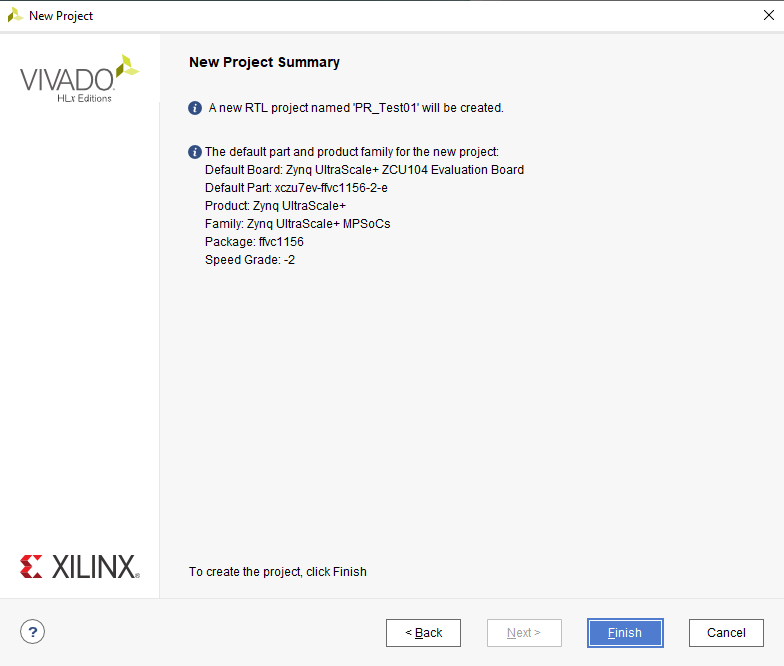
1. Create a Vivado project:



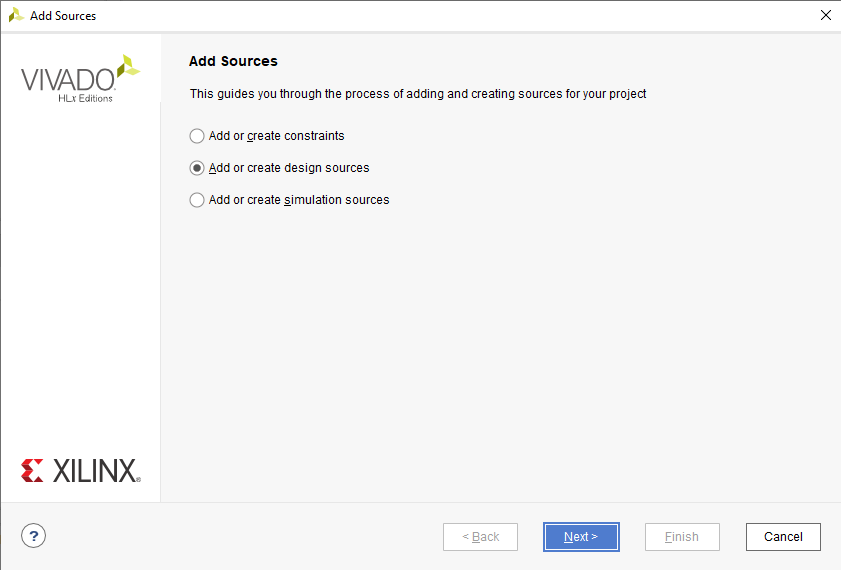


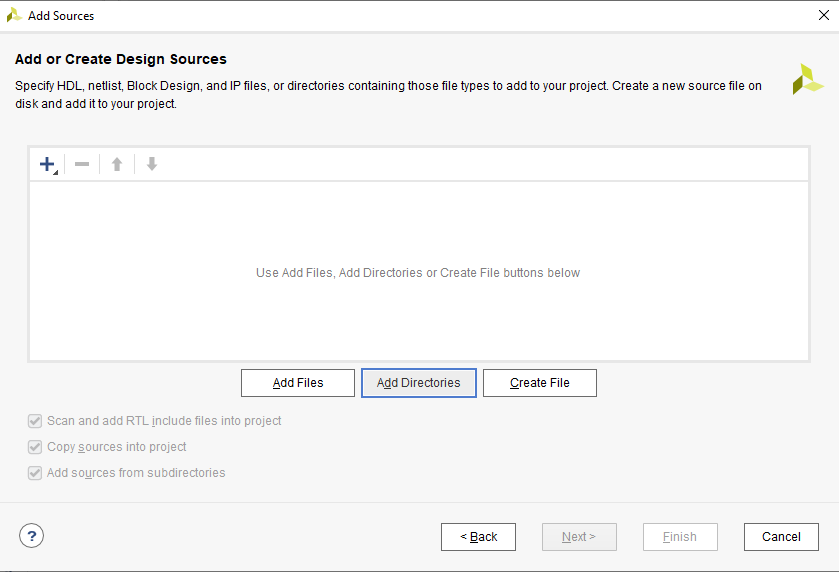


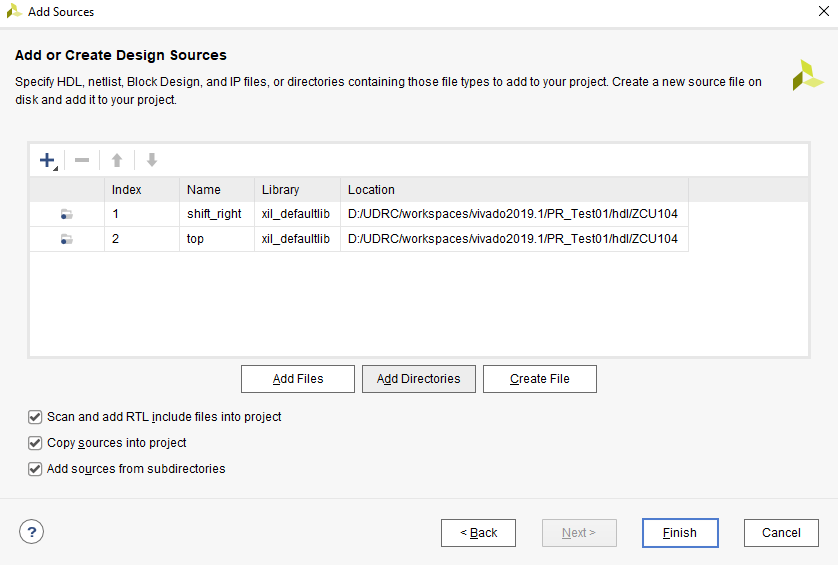




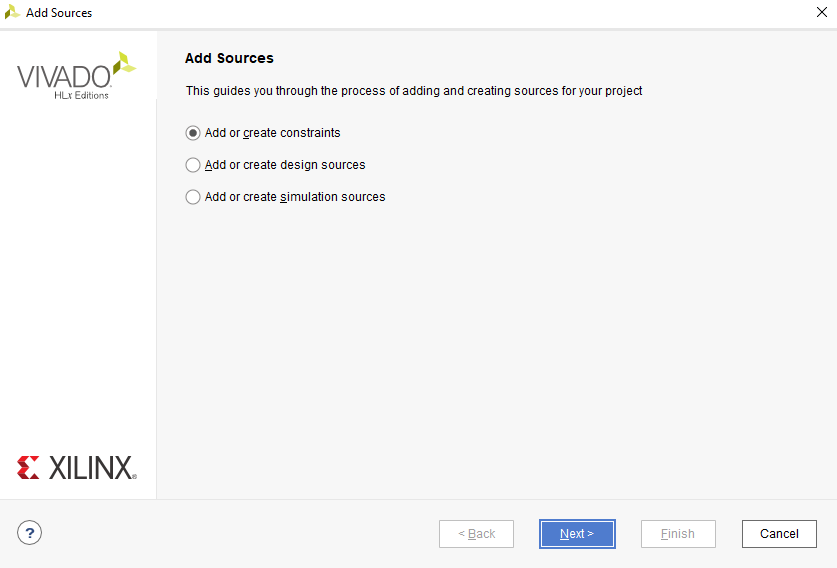
1. Add the design source file

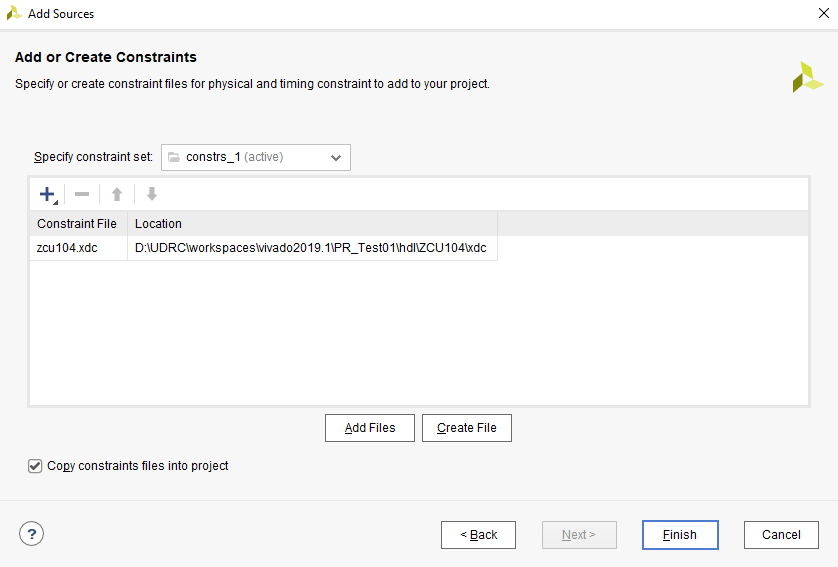




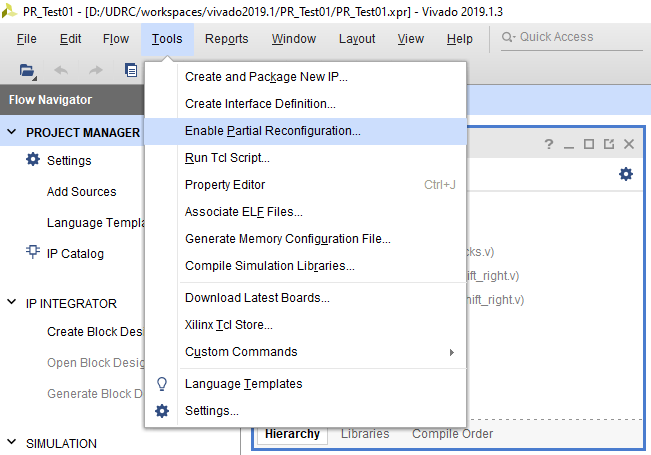


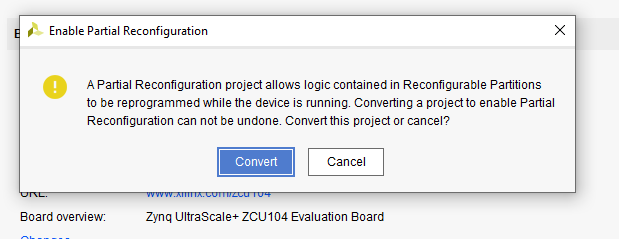
1. Add constraint file



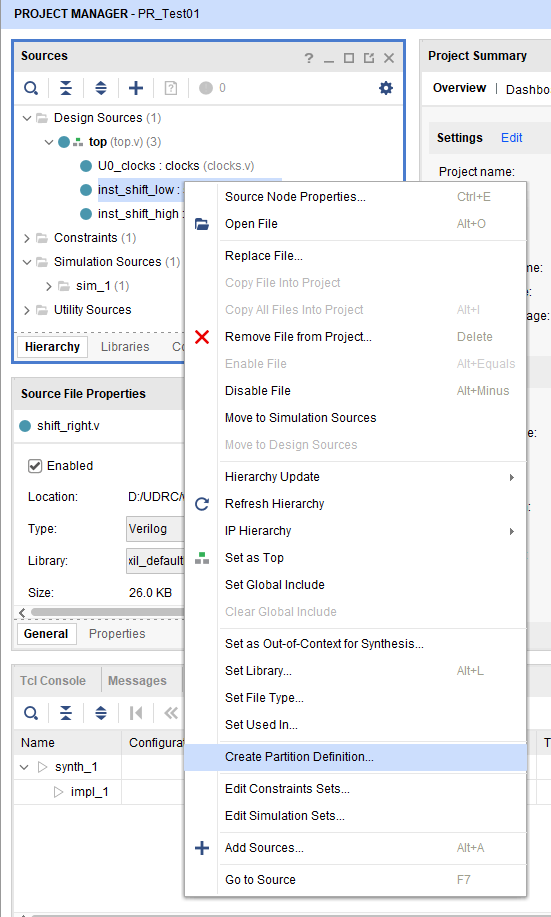


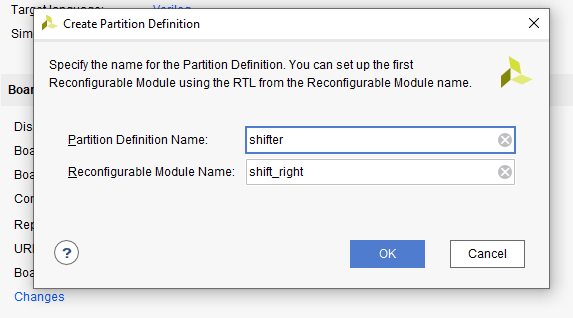
1. Enable the PR/DFX mode for Vivado project

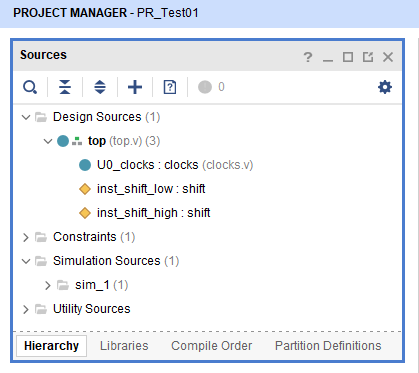




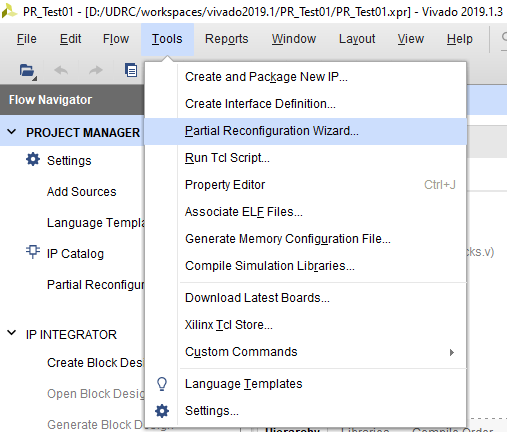
1. Create PR/DFX partition from the design module

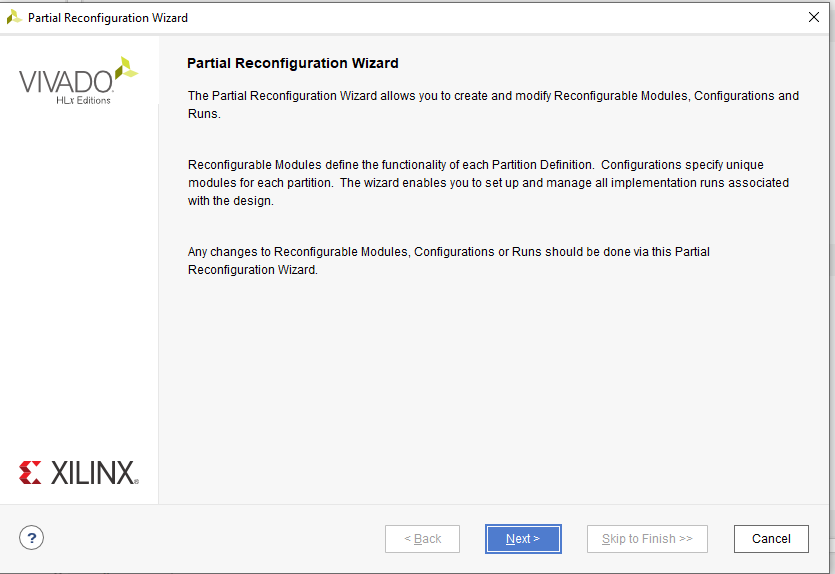


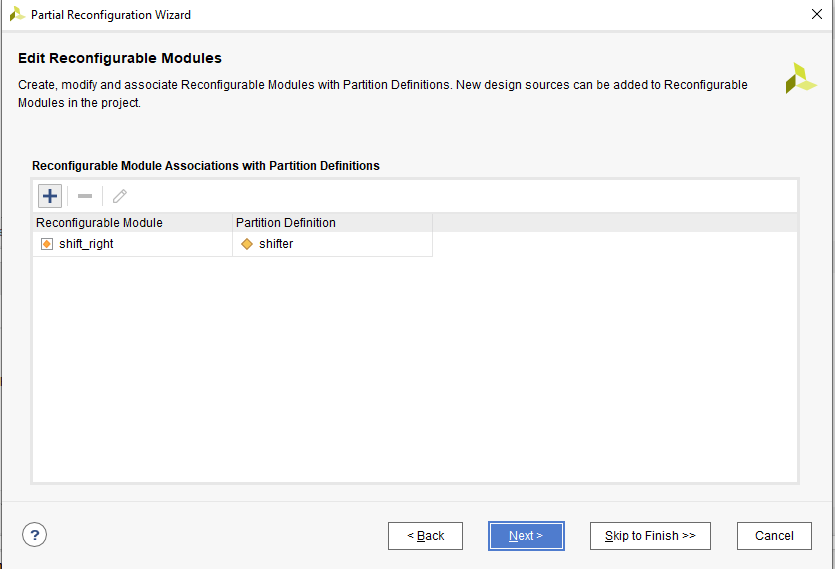


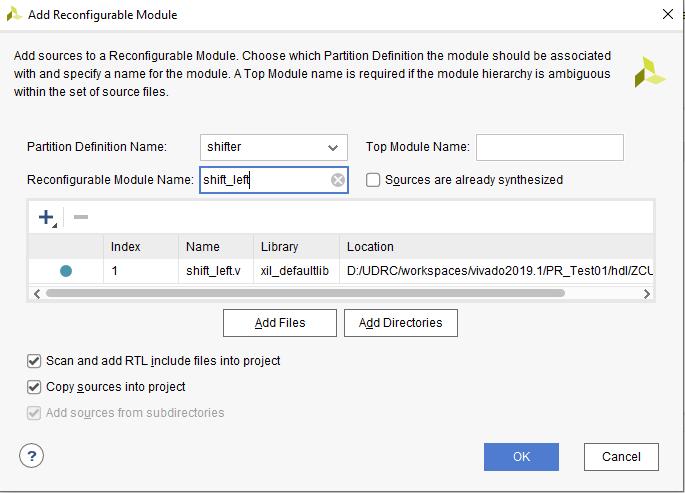


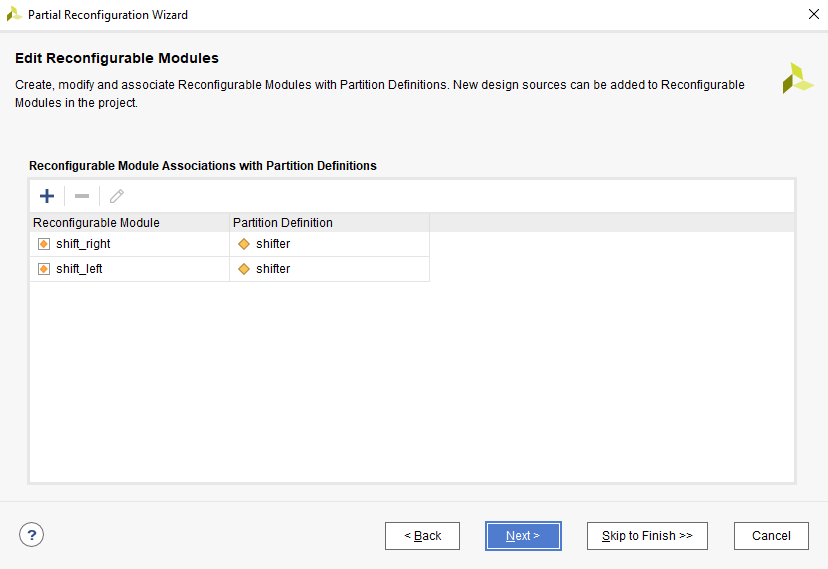
1. Using PR/DFX wizard to add reconfigurable partition design source

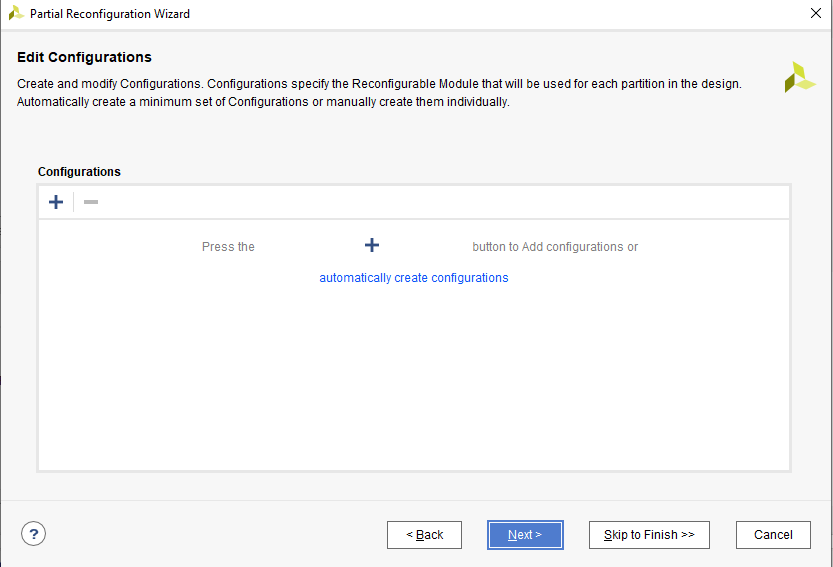


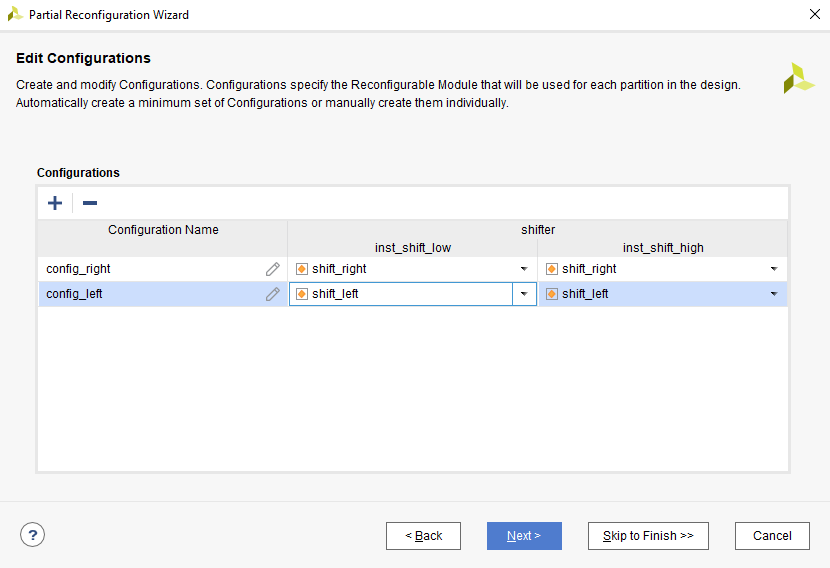


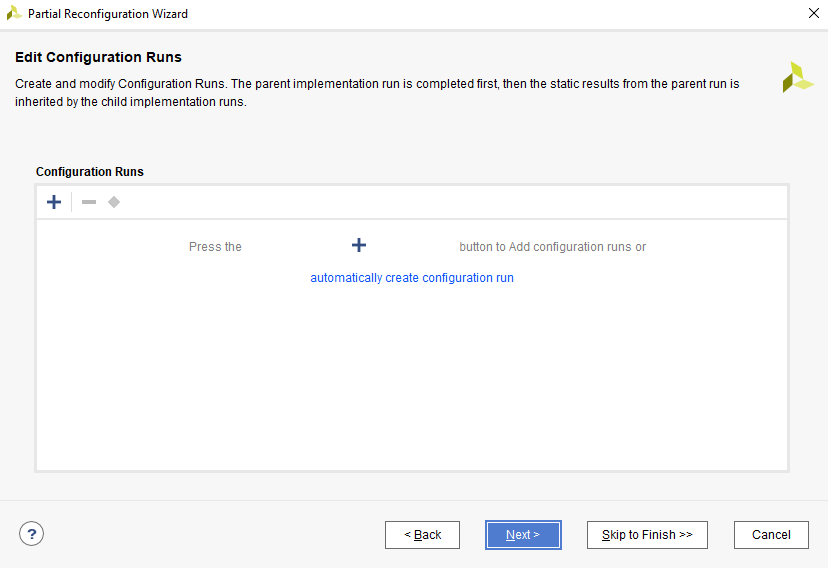


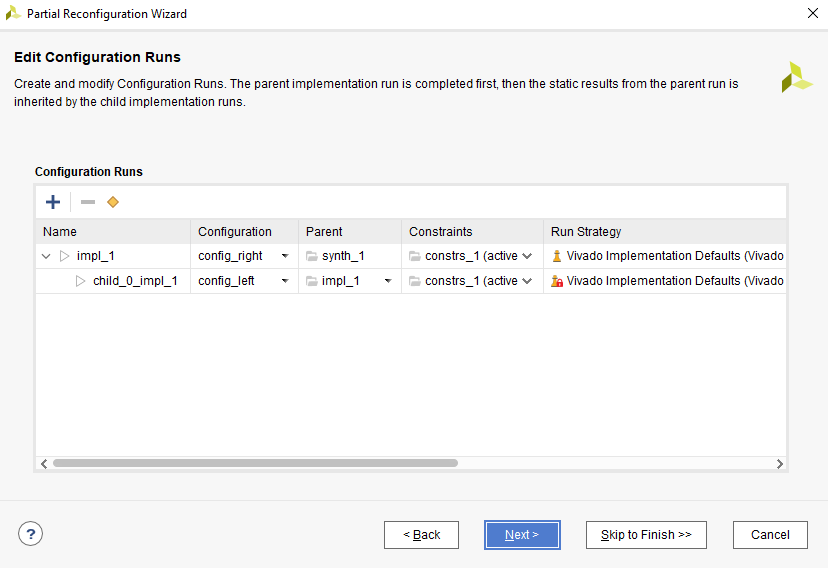


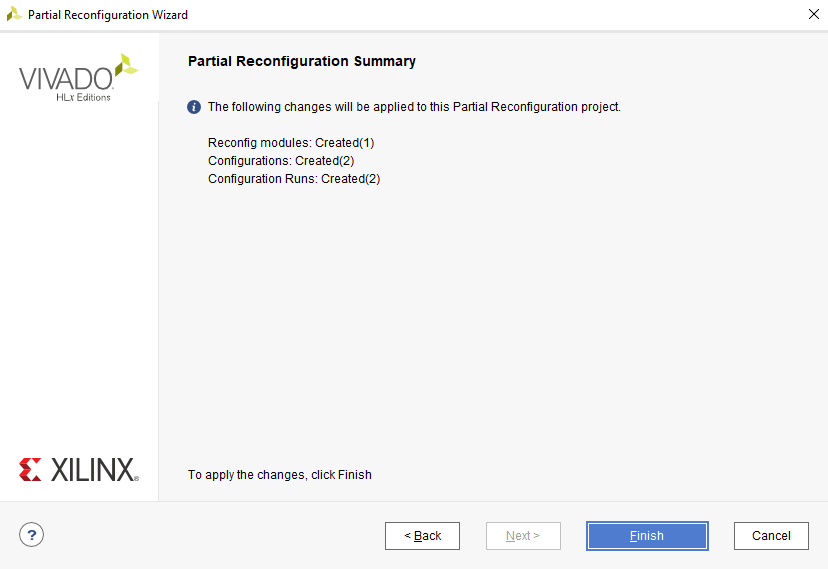




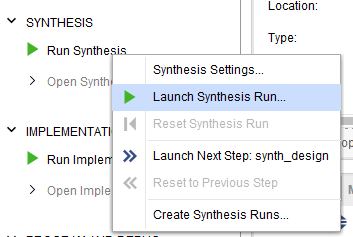


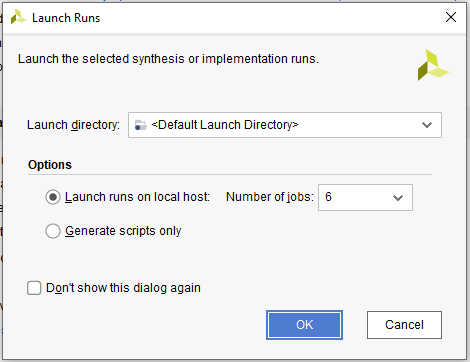


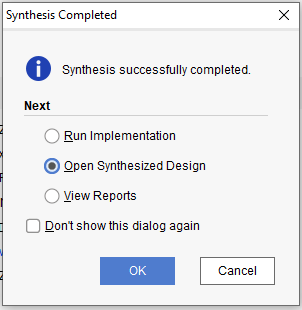


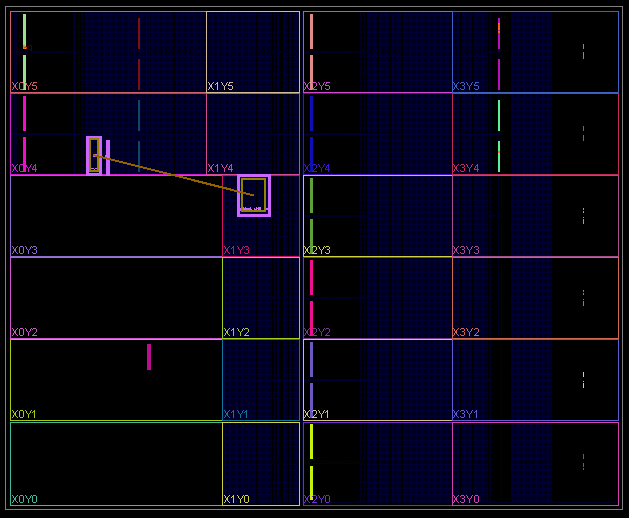


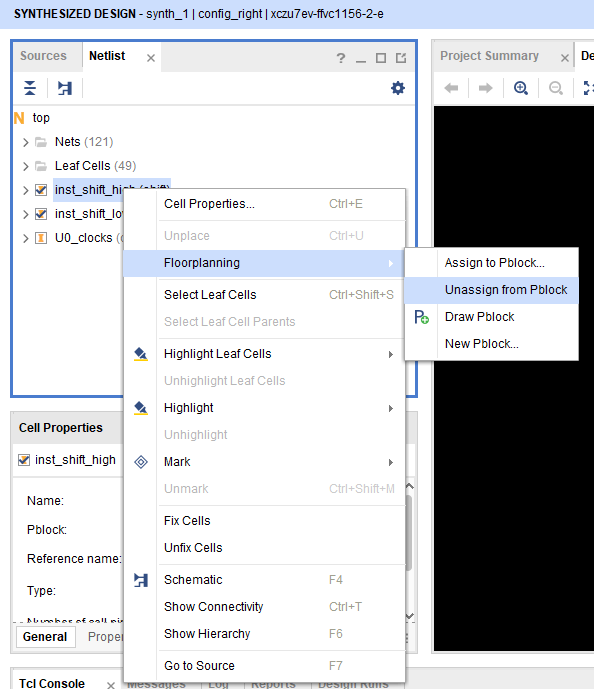
1. Launch the synthesis flow

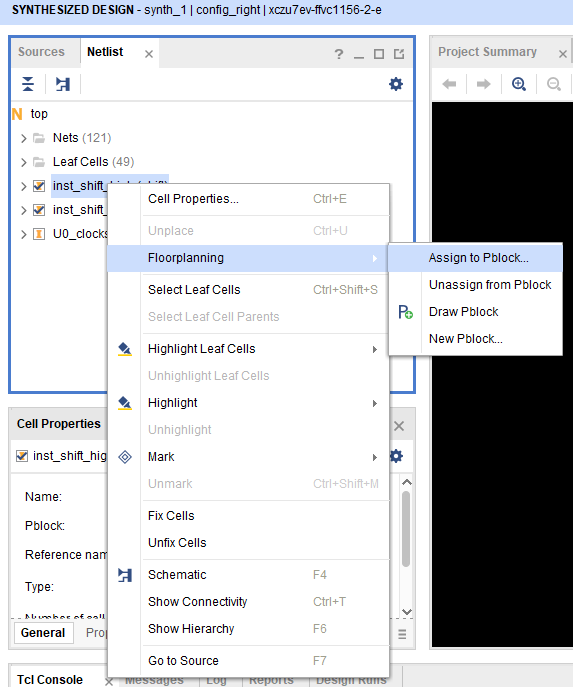




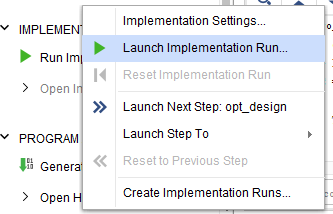


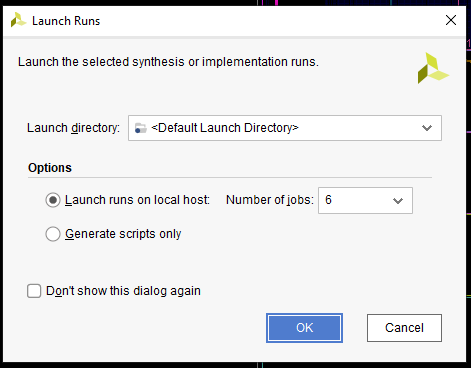




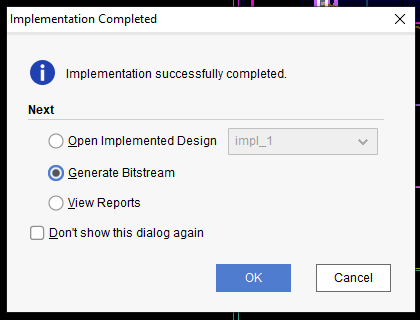


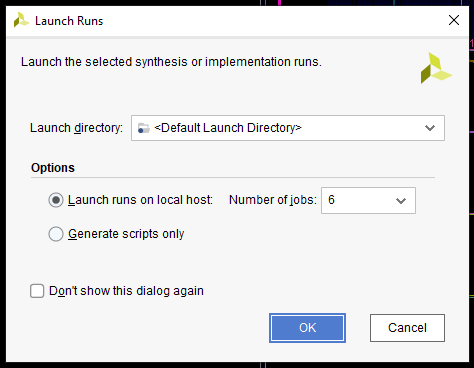
1. Launch the implementation flow

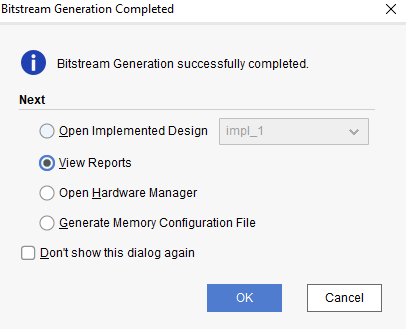




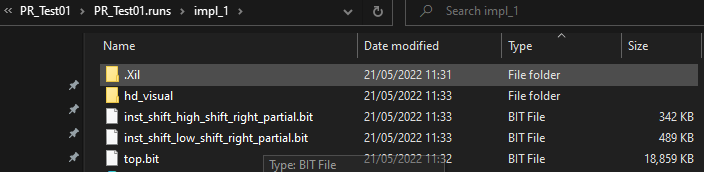
1. Generate the bitstream files



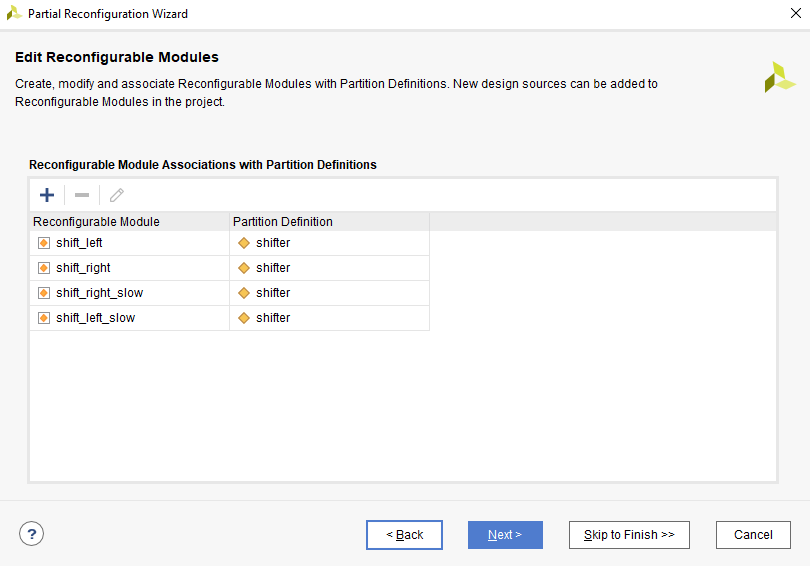


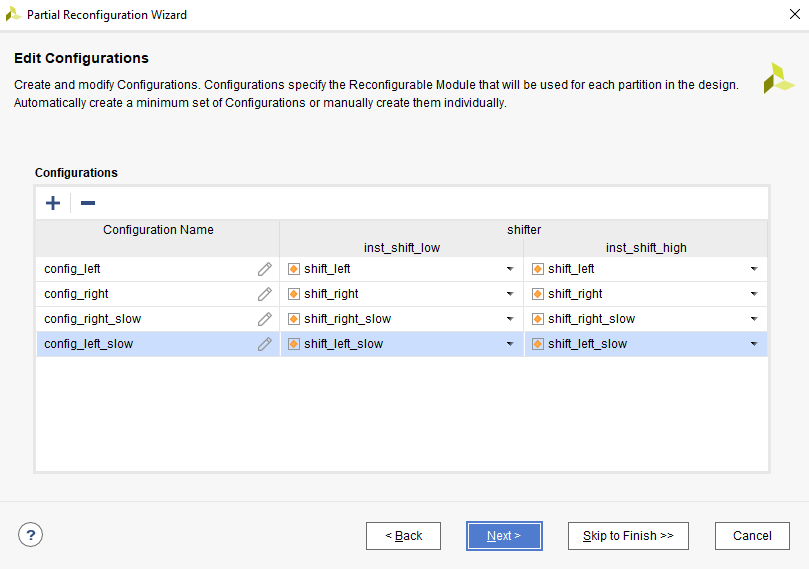


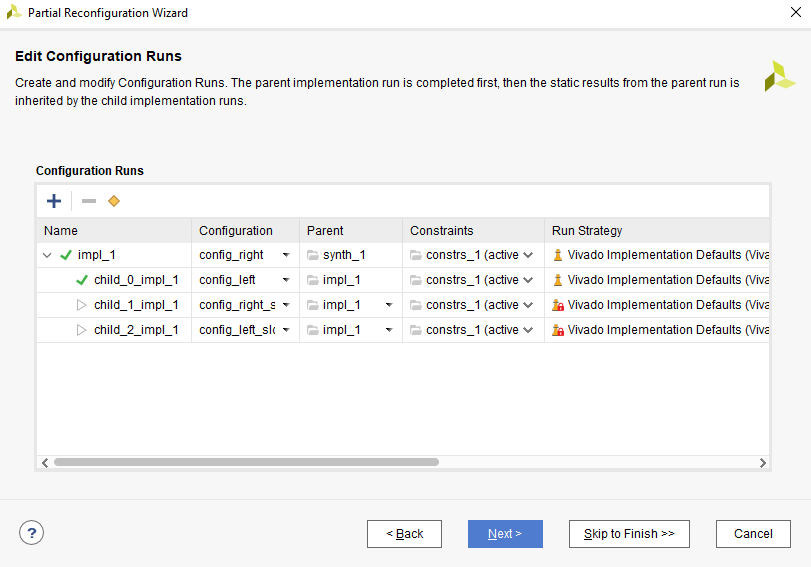
1. Check the top and partial bitstream files



1. Add more modules to the reconfiguration region using the PR/DFX wizard







1. The bitstream locations

