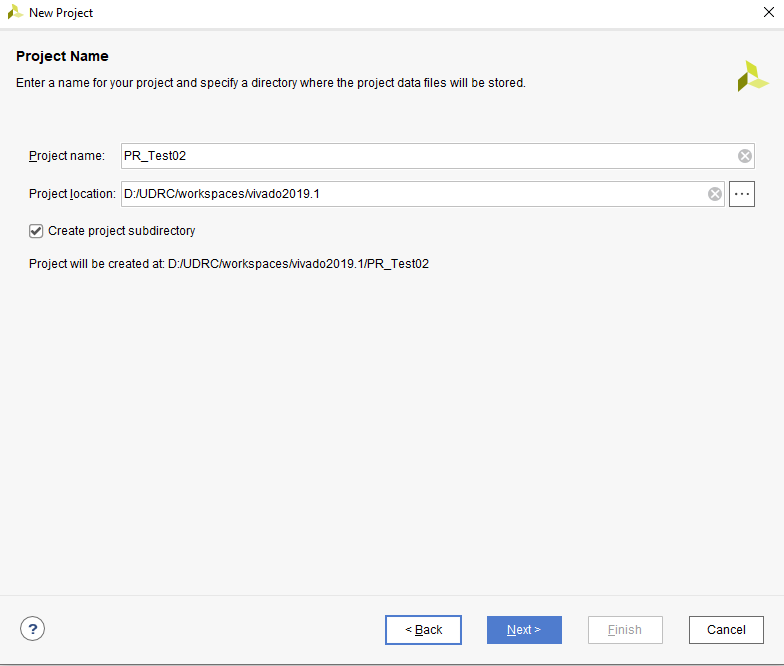
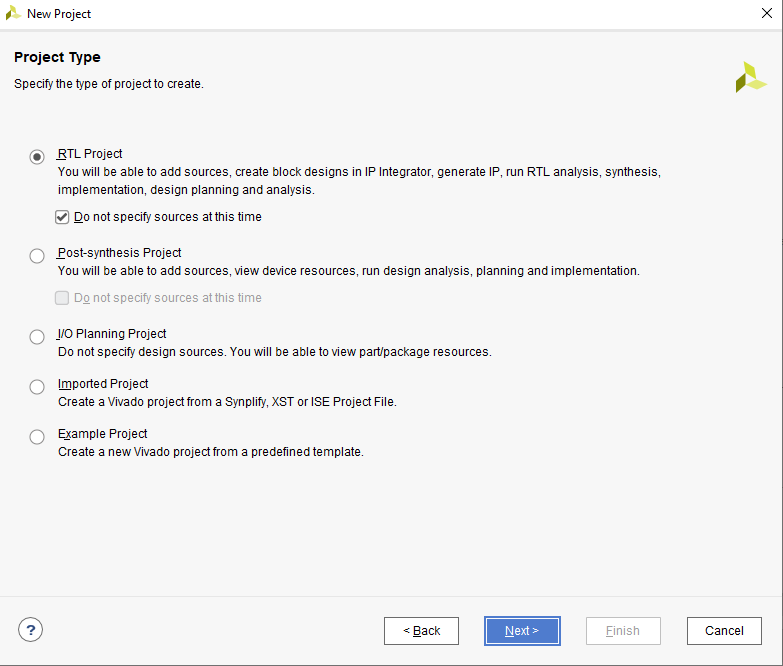
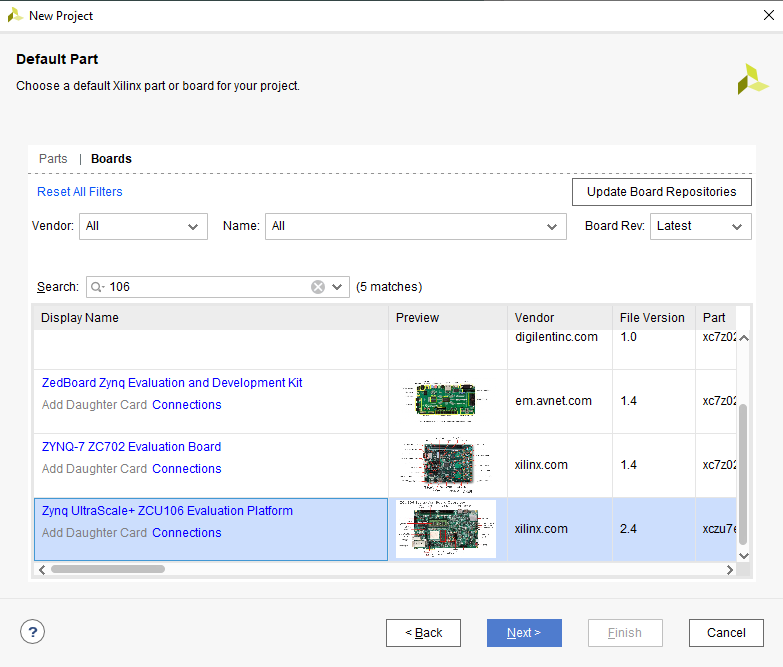
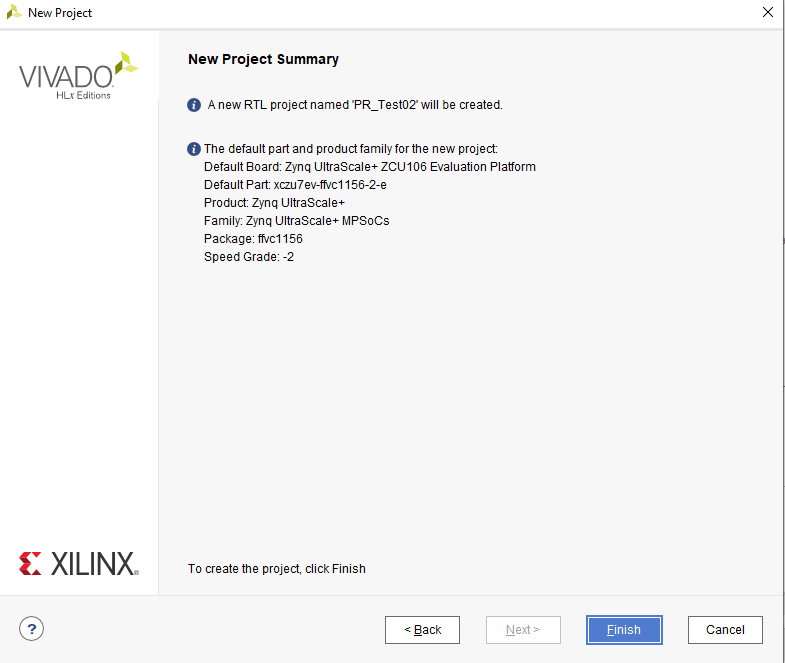
1. Create project

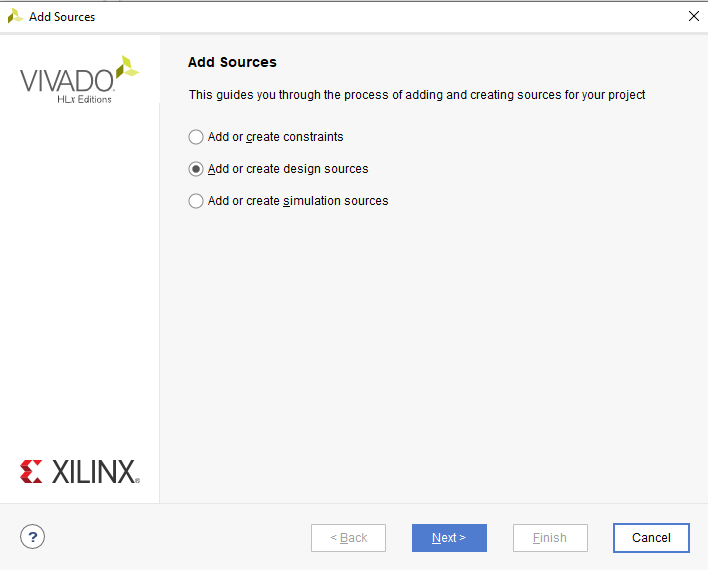


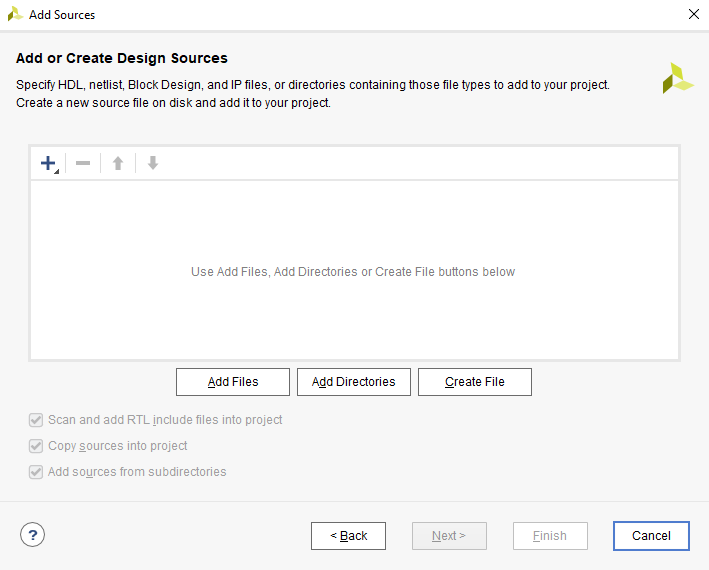


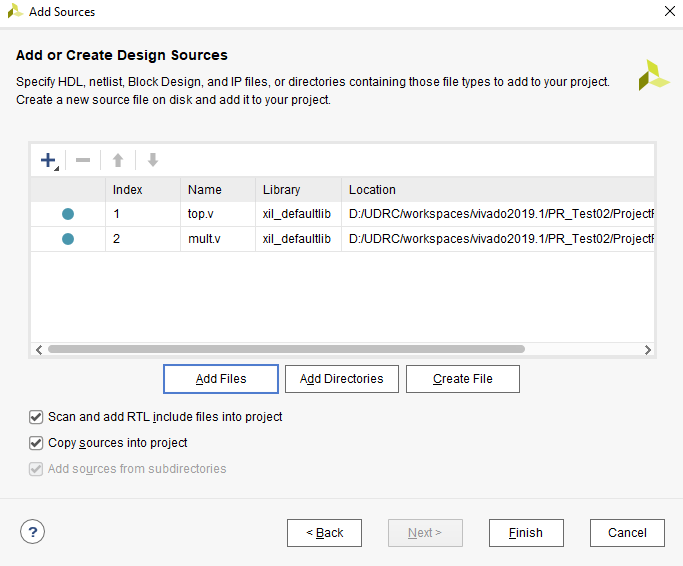


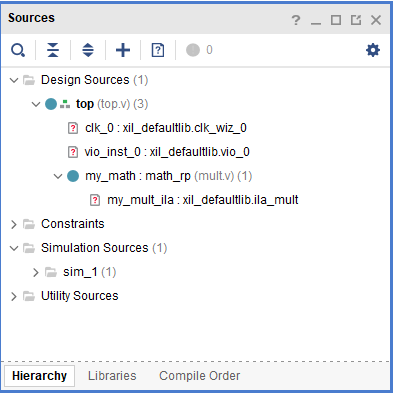


1. Add top and multiplier hdl files

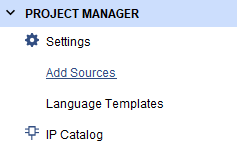


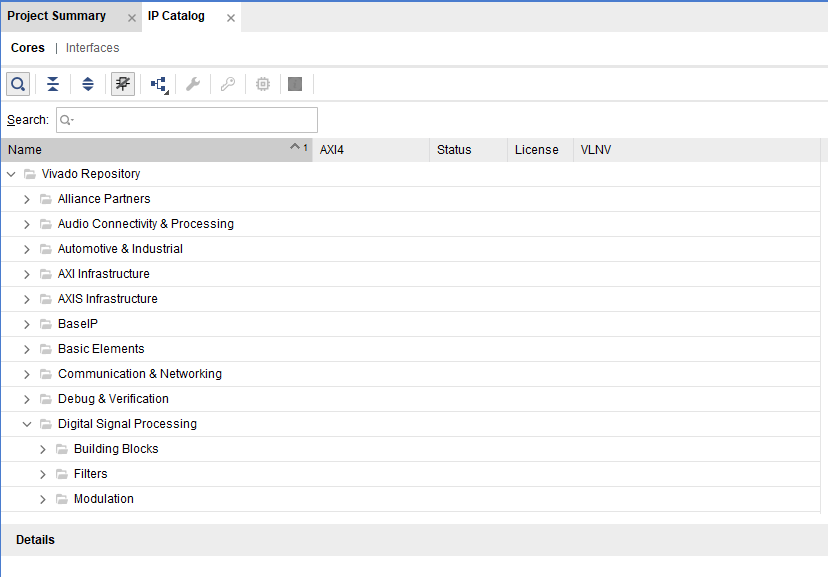


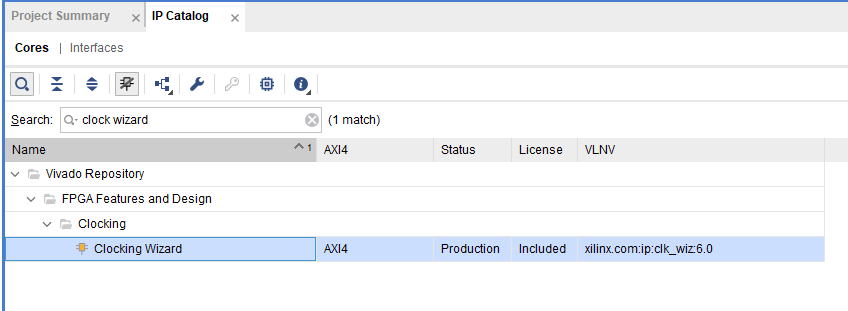


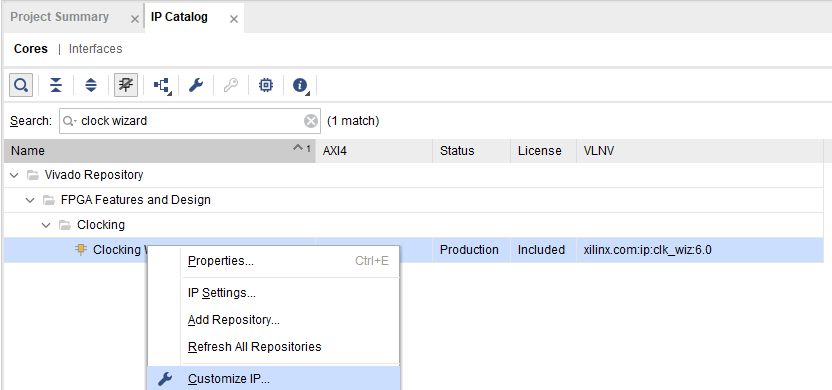


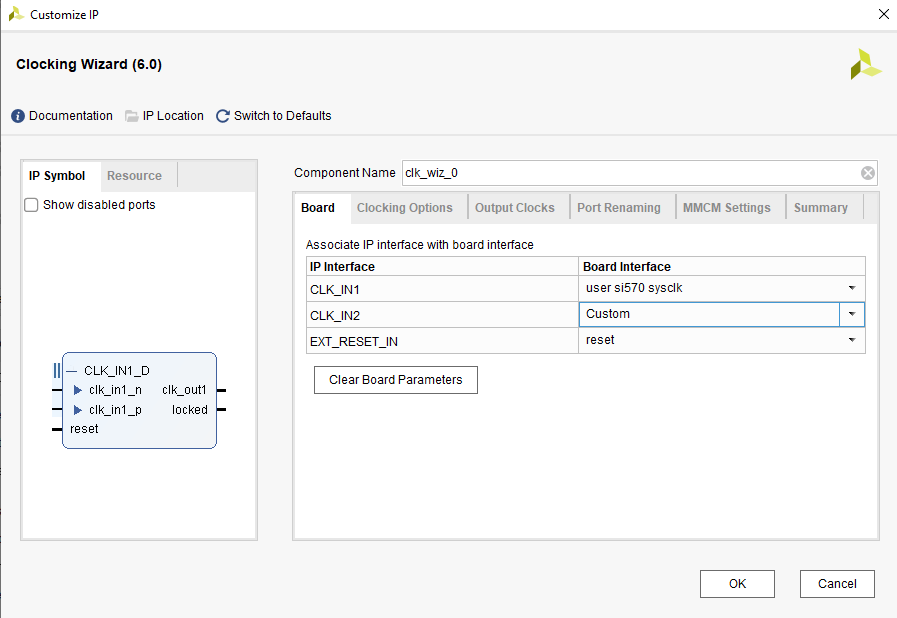
1. Create clock wizard IP from IP catalogue



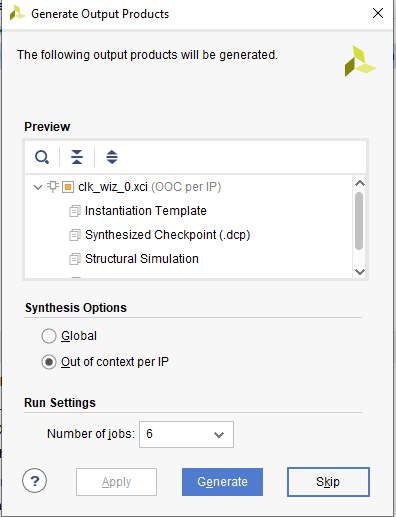




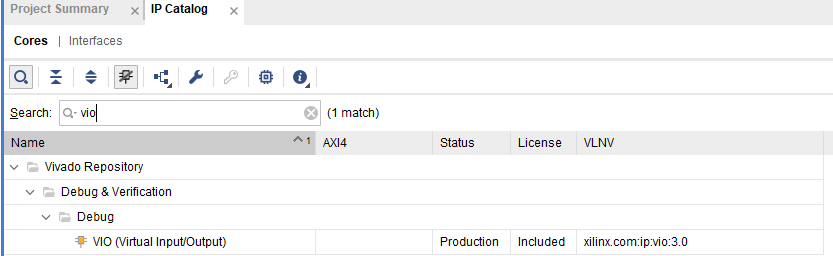


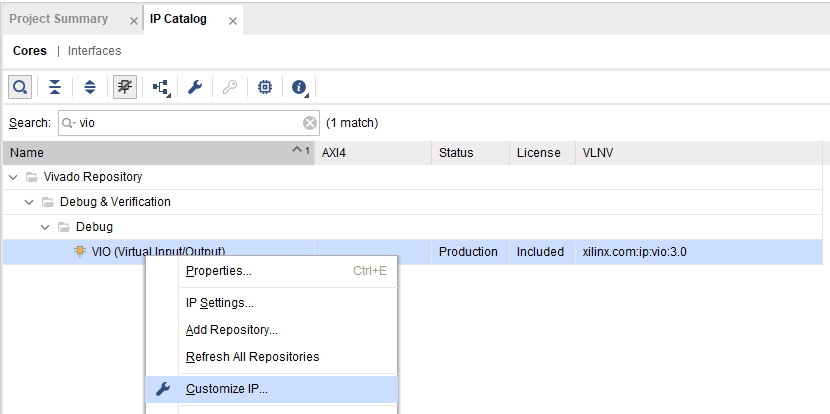


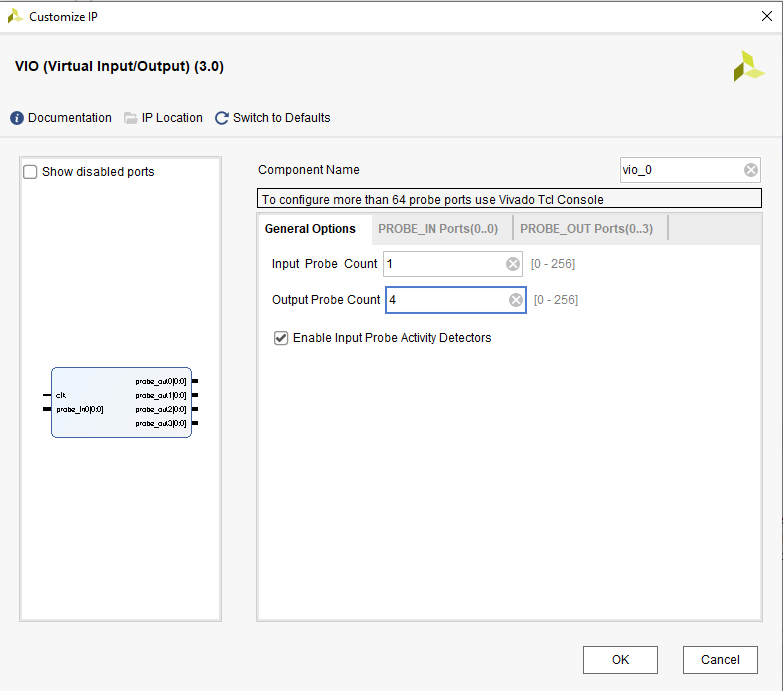
Choose skip instead of generate option.



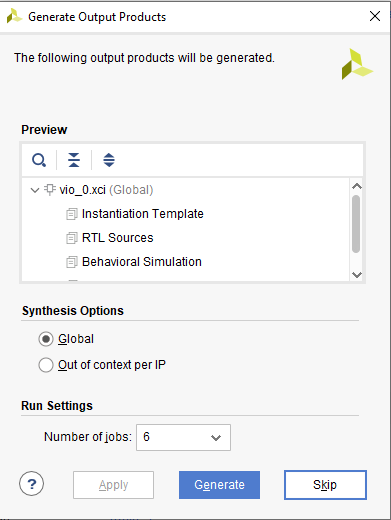
1. Create VIO IP from IP catalogue



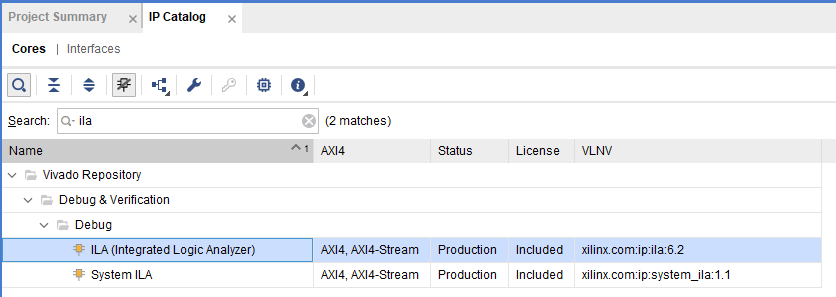


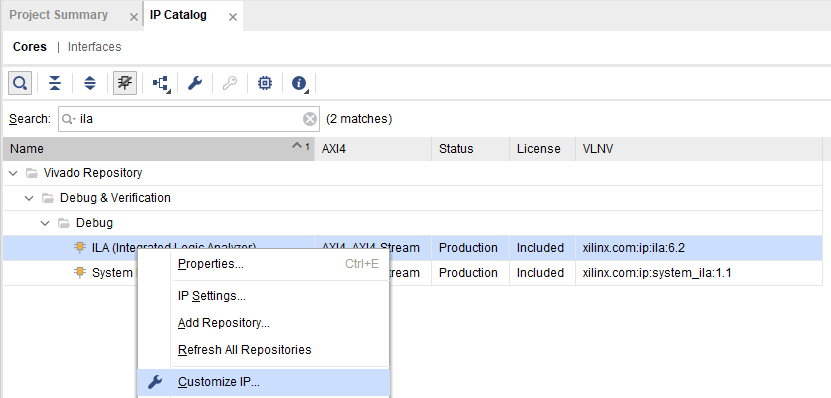


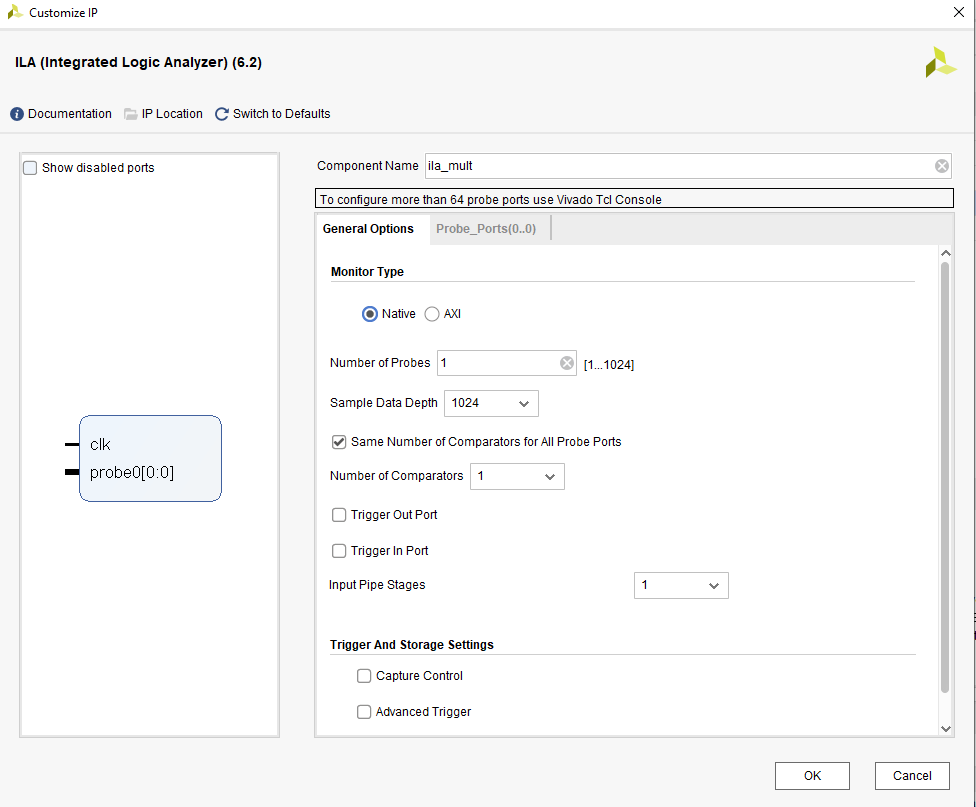
Choose skip instead of generate option.

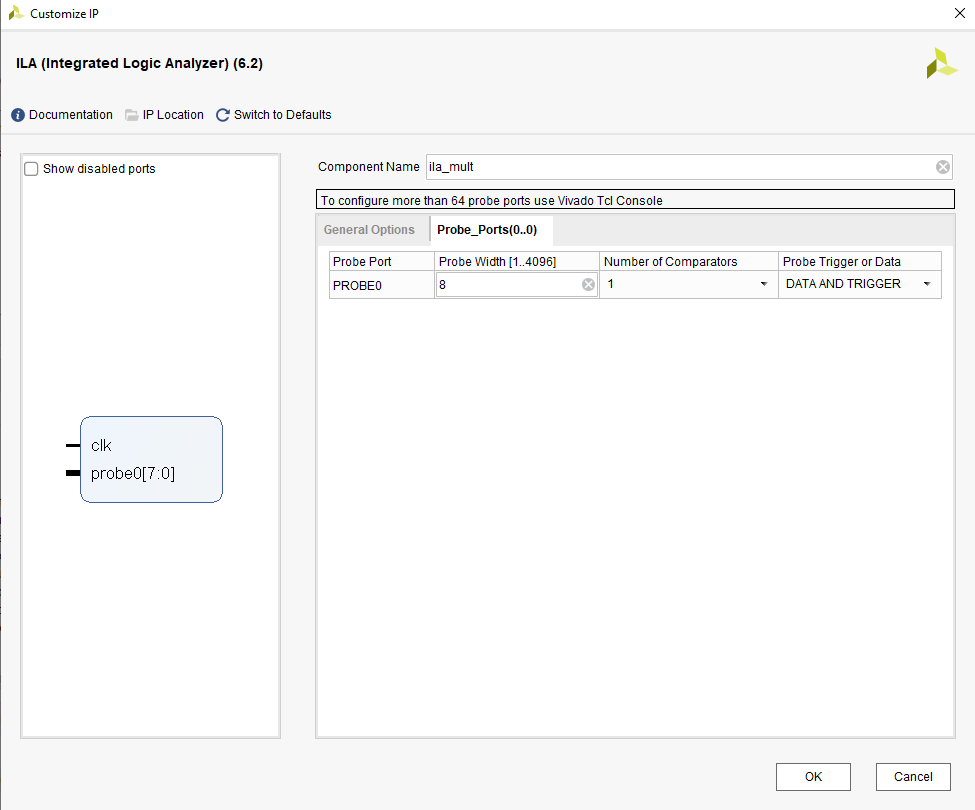


1. Create ILA IP from IP catalogue

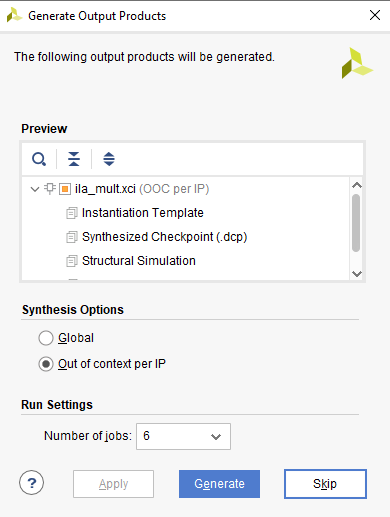




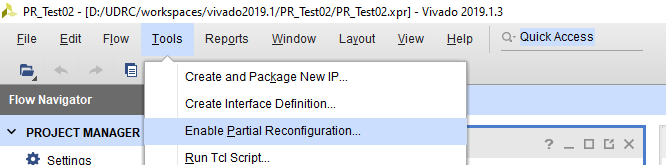


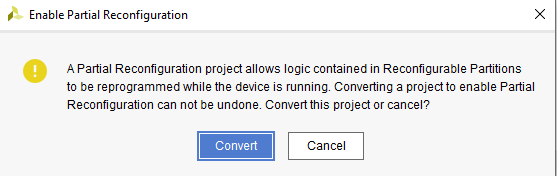


Choose skip instead of generate option.

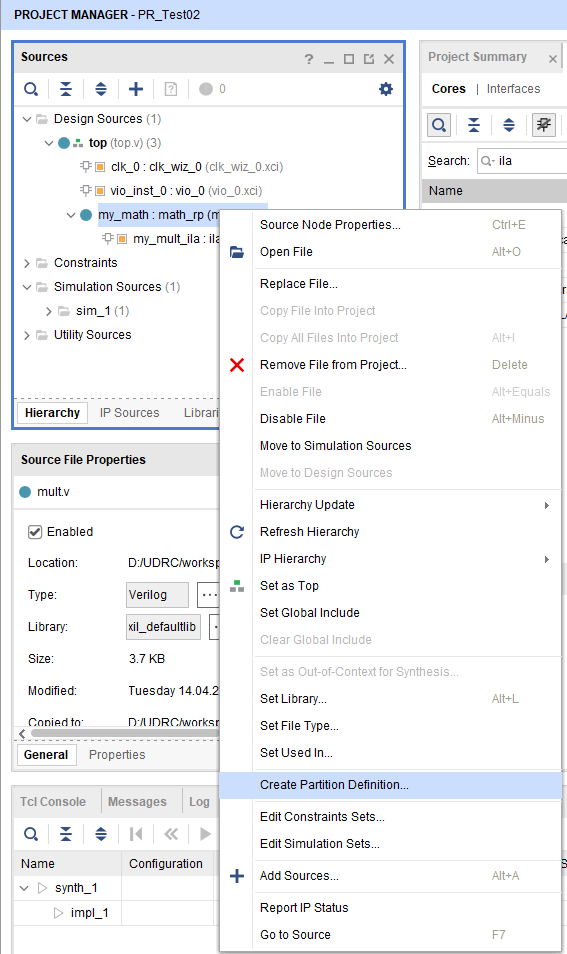


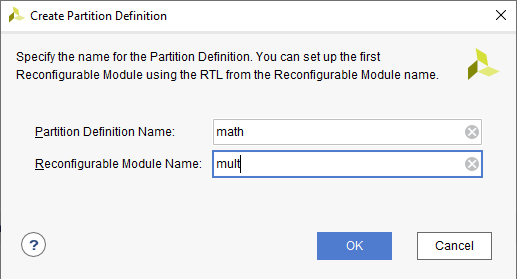
1. Convert project to enable dynamic function exchange

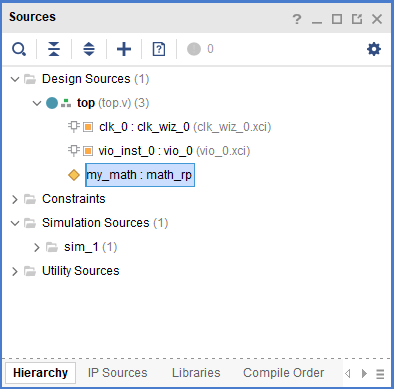


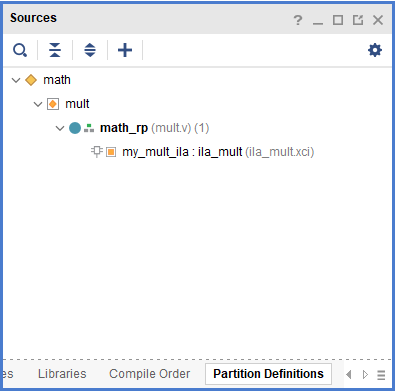


1. Create dynamic reconfiguration partition

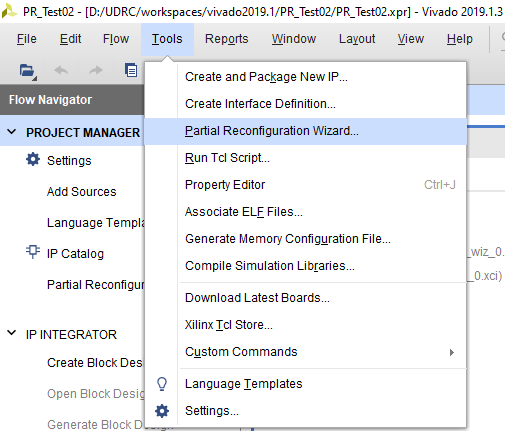


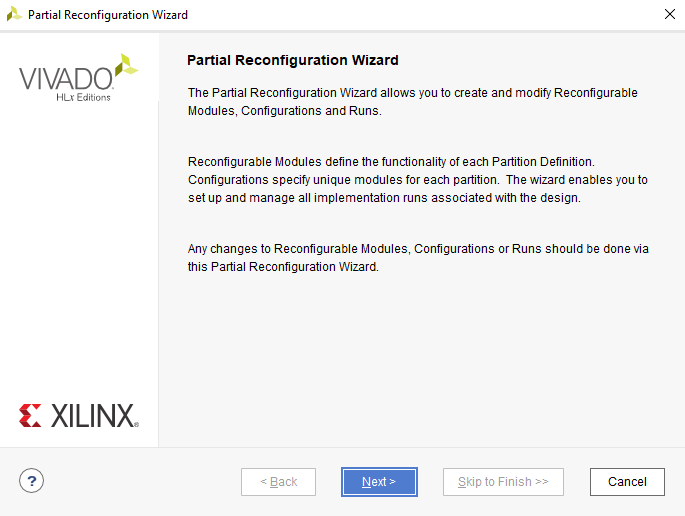


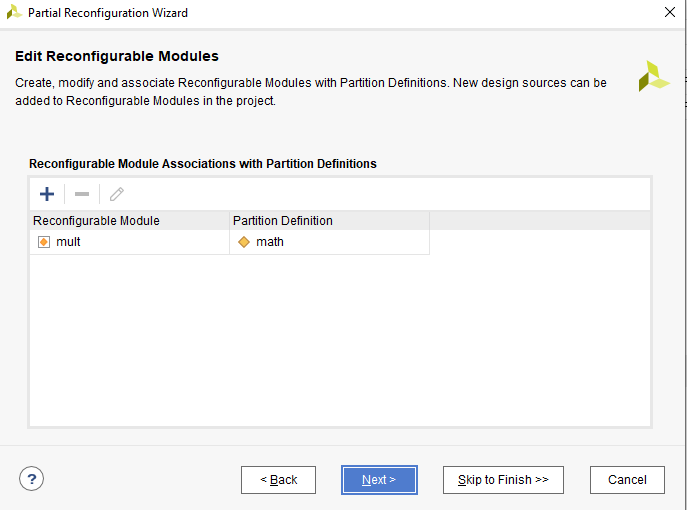


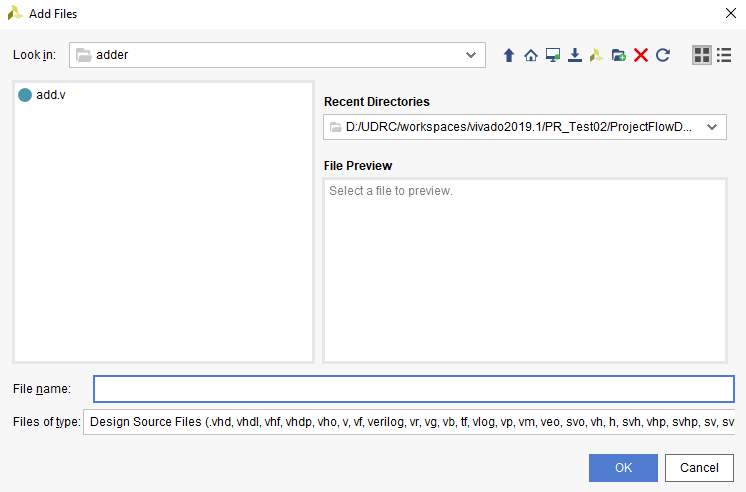


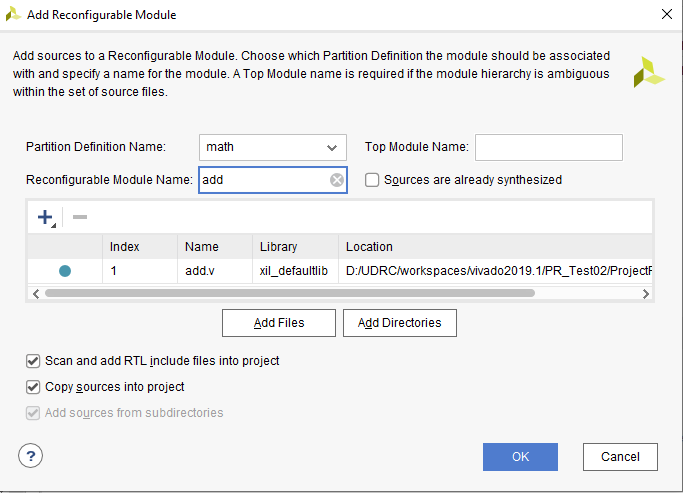
1. Launch Dynamic function eXchange Wizard to add the adder module

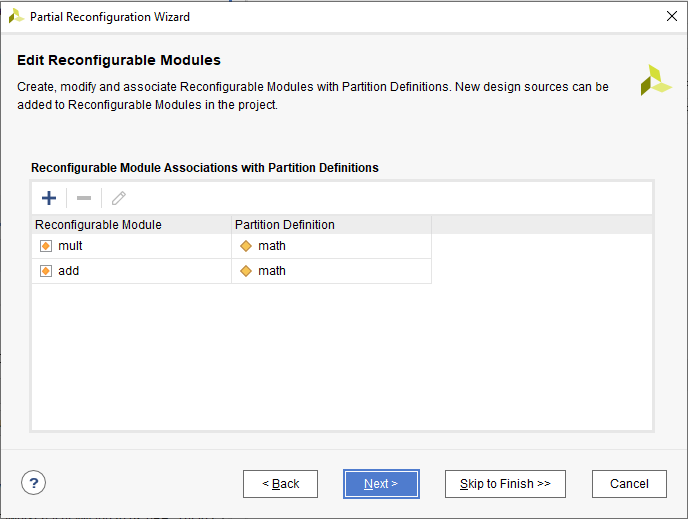


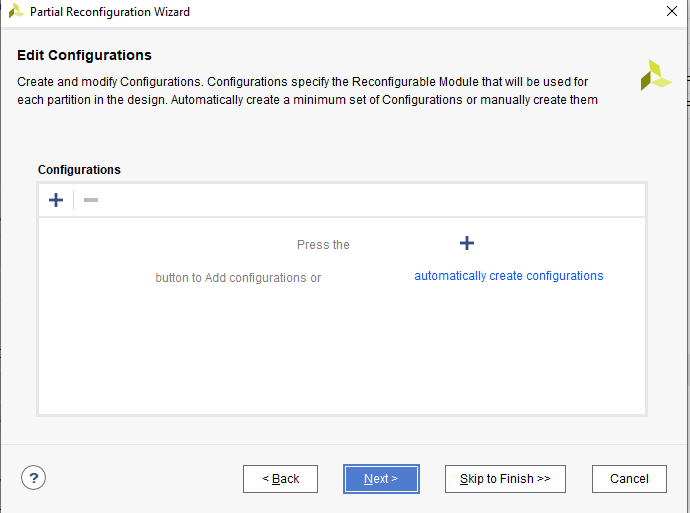




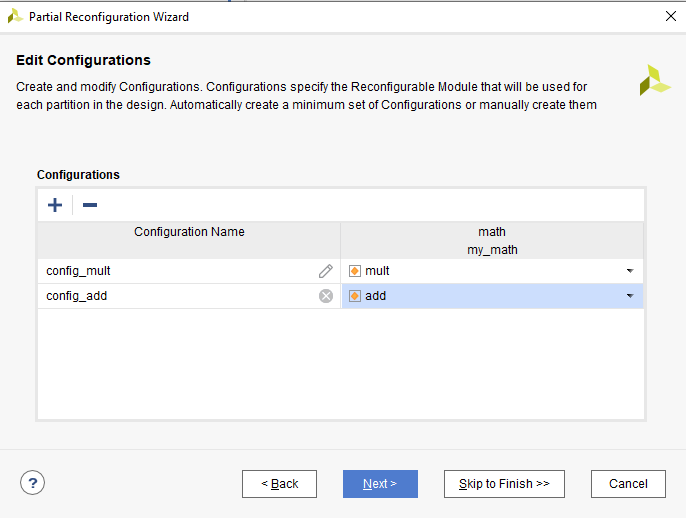


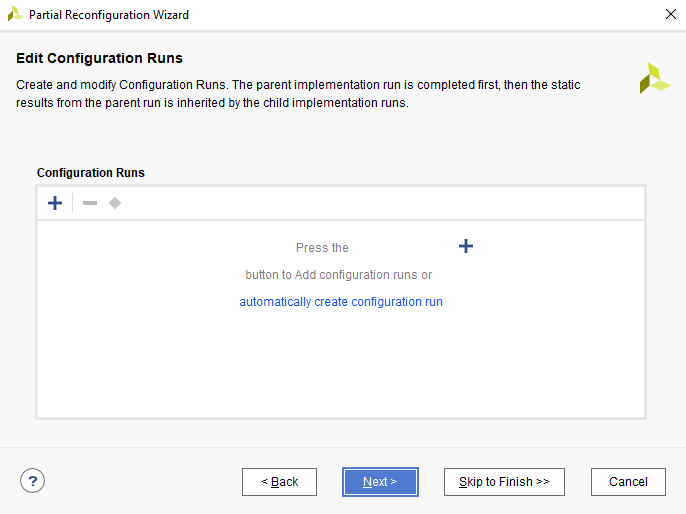




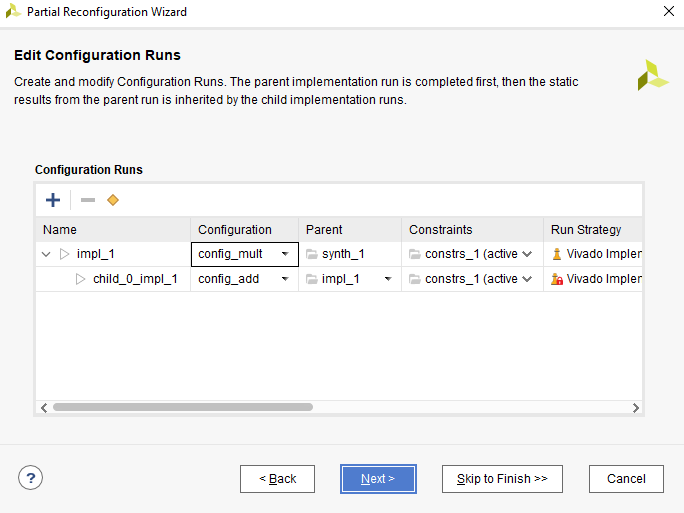


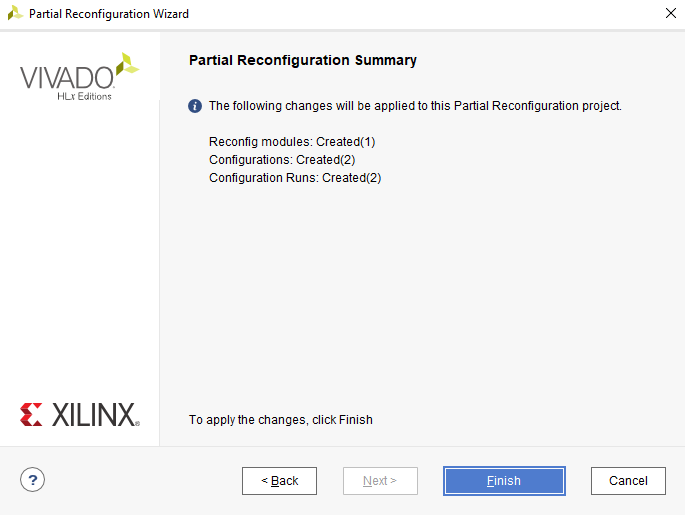
Choose automatically create configurations



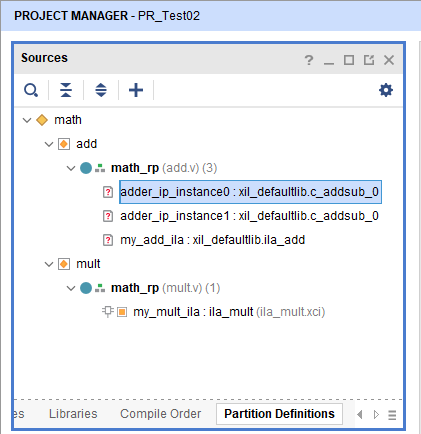


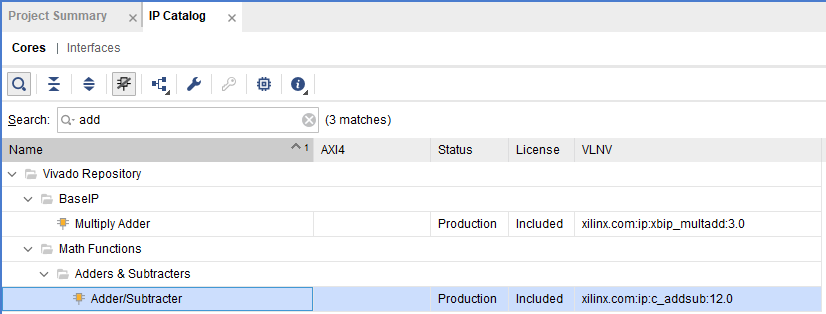
Choose the automatically configuration run

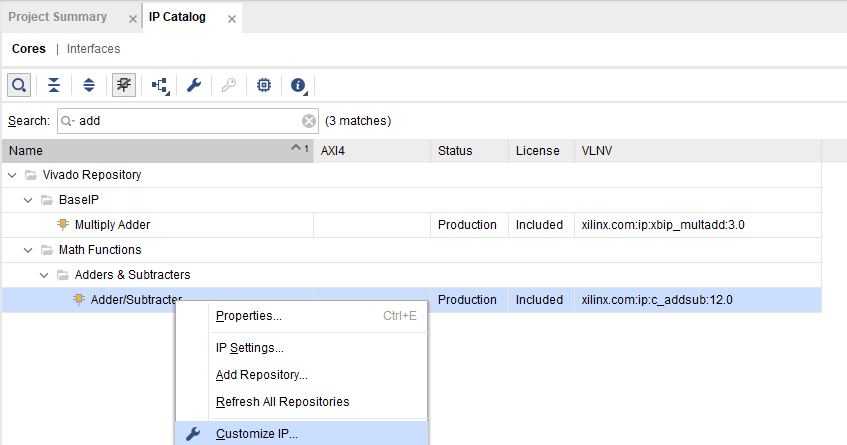


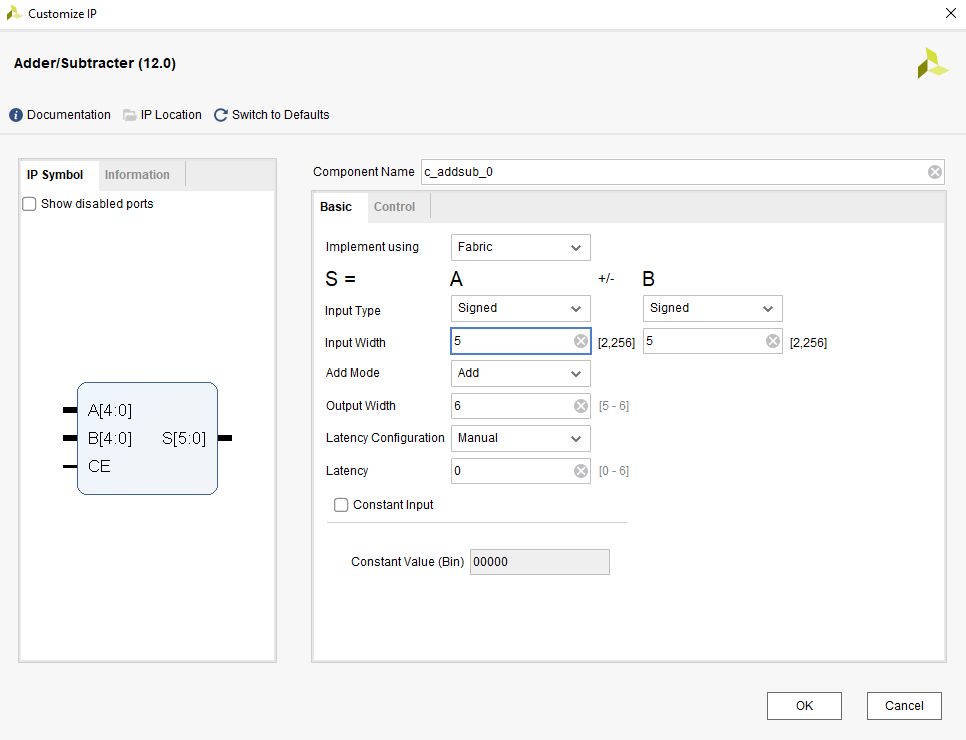


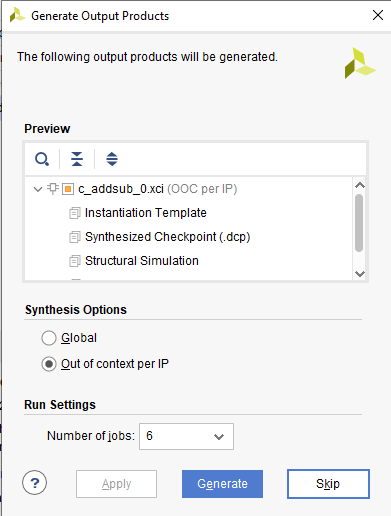
1. Add the adder IP from catalogue to the partial reconfiguration partition module

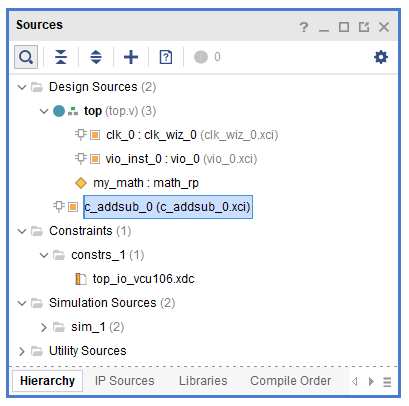




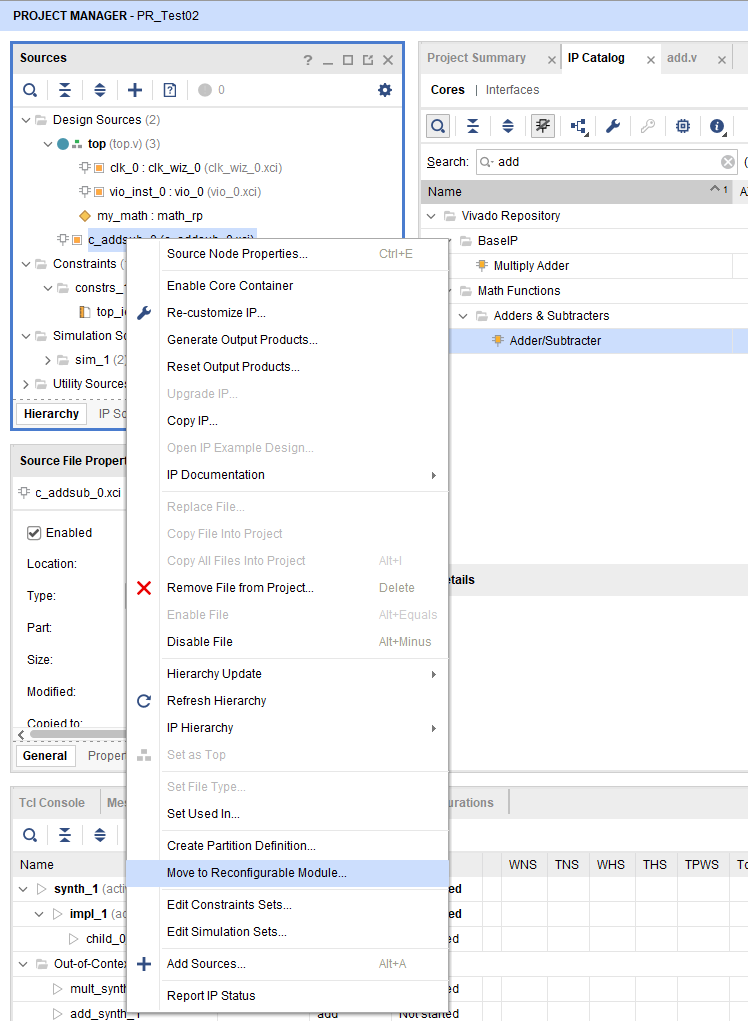


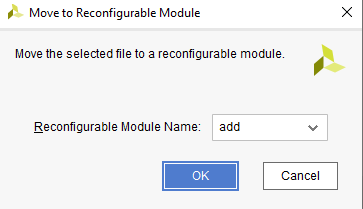


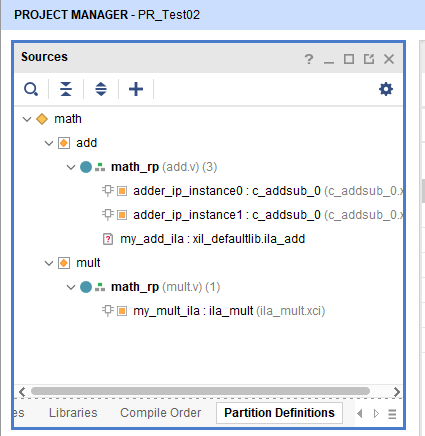




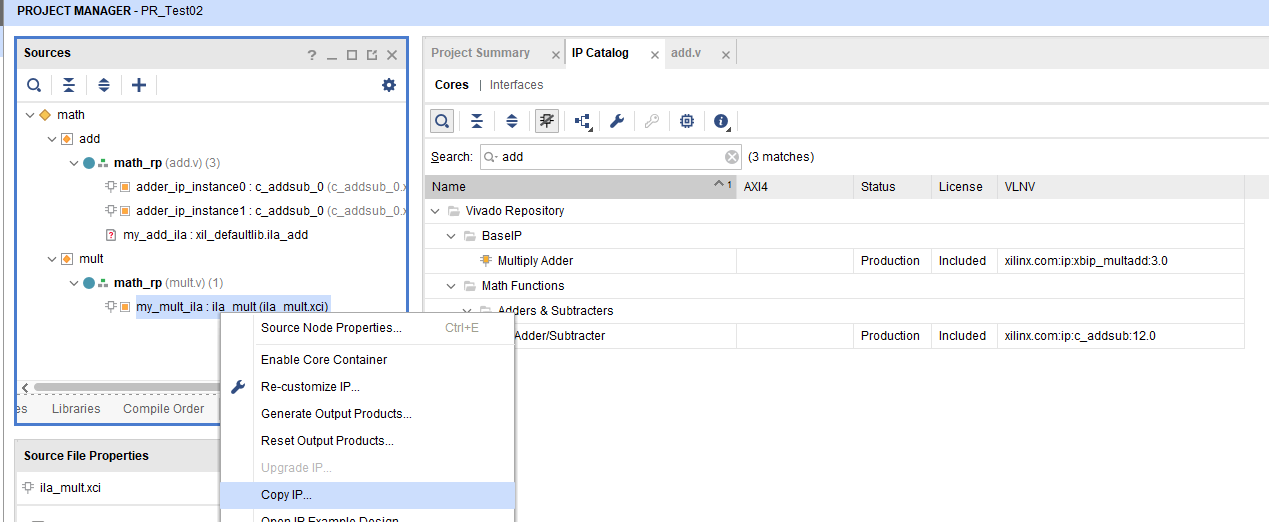
Move the added IP to the reconfigurable module

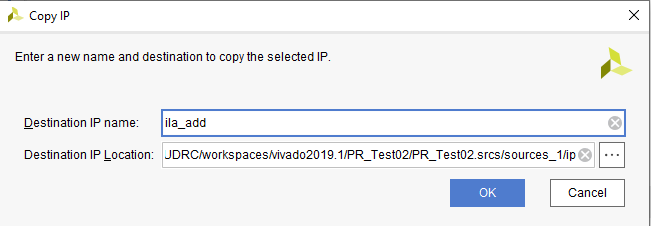


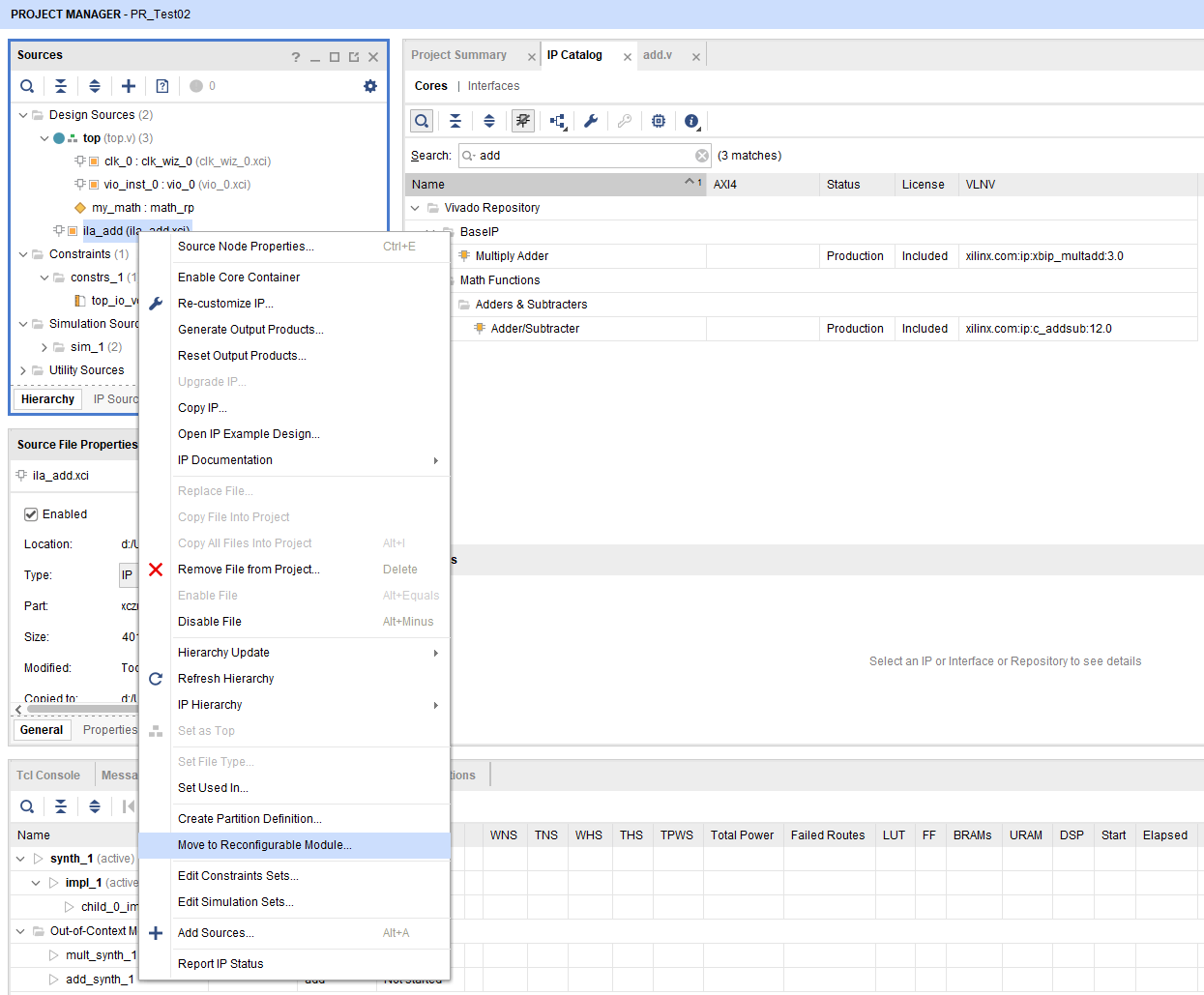


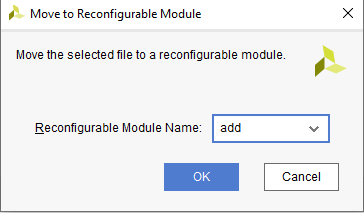


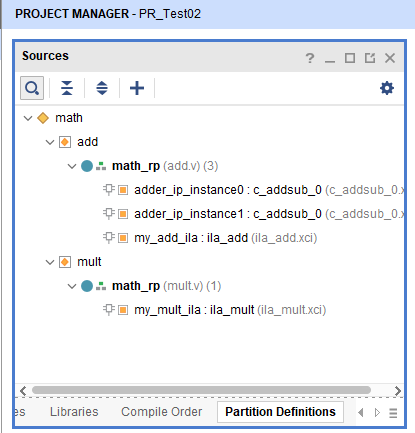
1. Copy the ILA IP from the multiplier to the adder



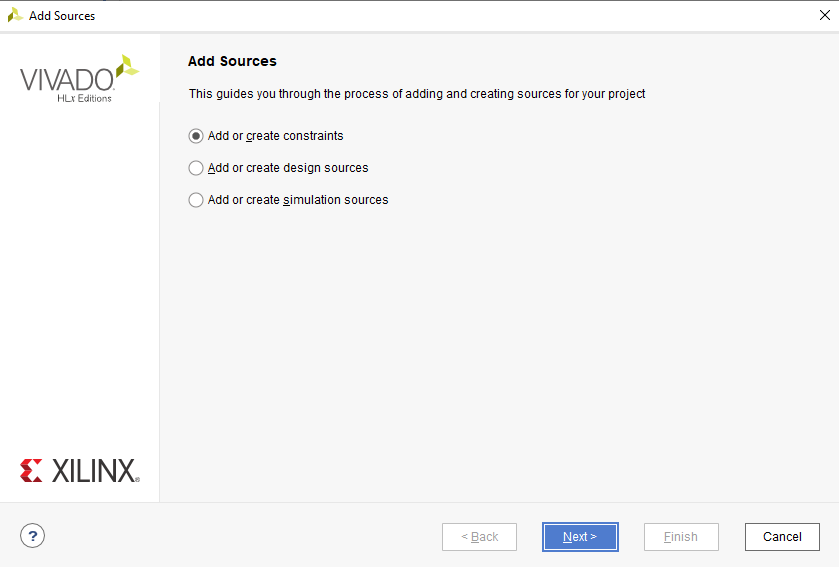


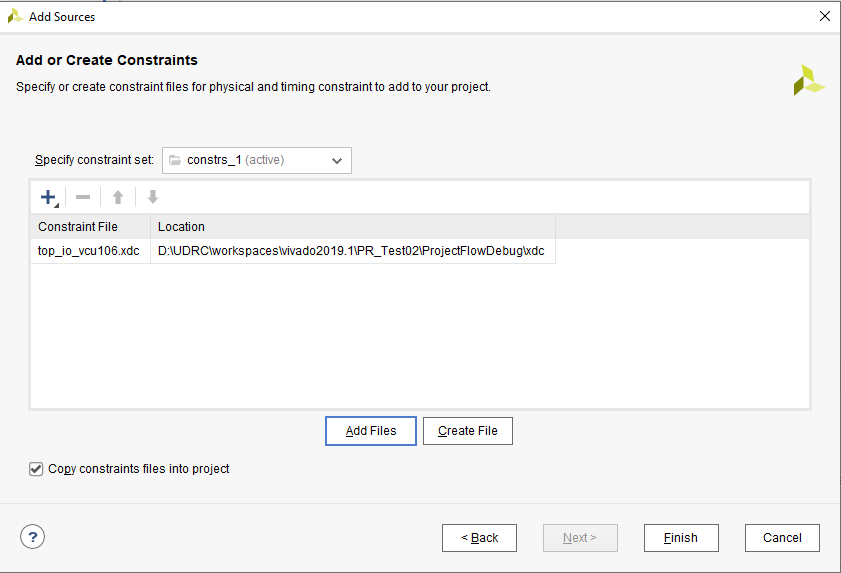


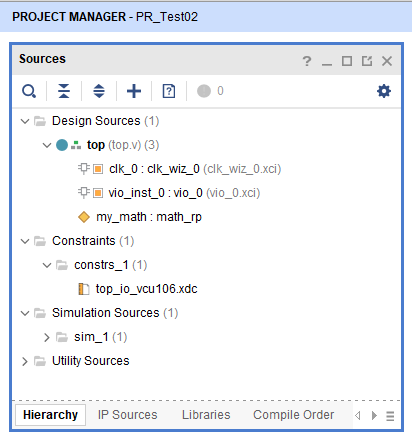




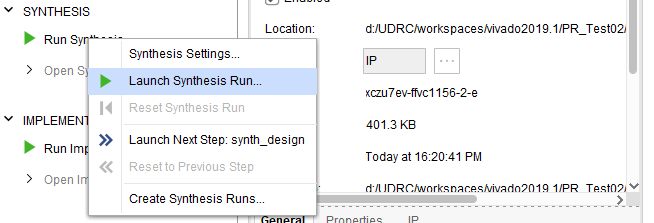
1. Add the constraint XDC file to the project

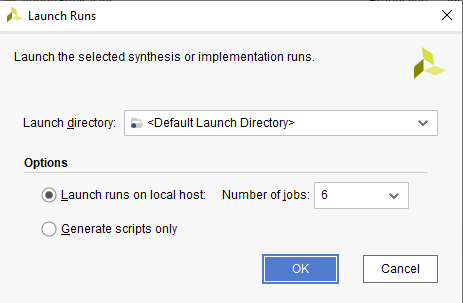




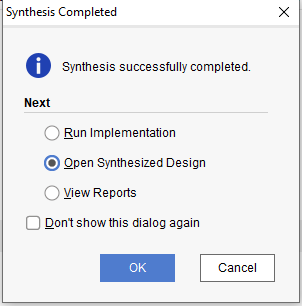


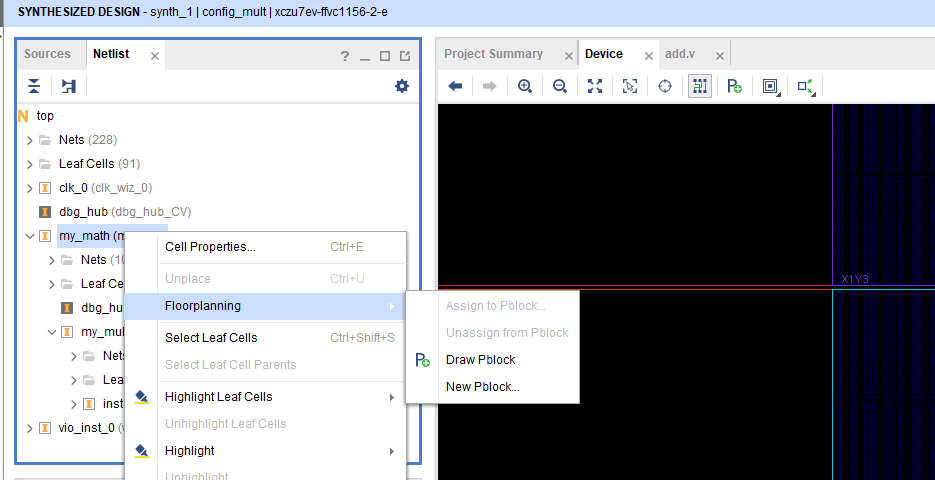
1. Synthesize the design

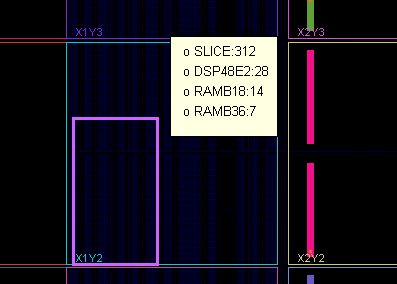


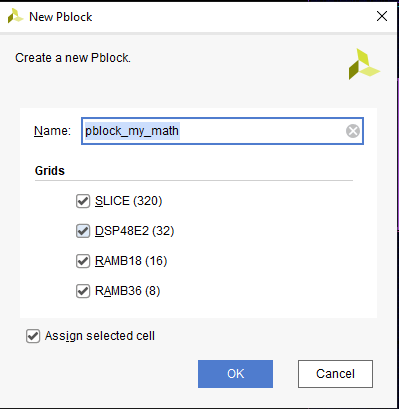


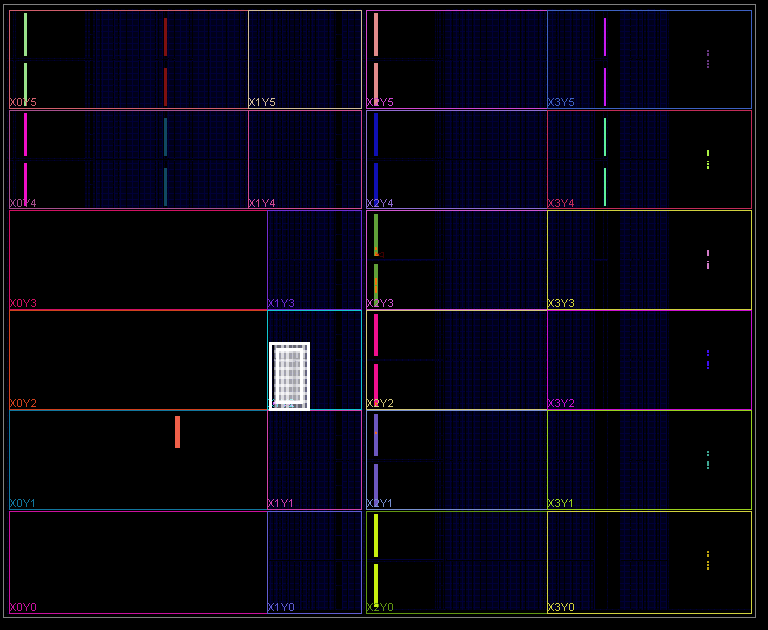
1. Open the synthesis design and choose the floorplanning for the reconfiguration partition



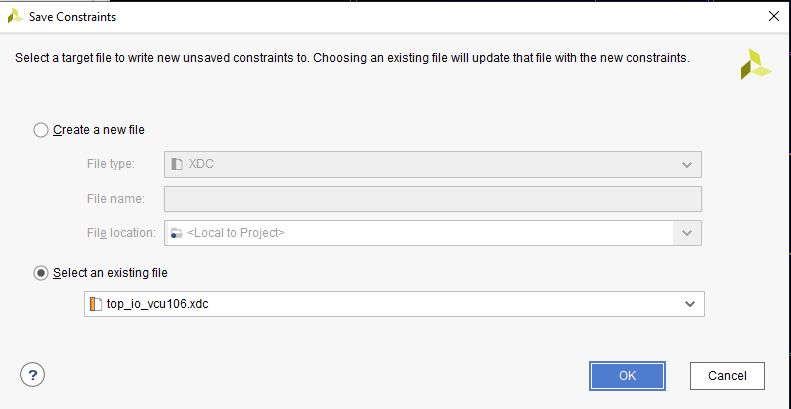


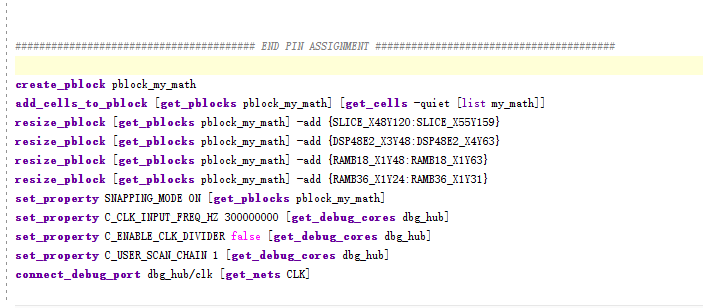




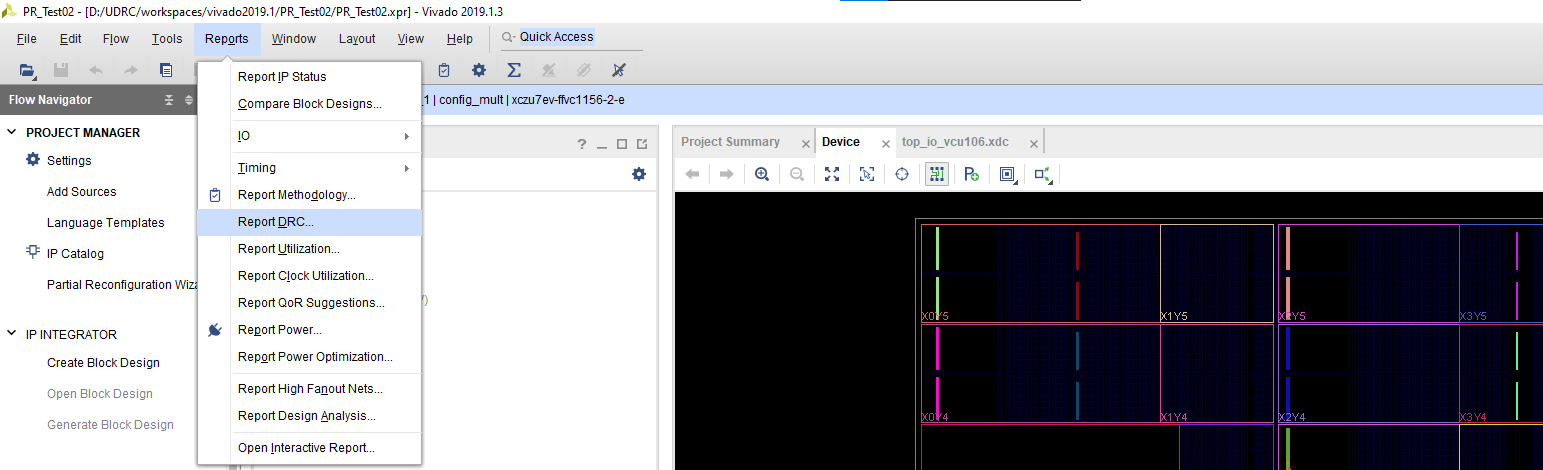


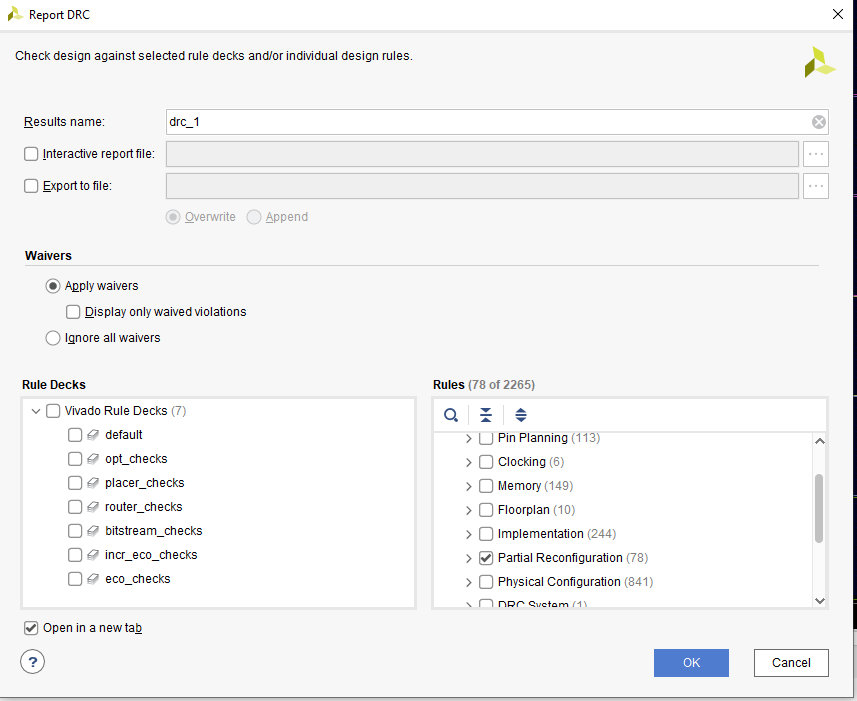
Then save the project which will initiate the constraint file update

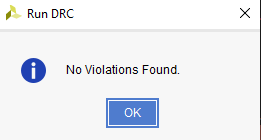




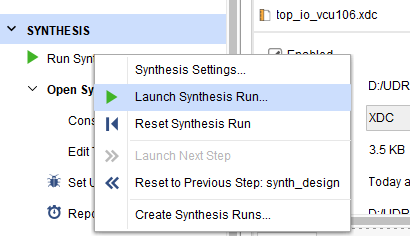
1. Do the design rule check

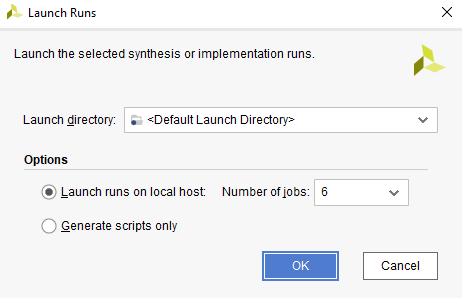




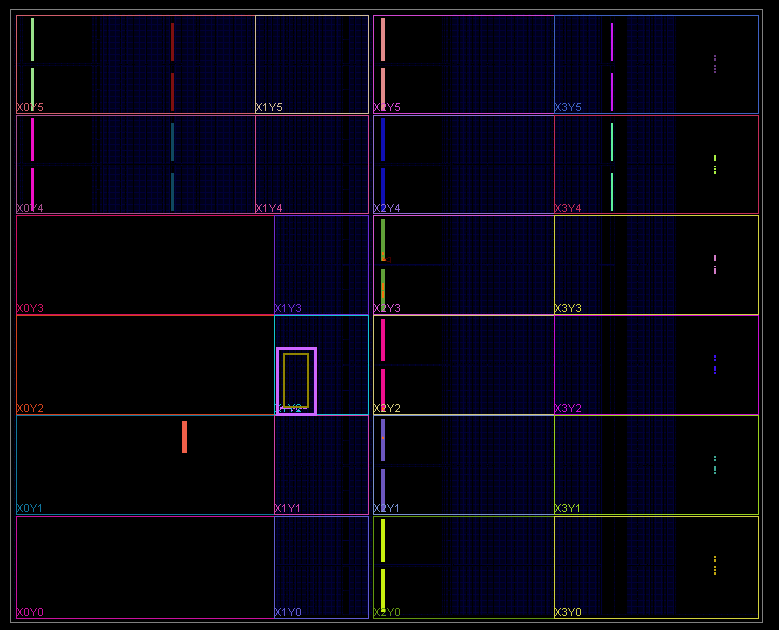


1. Redo the synthesis process for the project with the updated constraint file

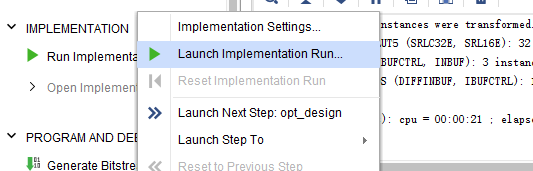


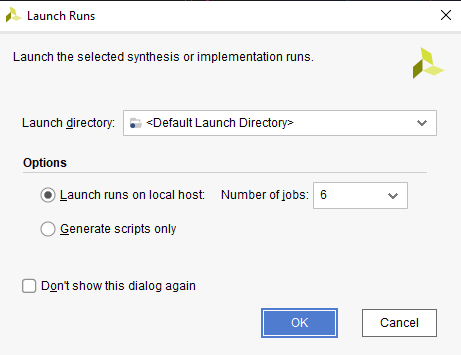


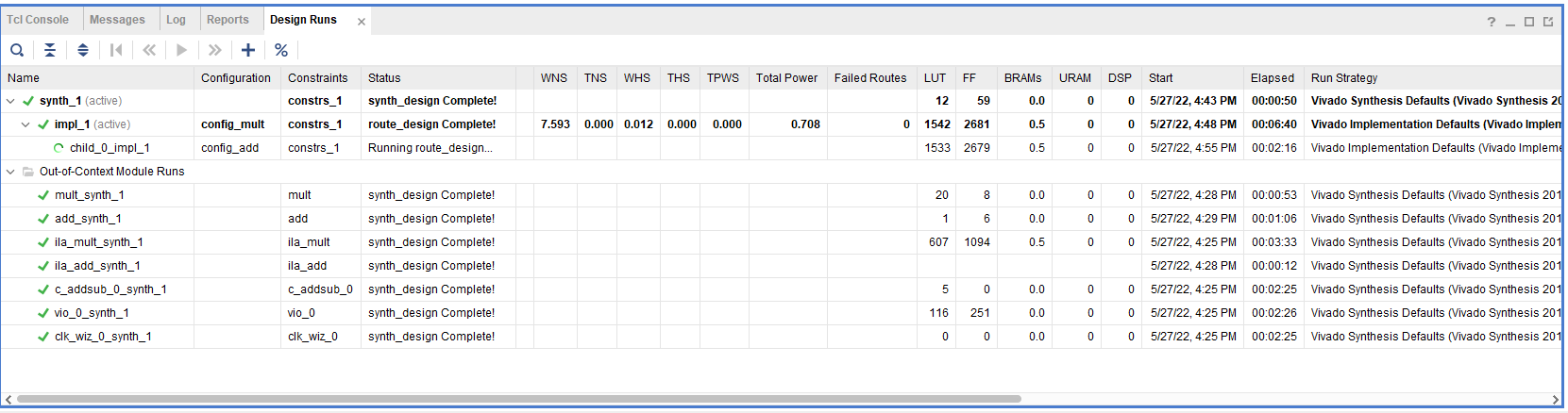
If open the synthesis design, the predefined floorplanning will constraint the place and route to specific location of netlist.

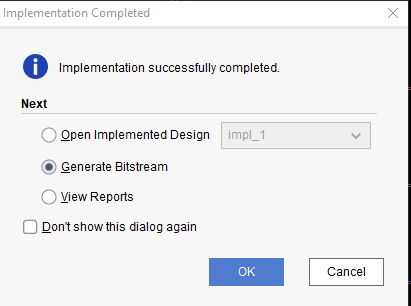


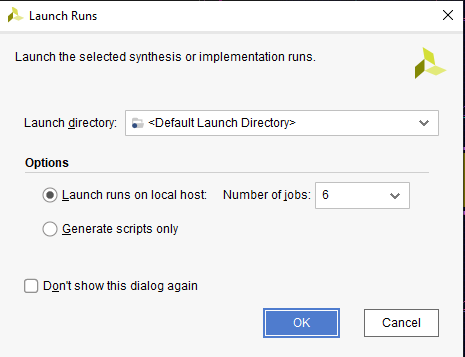
1. Run the implementation and generate the bitstream files

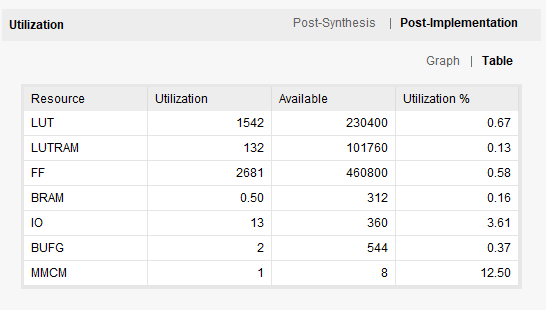


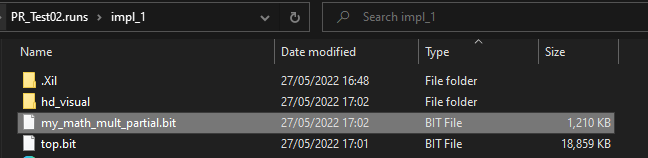


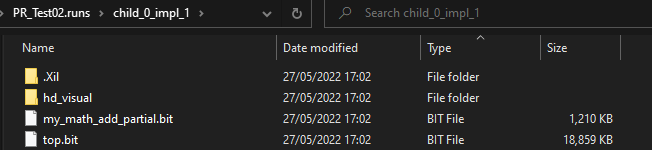




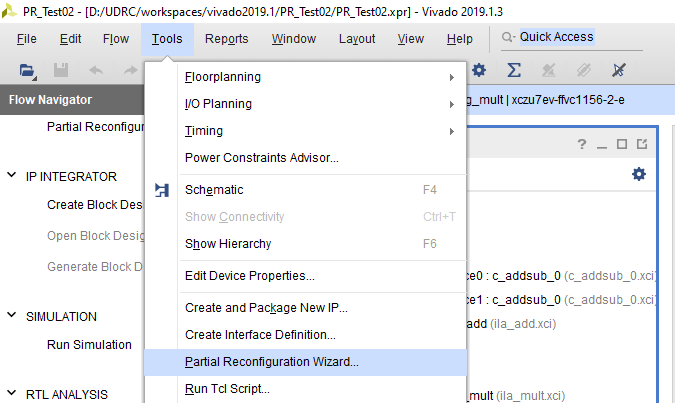


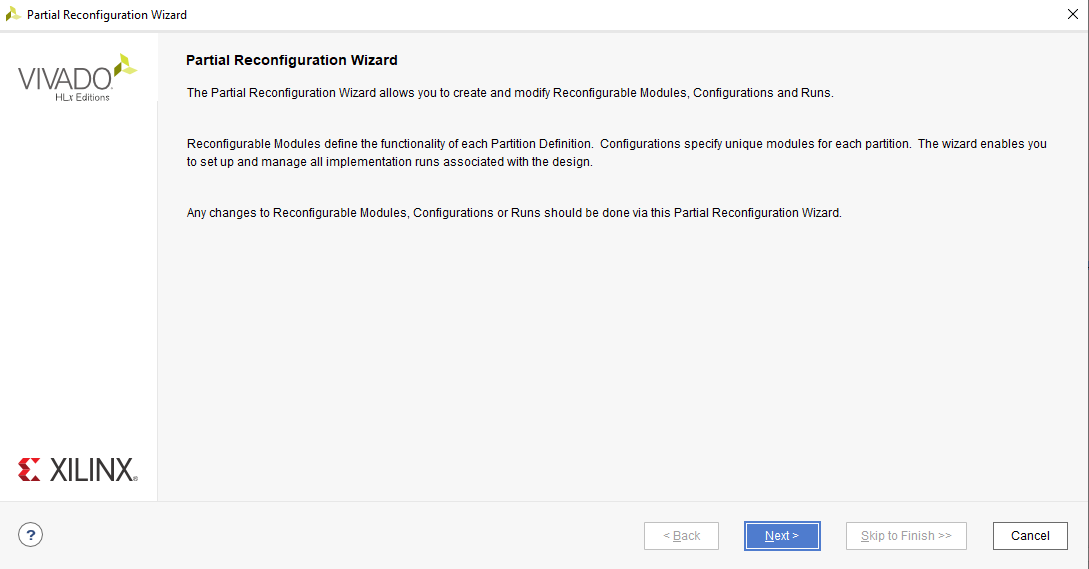




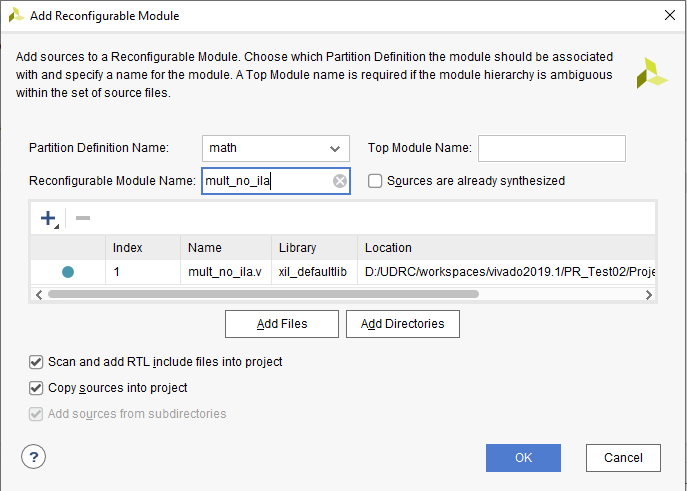


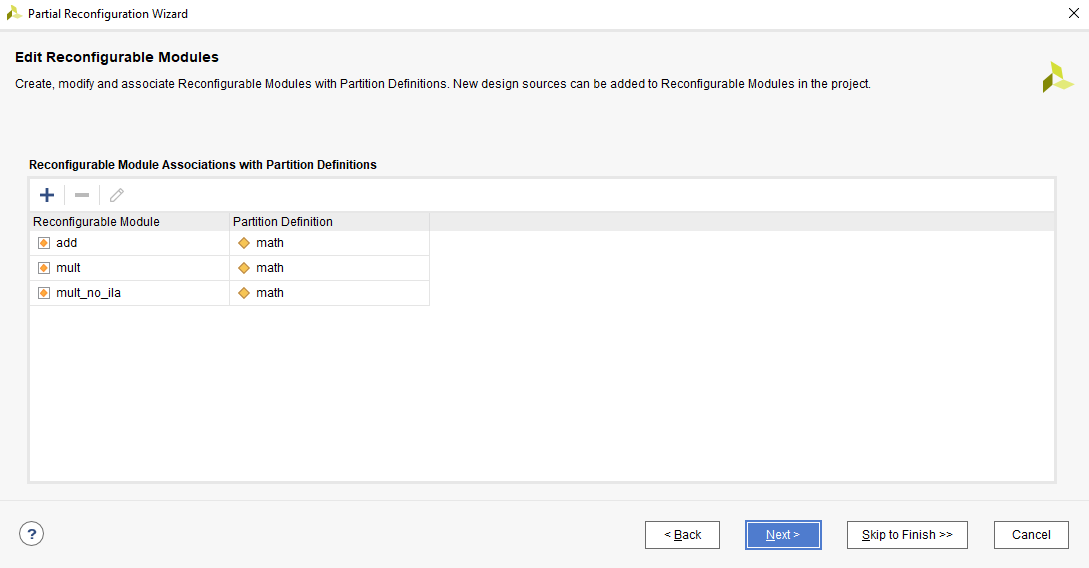
1. Add another reconfiguration module after bitstream generation

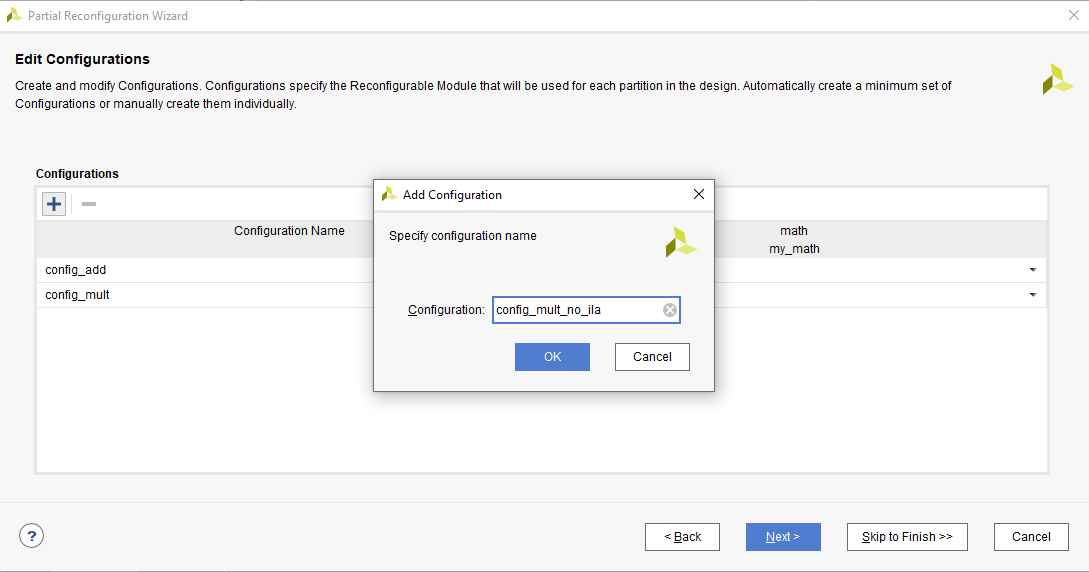


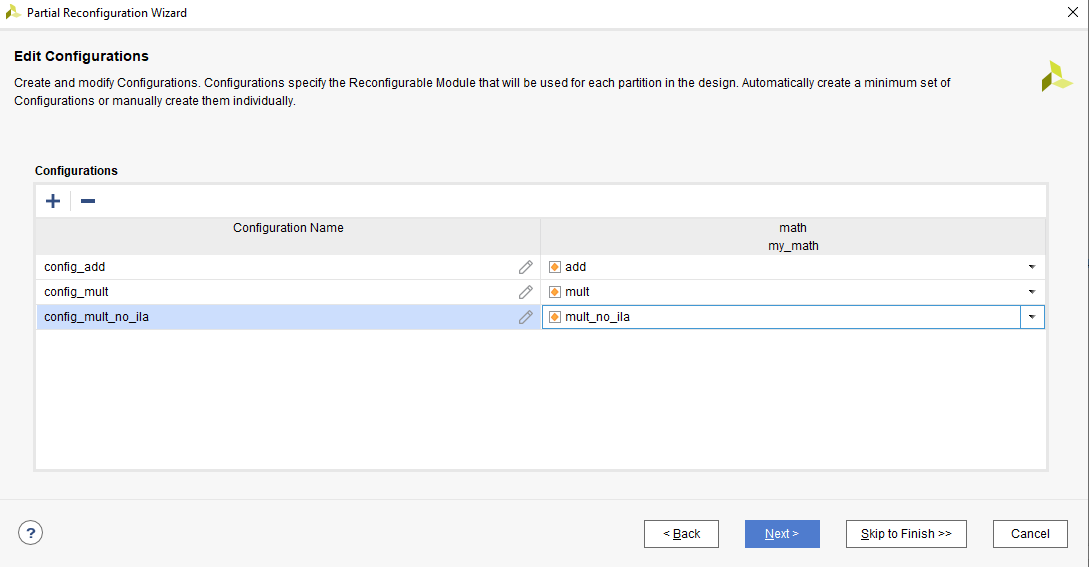


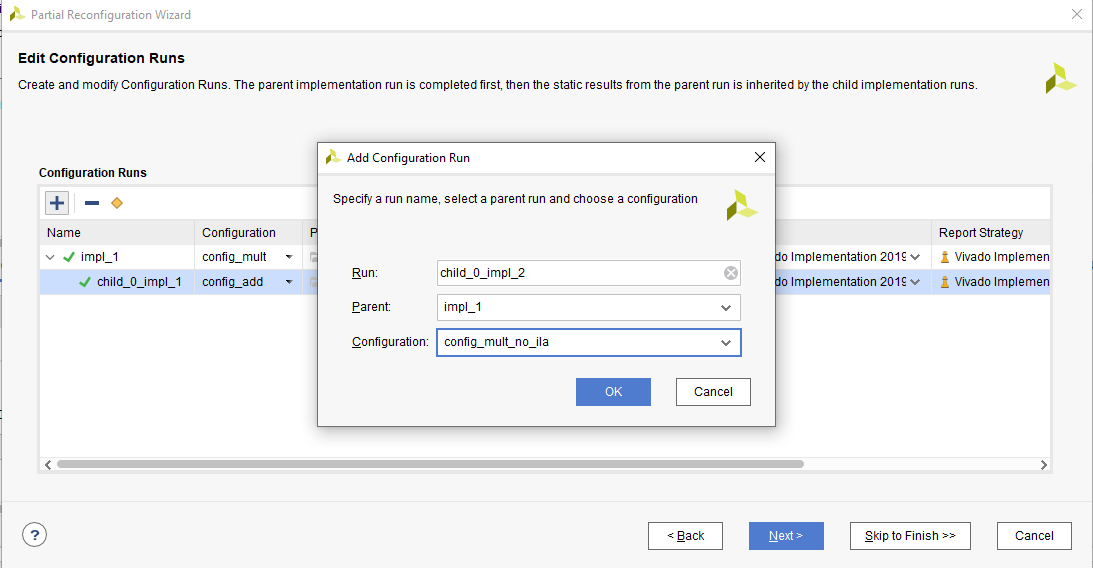


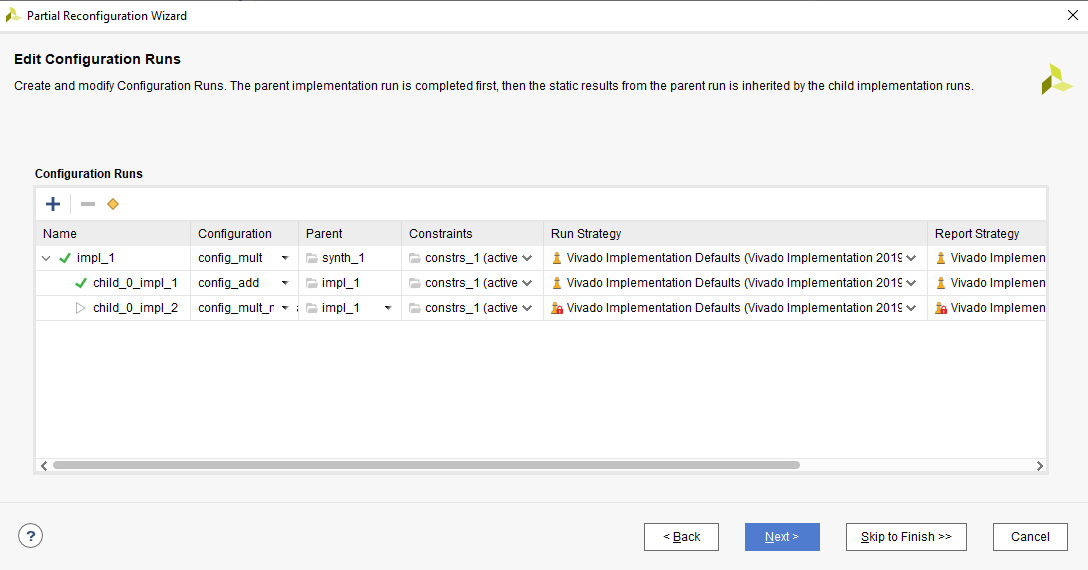


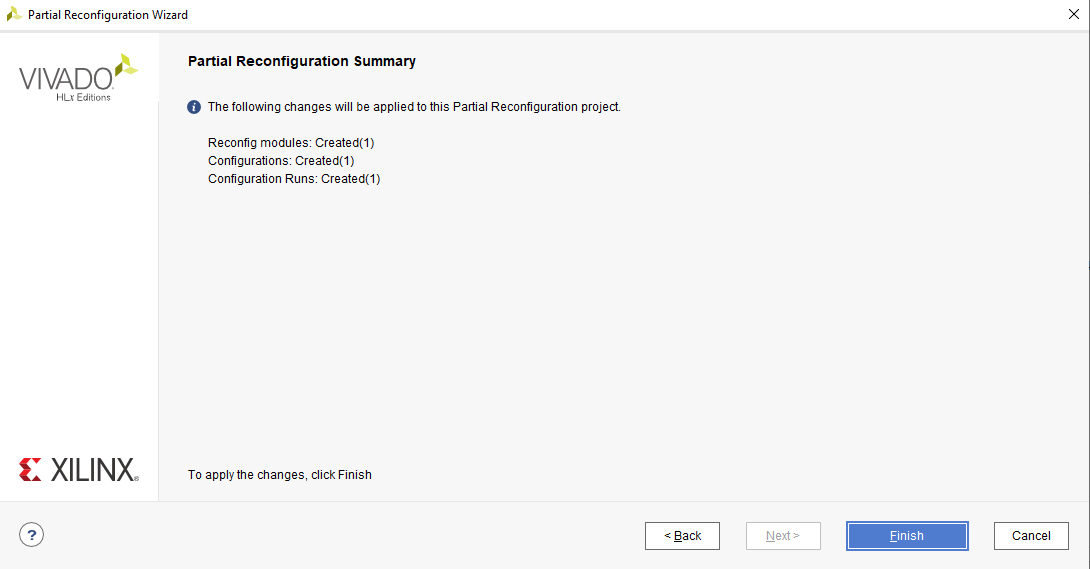




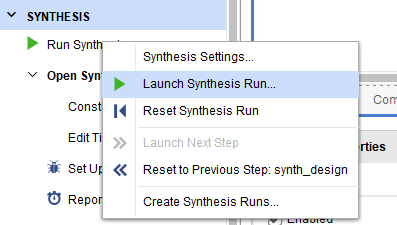


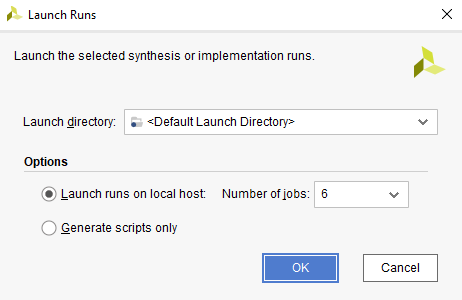


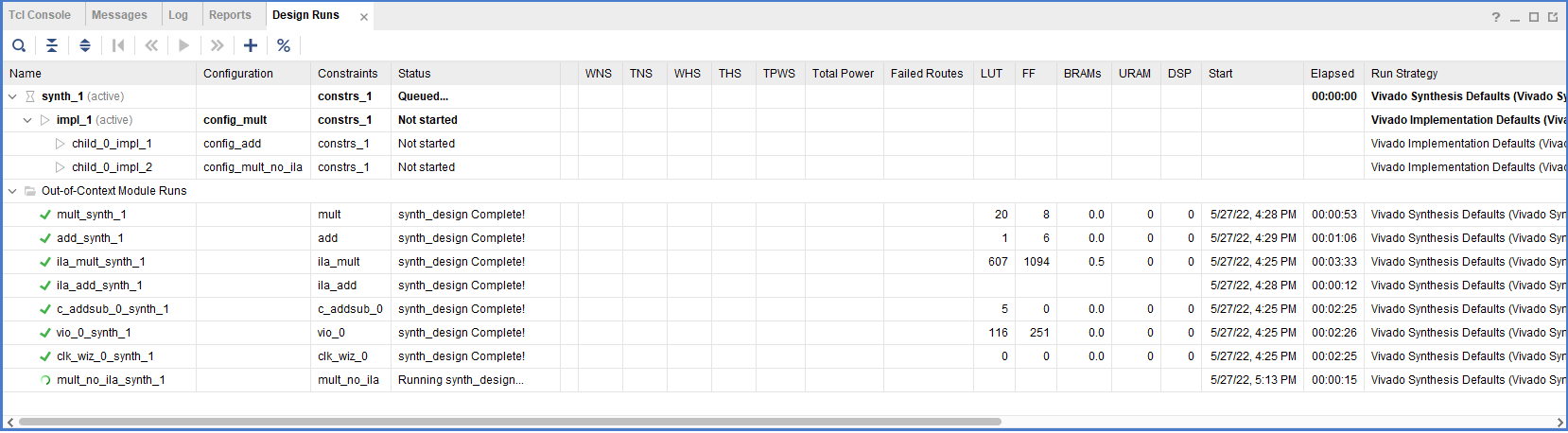


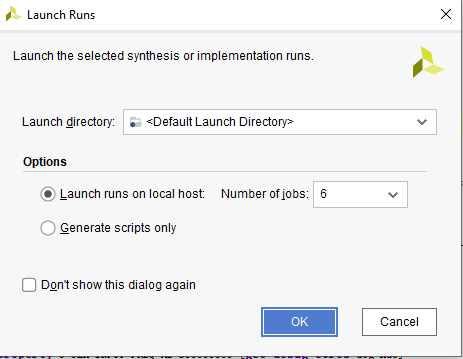


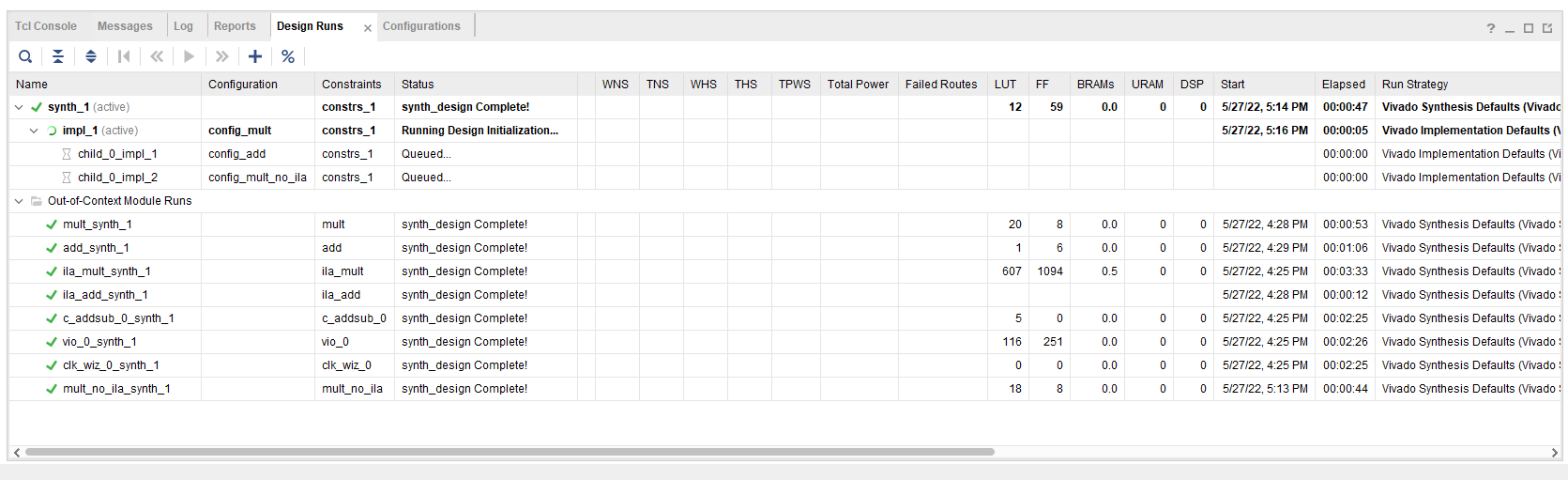
1. Launch the synthesis, implementation, and bitstream generation again.

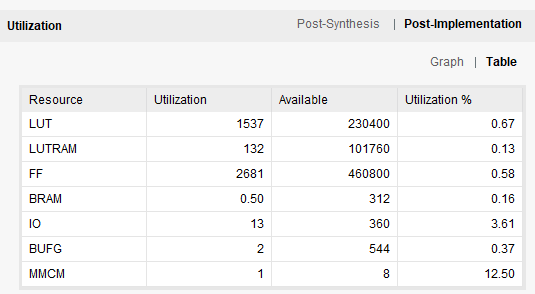


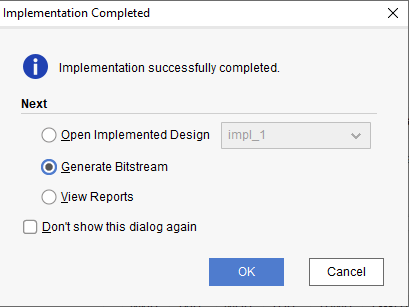


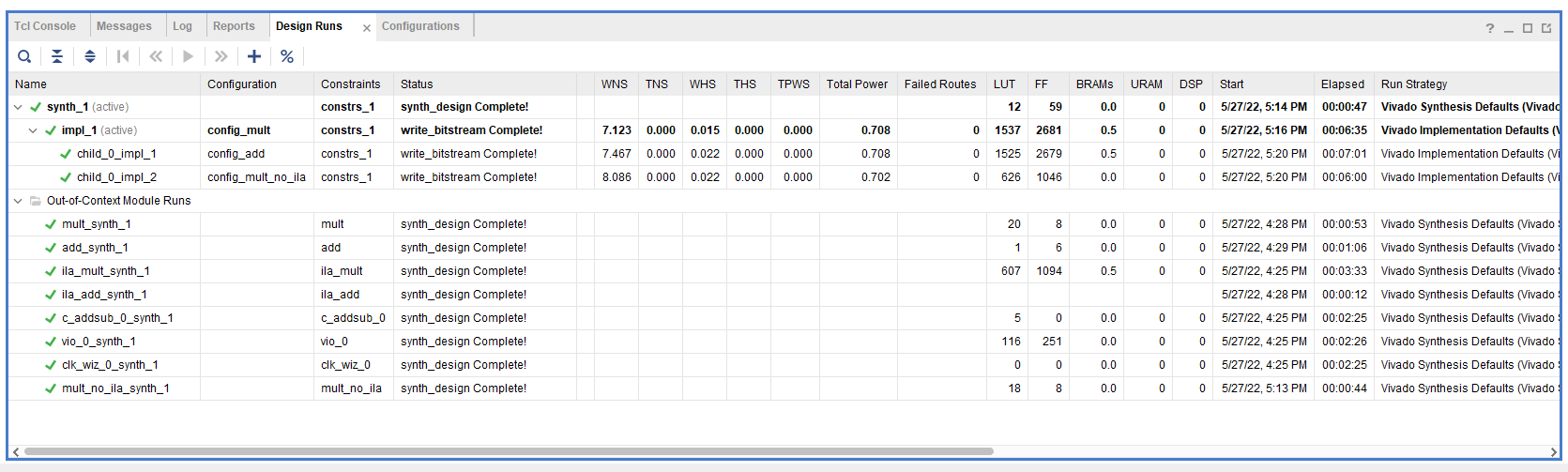


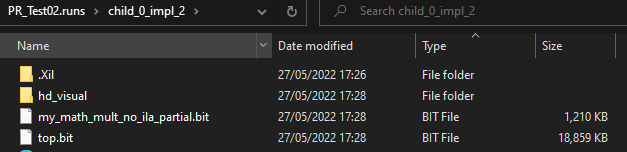












1. Onboard test