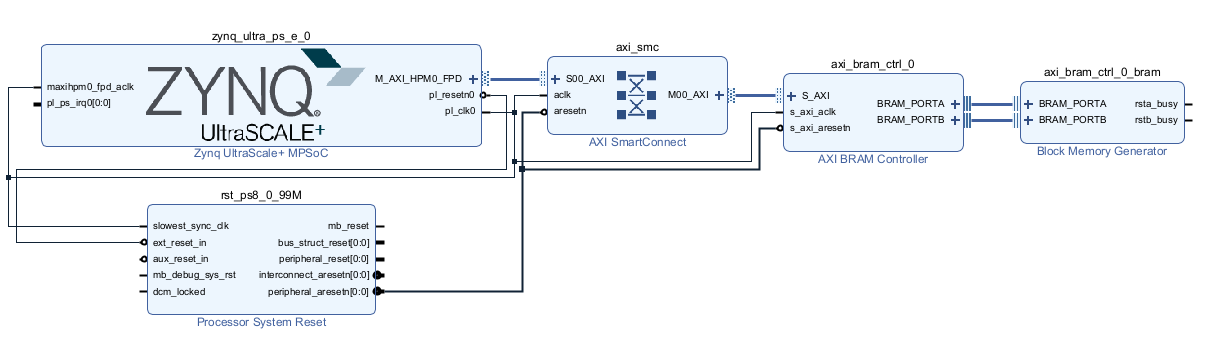
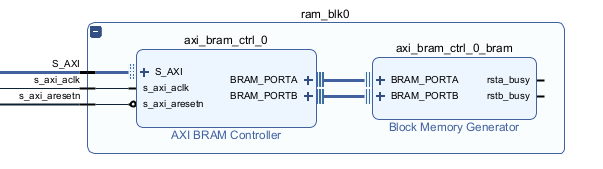
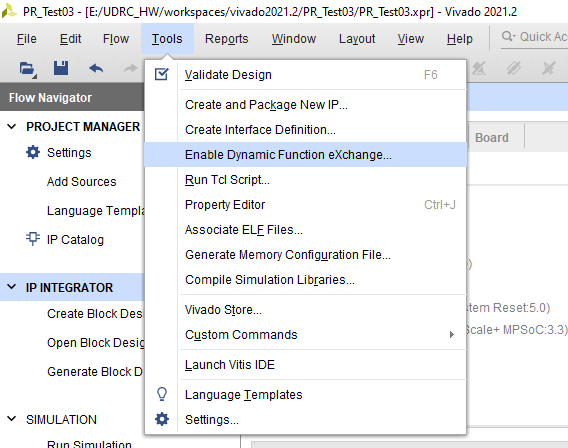
1. Create a simple BRAM controller project



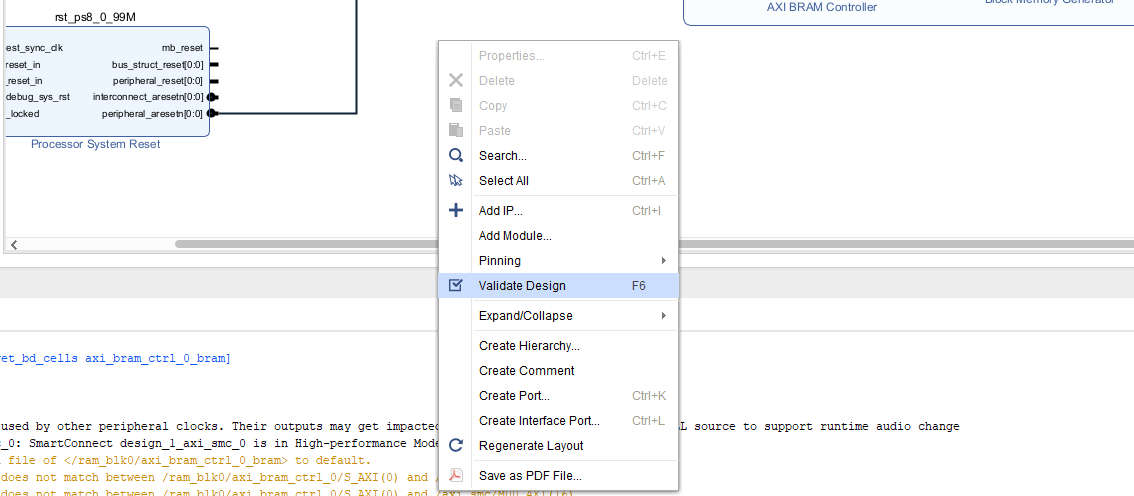
1. Group the BRAM controller and the BRAM generator



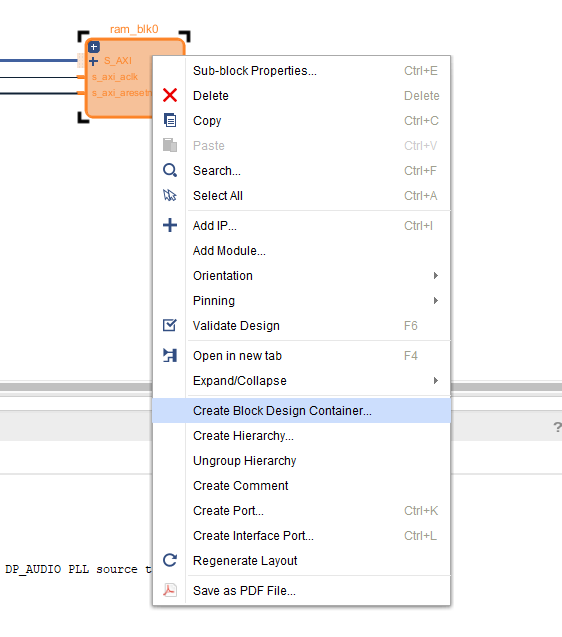
1. Enable dynamic function exchange option of project

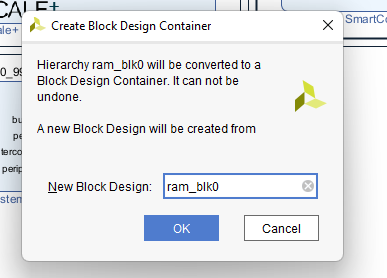


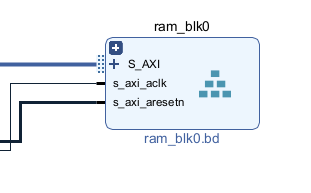
1. Validate the design



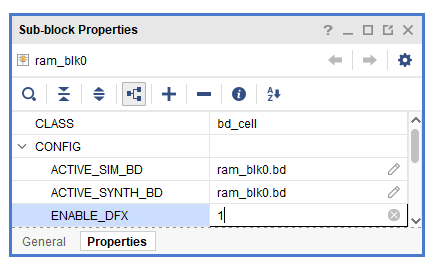
1. Create a block design container

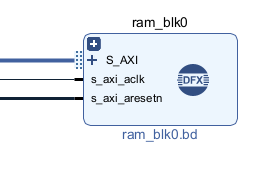




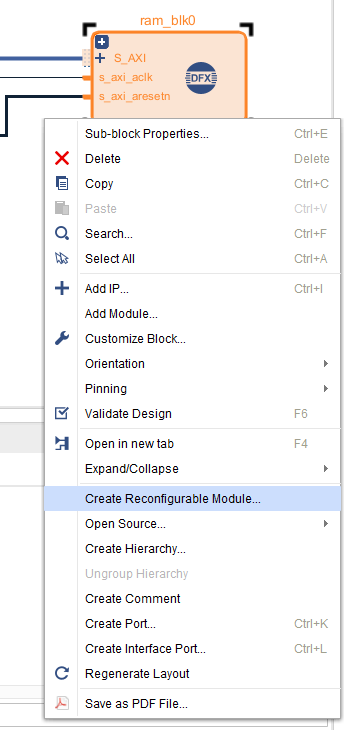


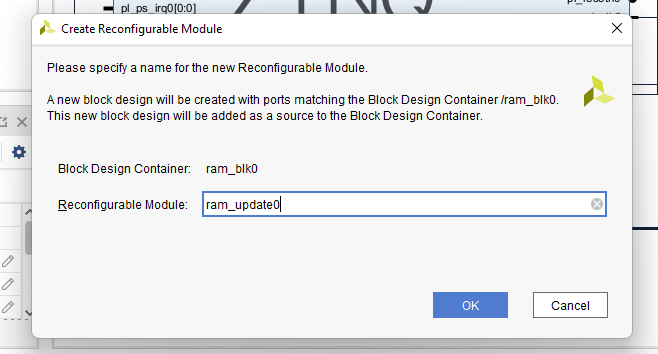
1. Set DFX enable option to be ‘1’

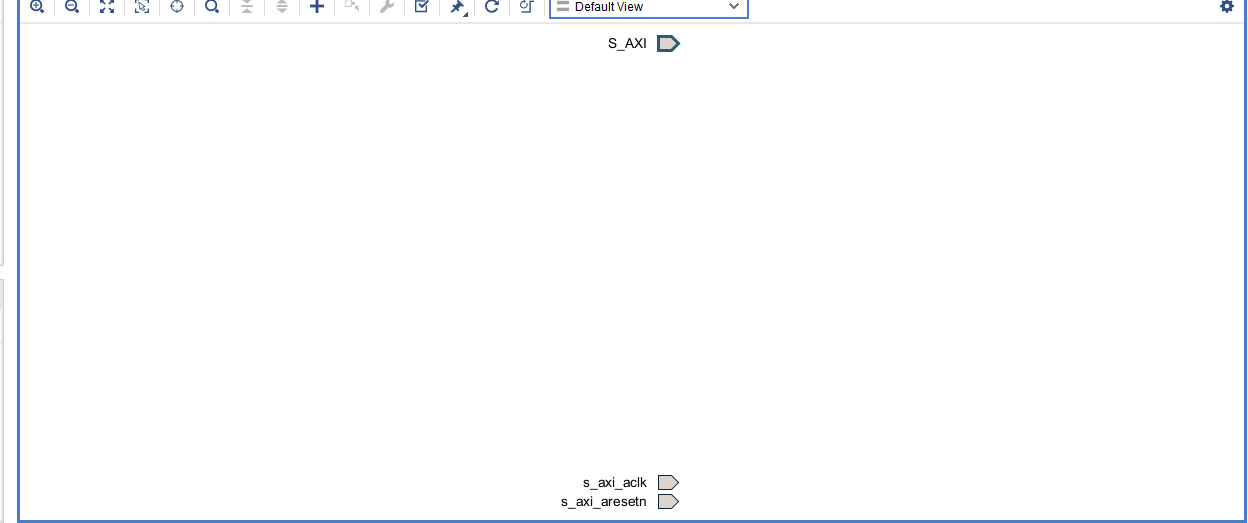


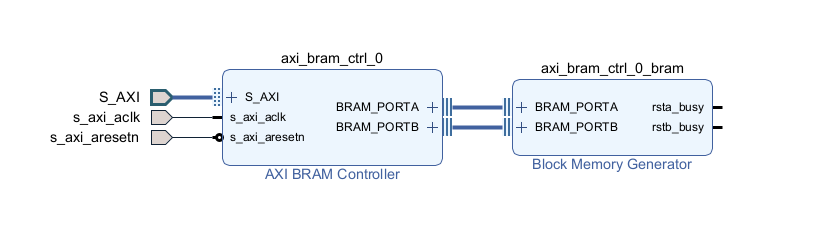


1. Validate the design
2. Create reconfigurable module

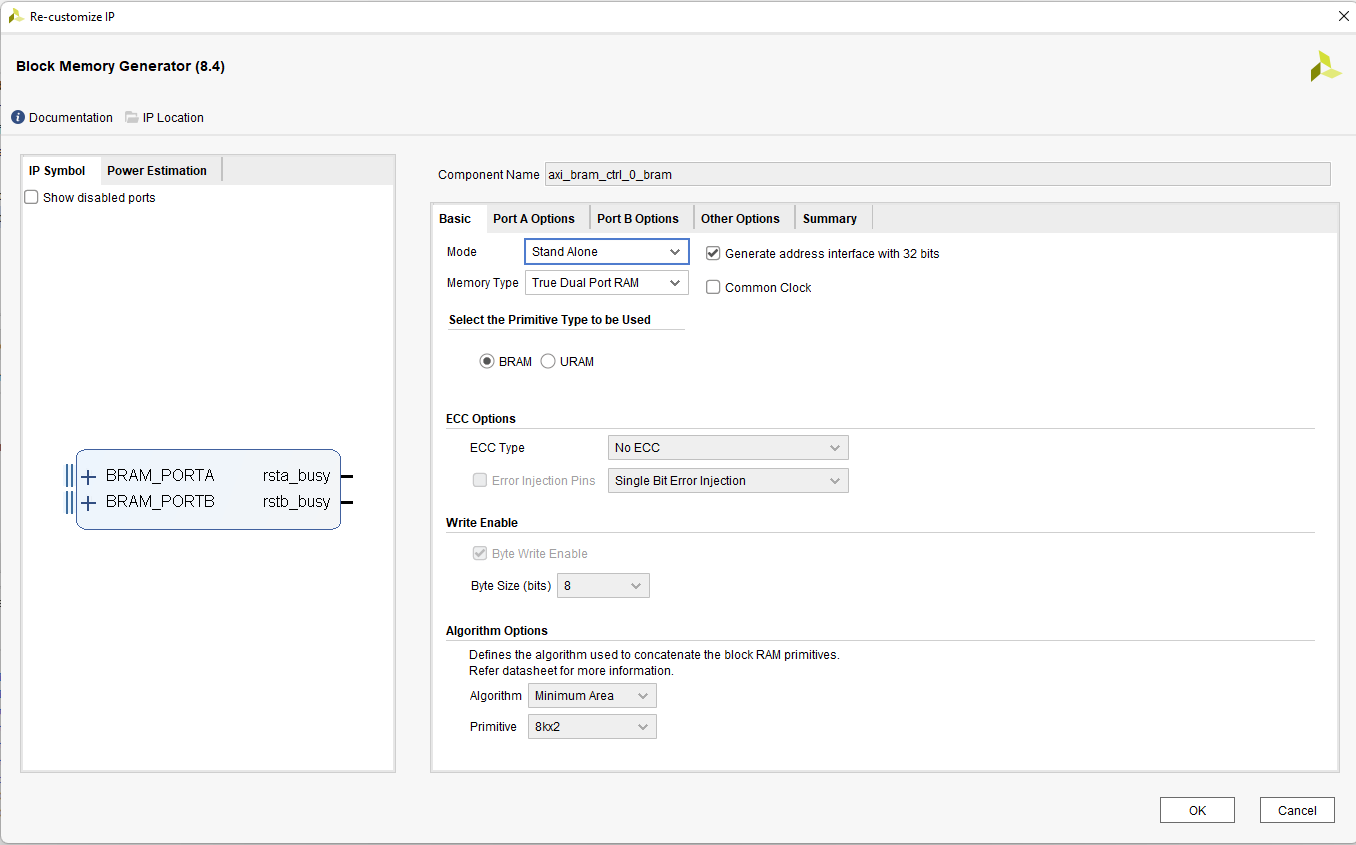


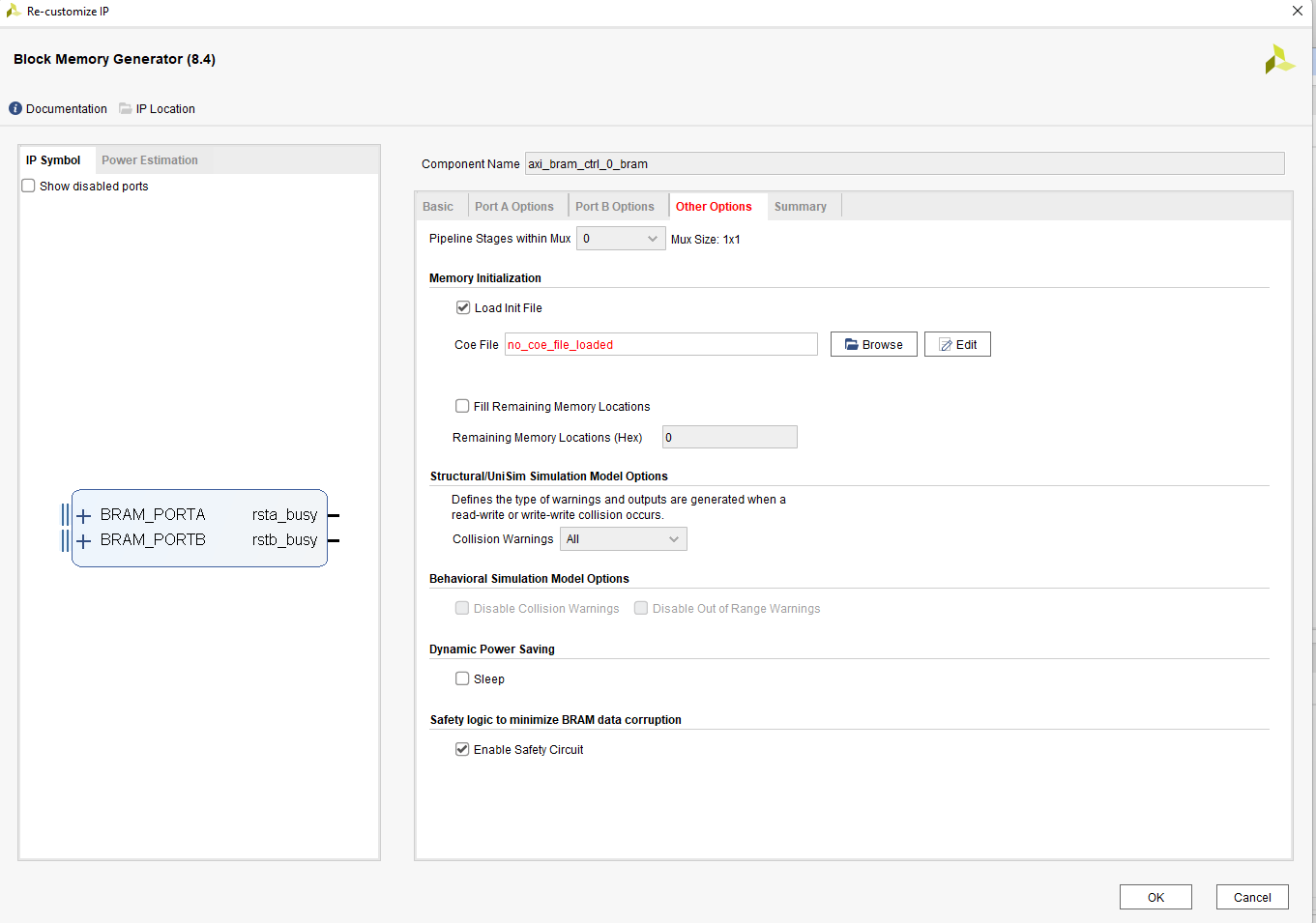


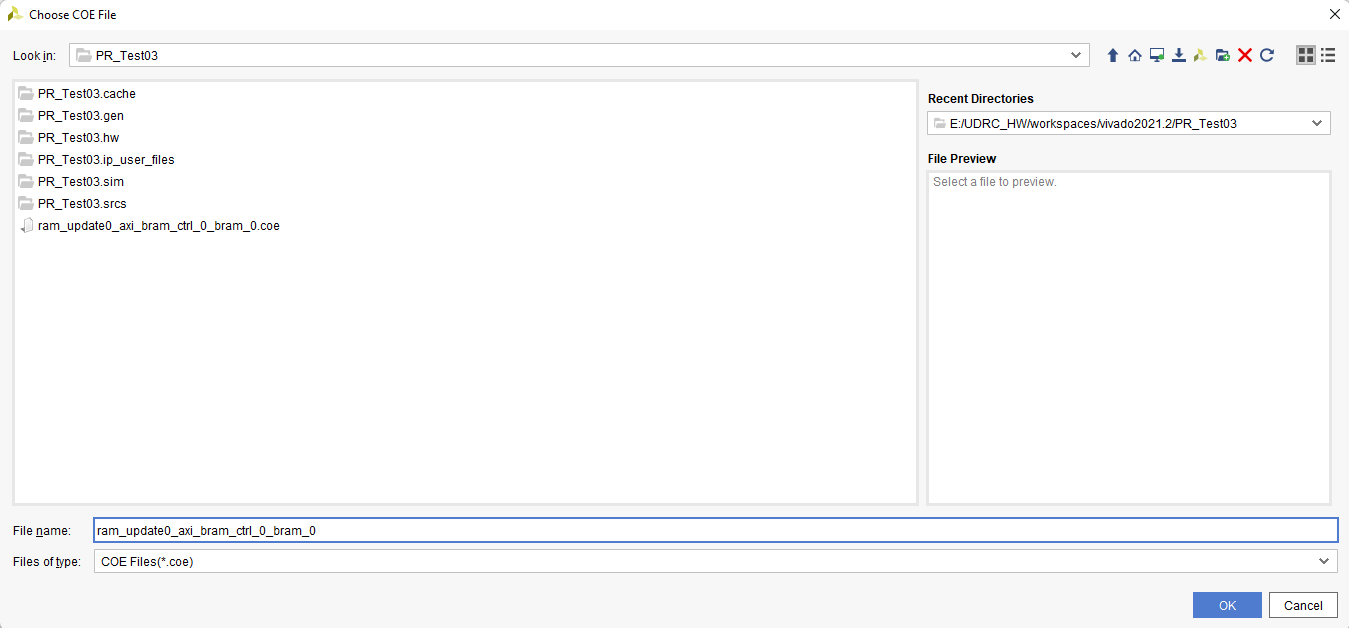


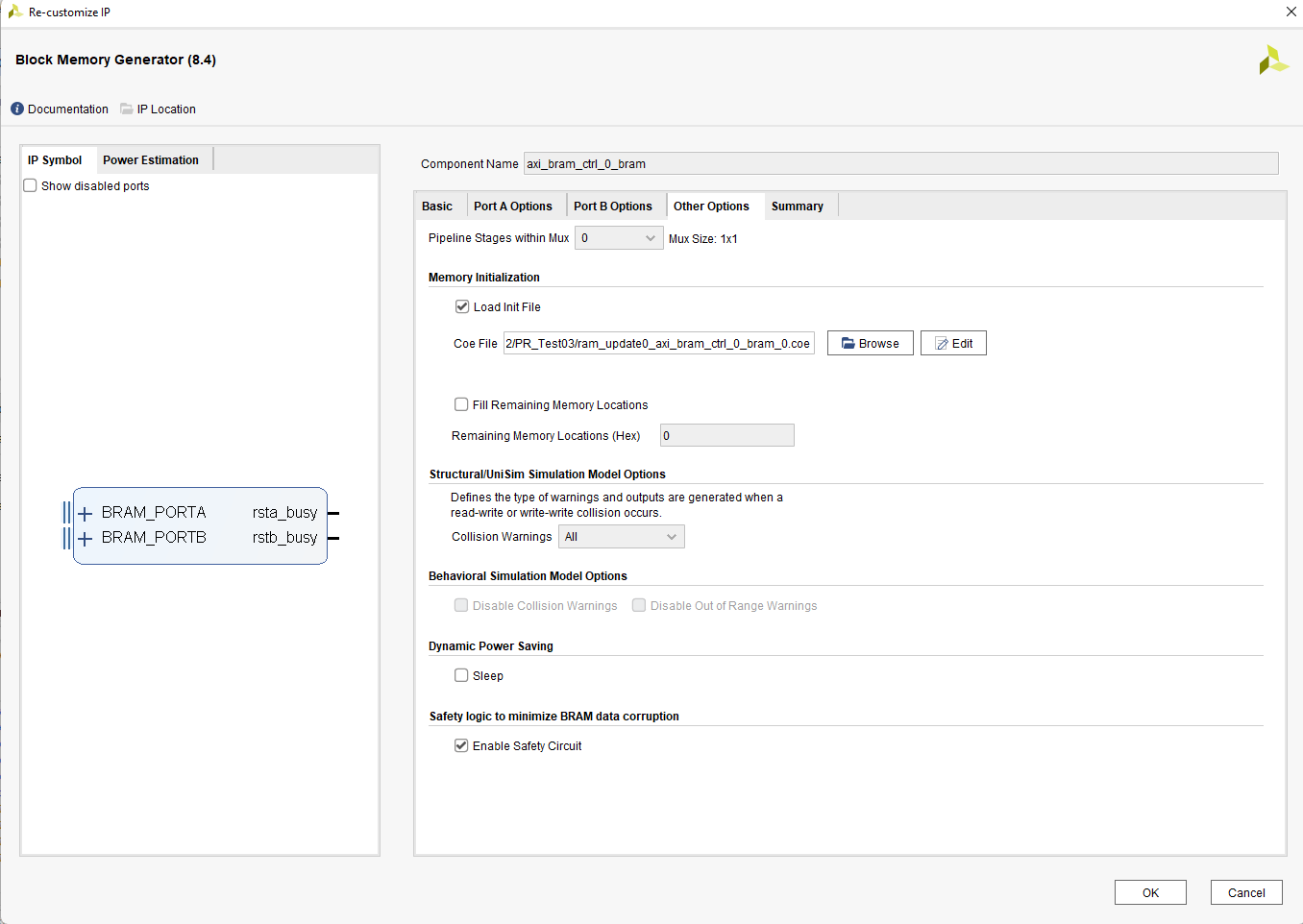


1. Add initial data to the BRAM module

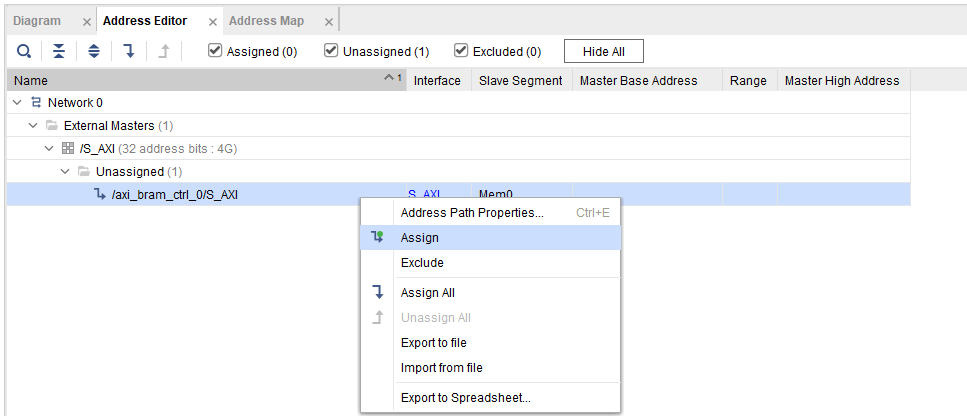


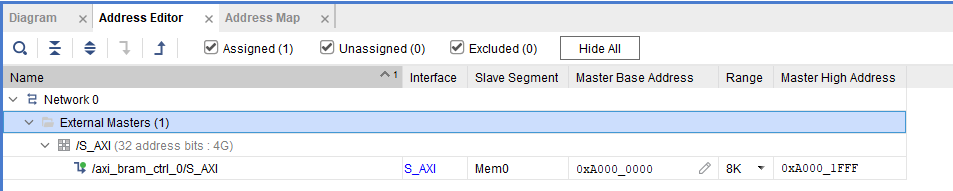




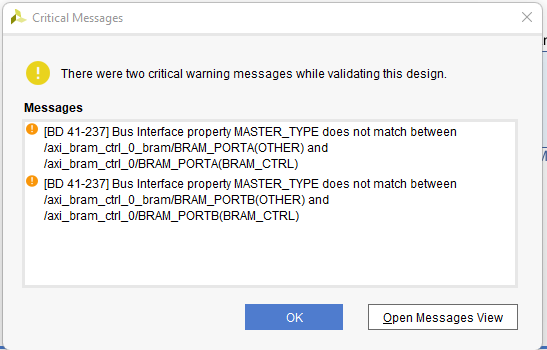


1. Assign address to the reconfigurable BRAM, use the same address offset as previous module

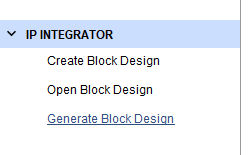


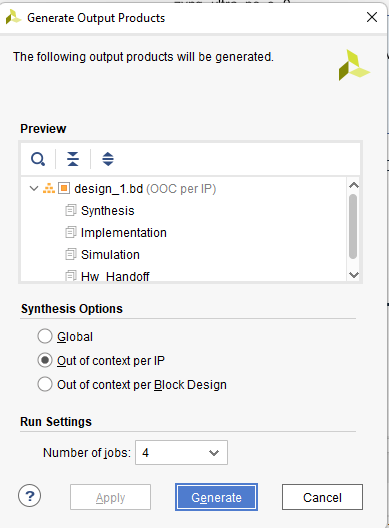


1. Validate the design and ignore the critical warning

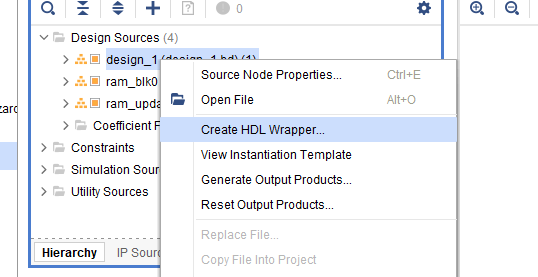


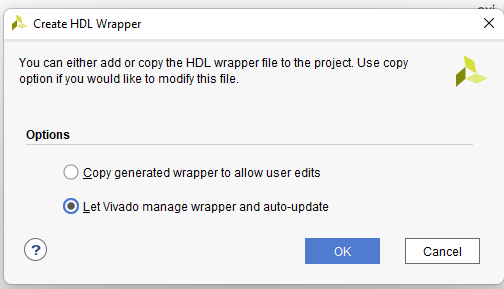
1. Generate block design



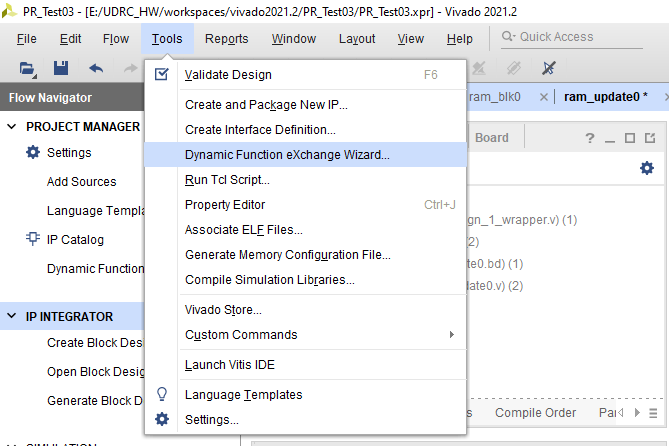


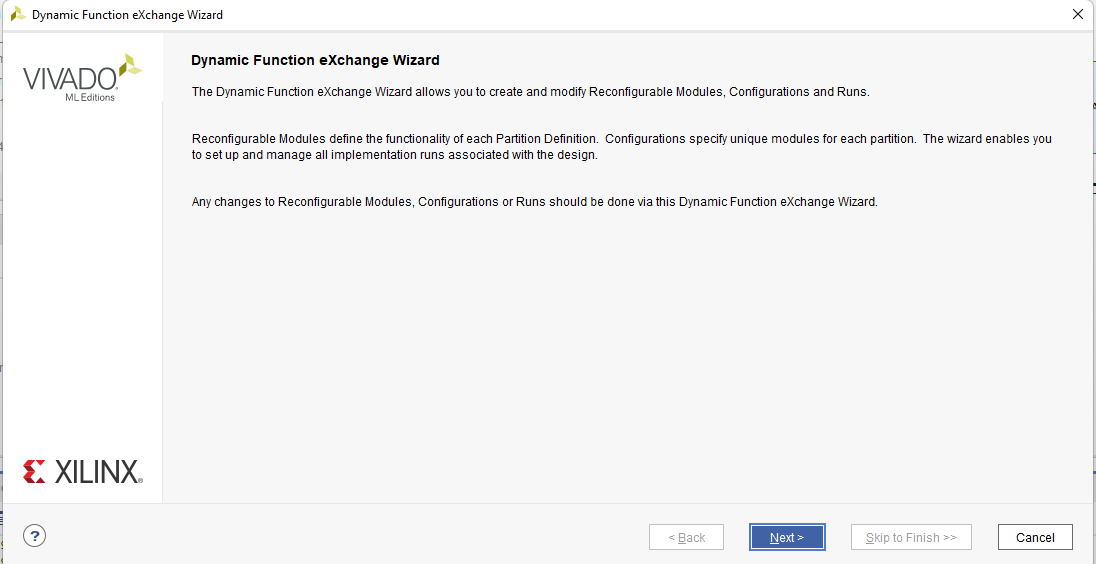
1. Create wrapper for the top design file

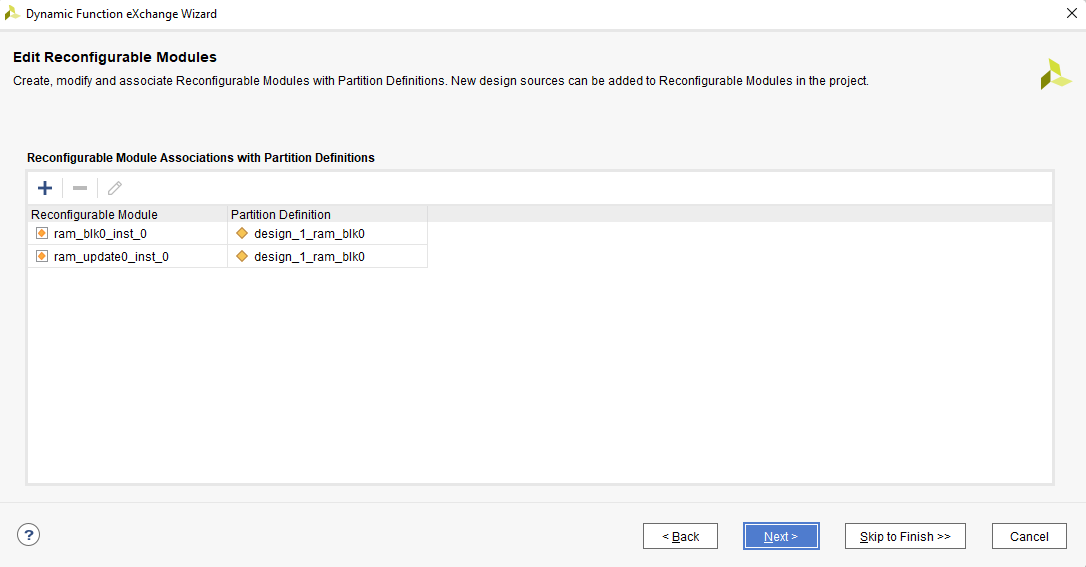


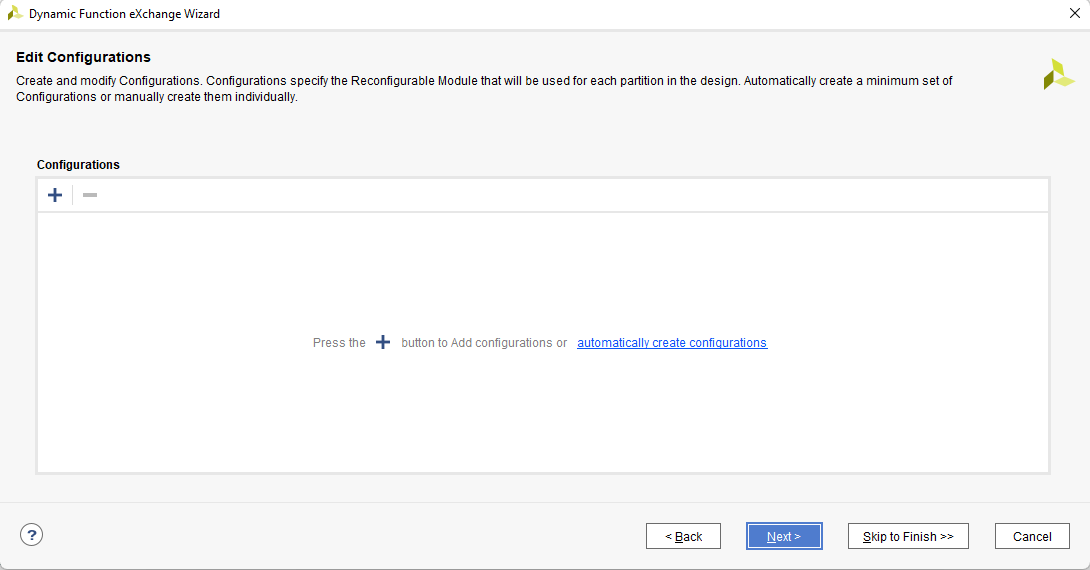


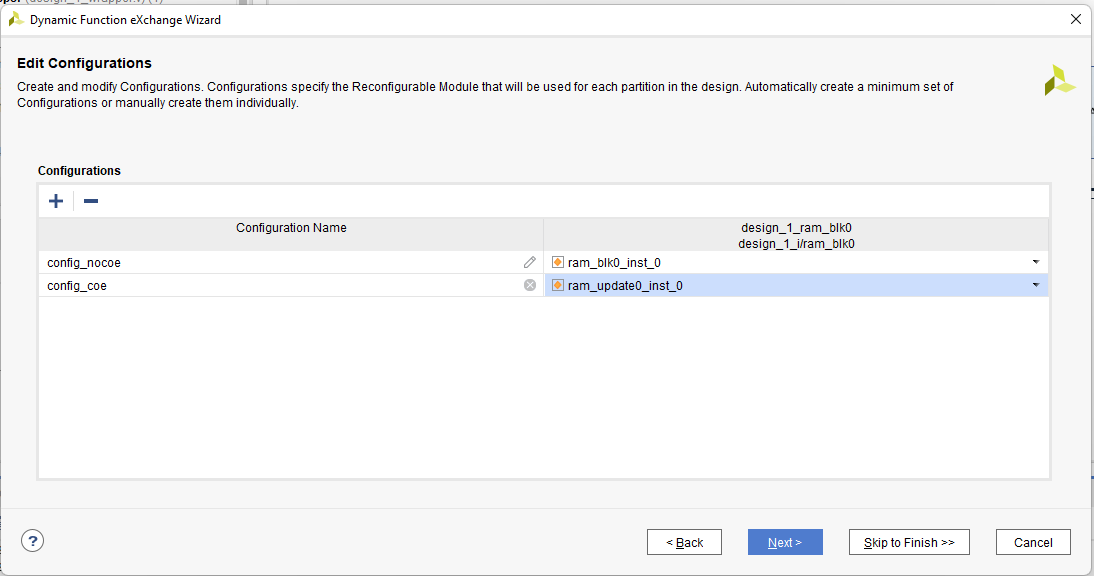
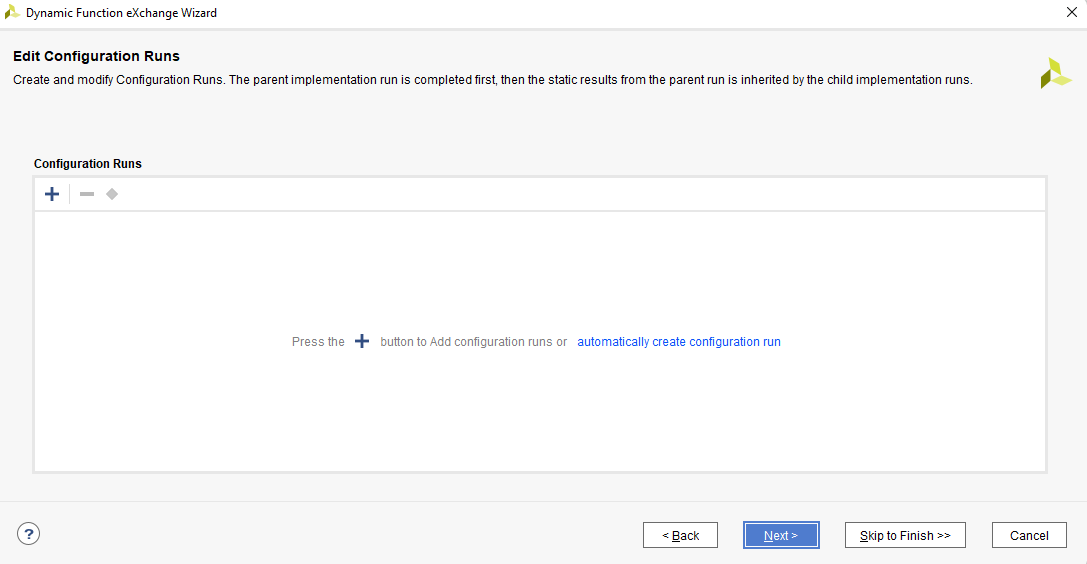
1. Use the Dynamic function exchange wizard

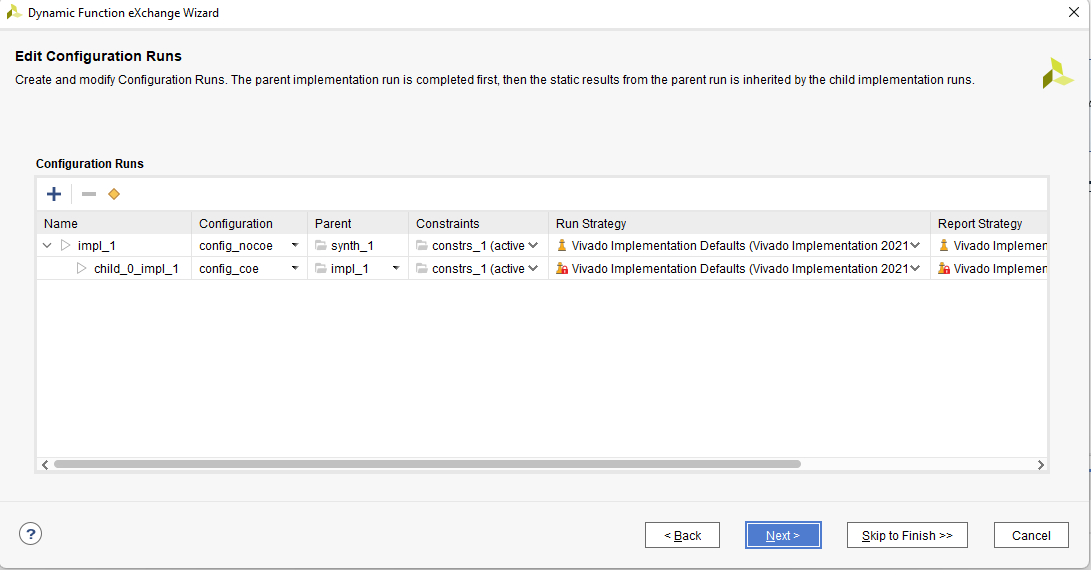


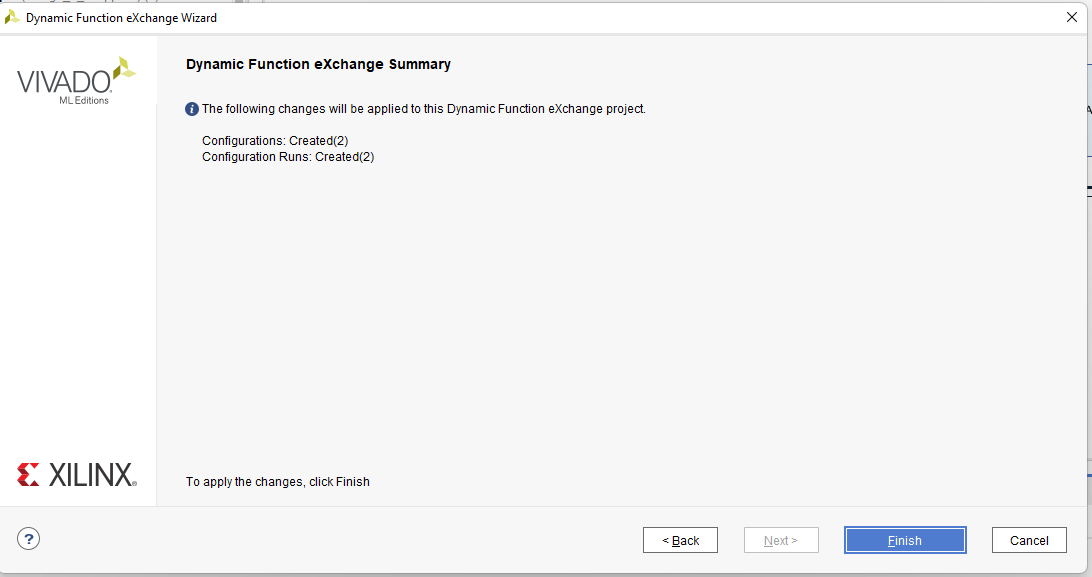




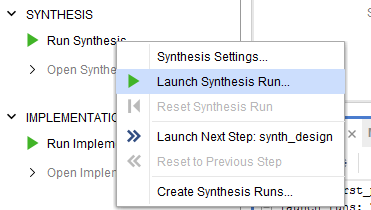


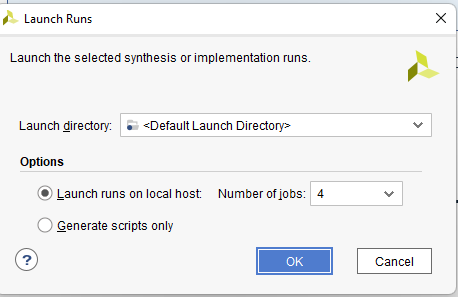
.



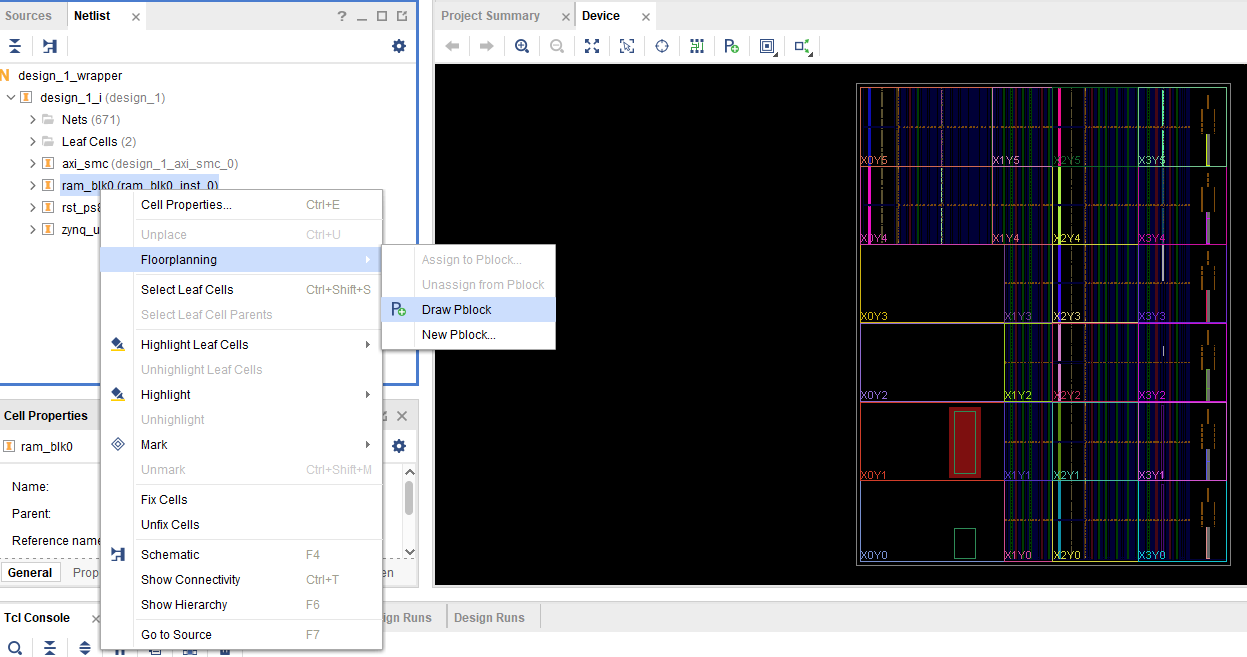


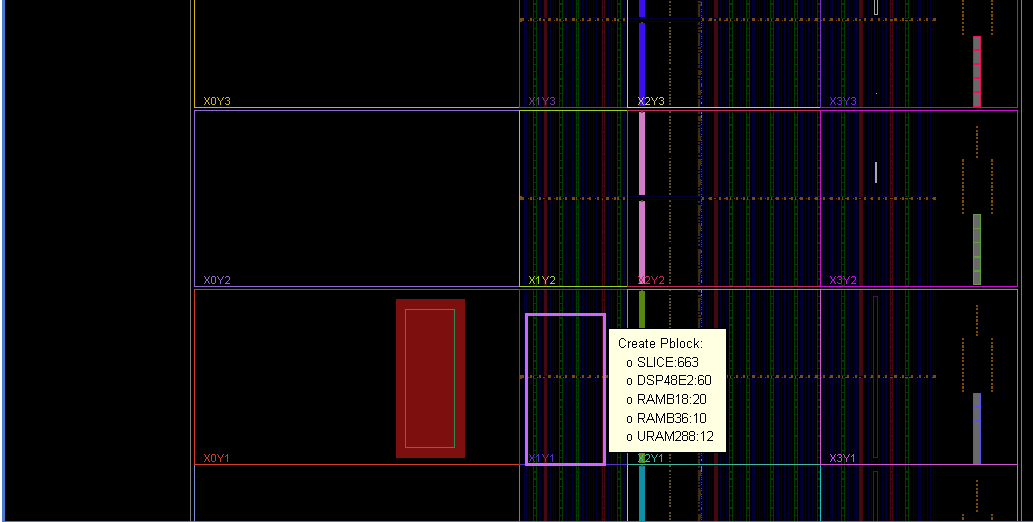
1. Synthesis the design

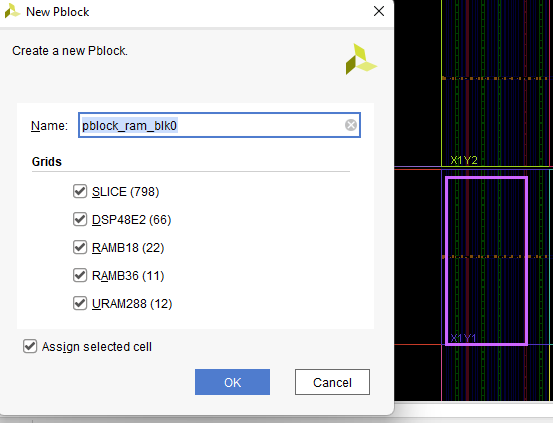


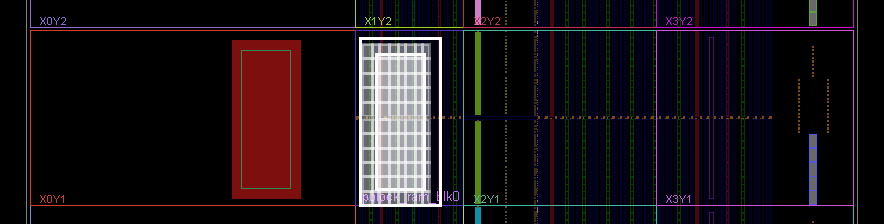


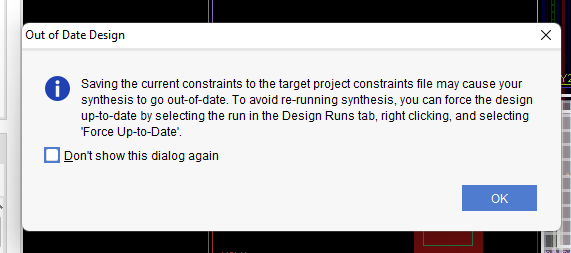
1. Open synthesized design and create floor-planning physical block

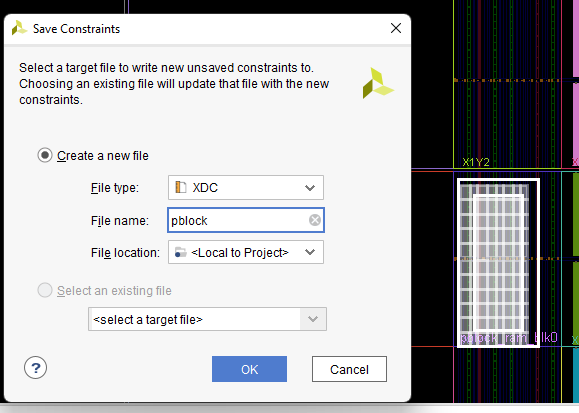


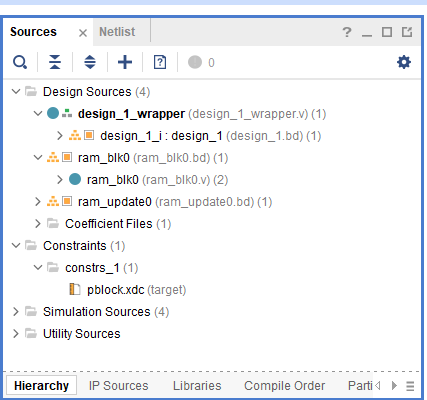




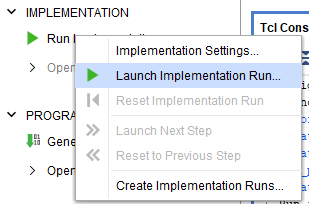


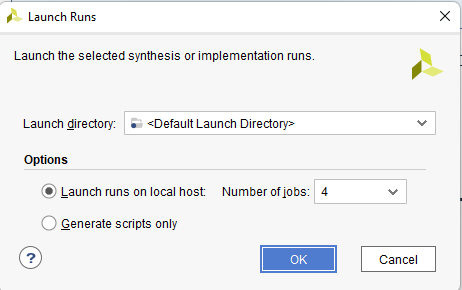




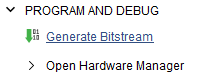


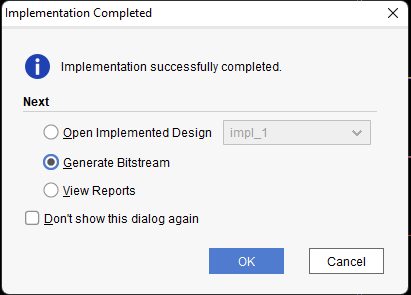
1. Implement the design





1. Generate bit files





1. Check the bit files

