

## 1.1 Introduction of K210 chip

### 1. What is K210 chip?

1. K210 is an MCU based on the RISC-V (Reduced Instruction Set Computing). It's biggest feature is that the chip architecture includes a self-developed neural network hardware accelerator KPU, which can perform convolutional neural network operations with high-performance.

According to Canaan official website, the KPU computing power of the K210 can up to 0.8TFLOPS.

(The computing power of latest Raspberry Pi 4B less than 0.1TFLOPS)

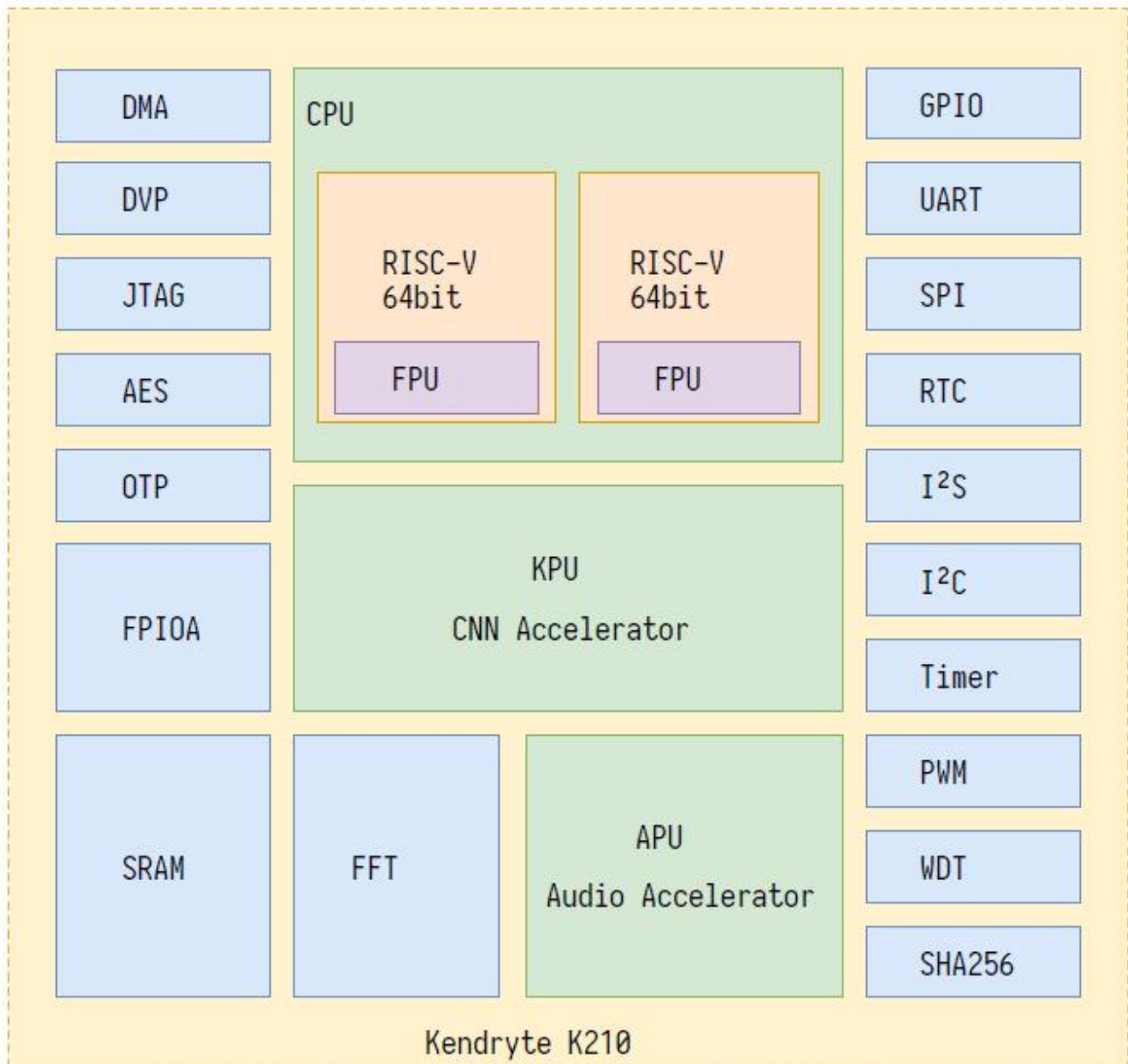
(The computing power of Jetson NANO about 0.47TFLOPS.

2. In addition to the excellent computing power of KPU, the K210 chip possess following features.

- Dual-core CPU, 64-bit instruction set , each core built-in independent FPU, can perform floating-point operations independently.
- Come with computing convolutional artificial neural network accelerator KPU and an APU for processing microphone arrays, which can perform machine vision and auditory processing with high performance
- Built-in FFT(Fast Fourier Transformation )accelerator, which can perform complex FFT calculations.
- Built-in AES and SHA256 algorithm accelerator , it can effectively protect the user's data security.
- MCU: K210 chip with a wealth of peripheral units, such as, DVP, JTAG, OTP, FPIOA, GPIO, UART, SPI, RTC, I2S, I2C, WDT, TIMER, PWM.
- K210 also has high-performance, low-power SRAM, a total of 8M, 2M is dedicated to AI calculation, 6M is used for programs. Dedicated external FLASH interface to increase its own storage space. DMA be used for data transmission.

3. The following is the K210 chip architecture diagram, as shown below. More detail please refer to Data sheet.

For specific reference information, please refer to the technical manual of the K210 chip.



## **2. What is the RISC-V instruction set?**

RISC-V is an open source instruction set architecture (ISA) based on the reduced instruction set (RISC) principle. V represents the fifth-generation reduced instruction set.

RISC-V possess the following characteristics:

- 1) Fully open source: Any company can freely use the RISC-V instruction set to manufacture and market its own chips.
- 2) Simple architecture: Compared with the X86 and ARM architectures. RISC-V is a brand-new instruction set that does not need to be compatible with old products. The entire RISC-V basic instruction set and other modular extension instructions less more than 40.
- 3) Easy to transplant: RISC-V provides privileged-level instructions and user-level instructions. It also provide RISC-V privilege-level instruction specifications and information of RISC-V user-level instruction specifications in detailed. So that developers can easily transplant Linux and unix systems to RISC-V platform.
- 4) Modular design: The RISC-V architecture can be composed of different modules with different functions, and the combination of modules can be flexibly used to customize the MCU that belongs to your own needs.
- 5) Complete tool chain.