

- All resistors rated 1% tolerance or better unless noted otherwise
- All capacitors rated 10V or higher unless noted otherwise

VGA 5V

MPZ20125102AT000

VESA DDC/CI standard recommends pull-up resistors on I2C signals at the host side so they are assumed to be optional here

U2 M24C02-FMN

C2 100n

C3 4.7u

R4 536

D3 LG R971-KN-1-0-20-R18 green

7-bit I2C address: 0x50 (8-bit write=0x80/read=0x81)

J1 L717HDE15PD4CH4R

SCL

VSYNC

HSYNC

SDA

R

G

B

U1A SN74HCS86DR

U1B SN74HCS86DR

R1 1.37k

R2 536

R3 75

C1 330p

D2 ESDA5WY

J2 HD15-25

R

G

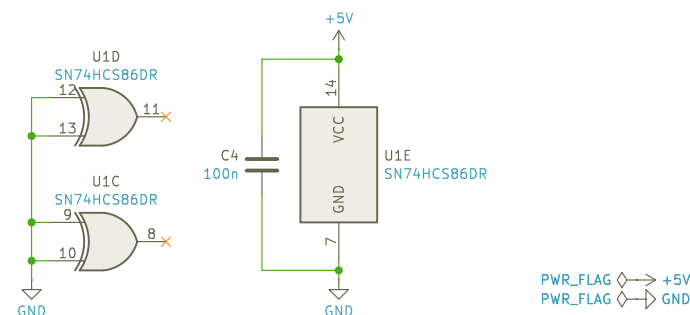
B

CSYNC

composite sync output @ 300mV pk-pk terminated into 75Ω load at remote end

simulation link

{R G B}



Source location: <https://github.com/windsorschmidt/vga-csync-xnor>

| | |
|--|-------------------|
| Sheet: / File: vga-csync-xnor.kicad_sch | |
| Title: VGA H/V to Composite Sync Generator (XNOR) | |
| Size: B | Date: 2025-08-03 |
| KiCad E.D.A. 9.0.3 | Rev: 1 Id: 1/1 |