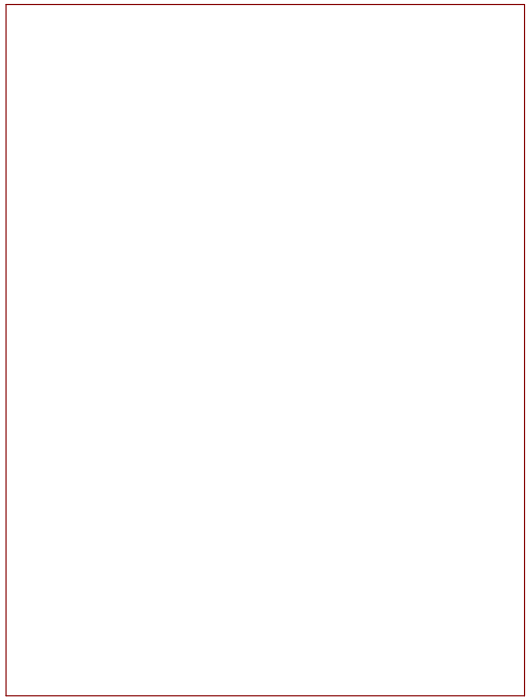
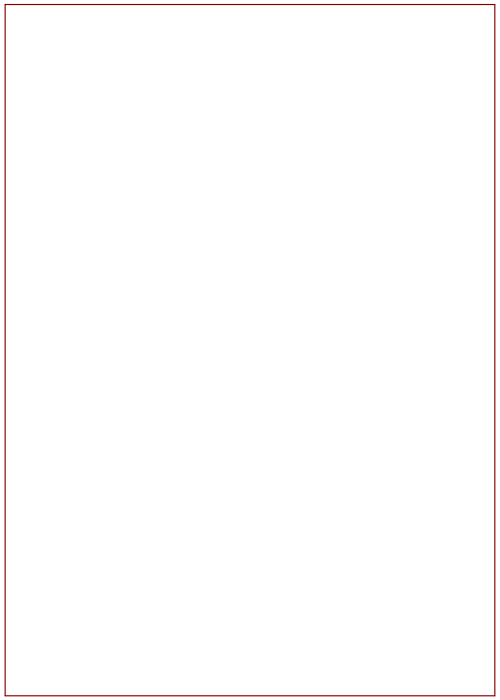
MCU sheet



File: mcu_sheet.kicad_sch

Batt

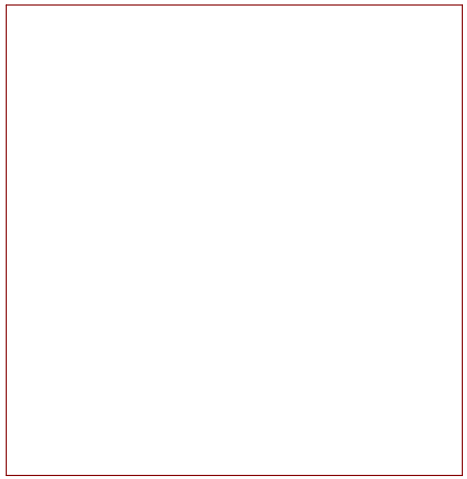


File: batt.kicad_sch

power

File: power.kicad_sch

Sensor Sheet



File: sensors.kicad_sch

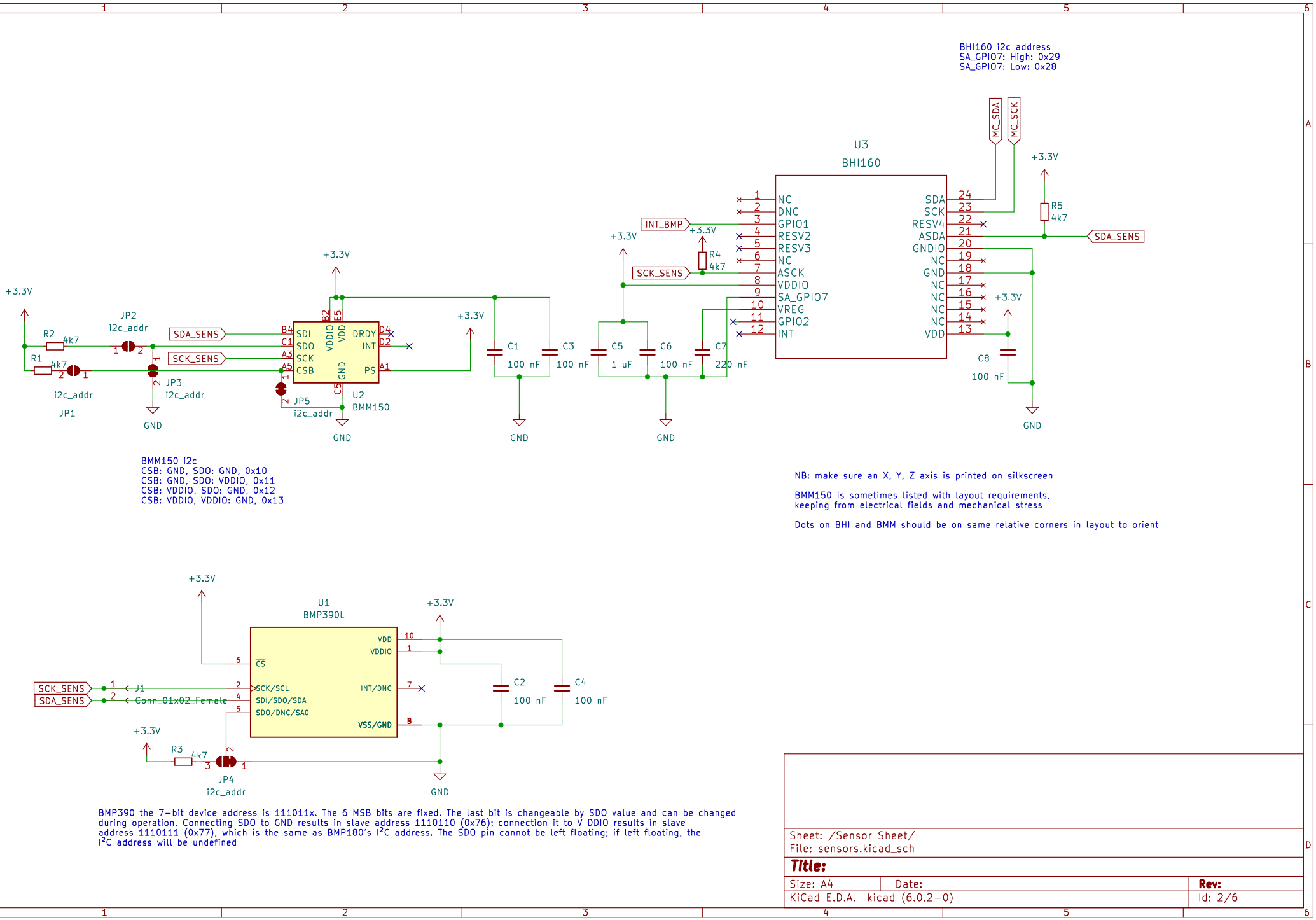
drivers

File: drivers.kicad_sch

Sheet: /
File: Catlin RP2040 Sensing Controller.kicad_sch

**Title:**

| Size: A4 | Date: | **Rev:** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.2-0) | | Id: 1/6 |


BHI160 i2c address
SA_GPIO7: High: 0x29
SA_GPIO7: Low: 0x28
U3
BHI160
MC_SDA
MC_SCK
+3.3V
R5
4k7
SDA_SENS
INT_BMP
SCK_SENS
R4
4k7
NC
DNC
GPIO1
RESV2
RESV3
NC
ASCK
VDDIO
SA_GPIO7
VREG
GPIO2
INT
SDA
SCK
RESV4
ASDA
GNDIO
NC
GND
NC
NC
NC
NC
VDD
C1
100 nF
C3
100 nF
C5
1 uF
C6
100 nF
C7
220 nF
C8
100 nF
GND
JP2
i2c_addr
R2
4k7
R1
4k7
JP1
i2c_addr
JP3
i2c_addr
SDA_SENS
SCK_SENS
SDI
SDO
SCK
CSB
VDDIO
VDD
GND
DRDY
INT
PS
U2
BMM150
JP5
i2c_addr
BMM150 i2c
CSB: GND, SDO: GND, 0x10
CSB: GND, SDO: VDDIO, 0x11
CSB: VDDIO, SDO: GND, 0x12
CSB: VDDIO, VDDIO: GND, 0x13
NB: make sure an X, Y, Z axis is printed on silkscreen
BMM150 is sometimes listed with layout requirements,
keeping from electrical fields and mechanical stress
Dots on BHI and BMM should be on same relative corners in layout to orient
U1
BMP390L
VDD
VDDIO
CS
SCK/SCL
SDI/SDO/SDA
SDO/DNC/SAO
INT/DNC
VSS/GND
SCK_SENS
SDA_SENS
J1
Conn_01x02_Female
C2
100 nF
C4
100 nF
R3
4k7
JP4
i2c_addr
BMP390 the 7-bit device address is 111011x. The 6 MSB bits are fixed. The last bit is changeable by SDO value and can be changed during operation. Connecting SDO to GND results in slave address 1110110 (0x76); connection it to V DDIO results in slave address 1110111 (0x77), which is the same as BMP180's I²C address. The SDO pin cannot be left floating; if left floating, the I²C address will be undefined
Sheet: /Sensor Sheet/
File: sensors.kicad_sch
Title:
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Date:
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KiCad E.D.A. kicad (6.0.2-0)
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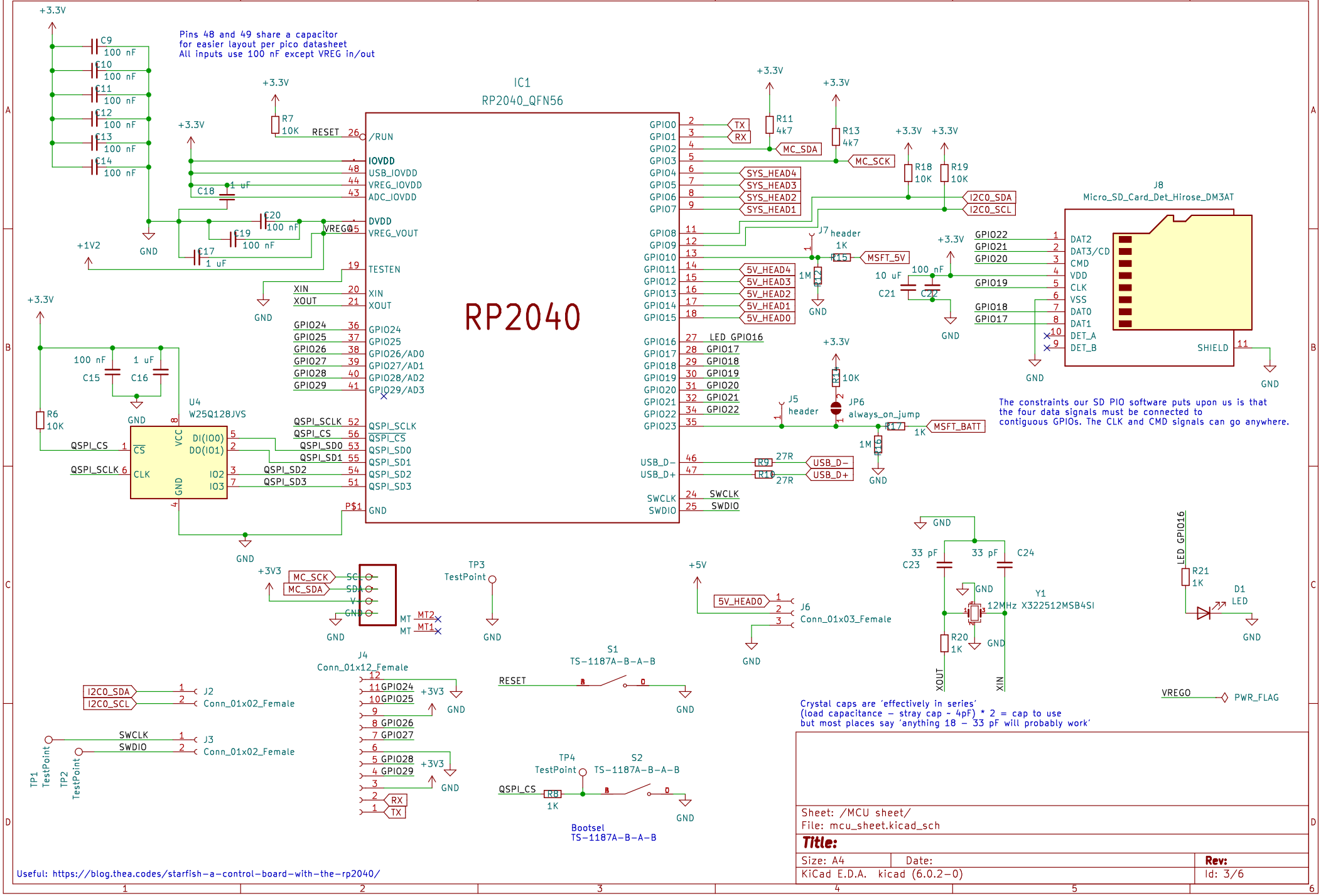
Pins 48 and 49 share a capacitor
for easier layout per pico datasheet
All inputs use 100 nF except VREG in/out
IC1
RP2040_QFN56
RP2040
The constraints our SD PIO software puts upon us is that
the four data signals must be connected to
contiguous GPIOs. The CLK and CMD signals can go anywhere.
Crystal caps are 'effectively in series'
(load capacitance − stray cap ~ 4pF) * 2 = cap to use
but most places say 'anything 18 − 33 pF will probably work'
Bootsel
TS-1187A-B-A-B
Useful: https://blog.thea.codes/starfish-a-control-board-with-the-rp2040/
Sheet: /MCU sheet/
File: mcu_sheet.kicad_sch
Title:
Size: A4
Date:
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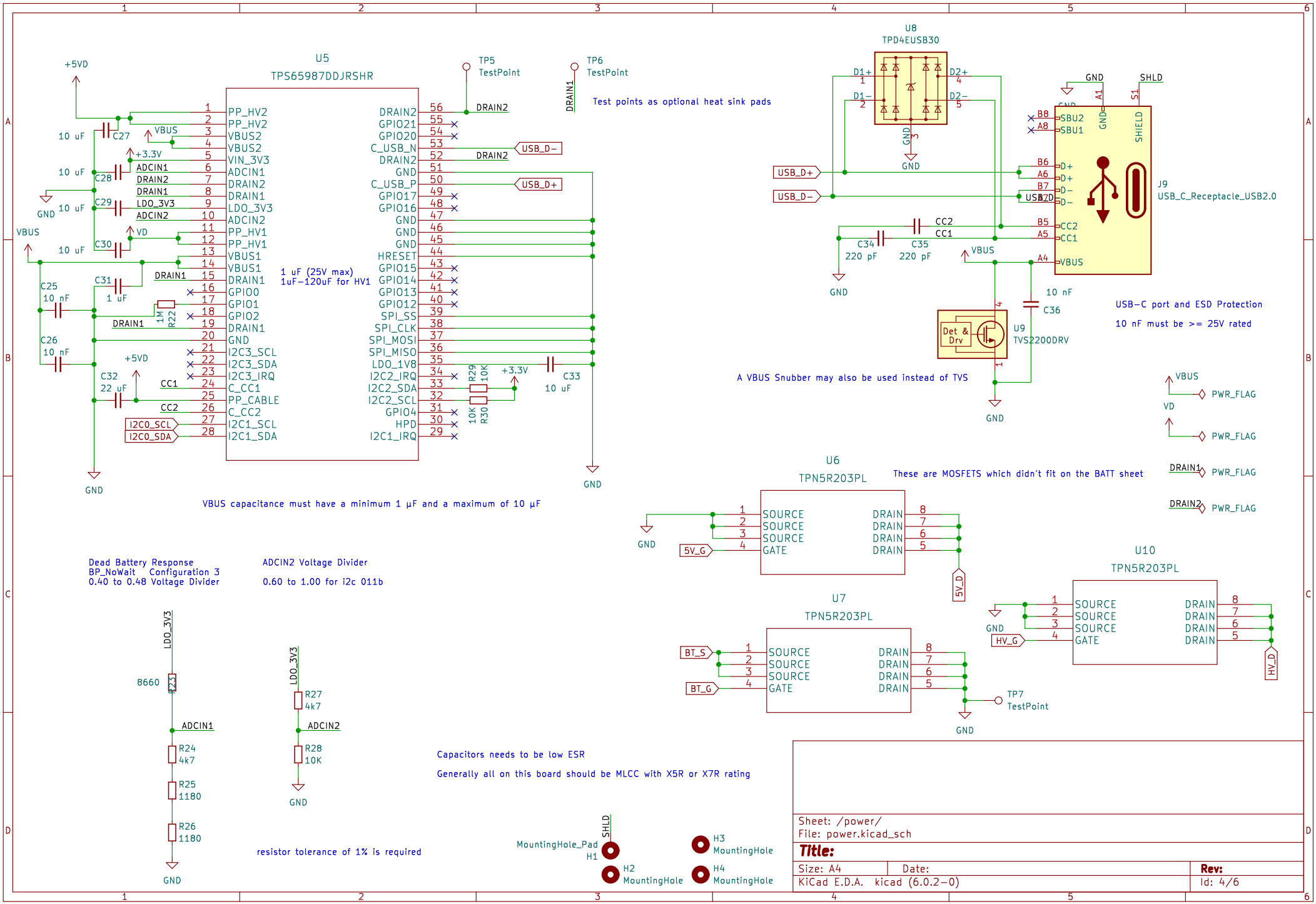
KiCad E.D.A. kicad (6.0.2-0)
Id: 3/6


U5
TPS65987DDJRSHR
+5VD
10 uF
C27
VBUS
+3.3V
ADCIN1
C28
DRAIN2
DRAIN1
LDO_3V3
C29
ADCIN2
VD
C30
C31
1 uF
C25
10 nF
C26
10 nF
C32
22 uF
CC1
CC2
I2C0_SCL
I2C0_SDA
R22
1M
PP_HV2
VBUS2
VIN_3V3
ADCIN1
DRAIN2
DRAIN1
LDO_3V3
ADCIN2
PP_HV1
VBUS1
DRAIN1
GPIO0
GPIO1
GPIO2
DRAIN1
GND
I2C3_SCL
I2C3_SDA
I2C3_IRQ
C_CC1
PP_CABLE
C_CC2
I2C1_SCL
I2C1_SDA
1 uF (25V max)
1uF-120uF for HV1
DRAIN2
GPIO21
GPIO20
C_USB_N
DRAIN2
GND
C_USB_P
GPIO17
GPIO16
GND
GND
GND
HRESET
GPIO15
GPIO14
GPIO13
GPIO12
SPI_SS
SPI_CLK
SPI_MOSI
SPI_MISO
LDO_1V8
I2C2_IRQ
I2C2_SDA
I2C2_SCL
GPIO4
HPD
I2C1_IRQ
R29 10K
R30 10K
+3.3V
C33
10 uF
TP5
TestPoint
DRAIN2
TP6
TestPoint
DRAIN1
Test points as optional heat sink pads
USB_D-
USB_D+
GND
VBUS capacitance must have a minimum 1 µF and a maximum of 10 µF
U8
TPD4EUSB30
D1+
D1-
D2+
D2-
GND
USB_D+
USB_D-
CC2
CC1
C34
220 pF
C35
220 pF
VBUS
10 nF
C36
U9
TVS2200DRV
Det & Drv
A VBUS Snubber may also be used instead of TVS
J9
USB_C_Receptacle_USB2.0
SHLD
SBU2
SBU1
D+
D-
CC2
CC1
VBUS
USB-C port and ESD Protection
10 nF must be >= 25V rated
U6
TPN5R203PL
These are MOSFETS which didn't fit on the BATT sheet
SOURCE
GATE
DRAIN
5V_G
5V_D
U7
TPN5R203PL
BT_S
BT_G
TP7
TestPoint
U10
TPN5R203PL
HV_G
HV_D
VBUS
VD
DRAIN1
DRAIN2
PWR_FLAG
Dead Battery Response
BP_NoWait Configuration 3
0.40 to 0.48 Voltage Divider
ADCIN2 Voltage Divider
0.60 to 1.00 for i2c 011b
LDO_3V3
8660
R23
ADCIN1
R24
4k7
R25
1180
R26
1180
R27
4k7
ADCIN2
R28
10K
resistor tolerance of 1% is required
Capacitors needs to be low ESR
Generally all on this board should be MLCC with X5R or X7R rating
MountingHole_Pad
SHLD
H1
H2
MountingHole
H3
MountingHole
H4
MountingHole
Sheet: /power/
File: power.kicad_sch
Title:
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The slave address of the IC is 0xD2h/0xD3h
The least significant bit is
the read/write indicator (1 for read, 0 for write)

Vsys is guaranteed 4V – 14V
Vsys should be between Vsysmin (8.4V programmable)
to Vbattreg (12V, programmable)
Max Current 10A

lower the inductor DCR (DC resistance) is, the higher the buck-boost efficiency is
DR127-3R3-R, SER2915, 7443320330

EVAL has 15nF caps on CSINP and CSINN, 10 nF used here

U11
MAX77961EFV06+

Using defaults for charge settings by tying to PVL
don't need resistors for those
The DNP caps there are actually placeholders for resistors
should those wished to be added to program the IC

LIPO Charging LED
STAT goes high when no charge or no power
Cycles low/high when charging and low when charged

STAT tied to PVL with 200K in datasheet, no LED there

Not using a thermistor.
THM to GND means battery removal cannot be detected,
but allows charging
THM to AVL is equivalent to battery removal detection,
and prevents charging

This switch is here to assure safe removal of battery

Hot Insertion Protection RC, copied from datasheet

DMN3016LFDE in EVAL, N-channel

EVAL has 220K and 470K here
datasheet has 470K and 910K
I used 200K + 200K and 1M as used elsewhere already

3S Lipo Plug, JST

3S ONLY

FETS are Terminals, controlled by switch from MCU

The primary distinction between an N-Channel and a P-Channel MOSFET
is that the N-Channel is usually connected to the Ground (–) side of the load,
while the P-Channel is connected to the VCC (+) side

TVS good for surge suppression
these TVS have some inductive load rev protection (500 mah)
but the Schottky is needed for higher current reverse protection
but Schottky has high leakage current

Extra N-channel is needed to make it
high 3.3V = on, GND = off

Low Amps for those, but sharing high Amps part needed on batt

| | |
|---|---|
| Sheet: /Batt/ | |
| File: batt.kicad_sch | |
| **Title:** | |
| Size: A4 | Date: |
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Useful: https://community.element14.com/products/roadtest/b/blog/posts/mps-mpm54304-evm-roadtest---snippets

"For parallel mode, you are welcome to connect the
SW1 and SW2 pins together or leave them untied.
We suggest floating them in parallel mode to avoid the wrong SMT."

Different Suffix versions of MPM54304 have different default settings
for which VOUT can be parallel (diff startup times otherwise).
Suffix 0002 is expected, 0004 should also work without modification

R0 between the two separate V5 nets should allow for the not-parallel setup
of the 0001 and 0003 suffixes, DNP this part for those

U15

MPM54304GMN-0002

By default, the I2C slave address is 0x68

GPIO default is PG (power good)

EVAL board shows PG to VCC with 100K
I'm using 200K just for simpler BOM

Space for optional large ripple capacitors

1150 for 5.118V
1170 for 5.041V
1180 for 5.003
against 8660
can do 8660 + 27R for slightly higher

4K7 v 1K for 3.42V
8660 v 1910 for 3.32V
(1180 + 470 + 470) v 470 for 3.306V
8660 + 1k + 1k  vs 1180 + 1180  for 3.363
10k vs 1k + 1180 for 3.352
4k7 vs 1k + 27 for 3.346

should work with any 3 same R for 1.8V

Voltage Dividers to set Buck V outs

FB Voltage on must suffixes is 0.6 V
which I assume is the same as Vref

A feed-forward cap on these Vout to FB can be used
Helpful when large current loads are present
33 nF is recommended

U16
TVS2200DRV

EN pin needs to be pulled high to activate (so to VS)
but can't tolerate more than 6V, hence the divider
150k and 49.9k is used in example

Internally EN is pulled low by 2M resistor

This capacitor enables soft start, not required here

| | |
|---|---|
| Sheet: /drivers/ | |
| File: drivers.kicad_sch | |
| **Title:** | |
| Size: A4 | Date: |
| KiCad E.D.A. kicad (6.0.2-0) | **Rev:** Id: 6/6 |