Software Specification

SC2430 Configuration and Control API

Number: SCT-SW0A21vc

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Revision History

Revision	Date	Author	Description
1.0.0	2022-Sept-20	K. Sumlak	Initial Release
1.0.1	2022-Sept-29	K. Sumlak	Updated Section 4 command examples
1.0.2	2022-Oct-03	K. Sumlak	Revised Sections 3.3.1 and 3.3.2. Corrected Table 1.
1.0.3	2023-Jan-18	K. Sumlak	Added default power-on settings to Section 5.

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1. Overview

This document describes the software API and hardware interfaces required to configure and control the SC2430 NR TDD Signal Conditioning Module (SCM).

The SCM is a front-end solution that provides signal conditioning and amplification for Software Define Radio (SDR) systems. It was designed specifically for use in conjunction with the NI Ettus-USRP X410.

1.1 Protocols

Two protocol types are available to configure and control the SC2430:

- Binary Protocols – The Binary Protocols operate over the front panel HDMI connector Interface. These protocols are intended for use with the NI Ettus-USRP X410 or other custom hardware systems. Additionally, the SPI interface offers higher speeds required for time-critical applications. See Section 3 for additional details.
- Console Protocol – The ASCII Protocol operates over the USB-C interface. This protocol is intended as a simple user-friendly interface for interactive control of the hardware. See Section 4 for additional details.

1.2 Hardware

An overview of the hardware system is shown in Figure 1. Section 2 describes the hardware interfaces including the HDMI GPIO, USB-C, and LED indicators.

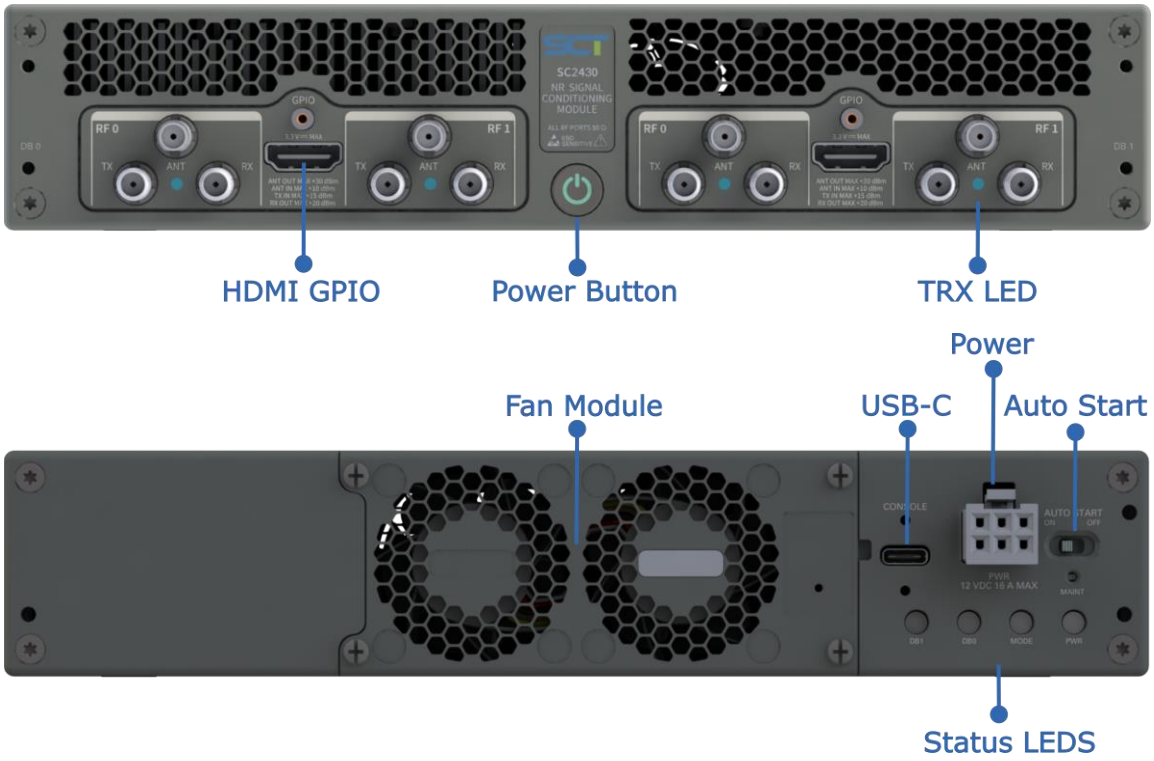

Figure 1 - SC2430 Hardware Overview

2. Hardware Details

2.1 Control Interfaces

This section provides details related to the hardware control interfaces and the pin designations.

2.1.1 HDMI

The front panel HDMI connector utilizes a non-standard pinout intended for interfacing with an NI Ettus-USRP X410. The pinout of the front panel connector is detailed in Figure 2. The functions of each pin are described in Table 1.

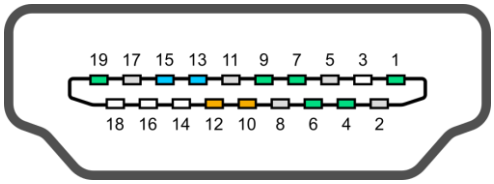

Figure 2 - Front Panel HDMI Connector Receptacle

Pin(s)	Function	Direction	Description
1	SPI SCK	Input	SPI Clock Signal
4	SPI SDO	Output	SPI Serial Data OUT
6	SPI SDI	Input	SPI Serial Data IN
7	SPI CS# (Control)	Input	SPI Chip Select, Control Protocol (Section 3.2)
9	SPI CS# (General)	Input	SPI Chip Select, General Protocol (Section 3.3)
10	ATR CH0	Input	Automatic Transmit/Receive control, Channel 0
12	ATR CH1	Input	Automatic Transmit/Receive control, Channel 1
13	Latch CH0	Input	Attenuator Latch control, Channel 0
15	Latch CH1	Input	Attenuator Latch control, Channel 1
19	SPI Reset#	Input	SPI Interface Reset, Active-Low
2, 5, 8, 11, 17	Ground	-	Ground (0V)
3, 14, 16, 18	*Reserved*	-	Reserved IO

Table 1 - Front Panel HDMI Pin Functions

2.1.1.1 SPI Bus

The SPI Bus supports the Binary Protocol as described in Section 3. Assert the SPI Reset signal before initializing communications to ensure the SPI interface is synchronized and ready. A minimum delay of 600ms is required after deasserting the SPI Reset signal before the SPI interface is ready for communication.

2.1.1.2 ATR Signal

The Antenna (ANT) port of the RF Daughterboard can be connected to either the Transmit or Receive path of the channel. The Automatic Transmit/Receive (ATR) front panel signal can be used to *automatically* control the path selected. To enable this control signal, configure the *ANT Direction Source* as described in Section 5.2.3.

2.1.1.3 Latch Signal

The Attenuator Latch front panel signal can be used to synchronize the change of the RF Daughterboard signal levels. To enable this control signal, configure the RX or TX *Attenuation Latch Source* as described in Sections 5.2.1 and 5.2.2.

2.1.2 USB-C

The rear-panel USB-C interface implements two serial interfaces that support the Console Protocol as described in Section 4. Each interface is associated with one RF Daughterboard (DB) installed in the SC2430 chassis. The RF DB associated with each serial interface can be identified using the *HW:ID?* Command (See Section 4.1.1.1). In addition to supporting the Console Protocol, the serial interface is also used to perform firmware updates.

When sending Console Protocol commands on this interface, it is important to read the returned response data to prevent buffer overflows. The hardware echoes all characters received on the serial interface. The serial interface settings are defined in Table 2.

Parameter	Setting
Baud Rate	115200
Parity	Even
Data Size	8 bits
Stop Bits	1
Flow Control	None

Table 2 – Serial Settings

2.2 LED Indicators

2.2.1 TRX LED

The Transmit/Receive indicators (TRX) are positioned on the front panel below the Antenna (ANT) port of each channel. There is a total of four TRX LED indicators, one for each channel. The significance of each of the LED states is described in Table 3.

State	Description
Green	RX path is connected to the ANT Port
Red	TX path is connected to the ANT Port

Table 3 - TRX LED Indicator Status

2.2.2 Status LED

Four status LEDs are located on the back panel. The significance of each of the LED states is described in Table 4.

LED	State	Description
DB0	OFF	DB0 power disabled
DB0	Amber	DB0 power enabled, unconfigured
DB0	Green	DB0 power enabled, configured
DB0	Red	DB0 power enabled, hardware fault
DB1	OFF	DB0 power disabled
DB1	Amber	DB0 power enabled, unconfigured
DB1	Green	DB0 power enabled, configured
DB1	Red	DB0 power disabled, hardware fault
MODE	Green	DB0/1 normal operation
MODE	Amber	DB0/1 firmware update
MODE	Red	DB0/1 power disabled
PWR	Green (slow blink)	Standby mode, DB0/1 power disabled
PWR	Green (solid)	Normal operation, DB0/1 power enabled
PWR	Green (fast blink)	Normal operation, DB0/1 power disabling
PWR	Red (slow blink)	Hardware fault, DB0/1 power disabled
PWR	Red (solid)	Hardware fault, DB0/1 power enabled
PWR	Red (fast blink)	Hardware fault, DB0/1 power disabling

Table 4 - Status LED Indicators

3. Binary Protocols

The Binary Protocols operates over the front panel HDMI connector. Two selectable protocols are available on the SPI interface and offer different features. The read/write General Purpose protocol provides similar functionality to the Console Protocol and operates at a slower rate. The write-only Control protocol operates at higher rates for time-critical configuration of the RF signal path.

3.1 Peripheral Timing

The SPI Controller must observe the Peripheral timing details listed in Table 5 and Figure 3.

Number	Symbol	Description	Min	Max	Units
1	F_{SCK}[1]	Frequency of operation (Control Protocol)	-	30	MHz
		Frequency of operation (General Protocol)	-	8.192	MHz
2	T_{SCK}	SCK period	$1 / F_{SCK}$	-	ns
3	T_{LEAD}	Enable lead time	2.0	-	ns
4	T_{HSCK}	SCK high time	$(T_{SCK} / 2) - 2$	$(T_{SCK} / 2) + 2$	ns
5	T_{SETUP}	Data setup time	1.0	-	ns
6	T_{HOLD}	Data hold time	2.0	-	ns
7	T_{VALID}	Data valid after SCK edge	-	16.0	ns
8	T_{ACCESS}	Peripheral access time	9.0	27.0	ns

Table 5 - SPI Peripheral Timing Specification

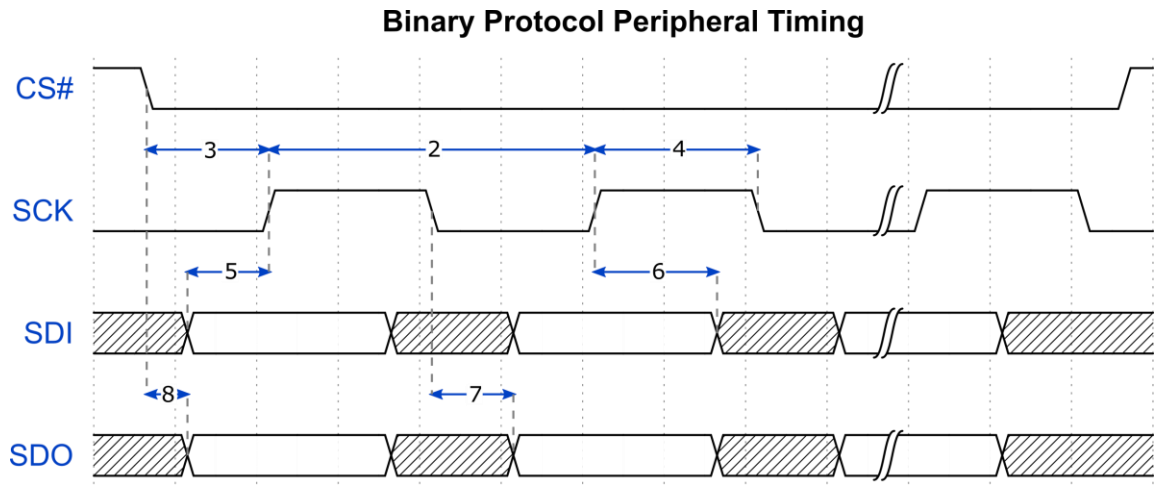

Figure 3 - Binary Protocol Peripheral Timing

[1] Requires the use of SCT Part Number SC2430-54 or SC2430-55

3.2 Control Protocol

3.2.1 Write Transaction

The Control Protocol Write Transaction consists of 16-bits. The upper and lower bytes contain the hardware control element and value to write. See Figure 4 for the Control Protocol Write Transaction.

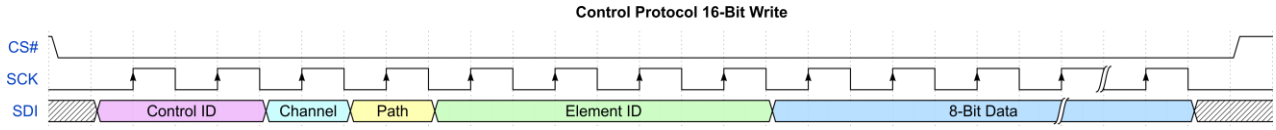

Figure 4 – Control Protocol Write

3.2.2 Transaction Data

3.2.2.1 Control Element Byte

The Control Element Byte is defined as follows:

Bit	7	6	5	4	3	2	1	0
Description	Control ID See Table 6.		Channel 0 = CH0 1 = CH1	Path 0 = RX 1 = TX	Element ID See Section 5.			

3.2.2.2 Data Byte

The Data Byte is defined as follows:

Bit	7	6	5	4	3	2	1	0
Description	Control Element Value: • For *Gain* elements, see Section 5.1. • For *Switch/Trigger* elements, see Section 5.2. • For *Filter* elements, see Section 5.3. • For *Attenuator* elements, see Section 5.4.							

3.3 General Protocol

3.3.1 Write Transaction

The General Protocol Write Transaction consists of 32-bits. The upper byte is the Register Byte containing the register address to write, and the lower bytes contain the 16-bit data value. See Figure 5 for the Write Transaction.

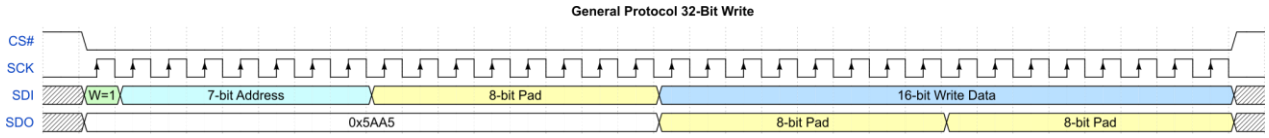

Figure 5 - General Protocol Write Command

3.3.2 Read Transaction

The General Protocol Read Transaction consists of 32-bits. Read command specifies the Register Byte followed by 24-bits of padding. The value of the padding bytes is arbitrary. The read data is returned in the lower 16-bits of the response. See Figure 6 for the Read Transaction.

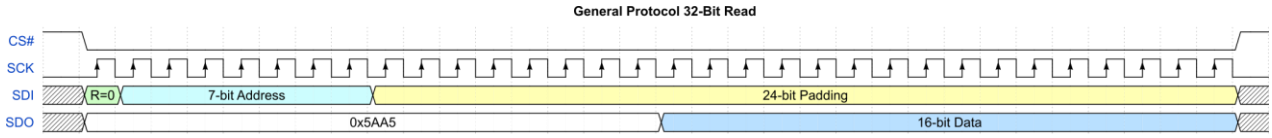

Figure 6 – General Protocol Read Command

3.3.3 Transaction Data

3.3.3.1 Register Byte

The Register Byte is defined as follows:

Bit	7	6	5	4	3	2	1	0
Description	Operation 1: Write 0: Read	Register Address (Section 3.3.4)						

3.3.3.2 Data Bytes

The Data Byte is defined as follows:

Bits	[15..8]	[7..0]
Description	Data Byte 0 (MSB)	Data Byte 1 (LSB)

3.3.4 Register Details

The General Protocol Registers are defined as follows:

ID	Description	Access	Section
0x00	Slot Detect	Read-only	3.3.4.1
0x01	Product ID	Read-only	3.3.4.2
0x02	Hardware Version	Read-only	3.3.4.3
0x03	Firmware Version	Read-only	3.3.4.4
0x04	Serial Number (MSB)	Read-only	3.3.4.5
0x05	Serial Number (LSB)	Read-only	3.3.4.6
0x06	*Reserved*	-	-
0x07	Scratch Register	Read/Write	3.3.4.7
0x08	Control Element ID	Read/Write	3.3.4.8
0x09	Control Element Value	Read-only	3.3.4.9
0x0A	System Health Status	Read-only	3.3.4.10
0x0B	System Health Element ID	Read/Write	3.3.4.11
0x0C	System Health Value (LSB)	Read-only	3.3.4.12
0x0D	System Health Value (MSB)	Read-only	3.3.4.13
0x0E	RF Gain Limits CH0-RX	Read-only	3.3.4.14
0x0F	RF Gain Limits CH0-TX	Read-only	3.3.4.15
0x10	RF Gain Limits CH1-RX	Read-only	3.3.4.16
0x11	RF Gain Limits CH1-TX	Read-only	3.3.4.17
0x12 - 0x7F	*Reserved*	-	-

3.3.4.1 0x00 – Slot Detect

This read-only register is used to indicate that the RF DB is installed into the chassis slot. A fixed value of *0x2020* indicates the RF DB is installed in the chassis.

3.3.4.2 0x01 – Product ID

Read-only register identifying the Product ID of the installed RF DB. A fixed value of *0x0901* is returned for an SC2430 DB.

3.3.4.3 0x02 – Hardware Version

Read-only register identifying the hardware version of the RF DB. The hardware version is identified using a Major and Minor version number represented as "*Major.Minor*".

Bit(s)	Name	Description
[15..8]	VER_MAJOR	Major Hardware Version
[7.0]	VER_MINOR	Minor Hardware Version

3.3.4.4 0x03 – Firmware Version

Read-only register identifying the firmware version of the RF DB. The firmware version is identified using a Major and Minor version number represented as "*Major.Minor*".

Bit(s)	Name	Description
[15..8]	VER_MAJOR	Major Firmware Version
[7.0]	VER_MINOR	Minor Firmware Version

3.3.4.5 0x04 – Serial Number (MSB)

This read-only register contains the most significant bytes of the RF DB serial number. For example, if the DB serial number is *0xABCD1234*, this register contains *0xABCD*. Read the register Serial Number (LSB) (Section 3.3.4.6) to obtain the lower bytes of the serial number.

Bit(s)	Name	Description
[15..8]	SERIAL_0	Serial Number Byte 0 (MSB)
[7.0]	SERIAL_1	Serial Number Byte 1 (LSB)

3.3.4.6 0x05 – Serial Number (LSB)

This read-only register contains the least significant bytes of the DB serial number. For example, if the DB serial number is *0xABCD1234*, this register contains *0x1234*. Read the register Serial Number (MSB) (Section 3.3.4.5) to obtain the upper bytes of the serial number.

Bit(s)	Name	Description
[15..8]	SERIAL_2	Serial Number Byte 2 (MSB)
[7.0]	SERIAL_3	Serial Number Byte 3 (LSB)

3.3.4.7 0x07 – Scratch

Read/Write non-functional register, typically used to validate successful communication with the RF DB.

3.3.4.8 0x08 – Control Element ID

Read/Write register containing the Control Element Byte (Section 3.2.2.1). Following the writing of this register, read register 0x09 (Section 3.3.4.9) to obtain the value associated with this element ID.

Bit(s)	Name	Description
[15..8]	*Reserved*	*Reserved*
[7..0]	CTRL_BYTE	Control Element Byte (Section 3.2.2.1)

A minimum delay of 30ms is required between the writing of this register and reading register 0x09.

3.3.4.9 0x09 – Control Element Value

This read-only register contains the value associated with the Control Element ID specified in register 0x08 (Section 3.3.4.8).

Bit(s)	Name	Description
[15..8]	*Reserved*	*Reserved*
[7.0]	CTRL_VALUE	Control Element Value: • For *Gain* elements, see Section 5.1. • For *Switch/Trigger* elements, see Section 5.2. • For *Filter* elements, see Section 5.3. • For *Attenuator* elements, see Section 5.4.

3.3.4.10 **0x0A – System Health Status**

Read-only register indicating the overall system health status.

Bit(s)	Name	Description
[15..2]	*Reserved*	*Reserved*
[1..0]	STATUS	System Health Status: • 0b00 = Normal • 0b01 = Warning • 0b10 = Alarm • 0b11 = Halted

3.3.4.11 **0x0B – System Health ID**

Read/Write register containing the System Health ID as specified below. Following the writing of this register, read registers 0x0C and 0x0D (Sections 3.3.4.12 and 3.3.4.13) to obtain the LSB and MSB value of the specified health ID.

Bit(s)	Name	Description
[15..4]	*Reserved*	*Reserved*
[3..0]	HEALTH_ID	System Health ID: • 0x0 = 3V3 RF Voltage Rail (V) • 0x1 = 12V2 TX1 Voltage Rail (V) • 0x2 = 5V0 RF Voltage Rail (V) • 0x3 = 3V3 Digital Voltage Rail (V) • 0x4 = -3V3 Voltage Rail (V) • 0x5 = -2V5 Voltage Rail (V) • 0x6 = Bias Controller Internal Temperature (°C) • 0x7 = Bias Controller Closed Loop Current CH0 (A) • 0x8 = Bias Controller Closed Loop Current CH1 (A) • 0x9 = Bias Controller Power Amplifier Voltage CH0 (V) • 0xA = Bias Controller Power Amplifier Voltage CH1 (V) • 0xB = External Temperature Sensor 1 (°C) • 0xC = External Temperature Sensor 5 (°C) • 0xD = Fan Speed 0 (Hz) • 0xE = Fan Speed 1 (Hz)

A minimum delay of 30ms is required between the writing of this register and reading registers 0x0C and 0x0D.

3.3.4.12 **0x0C – System Health Value (LSB)**

This read-only register contains the least significant bytes of the 32-bit floating point number associated with the System Health ID specified in register 0x0B (Section 3.3.4.11). For example, if the 32-bit floating point number is *0x405688CE*, this register contains *0x88CE*. Read the System Health Value (MSB) (Section 3.3.4.13) to obtain the upper bytes of the 32-bit floating point number.

Bit(s)	Name	Description
[15..8]	HEALTH_2	Health Value Byte 2 (MSB)
[7.0]	HEALTH_3	Health Value Byte 3 (LSB)

3.3.4.13 0x0D – System Health Value (MSB)

This read-only register contains the most significant bytes of the 32-bit floating point number associated with the System Health ID specified in register 0x0B (Section 3.3.4.11). For example, if the 32-bit floating point number is *0x405688CE*, this register contains *0x4056*. Read the System Health Value (LSB) (Section 3.3.4.12) to obtain the lower bytes of the 32-bit floating point number.

Bit(s)	Name	Description
[15..8]	HEALTH_0	Health Value Byte 0 (MSB)
[7.0]	HEALTH_1	Health Value Byte 1 (LSB)

3.3.4.14 0x0E – RF Gain Limits CH0-RX

This read-only register contains signed values indicating the gain limit of the CH0 RX path, for the current configuration.

Bit(s)	Name	Description
[15..8]	MAX_GAIN	Maximum Gain Value
[7.0]	MIN_GAIN	Minimum Gain Value

A minimum delay of 500µs is required after changing the path configuration and updating this register value.

3.3.4.15 0x0F – RF Gain Limits CH0-TX

This read-only register contains signed values indicating the gain limit of the CH0 TX path, for the current configuration.

Bit(s)	Name	Description
[15..8]	MAX_GAIN	Maximum Gain Value
[7.0]	MIN_GAIN	Minimum Gain Value

A minimum delay of 500µs is required after changing the path configuration and updating this register value.

3.3.4.16 0x10 – RF Gain Limits CH1-RX

This read-only register contains signed values indicating the gain limit of the CH1 RX path, for the current configuration.

Bit(s)	Name	Description
[15..8]	MAX_GAIN	Maximum Gain Value
[7.0]	MIN_GAIN	Minimum Gain Value

A minimum delay of 500µs is required after changing the path configuration and updating this register value.

3.3.4.17 0x11 – RF Gain Limits CH1-TX

This read-only register contains signed values indicating the gain limit of the CH1 TX path, for the current configuration.

Bit(s)	Name	Description
[15..8]	MAX_GAIN	Maximum Gain Value
[7.0]	MIN_GAIN	Minimum Gain Value

A minimum delay of 500µs is required after changing the path configuration and updating this register value.

4. Console Protocol

The console protocol is derived from but does not strictly adhere to SCPI/IEEE 488.2.

As per SCPI:

- ASCII based.
- Command Syntax structure obeys general SCPI rules in terms of structure and organization.
- Query commands are terminated with a “?” Character.

SCPI deviations:

- Input commands are terminated by a carriage return 0Dh only.
- A single command is accepted on a single line. There is no support for multiple commands separate by a semicolon on a single line.
- All commands will return their output on completion.
- All commands return a status indicator, “OK” for success, “ERR” for error.
- An error status (“ERR”) may be preceded with an error elaboration, describing the nature of the error.
- A prompt is returned as the “>” character. New commands can be input once the prompt is received.
- Numerical arguments can be either in decimal or hexadecimal format (preceded by 0x).

4.1 Command Details

The details of the Console Protocol commands are described in detail in the following sections.

4.1.1 **Hardware Control**

These commands control the SCM hardware.

4.1.1.1 **HW:ID?**

Description
Gets the slot ID of the Daughterboard (DBx) and the status of the adjacent slot.
Syntax
HW:ID?
Arguments
None
Response
• Slot ID: <0 - 1> • Adjacent Slot Status: <Installed | Not Installed>
Example

`> HW:ID?`
`SLot ID = 0`
`Adjacent Card Installed`
`OK`

4.1.1.2 **HW:GAIN**

Description
Sets the calibrated gain setting of the element specified.
Syntax
HW:GAIN <channel> <path> <element ID> <setting>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.1
• setting:
  ○ Represented as a signed integer
  ○ See Section 5.1

Example
`> HW:GAIN 0 RX 0x0 -19` `OK`

4.1.1.3 **HW:GAIN?**

Description
Gets the calibrated gain setting of the element specified.
Syntax
HW:GAIN? <channel> <path> <element ID>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.1

Response

• setting:
  ○ Represented as a signed integer
  ○ See Section 5.1

Example

`> HW:GAIN? 0 RX 0x0`
`GAIN Value = -19`
`OK`

4.1.1.4 **HW:GAINLIM?**

Description
Gets the upper and lower gain limits of the path specified for the current configuration.
Syntax
HW:GAINLIM? <channel> <path>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.

Response
• max gain: <-128 – 127> • min gain: <-128 – 127>
Example

`> HW:GAINLIM? 0 RX`
`Max GAIN = 27, Min GAIN = -25`
`OK`

4.1.1.5 **HW:SW**

Description
Sets the switch/trigger element specified.
Syntax
HW:SW <channel> <path> <element ID> <setting>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.2
• setting:
  ○ Represented as a hexadecimal value
  ○ See Section 5.2

Example
`> HW:SW 0 RX 0x0 0x01` `OK`

4.1.1.6 **HW:SW?**

Description
Gets the switch/trigger element specified.
Syntax
HW:SW? <channel> <path> <element ID>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.2

Response

• setting:
  ○ Represented as a hexadecimal value
  ○ See Section 5.2

Example

`> HW:SW? 0 RX 0x0`
`SWITCH Value = 0x00`
`OK`

4.1.1.7 **HW:FLT**

Description
Sets the filter element specified.
Syntax
HW:FLT <channel> <path> <element ID> <setting>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.3
• setting:
  ○ Represented as a hexadecimal value
  ○ See Section 5.3

Example
`> HW:FLT 0 RX 0x1 0xB4` `OK`

4.1.1.8 **HW:FLT?**

Description
Gets the filter element specified.
Syntax
HW:FLT? <channel> <path> <element ID>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.3

Response

• setting:
  ○ Represented as a hexadecimal value
  ○ See Section 5.3

Example

`> HW:FLT? 0 RX 0x1`
`FILTER Value = 0xB4`
`OK`

4.1.1.9 **HW:ATTN**

Description
Sets the attenuator element specified. This advanced low-level command sets the attenuator settings directly, bypassing the calibration coefficients utilized by the *HW:GAIN* command.
Syntax
HW:ATTN <channel> <path> <element ID> <setting>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.4
• setting:
  ○ Represented as a hexadecimal value
  ○ See Section 5.4

Example
`> HW:ATTN 0 RX 0x0 0x33` `OK`

4.1.1.10 **HW:ATTN?**

Description
Gets the attenuator element specified.
Syntax
HW:ATTN? <channel> <path> <element ID>
Arguments

• channel: <0 - 1>
• path: < TX | RX >
  ○ TX – The transmit path.
  ○ RX – The receive path.
• element ID:
  ○ See Section 5.4

Response

• setting:
  ○ Represented as a hexadecimal value
  ○ See Section 5.4

Example

`> HW:ATTN? 0 RX 0x0`
`ATTN Value = 0x33`
`OK`

4.1.1.11 **HW:TEMP?**

Description
Gets the hardware temperature readings.
Syntax
HW:TEMP?
Arguments
• None
Response
• reading: ID 0, °C • reading: ID 1, °C
Example

```
> HW:TEMP?
ID = 0, Temp = 54.88
ID = 1, Temp = 54.75
OK
```

4.1.1.12 **HW:VOLT?**

Description
Gets the hardware voltage readings.
Syntax
HW:VOLT?
Arguments
• None
Response
• reading: ID 0, V • … • reading: ID 6, V
Example

```
> HW:VOLT?
ID = 0, Voltage = 3.32
ID = 1, Voltage = 0.16
ID = 2, Voltage = 12.24
ID = 3, Voltage = 4.79
ID = 4, Voltage = 3.18
ID = 5, Voltage = -3.27
ID = 6, Voltage = -2.51
OK
```

4.1.1.13 **HW:HEALTH?**

Description
Gets the status of the system health monitor.
Syntax
HW:HEALTH?
Arguments
• None
Response
• reading: 3V3 RF Voltage Rail (V) • reading: 12V2 TX1 Voltage Rail (V) • reading: 5V0 RF Voltage Rail (V) • reading: 3V3 Digital Voltage Rail (V) • reading: -3V3 Voltage Rail (V) • reading: -2V5 Voltage Rail (V) • reading: Bias Controller Internal Temperature (°C) • reading: Bias Controller Closed Loop Current CH0 (A) • reading: Bias Controller Closed Loop Current CH1 (A) • reading: Bias Controller Power Amplifier Voltage CH0 (V) • reading: Bias Controller Power Amplifier Voltage CH1 (V) • reading: External Temperature Sensor 1 (°C) • reading: External Temperature Sensor 5 (°C) • reading: Fan Speed 0 (Hz) • reading: Fan Speed 1 (Hz)
Example

`> HW:HEALTH?`
`3V3 RF = 3.3250, Status = NORMAL`
`12V2 TX1 = 12.2376, Status = NORMAL`
`5V0 RF = 5.0116, Status = NORMAL`
`3V3 = 3.3250, Status = NORMAL`
`n3V3 = -3.2658, Status = NORMAL`
`n2V5 = -2.5147, Status = NORMAL`
`BCTL TEMP INT = 52.5000, Status = NORMAL`
`BCTL CLOOP CUR CH0 = 0.5000, Status = NORMAL`
`BCTL CLOOP CUR CH1 = 0.5059, Status = NORMAL`
`BCTL PA VOL CH0 = 15.0452, Status = NORMAL`
`BCTL PA VOL CH1 = 15.1062, Status = NORMAL`
`EXT TEMP ID 1 = 54.9375, Status = NORMAL`
`EXT TEMP ID 5 = 54.8125, Status = NORMAL`
`FAN SPEED ID 0 = 70.0000, Status = NORMAL`
`FAN SPEED ID 1 = 75.0000, Status = NORMAL`
`Overall Status = NORMAL`
`OK`

4.1.2 PA Control

These commands control the bias controller connected to the TX Power Amplifier (PA). The Bias Controller maintains the bias current setpoint of the PA in the Transmit (TX) path.

4.1.2.1 BIAS:LOOP

Description
Enables the closed-loop bias control. This effectively *enables* the Transmit Path Power Amplifier (PA).
Syntax
BIAS:LOOP <channel> <enable>
Arguments

• channel: <0 - 1>
• enable: <0 | 1>
  ○ 0: Disable
  ○ 1: Enable (default)

Example
`> BIAS:LOOP 0 1` `OK`

4.1.2.2 BIAS:CUR?

Description
Gets the measured currents of the closed-loop bias control.
Syntax
BIAS:CUR?
Arguments
• None
Response
• Reading: Channel 0 current (A) • reading: Channel 1 current (A)
Example

`> BIAS:CUR?`
`Channel = 0, Current = 0.500000`
`Channel = 1, Current = 0.504883`
`OK`

4.1.3 Maintenance

4.1.3.1 *IDN?

Description
Gets the hardware information.
Syntax
IDN?
Arguments
• None
Response
• manufacture: the device manufacture • part number: the device part number • serial number: the device serial number • firmware version: the device firmware version • hardware revision: the hardware revision • reserved revision.
Example

`> *IDN?`
`Signalcraft Technologies, SC2430, #H61607001, 1.00, 1.0, 0.0`
`OK`

4.1.3.2 *RST

Description
Performs a hardware reset, restarting the system, and restoring default settings.
Syntax
*RST
Arguments
• None
Example
`> *RST`

4.1.3.3 *TST?

Description
Performs a system self-test.
Syntax
*TST?
Arguments
• None
Example
`> *TST?` `OK`

4.1.3.4 **MAINT:GETMANUF?**

Description
Gets the hardware manufacturing information.
Syntax
MAINT:GETMANUF?
Arguments
• None
Response
• serial number: the device serial number • date: the date of manufacture using the format YYYY-MM-DD • revision: the hardware revision
Example

`> MAINT:GETMANUF?`
`61607001 2022-03-29 1.0`
`OK`

4.1.3.5 **MAINT:FWUPDATE**

Description
Enables the Firmware Update Mode. The Console Protocol is no longer active once this command has been executed.
Syntax
MAINT:FWUPDATE
Arguments
• None
Example
`> MAINT:FWUPDATE` `OK`

5. Control Elements

This section details the Hardware Control Element IDs and values referenced by both the Console and Binary Protocols.

The Control ID values are defined as shown in Table 6. See the relevant Section for each Control Type for specific details related to the Control Element ID and associated values.

Control ID	Control Type	Section
00b	Attenuator Element	5.1
01b	Gain Element	5.2
10b	Switch/Trigger Element	5.3
11b	Filter Element	5.4

Table 6 - Control ID

5.1 Gain Element

The following Gain Elements apply to the *HW:GAIN* (Section 4.1.1.2) and Binary Protocols (Section 3).

5.1.1 **0x0 – RX Gain Control (x1 CH)**

Element ID
0x0
Path
RX
Description
Set the RX calibrated gain setting for a single channel (0 or 1).
Value
The setting is represented as an 8-bit signed value, specified in dB. • Gain: <0x00 – 0xFF> ○ 0xFF = -1 dB ○ 0xFE = -2 dB ○ 0xF1 = -15 dB ○ … ○ 0x80 = -128 dB ○ 0x7F = +127 dB ○ … ○ 0x0F = +15 dB (default) ○ 0x01 = +1 dB ○ 0x00 = 0 dB

5.1.2 **0x0 – TX Gain Control (1x CH)**

Element ID
0x0
Path
TX
Description
Set the TX calibrated gain setting for a single channel (0 or 1).
Value
The setting is represented as an 8-bit signed value, specified in dB. • Gain: <0x00 – 0xFF> ○ 0xFF = -1 dB ○ 0xFE = -2 dB ○ 0xF1 = -15 dB ○ … ○ 0x80 = -128 dB ○ 0x7F = +127 dB ○ … ○ 0x0F = +15 dB (default) ○ 0x01 = +1 dB ○ 0x00 = 0 dB

5.1.3 **0x1 – RX Gain Control (x2 CH)**

Element ID
0x1
Path(s)
RX
Description
Set the RX calibrated gain setting for both channels (0 and 1).
Value
The setting is represented as an 8-bit signed value, specified in dB. • Gain: <0x00 – 0xFF> ○ 0xFF = -1 dB ○ 0xFE = -2 dB ○ 0xF1 = -15 dB ○ … ○ 0x80 = -128 dB ○ 0x7F = +127 dB ○ … ○ 0x0F = +15 dB (default) ○ 0x01 = +1 dB ○ 0x00 = 0 dB

5.1.4 **0x1 – TX PA Control**

Element ID
0x1
Path(s)
TX
Description
TX Power Amplifier (PA) control.
Value
The setting is represented as a Boolean. • Enable: <0x00 – 0x01> ○ 0: Disabled ○ 1: Enabled (default)

5.2 Switch/Trigger Element

The following Switch/Trigger Elements apply to the *HW:SW* (Section 4.1.1.5) and Binary Protocols (Section 3).

5.2.1 **0x0 – RX Attenuation Latch Source**

Element ID
0x0
Path(s)
RX
Description
Sets the RX Attenuation Source used to trigger the hardware to change the attenuator setting.
Value

The setting is represented as an enumeration.
• Source: <0x00 – 0x01>
  ○ 0x00: Attenuation Trigger, element 0x03/0x05 (Sections 5.2.4/5.2.6, default)
  ○ 0x01: Front panel GPIO Latch signal (Section 2.1.1.3).

5.2.2 **0x0 – TX Attenuation Latch Source**

Element ID
0x0
Path(s)
TX
Description
Sets the TX Attenuation Source used to trigger the hardware to change the attenuator setting.
Value

The setting is represented as an enumeration.
• Source: <0x00 – 0x01>
  ○ 0x00: Attenuation Trigger, element 0x03/0x05 (Sections 5.2.4/5.2.6, default)
  ○ 0x01: Front panel GPIO Latch signal (Section 2.1.1.3).

5.2.3 **0x1 – ANT Direction Source**

Element ID
0x1
Path(s)
RX, TX
Description
Sets the ANT Direction Source used to control the switch connecting the TX or RX path to the ANT port.
Value

The setting is represented as an enumeration.
• Source: <0x00 – 0x01>
  ○ 0x00: ANT Direction Trigger, element 0x04 (Section 5.2.5, default)
  ○ 0x01: Front panel GPIO ATR signal (Section 2.1.1.2).

5.2.4 **0x3 – Attenuation Trigger (x1 CH)**

Element ID
0x3
Path(s)
RX, TX
Description
Single Channel (0 or 1) Attenuation Trigger. Writing this element triggers the hardware to change attenuation settings, provided the TX and/or RX element 0x00 is set to a value of *0x00*. See Sections 5.2.1 and 5.2.2 to set the attenuation trigger source.
Value
The control accepts one value. • Trigger: <0x00>   ○ 0x00: Triggers a simultaneous change to the hardware attenuation.

5.2.5 **0x4 – ANT Direction Switch**

Element ID
0x4
Path(s)
RX, TX
Description
Sets the ANT Direction Switch path. Writing this element sets the ANT port direction if element 0x01 is set to a value of *0x00*. See Section 5.2.3 to set the ANT direction source signal.
Value

The setting is represented as an enumeration.
• Direction: <0x00 – 0x01>
  ○ 0x00: RX Path (default)
  ○ 0x01: TX Path

5.2.6 **0x5 – Attenuation Trigger (x2 CH)**

Element ID
0x5
Path(s)
RX, TX
Description
Dual Channel (0 and 1) Attenuation Trigger. Writing this element triggers the hardware to change attenuation settings, provided the TX and/or RX element 0x00 is set to a value of *0x00*. See Sections 5.2.1 and 5.2.2 to set the attenuation trigger source.
Value
The control accepts one value. • Trigger: <0x00>   ○ 0x00: Triggers a simultaneous change to the hardware attenuation.

5.3 Filter Element

The following Filter Elements apply to the *HW:FLT* (Section 4.1.1.7) and Binary Protocols (Section 3).

5.3.1 **0x1 – RX NR Filter Band Select**

<table>
<tr><td colspan="2">Element ID</td></tr>
<tr><td colspan="2">0x1</td></tr>
<tr><td colspan="2">Path(s)</td></tr>
<tr><td colspan="2">RX</td></tr>
<tr><td colspan="2">Description</td></tr>
<tr><td colspan="2">Sets the RX Path NR Filter Band and Frequency Index.</td></tr>
<tr><td colspan="2">Value</td></tr>
<tr><td colspan="2">The value is a packed 8-bit value where:</td></tr>
<tr><td>Filter Band [7..4]</td><td>Frequency Index [3..0]</td></tr>
<tr><td>The setting is represented as an enumeration.
Filter Band: <0x0 – 0xB>
0x0: n39 (1880 – 1920 MHz)
0x1: n34 (2010 – 2025 MHz)
0x2: n40 (2300 – 2400 MHz)
0x3: n41 (2496 – 2690 MHz)
0x4: n38 (2570 – 2620 MHz)
0x5: n78 (3300 – 3800 MHz)
0x6: n48 (3550 – 3700 MHz)
0x7: n77 (3300 – 4200 MHz)
0x8: n79 (4400 – 5000 MHz)
0x9: n46/n47 (5150 – 5925 MHz)
0xA: n96 (5925 – 7125 MHz)
0xB: bypass (350 – 7200 MHz, default)</td><td>This setting is represented as an integer where each value is an evenly spaced sub-frequency for the filter band specified.
Frequency Index: <0x0 – 0xF>
0x0 – Lower Band
…
0x7 – Mid Band
…
0xF – Upper Band</td></tr>
</table>

5.3.2 **0x2 – TX NR Filter Band Select**

<table>
<tr><th colspan="2">Element ID</th></tr>
<tr><td colspan="2">0x2</td></tr>
<tr><th colspan="2">Path(s)</th></tr>
<tr><td colspan="2">TX</td></tr>
<tr><th colspan="2">Description</th></tr>
<tr><td colspan="2">Sets the TX Path NR Filter Band and Frequency Index.</td></tr>
<tr><th colspan="2">Value</th></tr>
<tr><td colspan="2">The value is a packed 8-bit value where:</td></tr>
<tr><th>Filter Band: Bits [7..4]</th><th>Frequency Index: Bits [3..0]</th></tr>
<tr><td>The setting is represented as an enumeration.
Filter Band: <0x0 – 0xB>
0x0: n39 (1880 – 1920 MHz)
0x1: n34 (2010 – 2025 MHz)
0x2: n40 (2300 – 2400 MHz)
0x3: n41 (2496 – 2690 MHz)
0x4: n38 (2570 – 2620 MHz)
0x5: n78 (3300 – 3800 MHz)
0x6: n48 (3550 – 3700 MHz)
0x7: n77 (3300 – 4200 MHz)
0x8: n79 (4400 – 5000 MHz)
0x9: n46/n47 (5150 – 5925 MHz)
0xA: n96 (5925 – 7125 MHz)
0xB: bypass (350 – 7200 MHz, default)</td><td>This setting is represented as an integer where each value is an evenly spaced sub-frequency for the filter band specified.
Frequency Index: <0x0 – 0xF>
0x0 – Lower Band
…
0x7 – Mid Band
…
0xF – Upper Band</td></tr>
</table>

5.4 Attenuator Element

The following Attenuation Elements apply to the *HW:ATTN* (Section 4.1.1.9) and Binary Protocols (Section 3).

These advanced low-level elements set hardware components directly, bypassing the calibration coefficients utilized by the Gain elements (Section 5.1).

5.4.1 **0x0 – RX Attenuator**

Element ID
0x0
Path
RX
Description
Set the RX attenuator setting.
Value
The setting is represented as a 7-bit value, specified in 0.5 dB steps. • Attenuation: <0x00 – 0x3F> ○ 0x3F = 0 dB ○ 0x3E = 0.5 dB ○ … ○ 0x01 = 31 dB ○ 0x00 = 31.5 dB

5.4.2 **0x0 – TX Attenuator A**

Element ID
0x0
Path
TX
Description
Set the TX attenuator “A” setting.
Value
The setting is represented as a 7-bit value, specified in 0.5 dB steps. • Attenuation: <0x00 – 0x3F> ○ 0x3F = 0 dB ○ 0x3E = 0.5 dB ○ … ○ 0x01 = 31 dB ○ 0x00 = 31.5 dB

5.4.3 **0x1 – RX LNA Enable**

Element ID
0x1
Path(s)
RX
Description
RX LNA control.
Value

The setting is represented as a Boolean.
• Enable: <0x00 – 0x01>
  ○ 0: Disabled
  ○ 1: Enabled

5.4.4 **0x1 – TX Attenuator B**

Element ID
0x1
Path
TX
Description
Set the TX attenuator “B” setting.
Value

The setting is represented as a 7-bit value, specified in 0.5 dB steps.
• Attenuation: <0x00 – 0x3F>
  ○ 0x3F = 0 dB
  ○ 0x3E = 0.5 dB
  ○ …
  ○ 0x01 = 31 dB
  ○ 0x00 = 31.5 dB