Nonvolatile Processor THU1010N Datasheet

Content

1. Introduction

Product Outline

- **Type** THU-1010N[1]
- **Function** Nonvolatile processor for wireless sensor nodes
- **Package** VQFP100(Frame: C100-Q91)
- **Supply voltage** 1.5V±0.15V(Internal Core)，3.3±0.3V(I/0)
- **Temperature range** -40°C ~ 85°C

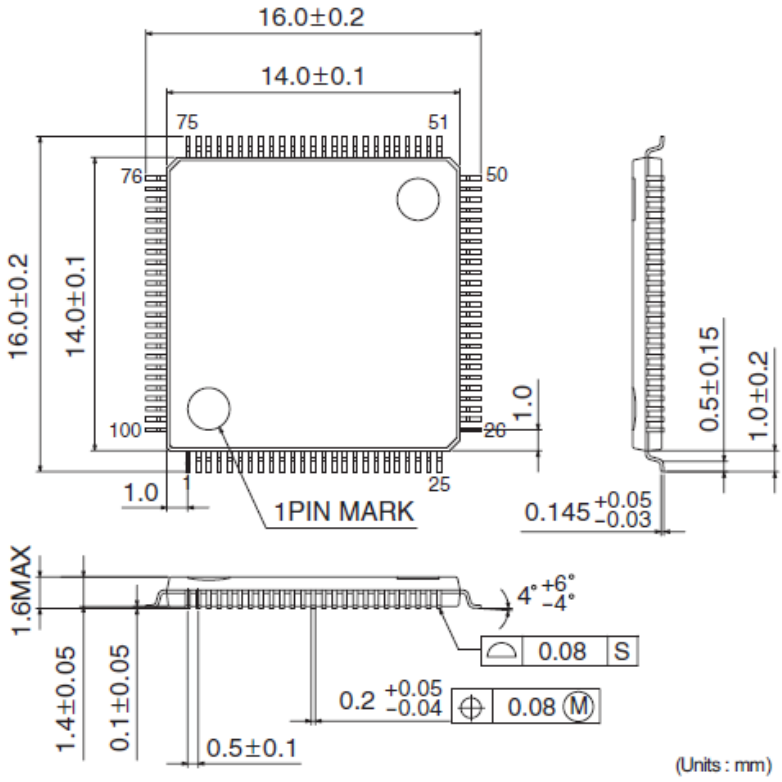
Feature

- Application Description 8051-Instruction Compatible
- Wireless sensor network
- Power management unit supported
- I2C，SPI，UART protocol Interface
- 8K-8bit internal RAM for MCU

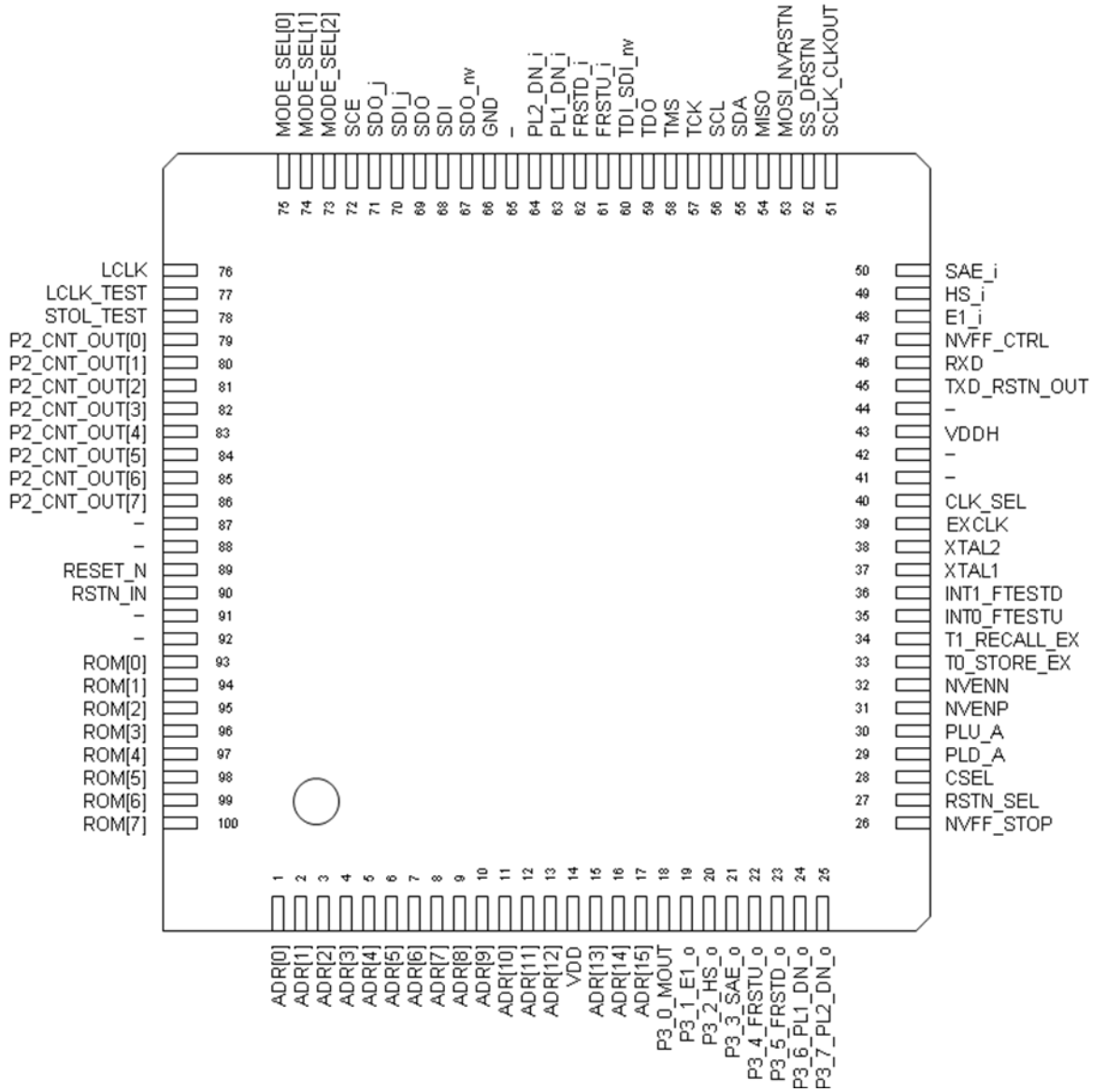
Chip Package

- Package name: VQFP100
- Pin pitch: 0.5 mm
- Size: 16 x 16 x 1.6 (mm)
- Frame type: C100-Q91
- Frame size: 3.4 X 3.4 mm[2]

[1] Naming Rules: THU - 10 10 N
TsingHua Uni. 8051 series # design version non-volatile

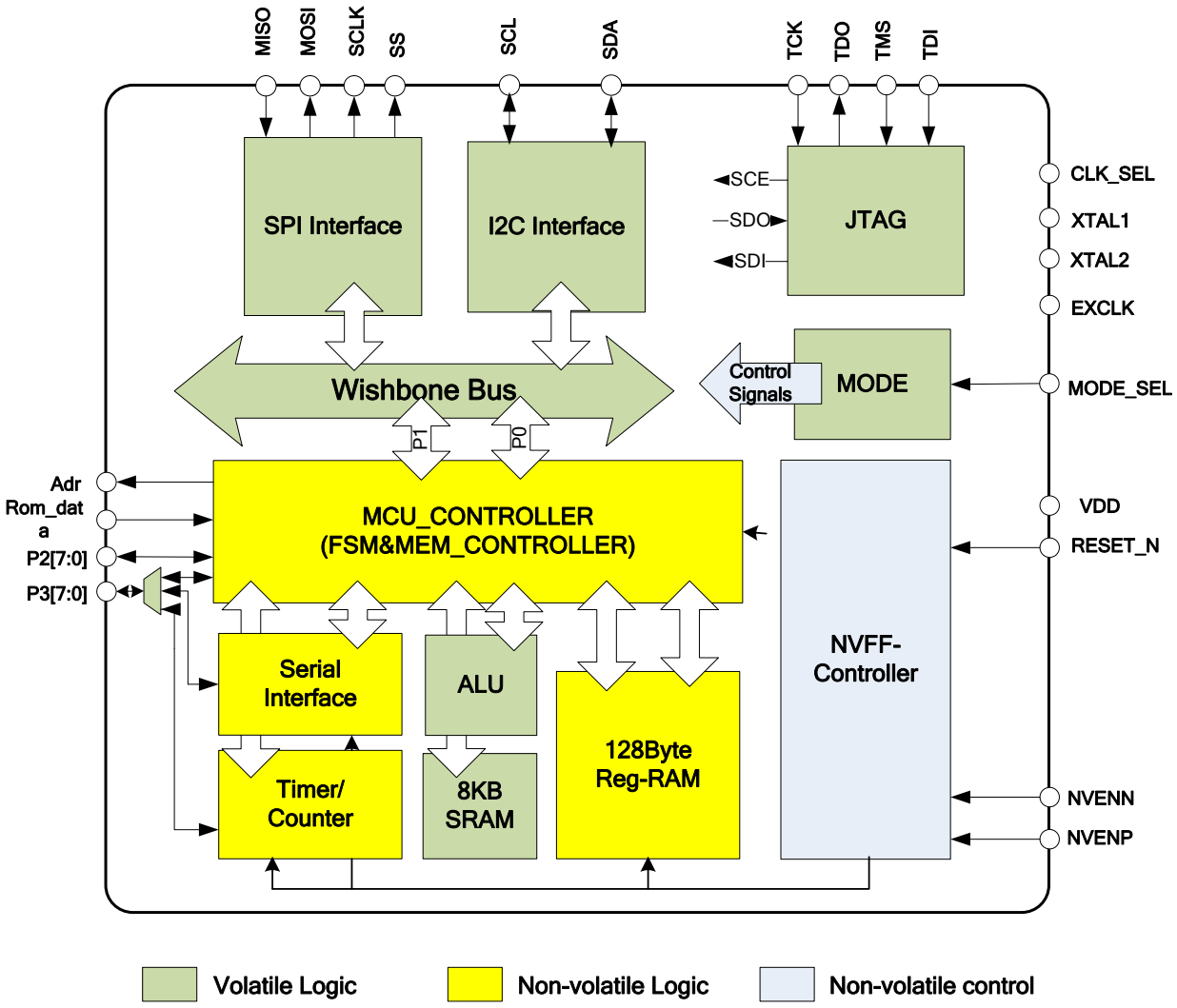

16.0±0.2
14.0±0.1
75
51
76
50
100
26
1
25
1.0
1PIN MARK
16.0±0.2
14.0±0.1
1.0
0.5±0.15
1.0±0.2
0.145 +0.05 −0.03
1.6MAX
4° +6° −4°
0.08 S
0.2 +0.05 −0.04
0.08 M
1.4±0.05
0.1±0.05
0.5±0.1
(Units : mm)

■ Pin Diagram


MODE_SEL[0]
MODE_SEL[1]
MODE_SEL[2]
SCE
SDO_i
SDI_i
SDO
SDI
SDO_nv
GND
_
PL2_DN_i
PL1_DN_i
FRSTD_i
FRSTU_i
TDI_SDI_nv
TDO
TMS
TCK
SCL
SDA
MISO
MOSI_NVRSTN
SS_DRSTN
SCLK_CLKOUT
LCLK
LCLK_TEST
STOL_TEST
P2_CNT_OUT[0]
P2_CNT_OUT[1]
P2_CNT_OUT[2]
P2_CNT_OUT[3]
P2_CNT_OUT[4]
P2_CNT_OUT[5]
P2_CNT_OUT[6]
P2_CNT_OUT[7]
RESET_N
RSTN_IN
ROM[0]
ROM[1]
ROM[2]
ROM[3]
ROM[4]
ROM[5]
ROM[6]
ROM[7]
SAE_i
HS_i
E1_i
NVFF_CTRL
RXD
TXD_RSTN_OUT
VDDH
CLK_SEL
EXCLK
XTAL2
XTAL1
INT1_FTESTD
INT0_FTESTU
T1_RECALL_EX
T0_STORE_EX
NVENN
NVENP
PLU_A
PLD_A
CSEL
RSTN_SEL
NVFF_STOP
ADR[0]
ADR[1]
ADR[2]
ADR[3]
ADR[4]
ADR[5]
ADR[6]
ADR[7]
ADR[8]
ADR[9]
ADR[10]
ADR[11]
ADR[12]
VDD
ADR[13]
ADR[14]
ADR[15]
P3_0_MOUT
P3_1_E1_o
P3_2_HS_o
P3_3_SAE_o
P3_4_FRSTU_o
P3_5_FRSTD_o
P3_6_PL1_DN_o
P3_7_PL2_DN_o

2. Block Diagram

■ Block Diagram



■ Block Description

- **8051 MCU Core:** main controller of entire SOC with 2 parallel I/O ports and an internal UART module. It uses standard 8051 instruction set.
  - **Timer/Counter**
    Module for timing and counting operation
  - **ALU**

Arithmetic Logic Unit of 8051

- **Serial Interface**
  Internal UART module of 8051
- **Special Function Register**
  Nonvolatile Register files of 8051
- **128Byte Reg-RAM**
  Internal non-volatile data memory of 8051
- **SRAM :**
  8K on-chip data memory to store large amounts of data
- **MCU_CONTROLLER**
  Main controller of 8051 containing FSM and memory controller

- **SPI Interface:**
  8051 controlled SPI interface.
- **I^2C Interface:**
  8051 controlled I^2C interface.
- **NVFF Controller module:**
  This module wraps NVFF_TimingController module which generates NVFF control signals, and clockgen module which generates timing and reset signals for NVFFs
- **JTAG:**
  This block scans in test vector to the on chip registers when the chip works in debug mode. It is based on standard JTAG protocol.
- **MODE**
  This block generates appropriate signals to JTAG module and MCU in different working modes including normal mode, scan mode, debug mode and NV-debug mode.

3. IO Pins Description

■ Pin Function Description (Total 92 Pins)

SIGNAL NAME	Pin #	Pin ID	I/O	Pin Description
Power/Clock/Reset/General Mode (12pins)				
GND	1		Power	Digital core ground
VDD	1		Power	1.5V digital core supply
VDDH	1		Power	3.3V Output driver supply
XTAL1	1		OS Input	External Oscillator Input
XTAL2	1		OS Output	External Oscillator Output
EXCLK	1		Input	External Clock signal input.
CLK_SEL	1		Input	Select the source of the system clock
RESET_N	1		Input	Device Reset Signal in Normal mode and NVDEBUG mode. An external source can initiate a system reset by driving this pin low.
RSTN_IN	1		Input	Reset Signal in Scan mode. An external source can initiate a system reset by driving this pin low.
Mode_Select	3		Input	8 Mode select signal. Definition seen in Section 16. Test and Debug Methodology
MCU/NVFF_Controller (54 pins)				
Adr[0:15]	16		Output	64kx8bit external instruction memory address
Rom_data[0:7]	8		Input	64kx8bit external instruction memory data. The memory is read only.
T0/ STORE_EX	1		Input	Timer/counter 0 inputs / Signal to request STORE action externally
T1/ RECALL_EX	1		Input	Timer/counter 1 inputs / Signal to request RECALL action externally
INT0 / FTESTU	1		Input	Interrupt 0 input. / Signal to select normal / NVFF-analog-test mode
INT1 / FTESTD	1		Input	Interrupt 1 input. / Signal to select normal / NVFF-analog-test mode
RXD	1		I/O	Data Output for UART mode0/Data input for UART in other modes
TXD/RSTN_OUT	1		Output	Data Output for serial interface units (UART). /NVFF Reset signal output (for NV DEBUG)
P3.0/ MOUT	1		I/O /Output	Parallel Port3.0/ BUSY signal
P3.1/ E1_o	1		I/O /Output	Parallel Port3.1/ Control signals for NVFFs (for monitoring)
P3.2/ HS_o	1		I/O /Output	Parallel Port3.2/ Control signals for NVFFs (for monitoring)
P3.3/ SAE_o	1		I/O /Output	Parallel Port3.3/ Control signals for NVFFs (for monitoring)
P3.4/	1		I/O	Parallel Port3.4/

FRSTU_o			/Output	Control signals for NVFFs (for monitoring)
P3.5 / FRSTD_o	1		I/O /Output	Parallel Port3.5/ Control signals for NVFFs (for monitoring)
P3.6 / PL1_DN_o	1		I/O /Output	Parallel Port3.6/ Control signals for NVFFs (for monitoring)
P3.7/ PL2_DN_o	1		I/O /Output	Parallel Port3.7/ Control signals for NVFFs (for monitoring)
P2[7:0]/ CNT_OUT	8		I/O /Output	Parallel Port2/ Signal indicating the value of internal counter
SCL	1		I/O	I^2C serial clock signal.
SDA	1		I/O	I^2C serial data signal.
sclk/CLKOUT	1		Output	SPI serial clock signal, change and latch signal at the edge of Sclk/ Clock output that NVFF_Controller drive the Logic Cell with(For NVDEBUG)
ss/DRSTN	1		Output	SPI interface slave select signal/ Volatile FF reset signal(For NV DEBUG)
mosi/NVRSTN	1		Output	SPI data master to slave/ Non-Volatile FF reset signal(For NV DEBUG)
miso	1		Input	SPI data slave to master
NVENN	1		Input	(NVENN, NVENP) = (0,1) : non-volatile mode
NVENP	1		Input	(NVENN, NVENP) ≠ (0,1) : volatile mode
Other NVFF_Controller signals (16 pins)				
CSEL	1		Input	Signal to select internal/external clock mode 0: internal clock mode 1: external clock mode (For NV DEBUG)
RSTN_SEL	1		Input	Signal to select internal/external reset mode 0: internal reset mode 1: external reset mode (For NV DEBUG)
NVFF_STOP	1		Input	Signal to select internal/external reset mode 0: internal reset mode 1: external reset mode (For NV DEBUG)
STOL_TEST	1		Input	Signal to select normal/STOL-test mode (For NV DEBUG)
LCLK_TEST	1		Input	Signal to select normal/internal-CLK-test mode (For NV DEBUG)
LCLK	1		Output	
PLU_A	1		Analog Input	Input of plate voltage in the non-volatile FF analog test mode (For NV DEBUG)
PLD_A	1		Analog Input	Input of plate voltage in the non-volatile FF analog test mode (For NV DEBUG)
NVFF_CTRL	1		Input	Switch signal for external NVFF control mode
E1_i	1		Input	External E1 signal
HS_i	1		Input	External HS signal
SAE_i	1		Input	External SAE signal
FRSTU_i	1		Input	External FRSTU signal

FRSTD_i	1		Input	External FRSTD signal
PL1_DN_i	1		Input	External PL1_DN signal
PL2_DN_i	1		Input	External PL2_DN signal
JTAG&SCAN (10 pins)				
TCK	1		Input	Test Clock for JTAG
TDO	1		Output	Test Data Output for JTAG
TMS	1		Input	Test Model Select for JTAG
TDI/ SDI_nv	1		Input	Test Data Input for JTAG and Scan Input for Non-volatile scan chain
SDO	1		Output	Scan Output for Volatile scan chain
SDI	1		Input	Scan Input for Volatile scan chain
SDO_nv	1		Output	Scan Input for Non-volatile scan chain
SDI_j	1		Input	Scan Input for JTAG module
SDO_j	1		Output	Scan Input for JTAG module
SCE	1		Input	Scan enable signal in SCAN Mode

1) Pints for MCU Part can be reduced further if EEPROM is embedded in the chip. There are 24 pins for EEPROM
2) Pins of timer and interrupt (4 pins) can be reduced if they share parallel ports.

■ Pin Description of Each Mode/ PAD Type Definition

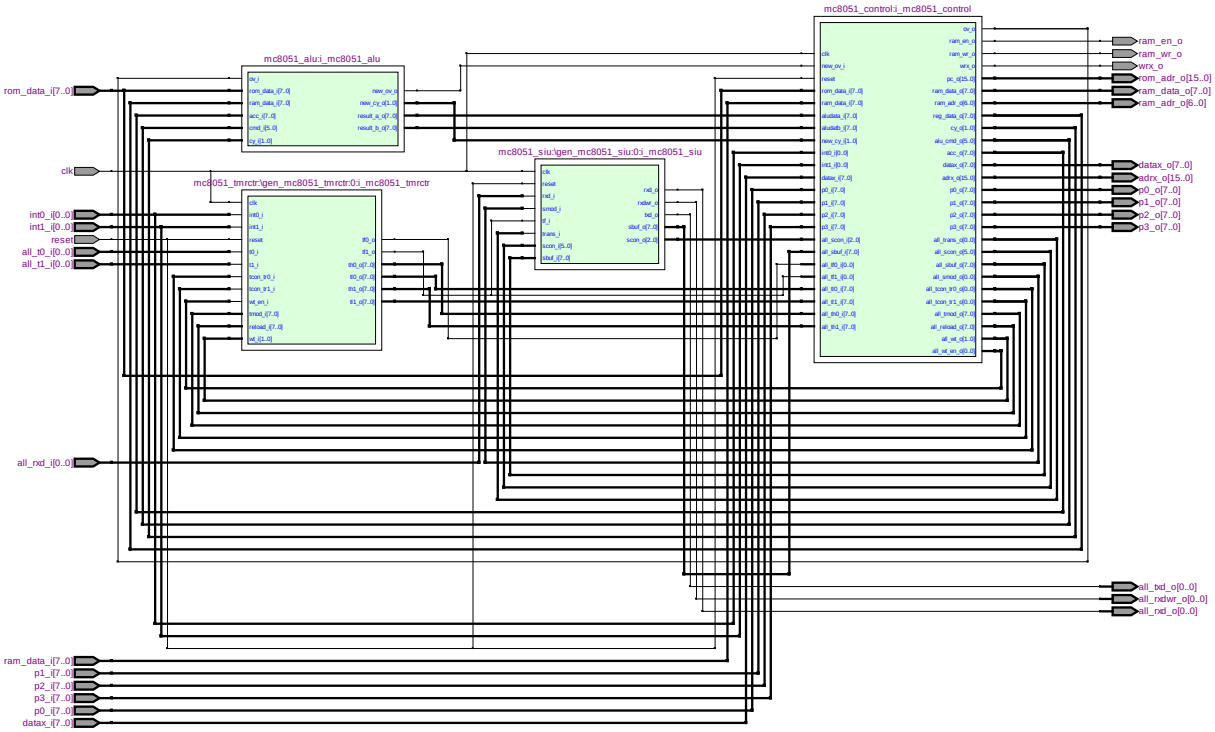
SIGNAL NAME	Pin No.	I/O	MODE ※			
			NORMAL	SCAN	NV DEBUG	DEBUG (JTAG)
GND	1	Power	Pin	Pin	Pin	Pin
VDD	1	Power	Pin	Pin	Pin	Pin
VDDH	1	Power	Pin	Pin	Pin	Pin
XTAL1	1	OSC Input	Pin	Pin	Pin	-
XTAL2	1	OSC Output	Pin	Pin	Pin	-
EXCLK	1	Input	Pin	Pin	Pin	-
CLK_SEL	1	Input	Pin	Pin	Pin	-
RESET_N	1	Input	Pin	-	Pin	-
RSTN_IN	1	Input	-	Pin	Pin	Pin
Mode_Select	3	Input	NORMAL	SCAN	NV DEBUG	DEBUG
Adr[0:15]	16	Output	Pin	-	-	Pin
Rom_data[0:7]	8	Input	Pin	-	-	Pin
T0/ STORE_EX	1	Input	all_t0_i	-	STORE_EX	all_t0_i
T1/ RECALL_EX	1	Input	all_t1_i	-	RECALL_EX	all_t1_i
INT0/ FTESTU	1	Input	int0_i	-	FTESTU	int0_i
INT1/ FTESTD	1	Input	int1_i	-	FTESTD	int1_i
RXD	1	I/O	Pin	-	-	Pin
TXD_o/RSTN_OUT	1	Output	txd_o	-	RSTN_OUT	txd_o
P3.0/MOUT	1	I/O /Output	P3.0	-	MOUT	P3.0
P3.1/E1_o	1	I/O /Output	P3.1	-	E1_o	P3.1
P3.2/HS_o	1	I/O /Output	P3.2	-	HS_o	P3.2
P3.3/SAE_o	1	I/O /Output	P3.3	-	SAE_o	P3.3
P3.4/ FRSTU_o	1	I/O /Output	P3.4	-	FRSTU_o	P3.4
P3.5 /FRSTD_o	1	I/O /Output	P3.5	-	FRSTD_o	P3.5
P3.6 /PL1_DN_o	1	I/O /Output	P3.6	-	PL1_DN_o	P3.6
P3.7 /PL2_DN_o	1	I/O /Output	P3.7	-	PL2_DN_o	P3.7
P2[7:0]/CNT_OUT	8	I/O /Output	P2[7:0]	-	CNT_OUT	P2
SCL	1	I/O	Pin	-	-	Pin
SDA	1	I/O	Pin	-	-	Pin
sclk/CLKOUT	1	Output	sclk	-	CLKOUT	Pin

ss/DRSTN	1	Output	ss	-	DRSTN	Pin
mosi/NVRSTN	1	Output	mosi	-	NVRSTN	Pin
Miso	1	Input	Pin	-	-	Pin
NVENN	1	Input	Pin	-	Pin	Pin
NVENP	1	Input	Pin	-	Pin	Pin
CSEL	1	Input	-	-	Pin	-
RSTN_SEL	1	Input	-	-	Pin	-
NVFF_STOP	1	Input	-	-	Pin	-
STOL_TEST	1	Input	-	-	Pin	-
LCLK_TEST	1	Input	-	-	Pin	-
LCLK	1	Output	-	-	Pin	-
PLU_A	1	Analog Input	-	-	Pin	-
PLD_A	1	Analog Input	-	-	Pin	-
NVFF_CTRL	1	Input	Pin	Pin	Pin	Pin
E1_i	1	Input	Pin	Pin	Pin	Pin
HS_i	1	Input	Pin	Pin	Pin	Pin
SAE_i	1	Input	Pin	Pin	Pin	Pin
FRSTU_i	1	Input	Pin	Pin	Pin	Pin
FRSTD_i	1	Input	Pin	Pin	Pin	Pin
PL1_DN_i	1	Input	Pin	Pin	Pin	Pin
PL2_DN_i	1	Input	Pin	Pin	Pin	Pin
TCK	1	Input	-	-	-	Pin
TDO	1	Output	-	-	-	Pin
TMS	1	Input	-	-	-	Pin
TDI/SDI_nv	1	Input	-	Pin	-	Pin
SDO_nv	1	Output	-	Pin	-	-
SDI	1	Input	-	Pin	-	-
SDO	1	Output	-	Pin	-	-
SDI_j	1	Input	-	Pin	-	-
SDO_j	1	Output	-	Pin	-	-
SCE	1	Input	-	Pin	-	-

※ DC/IDDQ modes are reserved.

4. MCU Core Block Specification

■ Function Diagram



■ Function Block Description

- **Mc8051_tmrctr**
  Module for timing and counting operations. See Timer/Counter sub-block specification for details.
- **Mc8051_alu**
  Arithmetic Logic Unit of 8051. See ALU sub-block specification for details.
- **Mc8051_siu**
  Internal UART module of 8051
- **Mc8051_control**
  Main controller of 8051 containing FSM and memory controller. See MCU Controller sub-block specification for details.

■ I/O Pins

Signal	I/O	Specification

adrx_o[0:15]	Out	Address output to external ram
all_t0_i	In	Timer/counter 0 inputs.
all_t1_i	In	Timer/counter 1 inputs.
all_rxd_i	In	Receive data input for serial interface units (UART).
all_rxd_o	Out	Data output for mode 0 operation of serial interface unit.
all_rxdwr_o	Out	Data direction signal for bidirectional rxd input/output (high = output) data.
all_txd_o	Out	Transmit data output for serial interface units (UART).
clk	In	Global Clock Input.
datax_i[0:7]	In	Data input from 8kx8bit external ram
datax_o[0:7]	Out	Data output to 8kx8bit external ram
int0_i	In	Interrupt 0 inputs.
int1_i	In	Interrupt 1 inputs..
P0_i[0:7]	In	8051 0th Parallel Input Port. 8 bit.
P0_o[0:7]	Out	8051 0th Parallel Output Port. 8 bit.
P1_i[0:7]	In	8051 1st Parallel Input Port. 8 bit.
P1_o[0:7]	Out	8051 1st Parallel Output Port. 8 bit.
P2_i[0:7]	In	8051 2nd Parallel Input Port. 8 bit.
P2_o[0:7]	Out	8051 2nd Parallel Output Port. 8 bit.
P3_i[0:7]	In	8051 3rd Parallel Input Port. 8 bit.
P3_o[0:7]	Out	8051 3rd Parallel Output Port. 8 bit.
ram_data_i[0:7]	In	Data input from 128x8bit ram.
ram_data_o[0:7]	Out	Data output to 128x8bit ram.
ram_adr_o[0:6]	Out	Address output to 128x8bit ram.
ram_en_o	Out	128x8bit ram enable signal
ram_wr_o	Out	128x8bit ram write/read signal (high:write)
reset	In	Device Reset Signal. An external source can initiate a system reset by driving this pin low.
rom_data_i[0:7]	In	64kx8bit external instruction memory data. The memory is read only.
rom_adr_o[0:15]	Out	64kx8bit external instruction memory address out.
wrx_o	Out	8kx8bit ram write/read signal (high:write)

■ 8051 Special Function Register (SFR) Table

Symbol	Address	Name	Bit Address (For Bit Addressable)		Sub-block
			Symbol	Address	
*ACC	E0H	Accumulator	ACC.7~ACC.0	E7H~E0H	MEM_CONTROLLER
*B	F0H	Multiply/Divide Register	B.7~B.0	F7H~F0H	MEM_CONTROLLER
*PSW	D0H	Program status word	PSW.7~PSW.0	D7H~D0H	MEM_CONTROLLER
SP	81H	Stack pointer			MEM_CONTROLLER
DPL	82H	XRAM Address(Low byte)			MEM_CONTROLLER
DPH	83H	XRAM Address(High byte)			MEM_CONTROLLER
*IE	A8H	Interrupt enable	IE.7~IE.0	AFH~A8H	MEM_CONTROLLER

		control			
*IP	B8H	Interrupt priority control	IP.7~IP.0	BFH~B8H	MEM_CONTROLLER
*P0	80H	Port 0	P0.7~P0.0	87H~80H	MEM_CONTROLLER
*P1	90H	Port 1	P1.7~P1.0	97H~90H	MEM_CONTROLLER
*P2	A0H	Port 2	P2.7~P2.0	A7H~A0H	MEM_CONTROLLER
*P3	B0H	Port 3	P3.7~P3.0	B7H~B0H	MEM_CONTROLLER
PCON	87H	Baud rate control(Only use SMOD)			MEM_CONTROLLER
* SCON	98H	Serial control	SCON.7~SCON.0	9FH~98H	Serial Interface
SBUF	99H	Serial data buffer			Serial Interface
*TCON	88H	Timer/counter control	TCON.7~TCON.0	8FH~88H	MEM_CONTROLLER
TMOD	89H	Timer/counter mode control			MEM_CONTROLLER
TL0	8AH	Timer/counter 0 low byte			Timer/Counter
TL1	8BH	Timer/counter 1 low byte			Timer/Counter
TH0	8CH	Timer/counter 0 high byte			Timer/Counter
TH1	8DH	Timer/counter 1 high byte			Timer/Counter

*: This register is bit-addressable

■ SFR Definition

■ SP : Stack Pointer; SFR Address = 0x81

Bit	7	6	5	4	3	2	1	0
Name	SP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	1	1

Bit	Name	Function
7:0	SP[7:0]	Stack Pointer. The Stack Pointer holds the location of the top of the stack. The stack pointer is incresed before every PUSH operation. The SP register defaults to 0x07 after reset.

■ ACC : Accumulator; SFR Page = All Pages; SFR Address = 0xE0; Bit-Addressable

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	ACC[7:0]	Accumulator. This register is the accumulator for arithmetic operations.

■ B : B register; SFR Address = 0xF0; Bit-Addressable

Bit	7	6	5	4	3	2	1	0
Name	B[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	B[7:0]	B Register. This register serves as a second accumulator for certain arithmetic operations.

■ PSW : Program Status Word; SFR Address = 0xD0; Bit-Addressable

Bit	7	6	5	4	3	2	1	0
Name	CY	AC	F0	RS[1:0]		OV	F1	PARITY
Type	R/W	R/W	R/W	R/W		R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7	CY	Carry Flag. This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to logic 0 by all other arithmetic operations.
6	AC	Auxiliary Carry Flag. This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to logic 0 by all other arithmetic operations.
5	F0	User Flag 0. This is a bit-addressable, general purpose flag for use under software control.
4:3	RS[1:0]	Register Bank Select. These bits select which register bank is used during register accesses. 00: Bank 0, Addresses 0x00-0x07 01: Bank 1, Addresses 0x08-0x0F 10: Bank 2, Addresses 0x10-0x17 11: Bank 3, Addresses 0x18-0x1F

2	OV	Overflow Flag. This bit is set to 1 under the following circumstances: • An ADD, ADDC, or SUBB instruction causes a sign-change overflow. • A MUL instruction results in an overflow (result is greater than 255). • A DIV instruction causes a divide-by-zero condition. The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.
1	F1	User Flag 1. This is a bit-addressable, general purpose flag for use under software control.
0	PARITY	Parity Flag. This bit is set to logic 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

■ DPL : Data Pointer Low Byte; SFR Address = 0x82

Bit	7	6	5	4	3	2	1	0
Name	DPL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	DPL[7:0]	Data Pointer Low. The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access addressed Flash memory or XRAM indirectly.

■ DPH : Data Pointer High Byte; SFR Address = 0x83

Bit	7	6	5	4	3	2	1	0
Name	DPH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	DPH[7:0]	Data Pointer High. The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access addressed Flash memory or XRAM indirectly.

■ IE : Interrupt Enable; SFR Address = 0xA8; Bit-Addressable

Bit	7	6	5	4	3	2	1	0
Name	EA	--	--	ES0	ET1	EX1	ET0	EX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7	EA	Enable All Interrupts. Globally enables/disables all interrupts. It overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	Unused	Unused. Read = 1b, Write = don't care.
5	Unused	Unused. Read = 0b, Write = don't care.
4	ES0	Enable UART0 Interrupt. This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	Enable Timer 1 Interrupt. This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupting requests generated by the TF1 flag.
2	EX1	Enable External Interrupt 1. This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupting requests generated by the INT1 input.
1	ET0	Enable Timer 0 Interrupt. This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupting requests generated by the TF0 flag.
0	EX0	Enable External Interrupt 0. This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupting requests generated by the INT0 input.

■ IP : Interrupt Priority; SFR Address = 0xB8; Bit-Addressable

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	PS0	PT1	PX1	PT0	PX0
Type	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bit	Name	Function
7	Unused	Unused. Read = 1b, Write = don't care.

6	Unused	Unused. Read = 0b, Write = don't care.
5	Unused	Unused. Read = 0b, Write = don't care.
4	PS0	UART0 Interrupt Priority Control. This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	Timer 1 Interrupt Priority Control. This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	External Interrupt 1 Priority Control. This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	Timer 0 Interrupt Priority Control. This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	External Interrupt 0 Priority Control. This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

■ SCON : Serial Port Control; SFR Address = 0x98; Bit-Addressable

Bit	76	5	4	3	2	1	0
Name	SM[1:0]	SM2	REN	TB8	RB8	TI	RI
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	00	0	0	0	0	0	0

Bit	Name	Function
7 6	SM[1:0]	Serial Port Operation Mode. Selects the UART0 Operation Mode. 00: mode0 8-bit UART with Baud Rate SYSCLK(20MHz)/12. 01: mode1 8-bit UART with Variable Baud Rate. 10: mode2 9-bit UART with Baud Rate SYSCLK(20MHz)/16 or SYSCLK(20MHz)/32. 11: mode3 9-bit UART with Variable Baud Rate.

5	SM2	Multiprocessor Communication Enable. For Mode 0/1 (8-bit UART): Checks for valid stop bit. 0: Logic level of stop bit is ignored. 1: RI will only be activated if stop bit is logic level 1. For Mode 2/3 (9-bit UART): Multiprocessor Communications Enable. 0: Logic level of ninth bit is ignored. 1: RI is set and an interrupt is generated only when the ninth bit is logic 1.
4	REN	Receive Enable. 0: UART reception disabled. 1: UART reception enabled.
3	TB8	Ninth Transmission Bit. The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 2, 3). Unused in 8-bit mode (Mode 0, 1).
2	RB8	Ninth Receive Bit. RB8 is assigned the value of the STOP bit in Mode 0, 1; it is assigned the value of the 9th data bit in Mode 2, 3.
1	TI	Transmit Interrupt Flag. Set by hardware when a byte of data has been transmitted by UART (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART interrupt service routine. This bit must be cleared manually by software.
0	RI	Receive Interrupt Flag. Set to 1 by hardware when a byte of data has been received by UART (set at the STOP bit sampling time). When the UART interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART interrupt service routine. This bit must be cleared manually by software.

- **TCON : Timer Control; SFR Address = 0x88; Bit-Addressable**

Bit	7	6	5	4	3	2	1	0
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7	TF1	Timer 1 Overflow Flag. Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
6	TR1	Timer 1 Run Control. Timer 1 is enabled by setting this bit to 1.

5	TF0	Timer 0 Overflow Flag. Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
4	TR0	Timer 0 Run Control. Timer 0 is enabled by setting this bit to 1.
3	IE1	External Interrupt 1. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.
2	IT1	Interrupt 1 Type Select. This bit selects whether the configured INT1 interrupt will be edge or level sensitive. INT1 is active high. 0: INT1 is level triggered. 1: INT1 is edge triggered.
1	IE0	External Interrupt 0. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.
0	IT0	Interrupt 0 Type Select. This bit selects whether the configured INT0 interrupt will be edge or level sensitive. INT0 is active high 0: INT0 is level triggered. 1: INT0 is edge triggered.

- **TMOD : Timer Mode; SFR Address = 0x89; Bit-Addressable**

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function

7	GATE1	Timer 1 Gate Control. 0: Timer 1 enabled when TR1 = 1 irrespective of INT1 logic level. 1: Timer 1 enabled only when TR1 = 1 AND INT1 is active.
6	C/T1	Counter/Timer 1 Select. 0: Timer: Timer 1 incremented by system clock. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	Timer 1 Mode Select. These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload. 11: Mode 3, Timer 1 Inactive.
3	GATE0	Timer 0 Gate Control. 0: Timer 0 enabled when TR0 = 1 irrespective of INT0 logic level. 1: Timer 0 enabled only when TR0 = 1 AND INT0 is active.
2	C/T0	Counter/Timer 0 Select. 0: Timer: Timer 0 incremented by system clock. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	Timer 0 Mode Select. These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

- **PCON: Baud rate Control; SFR Address = 0x87;**

Bit	7	6	5	4	3	2	1	0
Name	SMOD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Type	R/W	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function

7	SMOD	0: When in UART serial transmission, baud rate are pre-divided by 2 1: When in UART serial transmission, baud rate are not pre-divided.
6:0	Unused	Unused. Read = 1b, Write = don't care.

- **P0~P3: Registers for Parallel Port; SFR Address = 0x80, 0x90, 0xA0, 0xB0;**

Bit	0:7
Name	Pi
Type	R/W
Reset	0xFF

-

Bit	Name	Function
Pi		Only used as the ith Parallel Port

NVFF Replacement

In order to save the state and intermediate data of the MCU when power is down, we need to replace the following 578 bit + 128 byte registers..

- 128byte Register-RAM:

Table 6.1 8051 Register-RAM organization and corresponding address

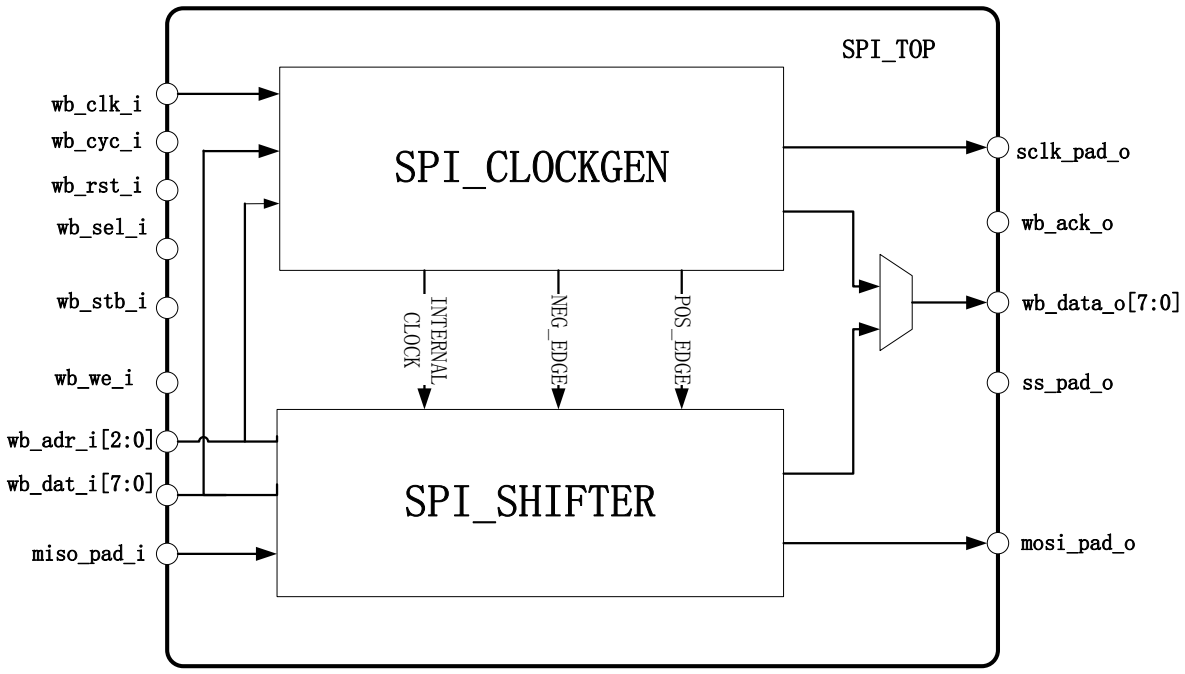
Address	Register Function Description
30H~7FH	Data Buffer Stack Workspace
20H~2FH	Bit addressable region
18H~1FH	R0~R7 (4)
10H~17H	R0~R7 (3)
08H~0FH	R0~R7 (2)
00H~07H	R0~R7 (1)

- 578bit registers
  - 466 bit registers in module “MCU_CONTROLLER” containing SFR described in Section 6.4 and other intermediate state registers.
  - 64 bit registers in module “Serial Interface” containing UART buffers and registers indicating serial transmission states.

- 48 bit registers in module “Timer/Counter” containing SFR {TL0,TL1,TH0,TH1} described in Section 6.4 and other intermediate state registers

5. SPI Controller Block Specification

■ Function Diagram



■ Function Block Description

- SPI_CLOCKGEN: SPI sequence signals generator, including sclk.
- SPI_SHIFTER: SPI data shifter, monitoring data fetching, sending and receiving.

■ I/O Pins

Signal	I/O	Specification
wb_clk_i	In	Master clock
wb_rst_i	In	Synchronous reset
wb_adr_i[2:0]	In	Lower address bits
wb_dat_i[7:0]	In	Data towards the core
wb_we_i	In	Write enable input (control read/write of SPI_RX/TX registers)
wb_sel_i	In	Core selection input
wb_cyc_i	In	Valid bus cycle input
wb_stb_i	In	Strobe signal
miso_pad_i	In	Master in slave out data signal input
mosi_pad_o	Out	Master out slave in data signal output
sclk_pad_o	Out	Serial clock output

ss_pad_o	Out	Slave select output signals
wb_ack_o	Out	Bus cycle acknowledge output
wb_data_o	Out	Data from the core

■ Register Table/Map

Name	Address	Width	Description
SPI_RX_0	3'b000	8	Reception buffer 0
SPI_RX_1	3'b001	8	Reception buffer 1
SPI_RX_2	3'b010	8	Reception buffer 2
SPI_RX_3	3'b011	8	Reception buffer 3
SPI_TX_0	3'b000	8	Transmission buffer 0
SPI_TX_1	3'b001	8	Transmission buffer 1
SPI_TX_2	3'b010	8	Transmission buffer 2
SPI_TX_3	3'b011	8	Transmission buffer 3
SPI_CTRL	3'b100	8	SPI control and status register
SPI_DEVIDE	3'b101	8	Clock division rate 8bit
SPI_SS	3'b110	8	Slave selection 8bit

■ SPI_DEVIDE: Adr = 3'b101;

Bit	7	6	5	4	3	2	1	0
Name	SPI_DEVIDE[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	SPI_DEVIDE[7:0]	This register indicates spi clock division rate: $f_{sclk} = \frac{f_{wb\_clk}}{(DIVIDER+1)*2}$.

■ SPI_CTRL: SPI control register Adr=3'b100

Bit	7	6	5	4	3	2	1	0
Name	ASS	Reserved	LSB	TX_NEGEDGE	RX_NEGEDGE	GO/BUSY	Reserved	Reserved
Type	R/W	R	R/W	R/W	R/W	R/W	R	R
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function

7	ASS	SS signal automation 0: slave select output signals (ss_pad_o) are asserted and de-asserted by writing and clearing bits in the SPI_SS register. 1: ss_pad_o signals are generated automatically.
6	Reserved	
5	LSB	1: LSB(bit TxL[0]) is sent first on the line, and the first bit received from the line will be put in the LSB of Rx register(bit RxL[0]). 0: MSB(bit TxL[7]) is transmitted first, and the first bit received from the line will be put in the MSB of Rx register(bit RxL[7])
4	TX_NEGEDGE	1: the mosi_pad_o signal is changed on the falling edge of sclk_pad_o 0: the mosi_pad_o signal is changed on the rising edge of sclk_pad_o.
3	RX_NEGEDGE	1: the miso_pad_i signal is latched on the falling edge of sclk_pad_o 0: the miso_pad_i signal is latched on the rising edge of sclk_pad_o.
2	GO/BUSY	Writing 1 to this bit starts the transfer. This bit remains set during the transfer and is automatically cleared after the transfer finished. Writing 0 to this bit has no effect.
1:0	Reserved	

■ Timing Chart Example

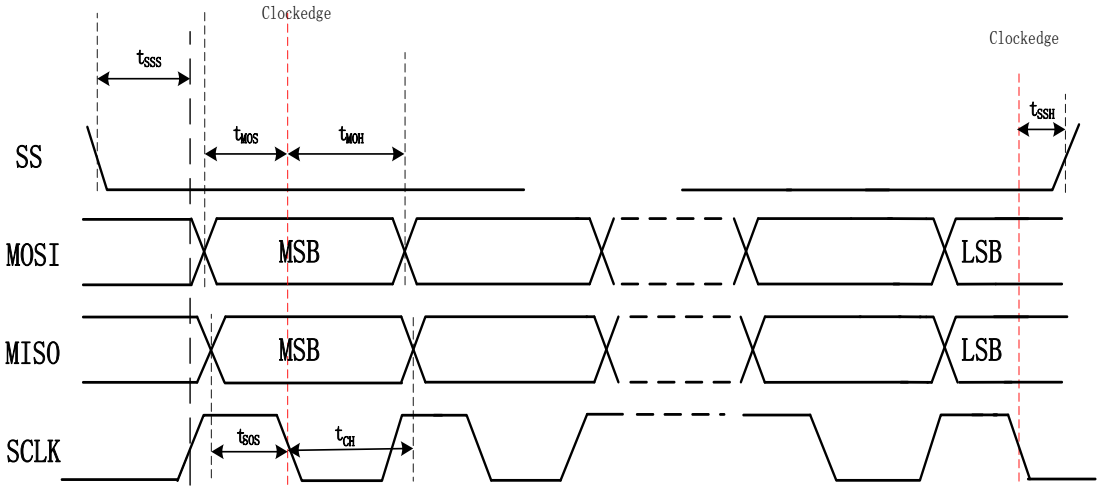


Figure 5.1 CTRL[TX_NEG]=0 CTRL[RX_NEG]=1 CTRL[LSB]=0

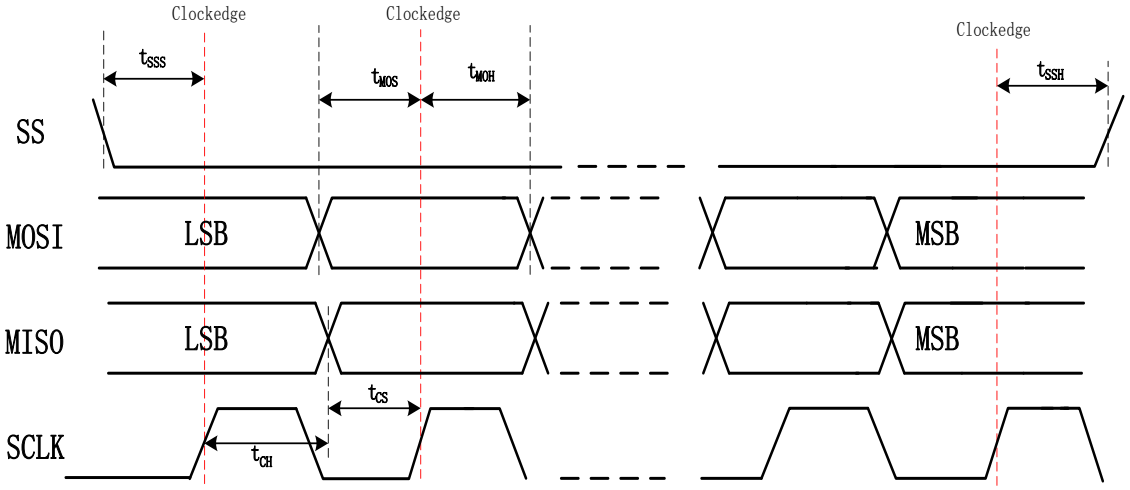
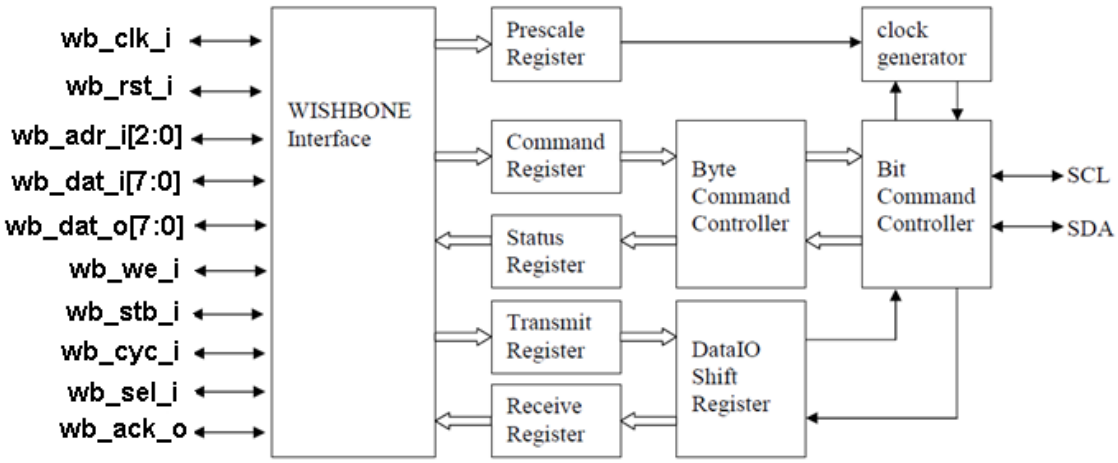


Figure 5.2 CTRL[TX_NEG]=1 CTRL[RX_NEG]=0 CTRL[LSB]=1

6. I²C Controller Block Specification

■ Function Diagram



■ Function Block Description

- WISHBONE Interface: Connecting I2C and Wishbone bus
- Byte command Controller: Transmission sequence controller for one byte
- Bit command Controller: Transmission sequence controller for one bit
- Data IO Shift Register: Data shifting FIFO
- Clock generator: clock divider to generate SCL and transmission sequence

■ I/O Pins

Signal	I/O	Specification
wb_clk_i	In	Master clock
wb_rst_i	In	Synchronous reset
wb_adr_i[2:0]	In	Lower address bits
wb_dat_i[7:0]	In	Data towads the core
wb_we_i	In	Write enable input (control read/write of TXR/RXR registers)
wb_sel_i	In	Core selection input
wb_cyc_i	In	Valid bus cycle input
wb_stb_i	In	Strobe signal
sda	I/O	Serial data line
scl	I/O	Serial clock line
wb_ack_o	Out	Bus cycle acknowledge output
wb_data_o	Out	Data from the core

■ Register Table/Map

Name	Address	Width	Access	Description
PRERlo	0x00	8	R/W	Clock Prescale register lo-byte
PRERhi	0x01	8	R/W	Clock Prescale register hi-byte
CTR	0x02	8	R/W	Control register
TXR	0x03	8	W	Transmit register
RXR	0x03	8	R	Receive register
CR	0x04	8	W	Command register
SR	0x04	8	R	Status register

■ Clock Prescale register (PRERlo, reset value = 0xFF, PRERhi, reset value = 0xFF)

Bit #	Access	Description
7:0	R/W	$f_{scl} = \frac{f_{sysclk}}{5 \times (PRER + 1)}, \ PRER = PRERhi \times 2^8 + PRERlo$ $f_{scl} = 400KHz, PRERhi = 0x00, PRERlo = 0x09$ $f_{scl} = 100KHz, PRER = 0x00, PRERlo = 0x27$

■ Control register (CTR)

Bit #	Access	Description
7	R/W	EN, I^2C core enable bit. When set to '1', the core is enabled. When set to '0', the core is disabled.
6	R/W	IEN, I^2C core interrupt enable bit. When set to '1', interrupt is enabled. When set to '0', interrupt is disabled.
5:0	R/W	Reserved

The core responds to new commands only when the 'EN' bit is set. Pending commands are finished. Clear the 'EN' bit only when no transfer is in progress, i.e. after a STOP command, or when the command register has the STO bit set. When halted during a transfer, the core can hang the I^2C bus.

■ Transmit register (TXR, reset value = 0x00)

Bit #	Access	Description
7:1	W	Next byte to transmit via I^2C
0	W	In case of a data transfer, this bit represents the data's LSB. In case of a slave address's transfer, this bit represents the RW bit. '1' = reading from slave '0' = writing to slave

- **Receive register (RXR, reset value = 0x00)**

Bit #	Access	Description
7:0	R	Last byte received via I^2C

- **Command register (CR, reset value = 0x00)**

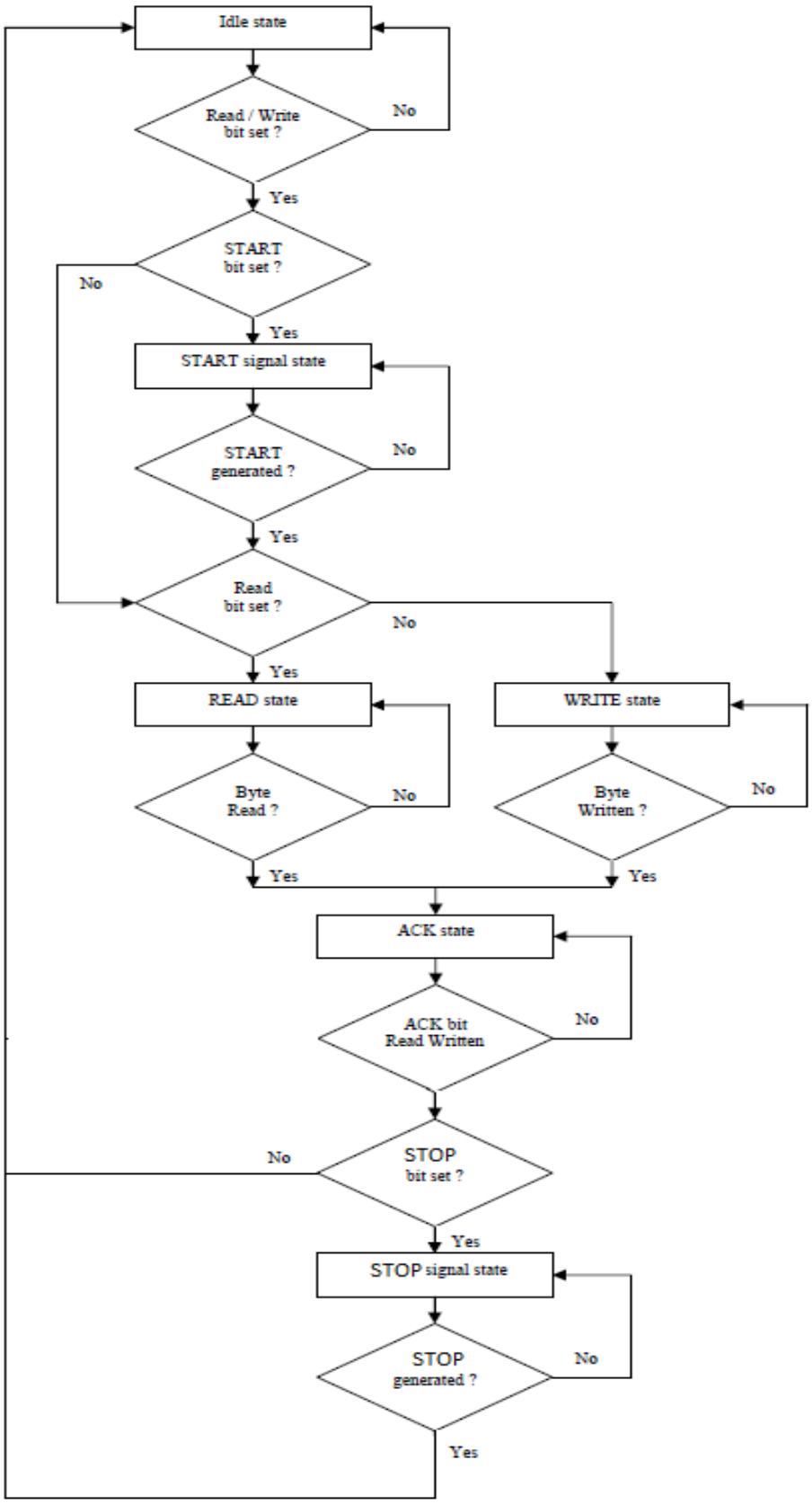
Bit #	Access	Description
7	W	STA, generate (repeated) start condition
6	W	STO, generate stop condition
5	W	RD, read from slave
4	W	WR, write to slave
3	W	ACK, when a receiver, sent ACK (ACK = '0') or NACK (ACK = '1')
2:1	W	*Reserved*
0	W	IACK, Interrupt acknowledge. When set, clear a pending interrupt.

The STA, STO, RD, WR, and IACK bits are cleared automatically. These bits are always read as zeros.

- **Status register (SR, reset value = 0x00)**

Bit #	Access	Description
7	R	RxACK, Received acknowledge from slave. This flag represents acknowledge from the addressed slave. ‘1’ = No acknowledge received ‘0’ = Acknowledge received
6	R	Busy, I^2C bus busy ‘1’ after START signal detected ‘0’ after STOP signal detected
5	R	AL, Arbitration lost This bit is set when the core lost arbitration. Arbitration is lost when: • a STOP signal is detected, but non requested • The master drives SDA high, but SDA is low. See *bus-arbitration* section for more information.
4:2	R	*Reserved*
1	R	TIP, Transfer in progress. ‘1’ when transferring data ‘0’ when transfer complete
0	R	IF, Interrupt Flag. This bit is set when an interrupt is pending, which will cause a processor interrupt request if the IEN bit is set. The Interrupt Flag is set when: • one byte transfer has been completed • arbitration is lost

■ Flow Chart


Idle state
Read / Write bit set ?
No
Yes
START bit set ?
No
Yes
START signal state
START generated ?
No
Yes
Read bit set ?
No
Yes
READ state
Byte Read ?
No
Yes
WRITE state
Byte Written ?
No
Yes
ACK state
ACK bit Read Written
No
STOP bit set ?
No
Yes
STOP signal state
STOP generated ?
No
Yes

- Timing Chart Example

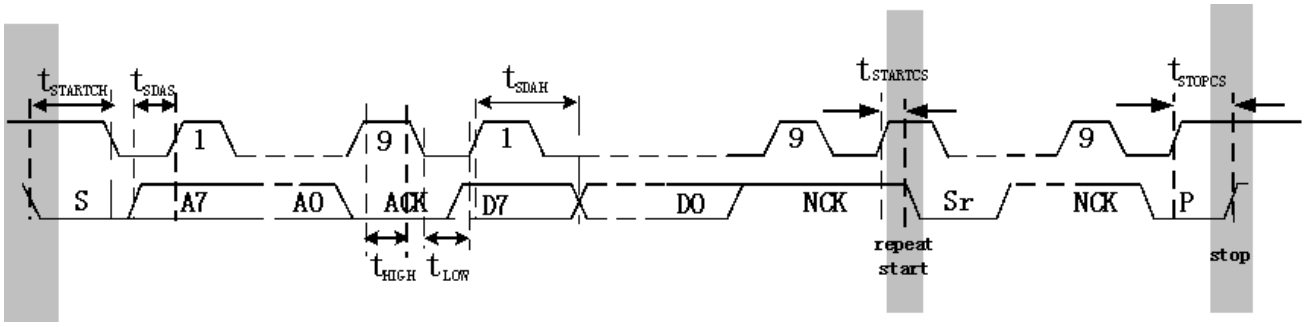
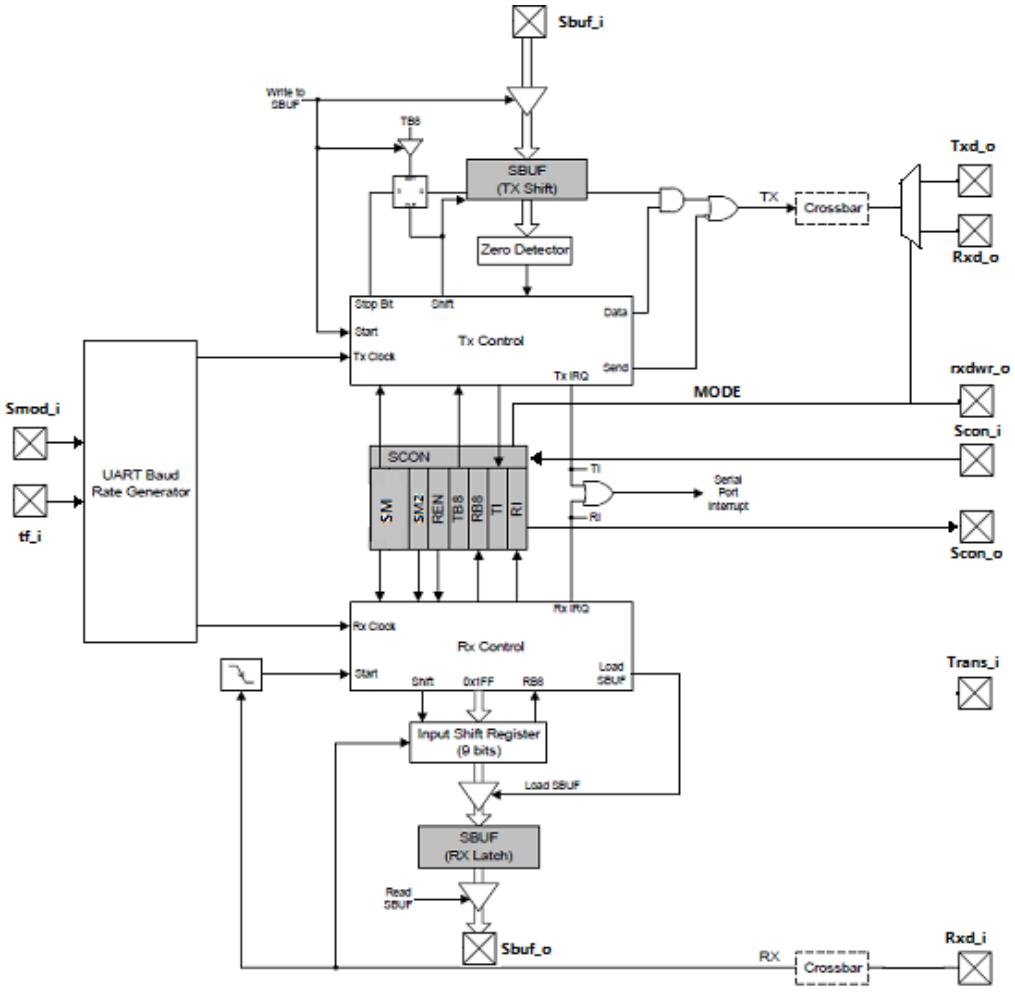


Figure 6.1 I2C timing table

7. Serial Interface Sub-Block Specification

■ Function Diagram



■ Function Block Description

- UART Baud Rate Generator: Generating UART transmission clock
- Tx Control: UART transmission controller, including fetching data from SBUF, shifting data and generating the stop bit
- Rx Control: UART reception controller, including receiving data and loading to SBUF.

■ I/O Pins

Signal	I/O	Specification
clk	In	System clock
reset	In	Reset signal active high
tf_i	In	Timer1 overflow flag
Trans_i	In	Transmission enable
Rxd_i	In	Serial data input
Scon_i	In	SCON SFR input bit
Sbuf_i	In	Data to be transmitted.
Smod_i	In	Transmission baud-rate high/low select
Sbuf_o	Out	Data received
Scon_o	Out	SCON SFR output bit
Rxdwr_o	Out	Rxd direction signal
Rxd_o	Out	Data output for mode 0 operation of serial interface unit.
Txd_o	Out	Serial data output

■ Register Table/Map

■ SCON: SFR Address = 0xF0; Bit-Addressable

Bit	7	5	4	3	2	1	0
Name	SM[1:0]	SM2	REN	TB8	RB8	TI	RI
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	00	0	0	0	0	0	0

Bit	Name	Function
7	SM[1:0]	Serial Port Operation Mode. Selects the UART0 Operation Mode. 00: mode0 8-bit UART with Baud Rate SYSCLK(20MHz)/12. 01: mode1 8-bit UART with Variable Baud Rate. 10: mode2 9-bit UART with Baud Rate SYSCLK(20MHz)/16 or SYSCLK(20MHz)/32. 11: mode3 9-bit UART with Variable Baud Rate.
5	SM2	Multiprocessor Communication Enable. For Mode 0 (8-bit UART): Checks for valid stop bit. 0: Logic level of stop bit is ignored. 1: RI will only be activated if stop bit is logic level 1. For Mode 1 (9-bit UART): 0: Logic level of ninth bit is ignored. 1: RI is set and an interrupt is generated only when the ninth bit is logic 1.

4	REN	Receive Enable. 0: UART reception disabled. 1: UART reception enabled.
3	TB8	Ninth Transmission Bit. The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 2, 3). Unused in 8-bit mode (Mode 0, 1).
2	RB8	Ninth Receive Bit. RB8 is assigned the value of the STOP bit in Mode 0, 1; it is assigned the value of the 9th data bit in Mode 2, 3.
1	TI	Transmit Interrupt Flag. Set by hardware when a byte of data has been transmitted by UART (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART interrupt service routine. This bit must be cleared manually by software.
0	RI	Receive Interrupt Flag. Set to 1 by hardware when a byte of data has been received by UART (set at the STOP bit sampling time). When the UART interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART interrupt service routine. This bit must be cleared manually by software.

- **SBUF: SFR Address = 0x99;**

Bit	7	6	5	4	3	2	1	0
Name	SBUF[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	SBUF[7:0]	**Serial Data Buffer Bits 7:0 (MSB–LSB).** This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF0, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF0 initiates the transmission. A read of SBUF0 returns the contents of the receive latch.

Timing Chart Example

- **8-Bit Synchronous UART mode** is the transmission only mode. The txd_o is used to generate synchronous clock with a frequency of SYSCLK(20MHz)/12. Rxd_i is disabled for rxdwr_o is set high while data is transimitted from the rxd_o pin. A total of 8 bits per data byte is transmitted. Different

from other modes, there is no start bit or stop bit in synchronous mode but only eight data bits (LSB first). Data are transmitted LSB first from the rxd_o pin.

Data transmission begins when software writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (The time 8th bit is sent).

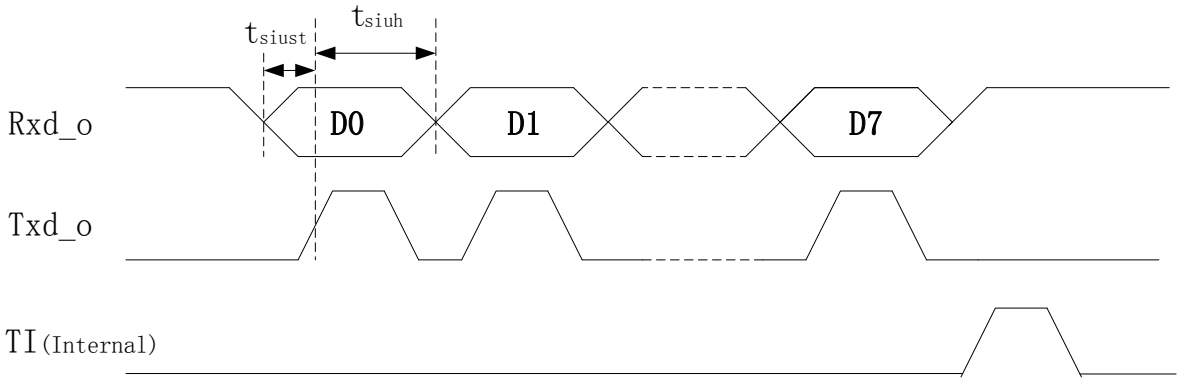


Figure 7.1 UART time table in mode0

- **8-Bit Asynchronous UART mode** uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the Txd_o pin and received at the Rxd_i pin. On receive, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2).

  Data transmission begins when software writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit (SCON.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF receive register if the following conditions are met: (1) RI is logic 0 during reception, (2) if SM2 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF receive register and the following overrun data bits are lost.

  If these conditions are met, the eight bits of data is stored in SBUF, the stop bit is stored in RB8 and the RI flag is set. If these conditions are not met, SBUF and RB8 will not be loaded and the RI flag will not be set. An interrupt will occur if enabled when either TI or RI is set.

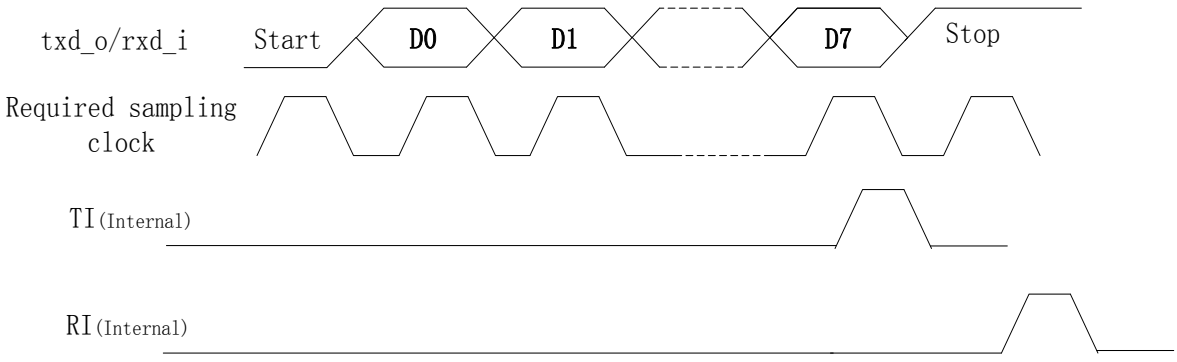


Figure 7.2 UART time table in mode1

- **9-bit UART mode** uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB8 (SCON.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB8 (SCON.2) and the stop bit is ignored.

  Data transmission begins when an instruction writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit (SCON.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF receive register if the following conditions are met: (1) RI must be logic 0 during reception, and (2) if SM2 is logic 1, the 9th bit must be logic 1 (when SM2 is logic 0, the state of the ninth data bit is unimportant).

  If these conditions are met, the eight bits of data are stored in SBUF, the ninth bit is stored in RB8, and the RI flag is set to 1. If the above conditions are not met, SBUF and RB8 will not be loaded and the RI flag will not be set to 1. A UART interrupt will occur if enabled when either TI or RI is set to 1.

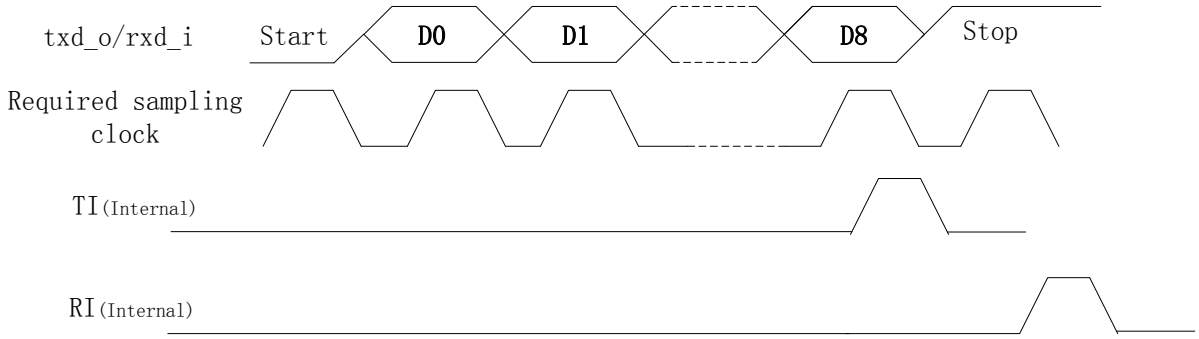


Figure 7.3 UART time table in mode2, 3

8. Timer/Counter Sub-Block Specification

■ Function Diagram

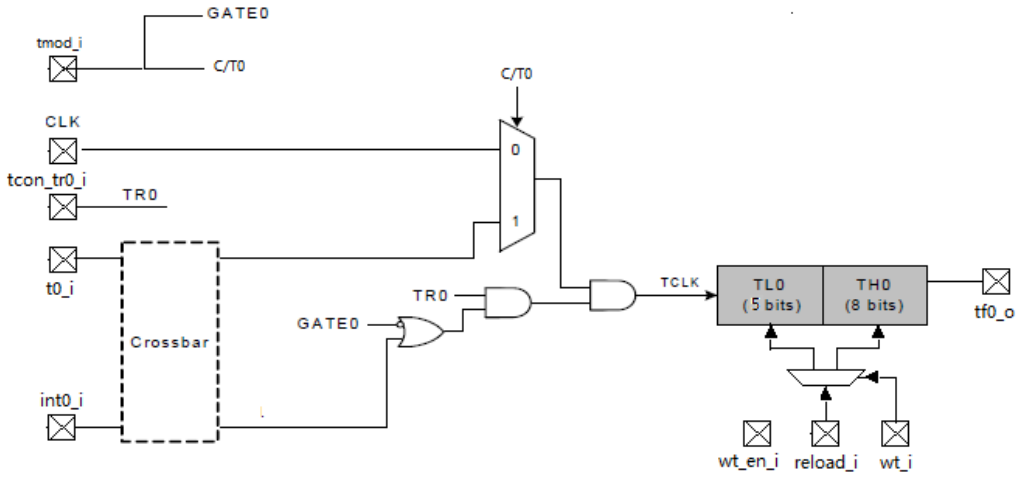


Figure 8.1 T0 in Mode0 Block Diagram (T1 the same)

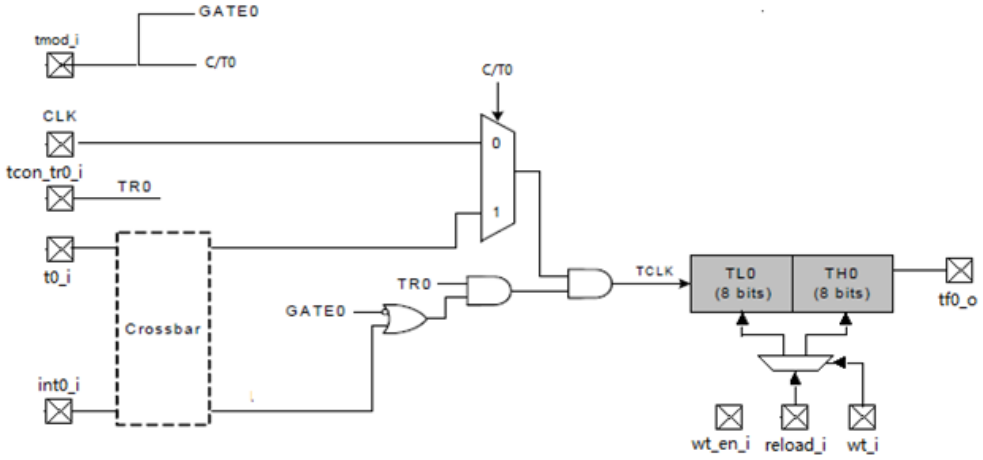


Figure 8.2 T0 in Mode1 Block Diagram (T1 the same)

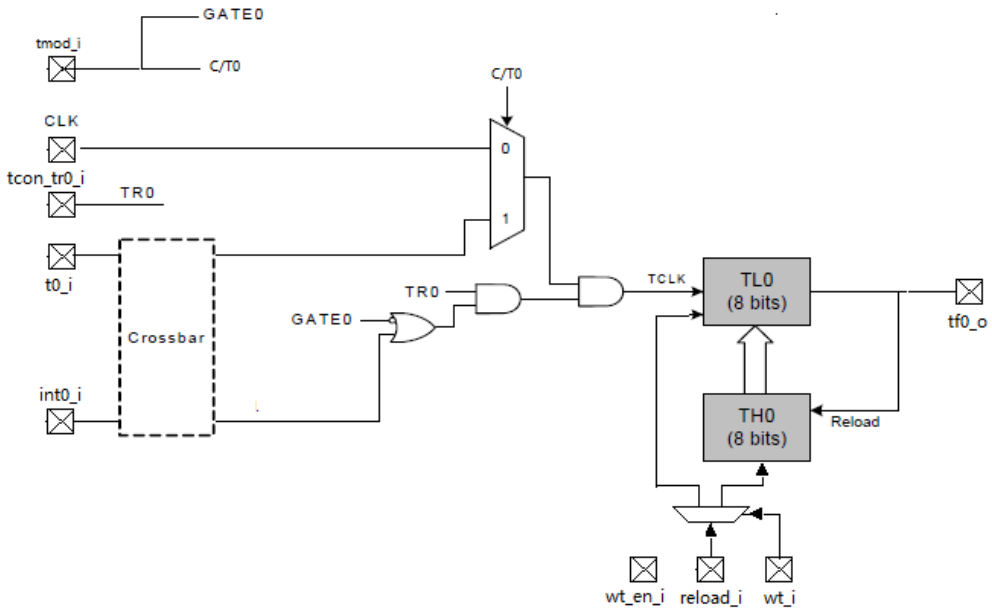


Figure 8.3 T0 in Mode2 Block Diagram (T1 the same)

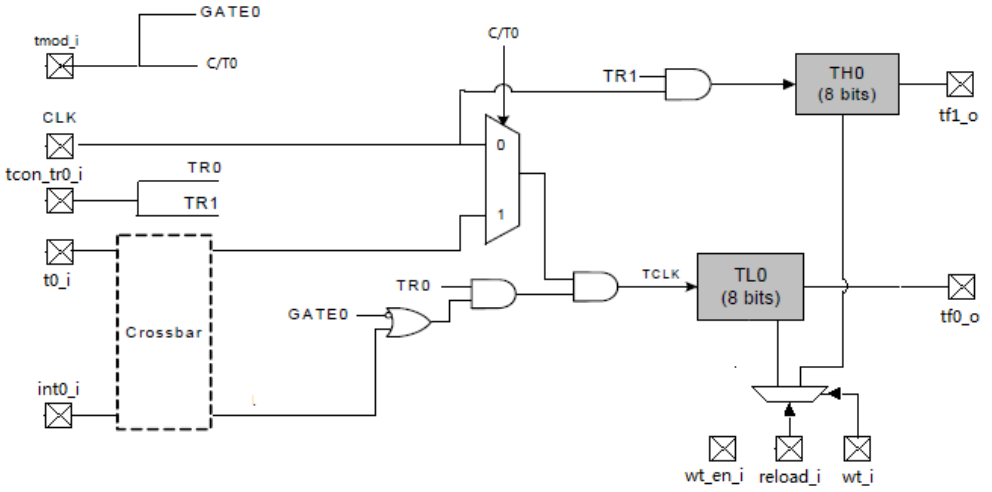


Figure 8.4 T0 in Mode3 Block Diagram (T1 disabled)

Function Block Description

- Crossbar: latch the external interrupt signals and external clock signals.
- TL0/TL1: Store the lower byte of 16bit counter of Timer0/Timer1
- TH0/TH1: Store the lower byte of 16bit counter of Timer0/Timer1

Register Table/Map

Symbol	Address	Name
TL0	8AH	Timer/counter 0 low byte
TL1	8BH	Timer/counter 1 low byte
TH0	8CH	Timer/counter 0 high byte
TH1	8DH	Timer/counter 1 high byte

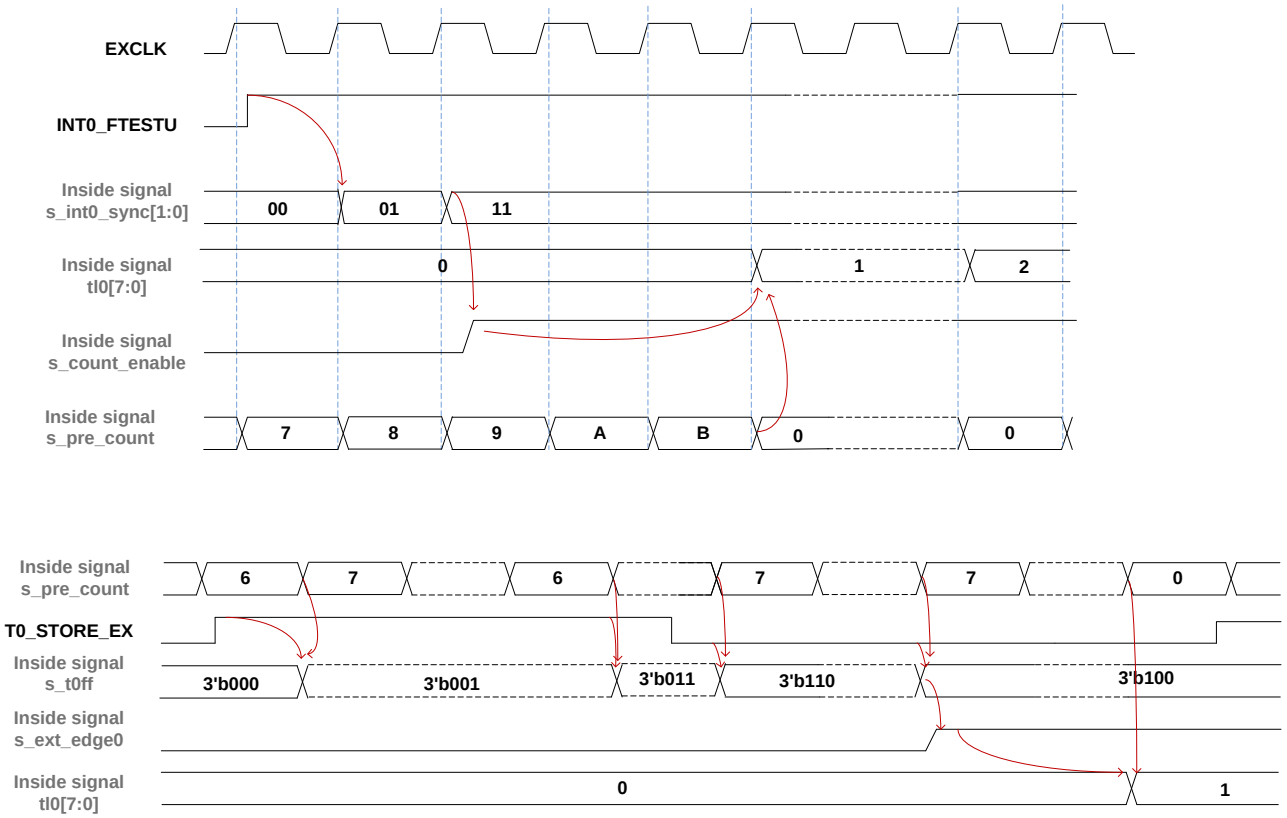
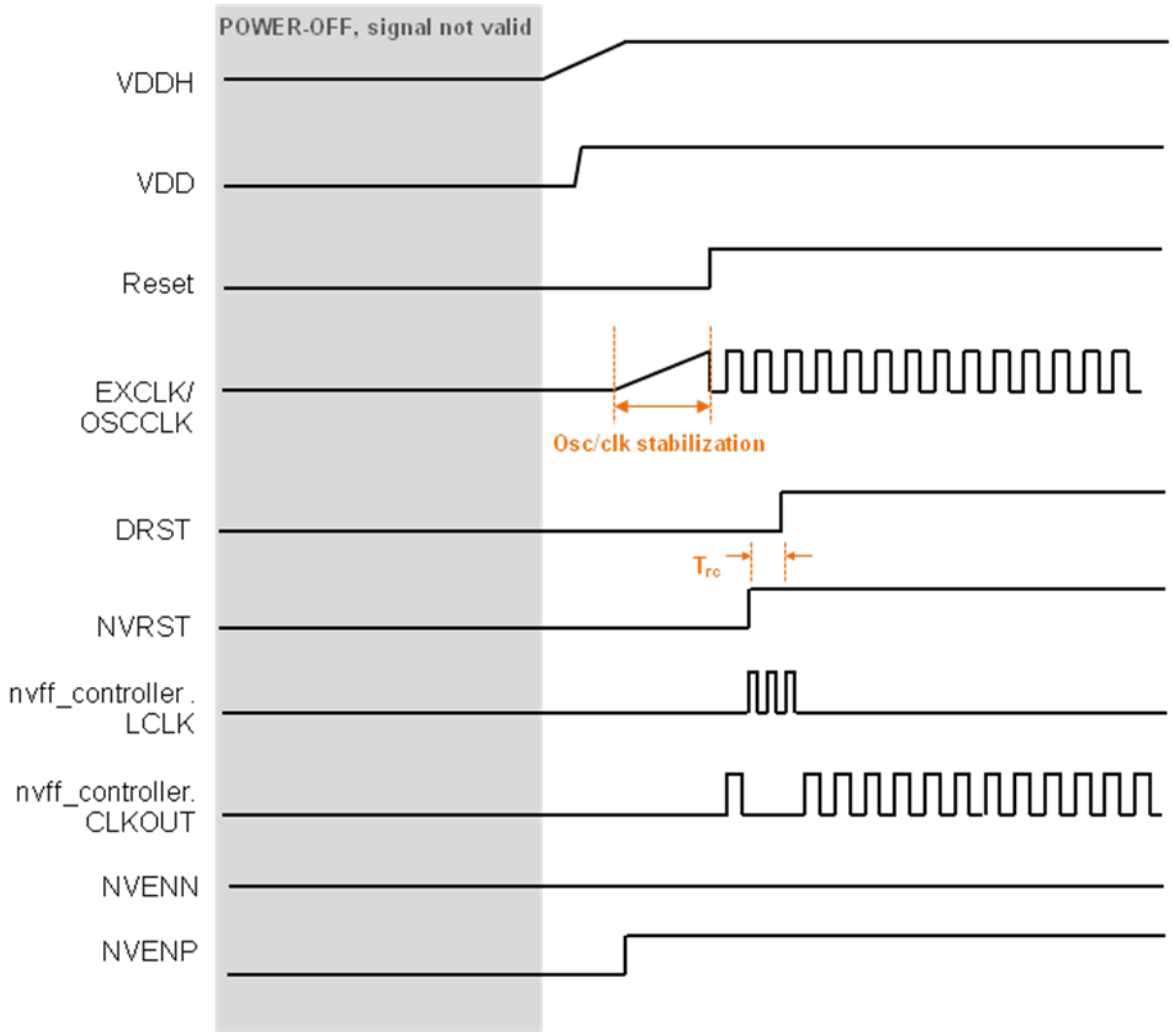


Figure 8.5 Timer cycle time

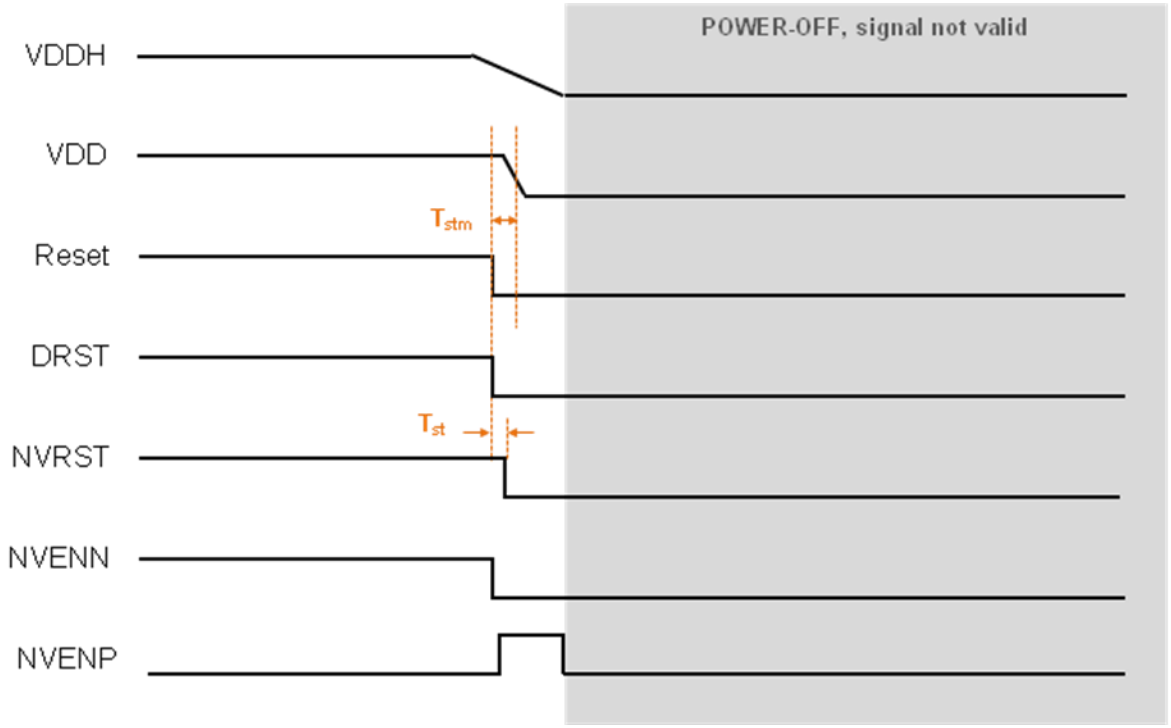
10. Power Management

PARAMETER	Symb.	VALUE			UNITS
		MIN	TYP	MAX	
Supply voltage (Core, Data Recall)	VDD	1.35	1.5	1.65	V
Supply voltage (Data Store)	VDD	1.25	-	1.65	V
Supply voltage (I/O)	VDDH	2.97	3.3	3.63	V
“High” input voltage	V_{IH}	0.7*VDDH			V
“Low” input voltage	V_{IL}			0.3*VDDH	V
STORE operation duration	T_{st}			18	µs
Margin value for STORE operation	T_{stm}		50		µs
RECALL operation duration	T_{rc}			11	µs

■ Starting-Up Sequence



■ Shutting-Down Sequence


POWER-OFF, signal not valid
VDDH
VDD
Tstm
Reset
DRST
Tst
NVRST
NVENN
NVENP

11. Test and Debug Methodology

Table11.1 Internal SRAM Test Interface

SIGNAL NAME	Pin No.	Pin ID	I/O	FUNCTION DESCRIPTIONS
SRAM_Adr[0:16]			Input	External Address to SRAM.
SRAM_Data[0:7]			Output	SRAM Data for one byte.
Byte_sel[0:1]			Input	Byte Select Signal.
Sram_clk			Input	SRAM Clock when Debugging.
We_n			Input	SRAM Write Enable Signal when Debugging. The SRAM can be written when Lowing this Signal

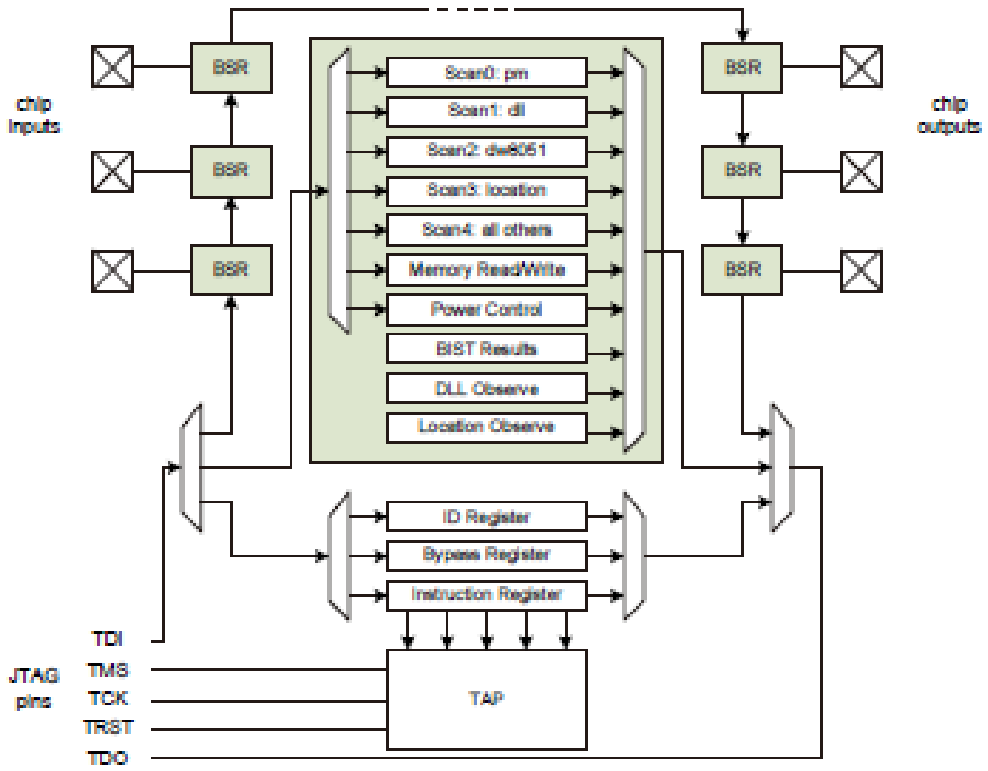


Figure 5.24: Block diagram of the JTAG test port logic.

- **Mode select**

Mode explanation, Port assignment (Table)

PIN	I/O	MODE

		DC	IDDQ	SCAN/BIST
CLK	IN	—	scan clock	pin
CLKOUT	OUT	clock	←	←
CLRN_RSTN ※1	IN	hardware reset (pin)	—	hardware reset (pin)
NVENN ※1	IN	pin	—	pin
NVENP ※1	IN	pin	—	pin
MOUT ※2	OUT	—	—	pin
DRSTN	OUT	volatile FF reset	←	←
NVRSTN	OUT	non-volatile FF reset	←	←
E1	OUT	open	←	←
HS	OUT	open	←	←
SAE	OUT	open	←	←
FRSTU	OUT	open	←	←
FRSTD	OUT	open	←	←
PL1_DN	OUT	open	←	←
PL2_DN	OUT	open	←	←
TESTU	OUT	open	←	←
TESTD	OUT	open	←	←
LCLK	OUT	X	X	pin
E1_o	OUT	X	X	pin
HS_o	OUT	X	X	pin
SAE_o	OUT	X	X	pin
FRSTU_o	OUT	X	X	pin
FRSTD_o	OUT	X	X	pin
PL1_DN_o	OUT	X	X	pin
PL2_DN_o	OUT	X	X	pin
NVFF_STOP	IN	1’b0	1’b1	pin
CSEL	IN	1’b0	1’b1	pin
RSTN_IN	IN	1’b1	scan reset	pin
RSTN_SEL	IN	1’b0	1’b1	pin
RSTN_OUT	OUT	X	X	pin
STORE	IN	1’b0	←	←
RECALL	IN	1’b0	←	←
STORE_EX	IN	1’b0	—	Pin
RECALL_EX	IN	1’b0	—	Pin
FTESTU	IN	1’b0	—	pin
FTESTD	IN	1’b0	—	pin
STOL_TEST	IN	1’b0	—	pin
LCLK_TEST	IN	1’b0	—	pin
CNT_OUT	OUT	X	X	pin
PLU_A	IN	—	—	pin
PLD_A	IN	—	—	pin

12. AC/DC Specification

■ Absolute Maximum Ratings

PARAMETER	VALUE			UNITS	COND.
	MIN	TYP	MAX		
Supply voltage	-0.3		2.1	V	Core
	-0.3		4.5	V	I/O
Ambient temperature under bias	-45		80	ºC	
Storage temperature range	-50		90	ºC	
Voltage on any Pin (except VDD and Port I/O) with respect to DGND	-0.3		VDD+0.3	V	
Voltage on any Port I/O Pin or RST with respect to DGND	-0.3		5.8	V	
Voltage on VDD with respect to DGND	-0.3		4.2	V	
Maximum Total current through VDD, AV+, DGND and AGND			800	mA	
Maximum output current sunk by any Port Pin			100	mA	
Maximum output current sunk by any other I/O Pin			50	mA	
Maximum output current sourced by any Port Pin			100	mA	
Maximum output current sourced by any other I/O Pin			50	mA	

■ Recommended Operation Conditions

PARAMETER	VALUE			UNITS	COND.
	MIN	TYP	MAX		
Supply voltage (Core, Data Recall)	1.35	1.5	1.65	V	
Supply voltage (Data Store)	1.25	-	1.65	V	
Supply voltage (I/O)	2.97	3.3	3.63	V	
Operating temperature	-40		85	ºC	

■ DC Specification

PARAMETER	VALUE			UNITS	COND.
	MIN	TYP	MAX		
“High” input voltage (V_{IH})	0.7x VDD			V	
“Low” input voltage (V_{IL})			0.3 x VDD	V	
“High” output voltage (V_{OH})	VDD-0.1			V	I_{OH}=-10μA, Port I/O Push-Pull
	VDD-0.7				I_{OH}=-3mA, Port I/O Push-Pull
		VDD-0.8			I_{OH}=-10mA, Port I/O Push-Pull
“Low” output voltage (V_{OL})			0.1	V	I_{OL}=10μA
			0.6		I_{OL}=8.5mA
		1.0			I_{OL}=25mAl

Input leakage current (I_{IZ})			±1	µA	Weak Pull-up Off	DGND<Port Pin<VDD, Pin Tri-state
		10			Weak Pull-up On	
Input capacitance		5		pF		
Output leakage current (I_{OZ})				µA		
Normal operation current						
Current when Store/Recall data				µA		

■ AC Specification

PARAMATER	SYM.	LIMIT			UNIT	Cond.
		MIN	TYP	MAX		
Non-volatile mode setup	t_{NVS}	0	-	-	ns	
Non-volatile hold	t_{NVH}	20	-	-	µs	
CLRn_RSTN high to first clock after power up	t_{FC}	20	-	-	µs	
Last clock to CLRn_RSTN low before power down	t_{LC}	20	-	-	Ns	
STORE duration	t_{ST}	-	-	18	µs	
RECALL duration	t_{RC}	-	-	11	µs	
Reset		3		10	Cycles	
Clk frequency	f_{CLK}	16	20	25	Mhz	
Clk high time	t_{CLKH}	30%	50%	70%	Cycle	
Clk low time	t_{CLKL}	70%	50%	30%	Cycle	
SS hold	t_{SSH}	25			ns	SPI slave sel
SS setup	t_{SSS}	25			ns	SPI slave sel
Mosi setup time	t_{MOS}	25	-	-	ns	SPI master out data latch (setup)
Mosi hold time	t_{MOH}	5	-	-	ns	SPI master out data latch (hold)
Miso setup time	t_{SOS}	25	-	-	ns	SPI slave out data latch (setup)
Miso hold time	t_{SOH}	25	-	-	ns	SPI slave out data latch (hold)

Sclk	f_{SCLK}			10	Mhz	SPI Clk
Repeat Start condition setup time	$t_{STARTCS}$	400K:0.6* 100K:4.7			us	I2C
(repeat)Start condition hold time	$t_{STARTCH}$	400K:0.6* 100K:4.0			us	I2C
Stop condition setup time	t_{STOPCS}	400K:0.6* 100K:4.0			us	I2C
Scl frequency	f_{SCL}	100		400	Khz	I2C clock
Scl low period	t_{LOW}	400K:1.3* 100K:4.7			us	I2C clock
Scl high period	t_{HIGH}	400K:0.6* 100K:4.0			us	I2C clock
Sda setup time	t_{SDAS}	400K:100* 100K:250			ns	I2C data
Sda hold time	t_{SDAH}	0		0.9** 3.45	us	I2C data

***:** 400K: I2C transmission in 400K bit rate
100K: I2C transmission in 100K bit rate

**:The maximum tSDAH has only to be met if the device does not stretch the LOW period (tLOW) of the SCL signal

13. Reliability Test

■ Reliability Test

Items	Condition	Other
High Temperature Case (Power Down)	+85°C, 2000H	
High Temperature Case (Active)	+80°C, 1000H	
Low Temperature Case (Active)	-30°C	10 times on-off
High Temperature & High Humility Bias Case (THB)	+65°C, 192H, Humidity 90~95%	