

# 数字逻辑与计算机组成实验

## (组合逻辑电路设计) lab01: 选择器

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(一) 实验目的

实现 2 位 4 选 1 的选择器

(二) 实验原理

多路选择器：多输入单输出

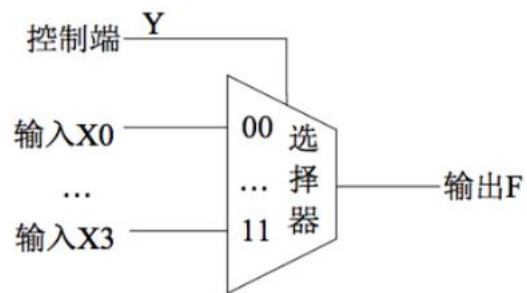


图 1-5: 2 位 4 选 1 选择器

(三) 实验环境/器材等

硬件器材：Nexys A7-100T 开发板

软件平台：Vivado 开发平台

(四) 实验过程

设计思路：case 语句 – 简洁

设计代码：

```

module lab01(
    input [1:0] X0,
    input [1:0] X1,
    input [1:0] X2,
    input [1:0] X3,
    input [1:0] Y,
    output reg [1:0] F
);

    always @ (Y or X0 or X1 or X2 or X3)
        case (Y)
            0: F = X0;
            1: F = X1;
            2: F = X2;
            3: F = X3;
            default: F = 2'b00;
        endcase

endmodule

```

测试代码：

```

module lab01_test(

);
    reg [1:0] X0;
    reg [1:0] X1;
    reg [1:0] X2;
    reg [1:0] X3;
    reg [1:0] Y;
    wire [1:0] F;

    lab01 i1 (
        .X0(X0),
        .X1(X1),
        .X2(X2),
        .X3(X3),
        .Y(Y),
        .F(F)
    );

```

```

initial
begin
    Y = 2'b00; X0 = 2'b11; X1 = 2'b00; X2 = 2'b00; X3 = 2'b00; #10;
        X0 = 2'b10; X1 = 2'b00; X2 = 2'b00; X3 = 2'b00; #10;
    Y = 2'b01; X0 = 2'b00; X1 = 2'b11; X2 = 2'b00; X3 = 2'b00; #10;
        X0 = 2'b00; X1 = 2'b10; X2 = 2'b00; X3 = 2'b00; #10;
    Y = 2'b10; X0 = 2'b00; X1 = 2'b00; X2 = 2'b11; X3 = 2'b00; #10;
        X0 = 2'b00; X1 = 2'b00; X2 = 2'b10; X3 = 2'b00; #10;
    Y = 2'b11; X0 = 2'b00; X1 = 2'b00; X2 = 2'b00; X3 = 2'b11; #10;
        X0 = 2'b00; X1 = 2'b00; X2 = 2'b00; X3 = 2'b10; #10;

end

endmodule

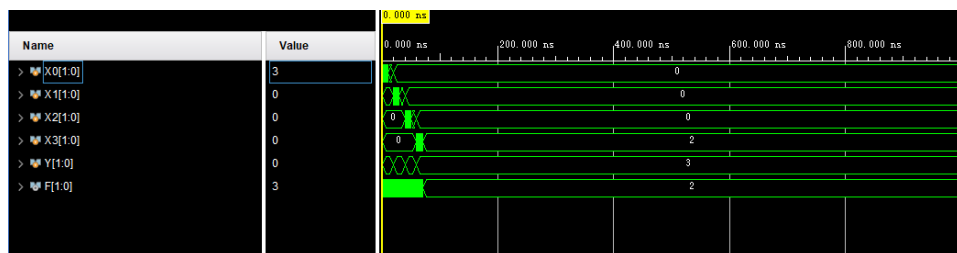
```

引脚分配：

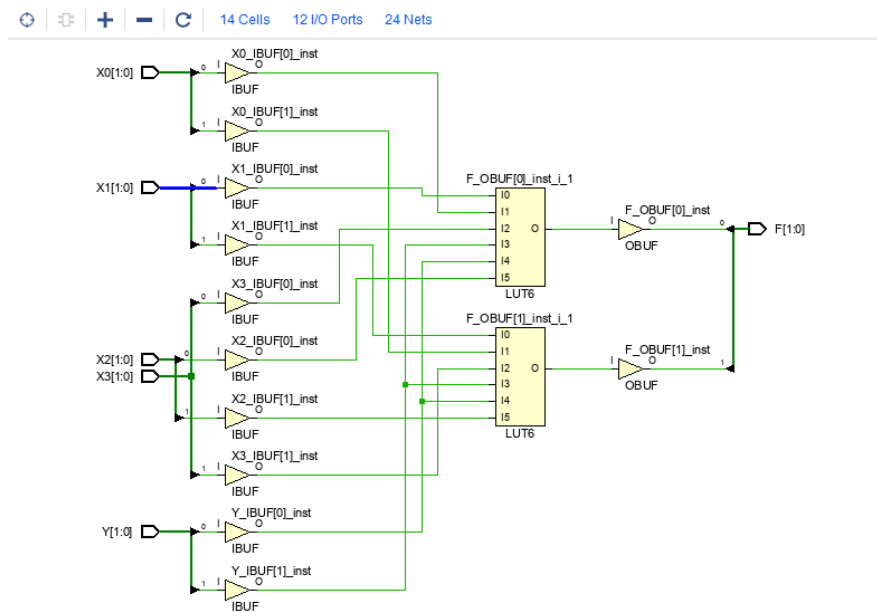
Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	IO Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
▼ All ports (12)													
▼ F (2) OUT	OUT			✓		15 LVCMOS33*	3.300		12	✓	NONE	FP_VTT_50	✓
F[1] OUT	OUT		H17	✓		15 LVCMOS33*	3.300		12	✓	NONE	FP_VTT_50	✓
F[0] OUT	OUT		K15	✓		15 LVCMOS33*	3.300		12	✓	NONE	FP_VTT_50	✓
▼ X0 (2) IN	IN			✓		14 LVCMOS33*	3.300				NONE	NONE	✓
X0[1] IN	IN		M13	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
X0[0] IN	IN		R15	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
▼ X1 (2) IN	IN			✓		14 LVCMOS33*	3.300				NONE	NONE	✓
X1[1] IN	IN		R17	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
X1[0] IN	IN		T18	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
▼ X2 (2) IN	IN			✓		14 LVCMOS33*	3.300				NONE	NONE	✓
X2[1] IN	IN		U18	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
X2[0] IN	IN		R13	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
▼ X3 (2) IN	IN			✓		34 LVCMOS33*	3.300				NONE	NONE	✓
X3[1] IN	IN		T8	✓		34 LVCMOS33*	3.300				NONE	NONE	✓
X3[0] IN	IN		U8	✓		34 LVCMOS33*	3.300				NONE	NONE	✓
▼ Y (2) IN	IN			✓	(Multiple)	LVCMOS33*	3.300				NONE	NONE	✓
Y[1] IN	IN		J15	✓		15 LVCMOS33*	3.300				NONE	NONE	✓
Y[0] IN	IN		L16	✓		14 LVCMOS33*	3.300				NONE	NONE	✓
Scalar ports (0)													

## (五) 实验结果

仿真结果：



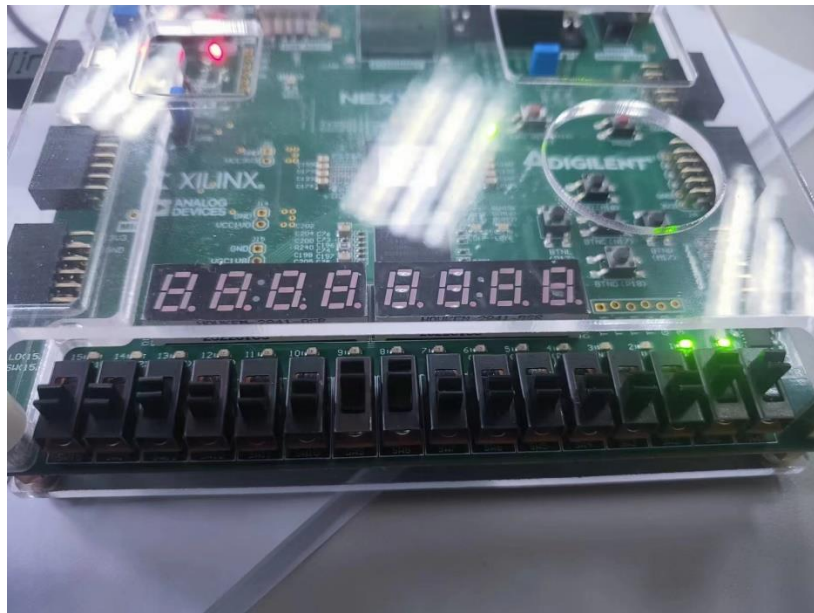
综合后生成的电路原理图：



硬件实现：







## (六) 实验中遇到的问题及解决方法

```
F = 2'b00; X0 = 2'b11; X1 = 2'b00; X2 = 2'b00; X3 = 2'b00; #10;
```

输出变量 Y 不小心写成 F

解决方法：写代码时仔细检查